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AX7015B Development Board

User Manual

Alinx Electronic Limited

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AMD Adaptive Computing Partner PREMIER

Document revision history

chapter	Revision Overview
V1.0	
all	First version released
V2.0	
1.3 DDR3 DRAM 2.6 Fiber Optic Interface	1. The original DDR3 model (SK Hynix H5TQ4G63AFR-PBI) has been discontinued and is now replaced with the Micron model MT41K256M16TW-107. 2. Add descriptions for the optical fiber interface silkscreens OPT1 and OPT2.

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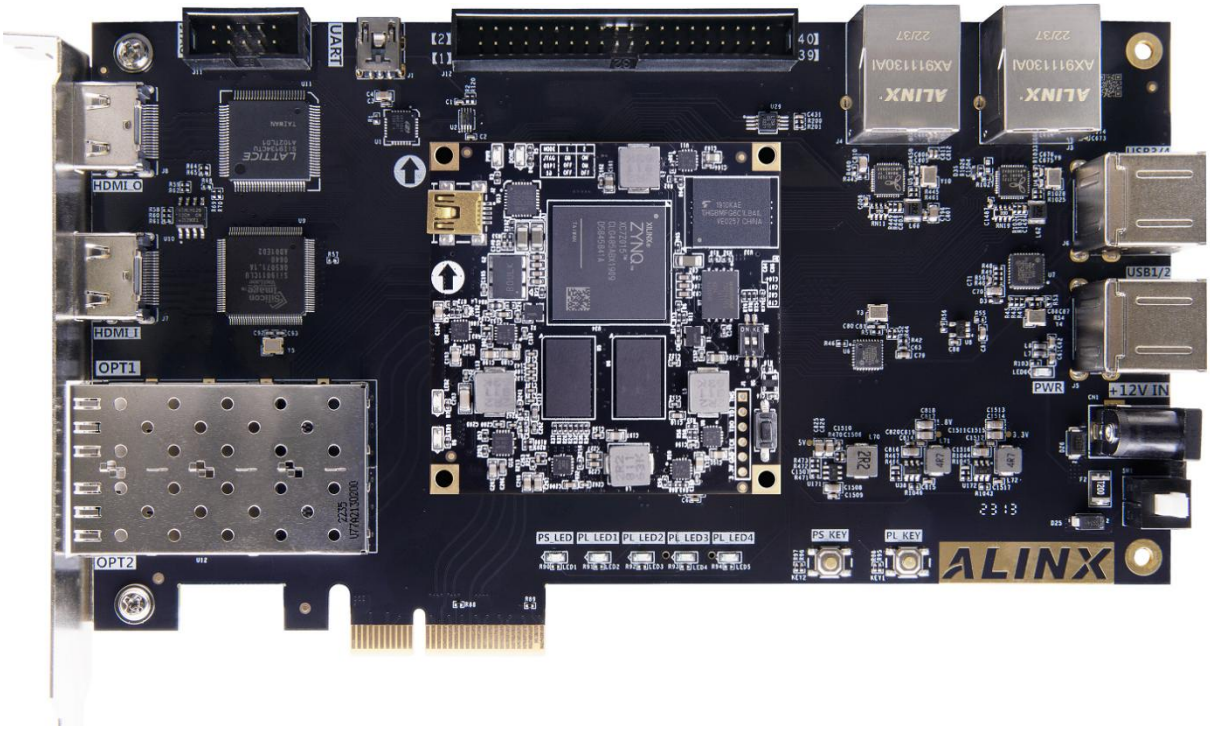
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Alinx Electronic Limited has officially released the 2018 version of its development board (model: AX7015B) based on the XILINX ZYNQ7000 development platform. To help you quickly understand this development platform, we have edited this user manual.

This ZYNQ7000 FPGA development platform adopts a core board plus expansion board model, facilitating secondary development and utilization of the core board by users. The core board uses Xilinx's Zynq7000 SOC chip XC7Z015 solution , which integrates a dual-core ARM Cortex-A9 processor and FPGA programmable logic onto a single chip using ARM + FPGA SOC technology . Additionally , the core board contains two 1GB high-speed DDR3 SDRAM chips, one 8GB eMMC memory chip, and one 256Mb QSPI FLASH chip.

In terms of baseboard design, we've expanded the peripheral interfaces for users with a wealth of features, such as one PCIe x 2 interface, two fiber optic interfaces, two Gigabit Ethernet interfaces, four USB 2.0 host interfaces, one HDMI input interface, one HDMI output interface, one UART serial port interface, one SD card interface, and one 40-pin expansion interface, etc. This meets users' various requirements for high-speed data exchange, data storage, video transmission and processing, and industrial control, making it a "professional-grade" ZYNQ development platform. It provides possibilities for high-speed data transmission and exchange, and for the initial verification and later application of data processing. We believe this product is very suitable for students, engineers, and other groups engaged in ZYNQ development.



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Development Board Introduction

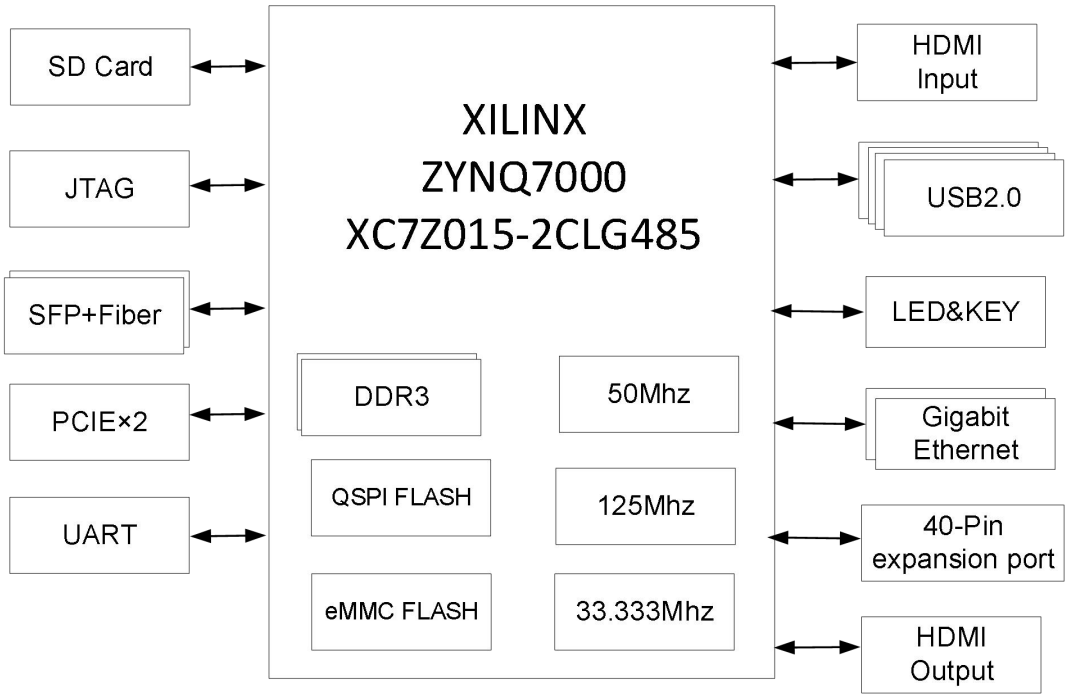
Here is a brief introduction to the features of the AX7015B ZYNQ development platform.

The development board's overall structure follows our established core board + expansion board design. High-speed board-to-board connectors connect the core board and expansion boards.

The core board primarily consists of a minimum system comprised of a ZYNQ7015 chip, two DDR3 memory chips, an eMMC chip, and a QSPI FLASH chip. It handles the high-speed data processing and storage functions of the ZYNQ system. The data bus width between the ZYNQ7015 and the two DDR3 chips is 32 bits, with the two DDR3 chips having a total capacity of 1GB. An 8GB eMMC FLASH chip and a 256Mb QSPI FLASH chip are used for static storage of the ZYNQ operating system, file system, and user data. Users can select different boot modes using DIP switches on the core board. The ZYNQ7015 uses a Xilinx Zynq7000 series chip , model XC7Z015-2CLG485. The ZYNQ7015 chip can be divided into a Processor System (PS) and a Programmable Logic (PL) section.

The baseboard provides a rich set of peripheral interfaces for the core board, including one PCIe x 2 interface, two fiber optic interfaces, two Gigabit Ethernet interfaces, four USB 2.0 host interfaces, one HDMI input interface, one HDMI output interface, one UART serial port interface, one SD card interface, one 40-pin expansion interface, and some button LEDs.

The following diagram shows the overall structure of the development system:



This diagram shows the interfaces and functions that our development platform can contain.

- The ZYNQ7000 core board consists of an XC7Z015+1GB DDR3+8GB eMMC FLASH+256Mb QSPI FLASH, and two crystal oscillators providing clocks: one at 33.3333MHz for the PS

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system and the other at 50MHz for the PL logic, along with one GTP differential reference clock at a frequency of 125MHz.

- 1 PCIe x 2 interface : Supports PCI Express 2.0 standard, provides standard PCIex2 high-speed data transmission interface, and single-channel communication rate can reach up to 5GBaud .
- Two SFP fiber optic interfaces : ZYNQ's GTP transceiver has two high-speed transceivers connected to two optical modules for transmission and reception, enabling two high-speed fiber optic communication interfaces. Each fiber optic data communication interface can transmit and receive data at speeds up to 6.25 Gb/s.
- Gigabit Ethernet Interface : Two 10/100M /1000M Ethernet RJ45 interfaces for Ethernet data exchange with computers or other network devices. The network interface chip uses the JL2121 industrial-grade GPHY chip from Jinglue Company. One Ethernet port connects to the PS terminal of the ZYNQ chip, and the other Ethernet port connects to the PL terminal of the ZYNQ chip.
- HDMI video output : 1 HDMI video output interface. We have selected the SIL9134 HDMI encoding chip from Silion Image, which supports up to 1080P@60Hz output and 3D output.
- HDMI video input : 1 HDMI video input interface. We selected the SIL9013 HDMI decoding chip from Silion Image, which supports up to 1080P@60Hz input and supports data input in different formats.
- USB 2.0 HOST Interface :Expands to 4 USB HOST interfaces via a USB Hub chip, used to connect external USB slave devices, such as mice, keyboards, USB flash drives, etc. The USB interface uses a flat USB connector (USB Type A) .
- USB UART Interface :Two UART-to-USB interfaces for communication with a computer, facilitating user debugging. One interface is on the core board for independent core board operation, and the other is on the baseboard for overall board debugging. The serial port chip uses the Silicon Labs CP2102GM USB- UART chip , and the USB interface uses a MINI USB interface.
- Micro SD Card Slot :1 Micro SD card slot for storing operating system images and file systems .
- 40-pin expansion port : One 40-pin, 2.54mm pitch expansion port allows connection to various Alinx modules (dual-lens cameras, TFT LCD screens, high-speed AD modules, etc.). The expansion port includes one 5V power supply, two 3.3V power supply channels, three ground channels, and 34 I/O ports.
- USB JTAG Port : One 10-pin 2.54mm standard JTAG port for FPGA program downloading and debugging. Users can debug and download ZYNQ systems using a Xilinx programmer.
- LEDs :10 LEDs, 4 on the core board and 6 on the baseboard. The core board has 1 power indicator, 1 DONE configuration indicator, and 2 user indicator lights. The baseboard has 1 power indicator and 5 user indicator lights.
- Buttons : There are 3 buttons, 1 reset button on the core board and 2 user buttons on the baseboard.

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01 AC7015B Core Board

1.1 Introduction

The AC7015B (core board model, hereinafter the same) core board uses the ZYNQ chip, which is based on Xilinx's ZYNQ7000 series XC7Z015-2CLG485I. The ZYNQ chip's PS system integrates two ARM Cortex™-A9 processors, AMBA® interconnect, internal memory, external memory interface, and peripherals. The ZYNQ chip's FPGA contains abundant programmable logic units, DSP, and internal RAM.

This core board uses two Micron MT41K256M16TW-107 DDR3 chips, each with a capacity of 4Gbit. The two DDR chips are combined to form a 32-bit data bus width, and the read and write data clock frequency between ZYNQ and DDR3 is as high as 533MHz. This configuration can meet the high bandwidth data processing requirements of the system.

To connect with the baseboard, this core board's four board-to-board connectors extend to include a USB port, a Gigabit Ethernet port, an SD card port, and other remaining MIO ports on the PS side; it also extends to include four pairs of ZYNQ high-speed transceiver GTP ports; and almost all 148 I/O ports (BANK13, BANK34, and BANK35) on the PL side. The I/O level of BANK35 can be modified by replacing the LDO chip on the core board to meet different user interface level requirements. For users requiring a large number of I/O ports, this core board is a good choice. Furthermore, the I/O connections feature equal-length and differential traces between the ZYNQ chips and the interfaces, and the core board's size is only 60*60 mm, making it ideal for secondary development.

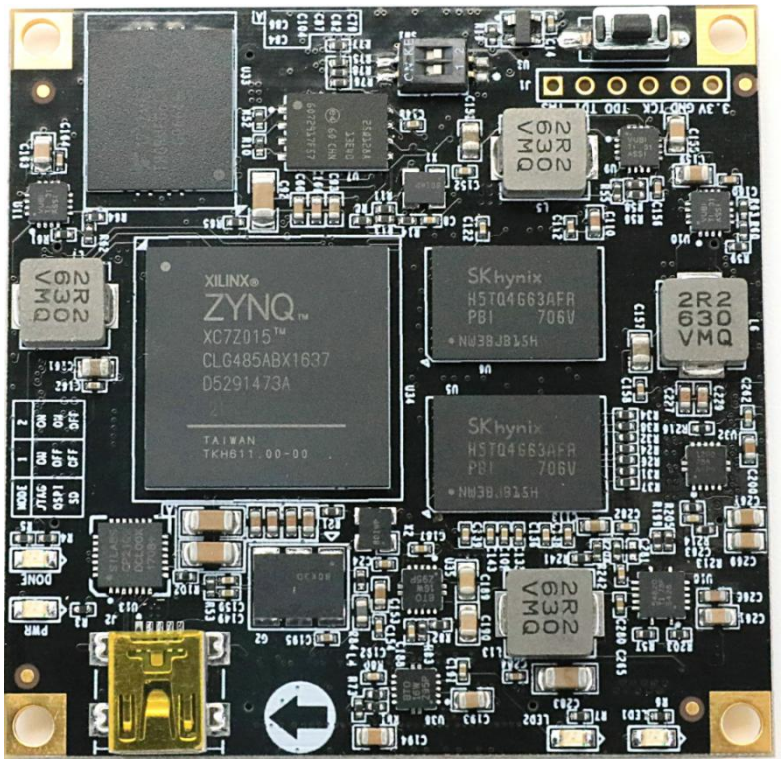


Figure 1.1.1 - AC7015B core board

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1.2 ZYNQ Chip

The development board uses a Xilinx Zynq 7000 series chip , model XC7Z015-2CLG485I. The chip's System-on-PS (PS) integrates two ARM Cortex™-A9 processors, AMBA® interconnect, internal memory, external memory interface, and peripherals. These peripherals mainly include a USB bus interface, Ethernet interface, SD/SDIO interface, I2C bus interface, CAN bus interface, UART interface, GPIO, etc. The PS can operate independently and boot upon power-on or reset. The overall block diagram of the ZYNQ7000 chip is shown in Figure 1.2.1.

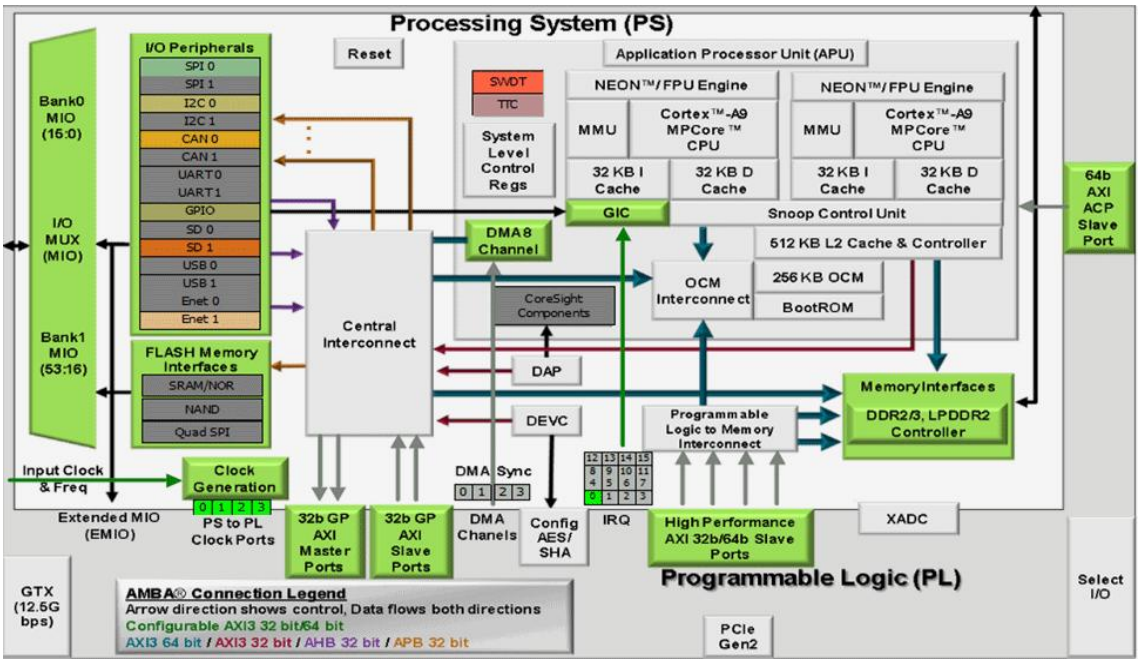


Figure 1.2.1 - Overall block diagram of the ZYNQ 7000 chip

The main parameters of the PS system are as follows:

- Application processors based on ARM dual-core Cortex A9, ARM-v7 architecture up to 766MHz
- Each CPU has 32KB of L1 instruction and data cache, and 512KB of L2 cache shared by both CPUs.
- On-chip boot ROM and 256KB on-chip RAM
- External storage interface, supports 16/32 bit DDR2 and DDR3 interfaces.
- Two Gigabit network cards support: Divergent-Convergent DMA, GMII, RGMII, and SGMII interfaces.
- Two USB 2.0 OTG ports, each supporting up to 12 nodes.
- Two CAN2.0B bus interfaces
- Two SD cards, SDIO, MMC compatible controller
- 2 SPI interfaces, 2 UARTs, 2 I2C interfaces
- 4 groups of 32-bit GPIOs, 54 (32+22) as PS system I/O, 64 connected to PL
- High-bandwidth connections within PS and from PS to PL

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The main parameters of the PL logic section are as follows:

- Logic Cells: 74K;
- Lookup table LUTs: 46,200
- Flip-flops : 92,400
- Multiplier 18x25 MACCs: 160;
- Block RAM: 3.3Mb;
- 4-channel high-speed GTP transceiver, supporting PCIe Gen2x4;
- Two analog-to-digital converters, capable of measuring on-chip voltage, temperature sensing, and up to 17 external differential input channels, 1 Mbps.

The XC7Z015-2CLG485I chip has a speed class of -2, is industrial grade, is packaged in a BGA484 package, and has a pin pitch of 0.8mm. The specific chip model definition of the ZYNQ7000 series is shown in Figure 1.2.2 below .

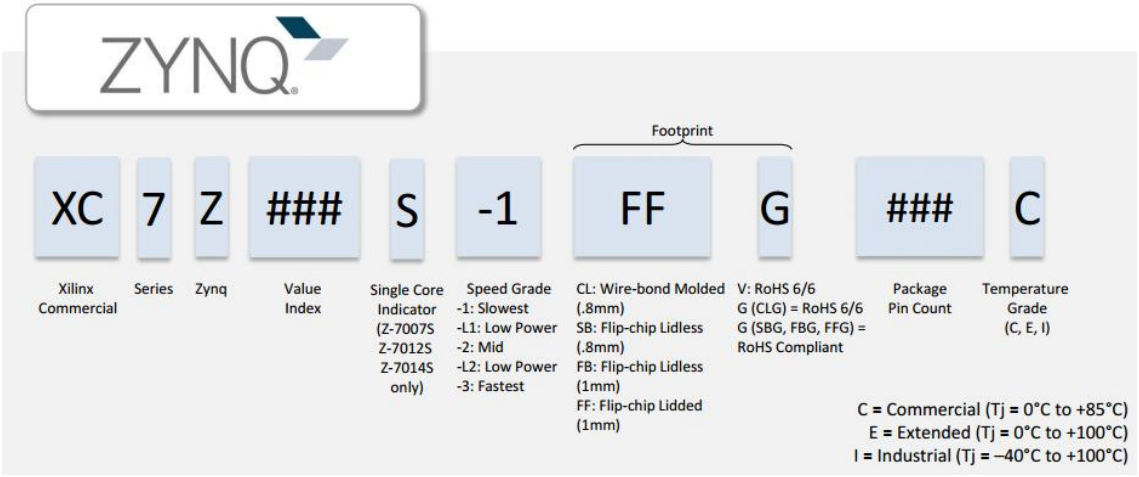


Figure 1.2.2 - ZYNQ model naming rules definition

1.3 DDR3 DRAM

The AC7015B core board features two Micron DDR3 SDRAM chips (totaling 1GB), model MT41K256M16TW-107 (compatible with Micron's MT41J256M16RE-125) .The DDR3 SDRAM has a total bus width of 32 bit. The maximum operating speed of the DDR3 SDRAM is 533 MHz (data rate 1066 Mbps) . This DDR3 memory system is directly connected to the memory interface of the ZYNQ processing system (PS) BANK502. The specific configuration of the DDR3 SDRAM is shown in Table 1.3.1 below .

Designator	Chip Model	Capacity	Factory
U5 , U6	MT41K256M16TW-107	256 M x 16bit	Micron

Table 1.3.1 - DDR3 SDRAM Configuration

The hardware design of DDR3 requires strict consideration of signal integrity. We have fully

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considered matching resistors/terminating resistors,trace impedance control, and trace length control during circuit and PCB design to ensure the high-speed and stable operation of DDR3.

The hardware connection method of DDR3 DRAM is shown in Figure 1.3.1 :

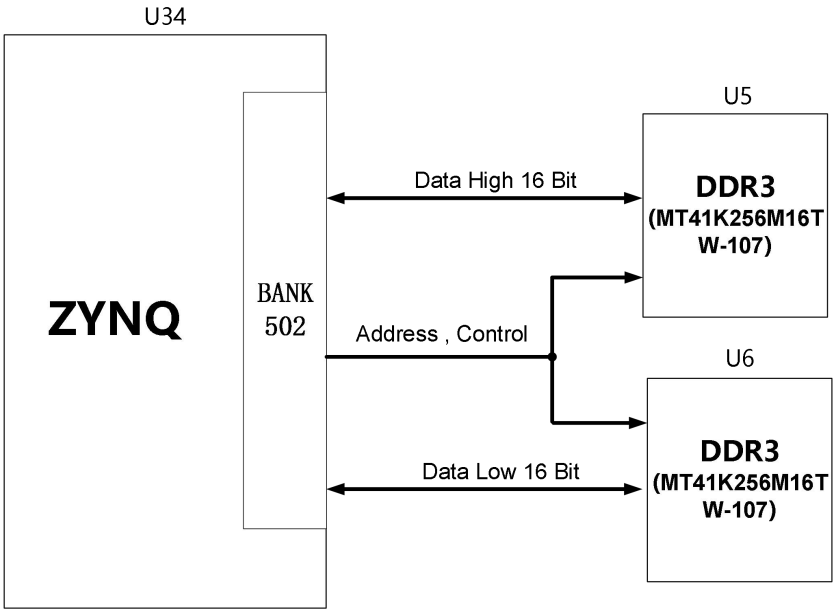


Figure 1.3.1 - Partial Schematic Diagram of DDR3 DRAM

DDR3 DRAM pin assignment:

Signal name	ZYNQ pin name	ZYNQ pin number
DDR3_DQS0_P	PS_DDR_DQS_P0_502	C21
DDR3_DQS0_N	PS_DDR_DQS_N0_502	D21
DDR3_DQS1_P	PS_DDR_DQS_P1_502	H21
DDR3_DQS1_N	PS_DDR_DQS_N1_502	J21
DDR3_DQS2_P	PS_DDR_DQS_P2_502	N21
DDR3_DQS2_N	PS_DDR_DQS_N2_502	P21
DDR3_DQS3_P	PS_DDR_DQS_P3_502	V21
DDR3_DQS 3_N	PS_DDR_DQS_N3_502	W21
DDR3_D0	PS_DDR_DQ0_502	D22
DDR3_D 1	PS_DDR_DQ 1_502	C20
DDR3_D 2	PS_DDR_DQ 2_502	B21
DDR3_D 3	PS_DDR_DQ 3_502	D20

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DDR3_D 4	PS_DDR_DQ 4_502	E20
DDR3_D 5	PS_DDR_DQ 5_502	E22
DDR3_D 6	PS_DDR_DQ 6_502	F21
DDR3_D 7	PS_DDR_DQ 7_502	F22
DDR3_D 8	PS_DDR_DQ 8_502	G21
DDR3_D 9	PS_DDR_DQ 9_502	G22
DDR3_D 1 0	PS_DDR_DQ 10_502	L22
DDR3_D 11	PS_DDR_DQ 11_502	L21
DDR3_D 12	PS_DDR_DQ 12_502	L20
DDR3_D 13	PS_DDR_DQ 13_502	K22
DDR3_D 14	PS_DDR_DQ 14_502	J22
DDR3_D 15	PS_DDR_DQ 15_502	K20
DDR3_D 16	PS_DDR_DQ 16_502	M22
DDR3_D 17	PS_DDR_DQ 17_502	T20
DDR3_D 18	PS_DDR_DQ 18_502	N20
DDR3_D 19	PS_DDR_DQ 19_502	T22
DDR3_D 20	PS_DDR_DQ 20_502	R20
DDR3_D 21	PS_DDR_DQ 21_502	T21
DDR3_D 22	PS_DDR_DQ 22_502	M21
DDR3_D 23	PS_DDR_DQ 23_502	R22
DDR3_D 24	PS_DDR_DQ 24_502	Y20
DDR3_D 25	PS_DDR_DQ 25_502	U22
DDR3_D 26	PS_DDR_DQ 26_502	AA22
DDR3_D 27	PS_DDR_DQ 27_502	U21
DDR3_D 28	PS_DDR_DQ 28_502	W22
DDR3_D 29	PS_DDR_DQ 29_502	W20
DDR3_D 30	PS_DDR_DQ 30_502	V20

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DDR3_D 31	PS_DDR_DQ 31_502	Y22
DDR3_DM0	PS_DDR_DM0_502	B22
DDR3_DM 1	PS_DDR_DM 1_502	H20
DDR3_DM 2	PS_DDR_DM 2_502	P22
DDR3_DM 3	PS_DDR_DM 3_502	AA21
DDR3_A0	PS_DDR_A0_502	M19
DDR3_A 1	PS_DDR_A 1_502	M18
DDR3_A 2	PS_DDR_A 2_502	K19
DDR3_A 3	PS_DDR_A 3_502	L19
DDR3_A 4	PS_DDR_A 4_502	K17
DDR3_A 5	PS_DDR_A 5_502	K18
DDR3_A 6	PS_DDR_A 6_502	J16
DDR3_A 7	PS_DDR_A 7_502	J17
DDR3_A 8	PS_DDR_A 8_502	J18
DDR3_A 9	PS_DDR_A 9_502	H18
DDR3_A 1 0	PS_DDR_A 10_502	J20
DDR3_A 11	PS_DDR_A 11_502	G18
DDR3_A 12	PS_DDR_A 12_502	H19
DDR3_A 13	PS_DDR_A 13_502	F19
DDR3_A 14	PS_DDR_A 14_502	G19
DDR3_BA0	PS_DDR_BA0_502	L16
DDR3_BA1	PS_DDR_BA 1_502	L17
DDR3_BA2	PS_DDR_BA 2_502	M17
DDR3_S0	PS_DDR_CS_B_502	P17
DDR3_R AS	PS_DDR_RAS_B_502	R18
DDR3_CAS	PS_DDR_CAS_B_502	P20
DDR3_WE	PS_DDR_WE_B_502	R19

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DDR3_ODT	PS_DDR_ODT_502	P18
DDR3 RESET	PS_DDR_DRST_B_502	F20
DDR3_CLK0_P	PS_DDR_CKP_502	N19
DDR3_CLK0_N	PS_DDR_CKN_502	N18
DDR3_CKE	PS_DDR_CKE_502	T19

Table 1.3.2 - DDR3 DRAM Pin Assignment

1.4 QSPI Flash

The core board is equipped with a 256 MB Quad-SPI FLASH chip, model W25Q256FVEI , which uses the 3.3V CMOS voltage standard. Due to the non-volatile nature of the QSPI FLASH, it can be used as a system boot device to store the system boot image. These images mainly include the FPGA bit file, ARM application code, and other user data files. Specific models and related parameters of the QSPI FLASH are shown in Table 1.4.1 .

Designator	Chip type	Capacity	Factory
U7	W25Q256FVEI	32M Byte	Winbond

Table 1.4.1 - QSPI Flash Models and Parameters

BANK500 of the ZYNQ chip . In the system design, these PS-side GPIO ports need to be configured as QSPI FLASH interfaces. Figure 1.4.1 shows the QSPI Flash portion in the schematic diagram.

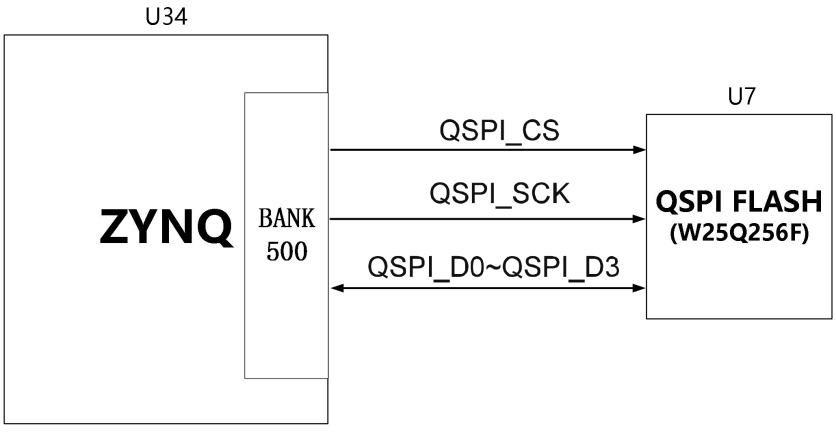


Figure 1.4.1 - QSPI Flash Connection Diagram

Configure chip pin assignments:

Signal name	ZYNQ pin name	ZYNQ pin number
QSPI_SCK	PS_MIO6_500	A19

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QSPI_CS	PS_MIO1_500	A22
QSPI_D0	PS_MIO2_500	A21
QSPI_D1	PS_MIO3_500	F17
QSPI_D2	PS_MIO4_500	E19
QSPI_D3	PS_MIO5_500	A20

Table 1.4.2 - QSPI Flash Pin Configuration

1.5 eMMC Flash

The core board is equipped with a large-capacity 8GB eMMC FLASH chip, model MTFC4GACAAAM-1M , which supports the JEDEC e-MMC V5.0 standard HS-MMC interface and voltage levels of 1.8V or 3.3V . The data width between the eMMC FLASH and ZYNQ is 4 bits. Due to the large capacity and non-volatile nature of the eMMC FLASH , it can be used as a large-capacity storage device in the ZYNQ system , such as storing ARM application programs , system files , and other user data files. Specific models and related parameters of the eMMC FLASH are shown in Table 1.5.1 .

Designator	Chip type	Capacity	Factory
U33	MTFC4GACAAAM-1M	8G Byte	Micron

Table 1.5.1- eMMC Flash Model and Specifications

The eMMC FLASH is connected to the GPIO ports of the PS section BANK501 of the ZYNQ chip . In the system design, these PS-side GPIO ports need to be configured as SD interface ports. Figure 1.5.1 shows the eMMC. The part of the Flash memory shown in the schematic diagram.

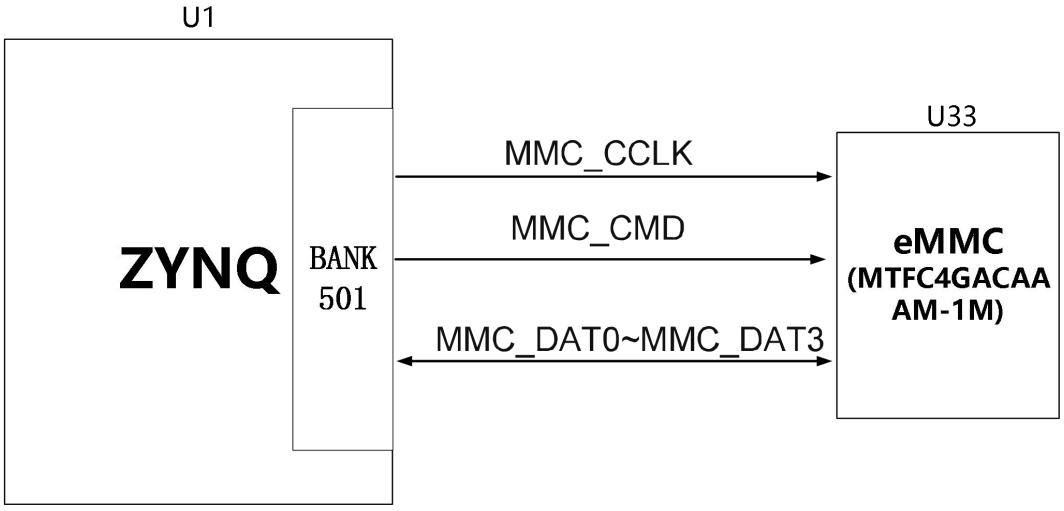


Figure 1.5.1 - Schematic diagram of eMMC Flash connection

Configure chip pin assignments:

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Signal name	ZYNQ pin name	ZYNQ pin number
MMC_CCLK	PS_MIO48_501	D12
MMC_CMD	PS_MIO47_501	B13
MMC_D0	PS_MIO46_501	D11
MMC_D1	PS_MIO49_501	C9
MMC_D2	PS_MIO50_501	D10
MMC_D3	PS_MIO51_501	C13

Table 1.5.2 - eMMC Flash Pin Assignment

1.6 Clock Configuration

The AC7015B core board provides active clocks for the PS system, PL logic section, and GTP transceiver, allowing each component to operate independently. The PS and PL terminals use single-ended crystal oscillators, while the GTP terminal uses a differential crystal oscillator.

PS system clock source

The ZYNQ chip provides a 33.333MHz clock input to the PS section via the X1 crystal oscillator on the development board. The clock input is connected to the PS_CLK_500 pin of the ZYNQ chip's BANK500. Clock pin assignment:

Signal name	ZYNQ pin
PS_GCLK	F16

Table 1.6.1 - PS System Clock Source Pin Assignment

PL system clock source

The AC7015B core board provides a single-ended 50MHz PL system clock source, powered by 3.3V. The crystal oscillator output is connected to the global clock (MRCC) of FPGA BANK13, which can be used to drive user logic circuits within the FPGA . PL clock pin assignment:

Signal name	ZYNQ pin
PL_GCLK	Y14

Table 1.6.2 - PL System Clock Source

GTP Differential Clock

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The AC7015B core board provides a differential 125 MHz GTP reference clock. The differential LVDS clock output is connected to the BANK112 reference clock; this 125 MHz clock can be used as the reference clock for the backplane's fiber optic data communication. GTP clock pin assignment:

Signal name	ZYNQ pin
MGT_CLK 1 _P	U5
MGT_CLK 1 _N	V5

Table 1.6.3 - GTP Differential Clock

1.7 USB to Serial Port

For the AC7015B core board to operate and debug independently, we equipped it with a UART-to-USB interface. This is used for independent power supply and debugging of the core board. The conversion chip is the Silicon Labs CP2102GM USB- UART chip , and the USB interface is a MINI USB interface. It can be connected to the PC 's USB port with a USB cable for independent power supply and serial data communication of the core board. A schematic diagram of the USB UART circuit design is shown below :

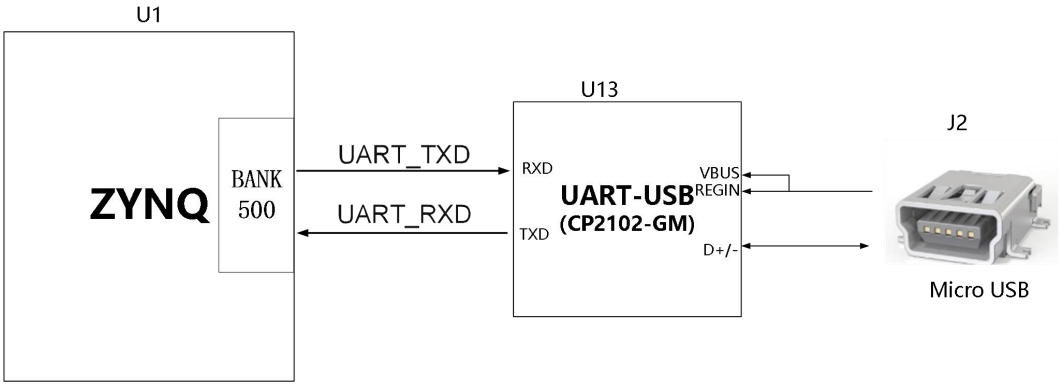


Figure 1.7.1 - Schematic diagram of USB to serial port adapter

ZYNQ pin assignments for UART to serial port conversion:

Signal name	ZYNQ pin name	ZYNQ pin number	Remark
UART_RXD	PS_MIO14_500	B17	UART data input
UART_TXD	PS_MIO15_500	E17	UART data output

Table 1.7.1 - UART to Serial Port Pin Assignment

1.8 LED lights

The AC7015B core board has four red LEDs: one power indicator (PWR), one configuration LED (DONE), and two user LEDs (LED1~LED2). The power indicator lights up when the core board is

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powered on; the configuration LED lights up after the FPGA configuration program is executed. One user LED is connected to the PS's MIO, and the other is connected to the PL's I/O. Users can control the LEDs' on/off state via the program. When the I/O voltage connected to a user LED is high, the LED is off; when the I/O voltage is low, the LED is on. A schematic diagram of the LED hardware connection is shown in Figure 1.8.1 .

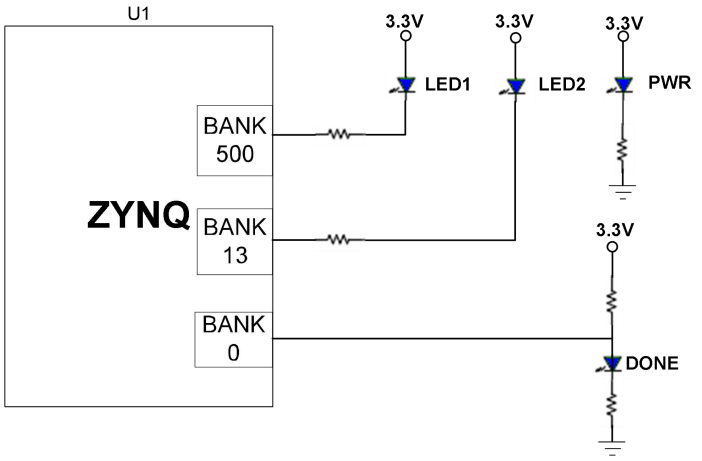


Figure 1.8.1 - Hardware connection diagram of LED lights on the core board

Pin assignment for user LED lights

Signal name	ZYNQ pin name	ZYNQ pin number	Remark
MIO0_LED	PS_MIO0_500	G17	User LED1 light
PL_LED	IO_0_13	T16	User LED2 lights

Table 1.8.1 - Pin Assignments for User LEDs

1.9 Reset button

The AC7015B core board has a reset button and circuit. The reset signal is connected to the PS reset pin of the ZYNQ chip, allowing the user to reset the ZYNQ system using this button. When the reset button is pressed, the reset chip generates a low-level reset signal to the ZYNQ chip. A schematic diagram of the connection between the reset button and the reset chip is shown in Figure 1.9.1 .

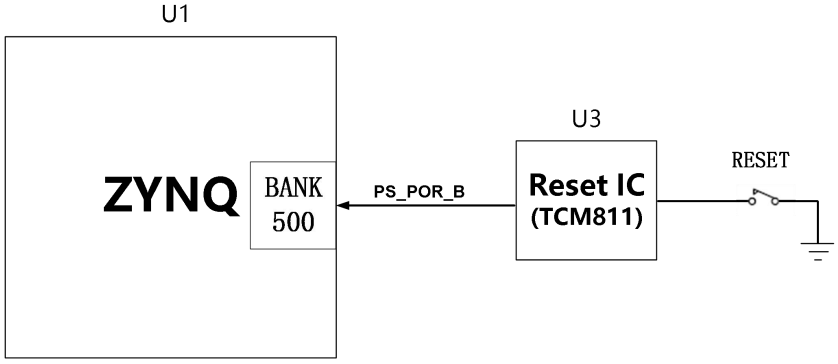


Figure 1.9.1 - Schematic diagram of reset button connection

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ZYNQ pin assignment for the reset button

Signal name	ZYNQ pin name	ZYNQ pin number	Remark
PS_POR_B	PS_POR_B_500	B18	ZYNQ system reset signal

Table 1.9.1 - Pin Assignment for Reset Button

1.10 JTAG Interface

The AC7015B core board also includes a JTAG test connector J1 for independent JTAG downloading and debugging. This involves six signals: TMS, TDI, TDO, TCK, GND, and +3.3V.

The JTAG interface J1 on the core board uses a 6-pin, 2.54mm pitch single-row test header. Users needing to connect and debug via JTAG on the core board must solder a 6-pin single-row header.

1.11 DIP switch configuration

The AC7015B core board has a 2-position DIP switch SW1 used to configure the boot mode of the ZYNQ system. The AC7015B system development platform supports three boot modes. These three boot modes are JTAG debugging mode, QSPI FLASH and SD card boot modes. After power-on, the XC7Z015 chip detects the level of the MIO ports (MIO5 and MIO4) to determine the boot mode. Users can select different boot modes using the DIP switch SW1 on the core board. The SW1 boot mode configuration is shown in Table 1.11.1 below .

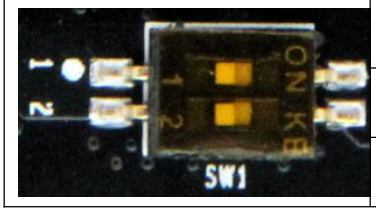
SW1	DIP switch position (1, 2)	MIO5, MIO4 level	Startup mode
	ON, ON	0, 0	JTAG
	OFF, OFF	1, 1	SD card
	OFF, ON	1, 0	QSPI FLASH

Table 1.11.1 - SW1 Boot Mode Configuration

1.12 Power Supply

The AC7015B core board is powered by DC 5V. When used alone, it is powered via the Mini USB interface; when connected to the baseboard, it is powered via the baseboard. Please note that the Mini USB and baseboard should not be powered simultaneously to avoid damage. The power supply design diagram on the board is shown in Figure 1.12.1 below :

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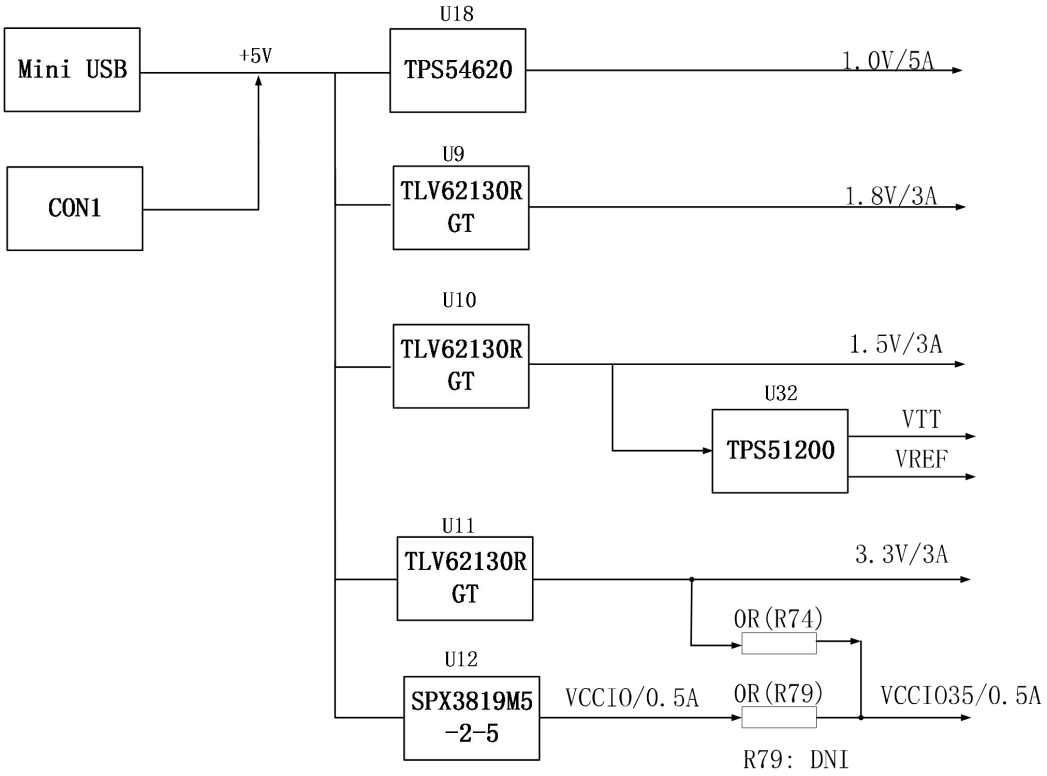


Figure 1.12.1 - Power interface section in the schematic diagram

The development board is powered by +5V, which is converted into four power supplies: +1.0V, +1.8V, +1.5V, and +3.3V via four DC/DC power chips (TPS54620 and TLV62130RGT). The +1.0V output current can reach up to 5A, while the other three power supplies have a current of 3A. Additionally, a single LDO (SPX3819M5-2-5) generates a 2.5V VCCIO power supply. This 2.5V VCCIO power supply is primarily reserved for the FPGA's BANK35 bank power supply. Users can select the BANK35 power supply using two 0-ohm resistors (R74 and R79). By default, R74 is installed on the development board, while R79 is not installed, so the BANK35 power supply is +3.3V. Users can change the resistors to make the BANK35's I/O input/output voltage standard 2.5V. The 1.5V is generated by TI's TPS51200 to provide the VTT and VREF voltages required for DDR3. The functions of each power distribution unit are shown in the table below:

Power supply	Function
+1.0V	ZYNQ PS and PL core voltage
+1.8V	ZYNQ PS and PL auxiliary voltages, BANK501 IO voltages, eMMC
+3.3V	ZYNQ Bank0, Bank500, Bank13, and Bank34's VCCIO, QSPI FLASH, and Clock crystal oscillators
+1.5V	DDR3, ZYNQ Bank501
VREF, VTT (+0.75V)	DDR3
VCCIO(+2.5V)	Reserved for ZYNQ Bank35

Table 1.12.1 - Power Function Allocation

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Because ZYNQ FPGAs have power-on sequence requirements, we have designed the circuit according to the chip's power requirements, with the power-on sequence being + 1.0V -> + 1.8V -> (+ 1.5V , + 3.3V , VCCIO) to ensure the chip's normal operation.

1.13 Structural Diagram

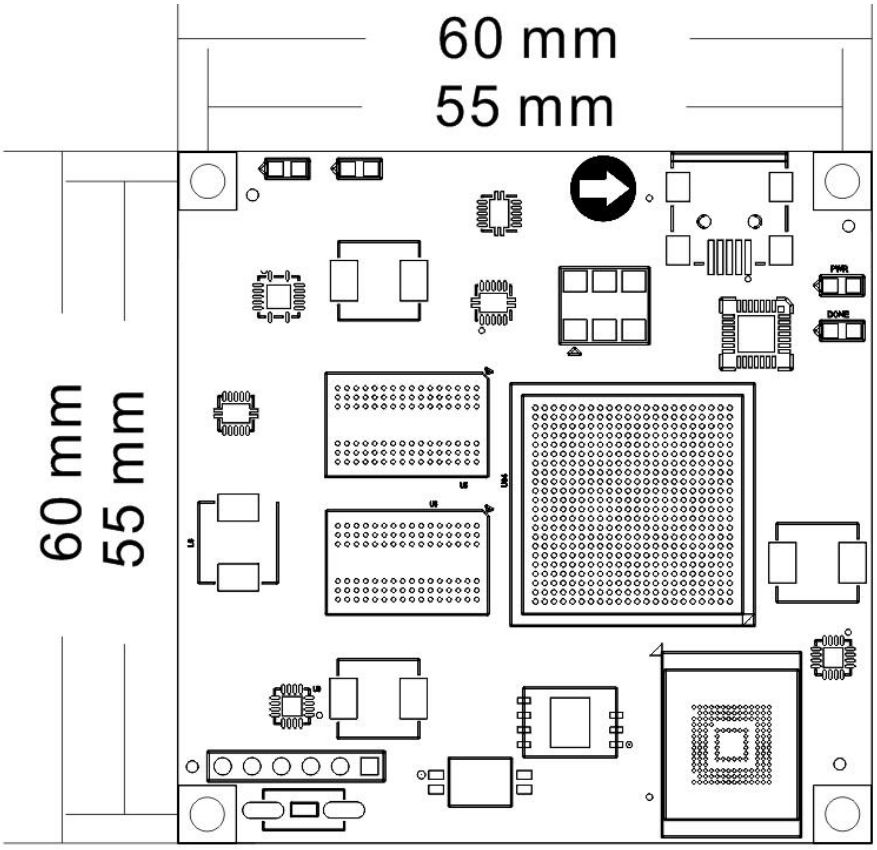


Figure 1.13.1 - Core Plate Structure Diagram

1.14 Connector Pin Definitions

The core board has four high-speed expansion ports, connected to the baseboard via four 80-pin board-to-board connectors (CON1~CON4), with a pin pitch of 0.5mm. CON1 connects to the power input, PS MIO signal, and JTAG signal. CON2~CON4 connect to the PB's BANK13, BANK34, and BANK35 I/O signals and GTP transceiver signals. The BANK35 I/O level can be changed by replacing the LDO chip (U12) on the board; the default is 3.3V.

Pin assignment of CON1 connector

CON1 pin	Signal name	ZYNQ pin number	CON1 pin	Signal name	ZYNQ pin number
1	+5V	-	2	+5V	-
3	+5V	-	4	+5V	-
5	+5V	-	6	+5V	-

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7	+5V	-	8	+5V	-
9	GND	-	10	GND	-
11	PS_MIO13	A17	12	ETH_TXD0	E14
13	PS_MIO12	C18	14	ETH_TXD1	A16
15	-	-	16	ETH_TXD2	E13
17	-	-	18	ETH_TXD3	A15
19	GND	-	20	GND	-
21	-	-	22	ETH_TXCK	D17
23	-	-	24	ETH_TXCTL	F12
25	-	-	26	ETH_RXD3	A10
27	-	-	28	ETH_RXD2	F11
29	GND	-	30	GND	-
31	PS_MIO7	D18	32	ETH_RXD1	B16
33	PS_MIO8	E18	34	ETH_RXD0	E12
35	PS_MIO9	C19	36	ETH_RXCTL	D16
37	PS_MIO11	B19	38	ETH_RXCK	A9
39	GND	-	40	GND	-
41	-	-	42	ETH_MDC	D13
43	-	-	44	ETH_MDIO	C11
45	-	-	46	OTG_STP	A12
47	-	-	48	OTG_DIR	E15
49	GND	-	50	GND	-
51	XADC_VP	L12	52	OTG_CLK	A14
53	XADC_VN	M11	54	OTG_NXT	F14
55	-	-	56	OTG_DATA0	C16
57	PS_MIO10	G16	58	OTG_DATA1	G11
59	GND	-	60	GND	-

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61	SD_CLK	E9	62	OTG_DATA2	B11
63	SD_D1	B12	64	OTG_DATA3	F9
65	SD_D0	D15	66	OTG_DATA4	A11
67	SD_CMD	C15	68	OTG_DATA5	B9
69	GND	-	70	GND	-
71	SD_D3	B14	72	OTG_DATA6	F10
73	SD_D2	E10	74	OTG_DATA7	C10
75	-	-	76	-	-
77	FPGA_TMS	H10	78	FPGA_TCK	H11
79	FPGA_TDO	G9	80	FPGA_TDI	H9

Table 1.14.1 - Pin Assignment of CON1 Connector

CON2 connector pin assignment

CON2 pin	Signal name	ZYNQ pin number	CON2 pin	Signal name	ZYNQ pin number
1	B34_L19_N	N5	2	B3 4_L1 3_N	T1
3	B34_L19_P	N6	4	B3 4_L1 3_P	T2
5	B34_L2_P	J7	6	B3 4_L 21_N	N3
7	B34_L2_N	J6	8	B3 4_L 21_P	N4
9	GND	-	10	GND	-
11	B34_L 1_P	J8	12	B3 4_L1 2_N	L4
13	B34_L 1_N	K8	14	B3 4_L1 2_P	L5
15	B3 4_L 11_N	K3	16	B3 5_L 4_P	G8
17	B3 4_L 11_P	K4	18	B3 5_L 4_N	G7
19	GND	-	20	GND	-
21	B3 5_L 24_P	H1	22	B3 5_L 19_P	H4
23	B3 5_L 24_N	G1	24	B3 5_L 19_N	H3
25	B3 4_L 8_N	J1	26	B3 5_L 22_P	G3
27	B3 4_L 8_P	J2	28	B3 5_L 22_N	G2

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29	GND	-	30	GND	-
31	B3 5_IO25	H5	32	B3 5_L 21_P	E4
33	B3 5_IO0	H6	34	B3 5_L 21_N	E3
35	B3 5_L20_P	G4	36	B3 5_L 2_P	D7
37	B3 5_L 20_N	F4	38	B3 5_L 2_N	D6
39	GND	-	40	GND	-
41	B 35_L 5_P	F5	42	B3 5_L 23_P	F2
43	B 35_L 5_N	E5	44	B3 5_L 23_N	F1
45	B 35_L 6_P	G6	46	B3 5_L 17_P	E2
47	B 35_L 6_N	F6	48	B3 5_L 17_N	D2
49	GND	-	50	GND	-
51	B 35_L 1_N	E7	52	B3 5_L 16_P	D1
53	B 35_L 1_P	F7	54	B3 5_L 16_N	C1
55	B 35_L 14_P	D3	56	B3 5_L 18_N	B1
57	B 35_L 14_N	C3	58	B3 5_L 18_P	B2
59	GND	-	60	GND	-
61	B 35_L 12_N	C4	62	B3 5_L 15_N	A1
63	B 35_L 12_P	D5	64	B3 5_L 15_P	A2
65	B 35_L 11_N	C5	66	B3 5_L 13_N	B3
67	B 35_L 11_P	C6	68	B3 5_L 13_P	B4
69	GND	-	70	GND	-
71	B 35_L 3_P	E8	72	B3 5_L 10_N	A4
73	B 35_L 3_N	D8	74	B3 5_L 10_P	A5
75	B 35_L 8_P	B7	76	B3 5_L 9_N	A6
77	B 35_L 8_N	B6	78	B3 5_L 9_P	A7
79	B 35_L 7_P	C8	80	B 35_L 7_N	B8

Table 1.14.2 - Pin Assignment of CON2 Connector

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CON3 connector pin assignment

CON3 pin	Signal name	ZYNQ pin number	CON3 pin	Signal name	ZYNQ pin number
1	MGT_CLK0_P	U9	2	-	-
3	MGT_CLK0_N	V9	4	GND	-
5	GND	-	6	MGT_RX2_ N	AB9
7	-	-	8	MGT_RX2_p	AA9
9	GND	-	10	GND	-
11	MGT_RX1_P	W8	12	-	-
13	MGT_RX1_N	Y8	14	GND	-
15	GND	-	16	MGT_TX2_P	AA5
17	-	-	18	MGT_TX2_N	AB5
19	GND	-	20	GND	-
21	MGT_TX1_P	W4	22	-	-
23	MGT_TX1_N	Y4	24	GND	-
25	GND	-	26	MGT_RX3_N	Y6
27	-	-	28	MGT_RX3_P	W6
29	GND	-	30	GND	-
31	MGT_RX0_P	AA7	32	-	-
33	MGT_RX0_N	AB7	34	GND	-
35	GND	-	36	MGT_TX3_P	W2
37	-	-	38	MGT_TX3_N	Y2
39	GND	-	40	GND	-
41	MGT_TX0_P	AA3	42	-	-
43	MGT_TX0_N	AB3	44	-	-

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45	GND		46	B 34_L3_P	K7
47	-		48	B 34_L3_N	L7
49	GND	-	50	GND	-
51	B 34_L4_N	M6	52	-	-
53	B 34_L4_P	L6	54	-	-
55	-	-	56	B 34_L14_N	U1
57	-	-	58	B 34_L14_P	U2
59	GND	-	60	GND	-
61	B 34_L20_N	P5	62	-	
63	B 34_L20_P	P6	64	-	
65	-	-	66	B 34_L9_N	K2
67	-	-	68	B 34_L9_P	J3
69	GND	-	70	GND	-
71	B 34_L10_N	L1	72	-	-
73	B 34_L10_P	L2	74	-	-
75	-	-	76	-	-
77	B 34_IO25	R8	78	B 34_L7_P	J5
79	B 34_IO0	H8	80	B 34_L7_N	K5

Table 1.14.3 - Pin Assignment of CON3 Connector

CON4 connector pin assignment

CON4 pin	Signal name	ZYNQ pin number	CON4 pin	Signal name	ZYNQ pin number
1	B13_L22_N	U18	2	B13_L20_P	U19
3	B13_L22_P	U17	4	B13_L20_N	V19
5	B13_L23_P	V16	6	B13_L19_N	T17
7	B13_L23_N	W16	8	B13_L19_P	R17

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9	GND	-	10	GND	-
11	B13_L14_N	AA17	12	B13_L18_N	AA20
13	B13_L14_P	AA16	14	B13_L18_P	AA19
15	B13_L13_N	Y19	16	B13_L15_N	AB22
17	B13_L13_P	Y18	18	B13_L15_P	AB21
19	GND	-	20	GND	-
21	B13_L11_N	AA15	22	B13_L21_P	V18
23	B13_L11_P	AA14	24	B13_L21_N	W18
25	B13_L17_P	AB16	26	B13_L24_P	W17
27	B13_L17_N	AB17	28	B13_L24_N	Y17
29	GND	-	30	GND	-
31	B13_L16_N	AB19	32	B13_L2_P	V15
33	B13_L16_P	AB18	34	B13_L2_N	W15
35	B34_L22_P	M4	36	B13_L9_N	AB14
37	B34_L22_N	M3	38	B13_L9_P	AB13
39	GND	-	40	GND	-
41	B13_L12_N	Y15	42	B13_L6_N	U14
43	B13_IO25	U16	44	B13_L6_P	U13
45	B34_L6_P	M8	46	B34_L23_P	R5
47	B34_L6_N	M7	48	B34_L23_N	R4
49	GND	-	50	GND	-
51	B13_L1_N	V14	52	B13_L8_N	AB12
53	B13_L1_P	V13	54	B13_L8_P	AA12
55	B13_L7_N	AB11	56	B34_L17_N	R2
57	B13_L7_P	AA11	58	B34_L17_P	R3
59	GND	-	60	GND	-
61	B34_L24_P	P7	62	B34_L5_P	N8

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63	B34_L24_N	R7	64	B34_L5_N	P8
65	B13_L4_P	V11	66	B34_L18_P	P3
67	B13_L4_N	W11	68	B34_L18_N	P2
69	GND	-	70	GND	-
71	B13_L3_P	W12	72	B13_L10_P	Y12
73	B13_L3_N	W13	74	B13_L10_N	Y13
75	B13_L5_N	U12	76	B34_L15_N	M1
77	B13_L5_P	U11	78	B34_L15_P	M2
79	B34_L16_N	P1	80	B34_L16_P	N1

Table 1.14.4 - Pin Assignment for CON4 Connector

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02 Expansion Board

2.1 Introduction

Through the preceding functional overview, we can understand the functions of the expansion board.

- 1 PCIe x2 interface
- 2-way fiber optic interface
- 2-way 10 /100M /1000M Ethernet RJ-45 interfaces
- 1 HDMI video output interface
- 1 HDMI video input interface
- 4-way USB HOST interface
- 1-channel USB UART communication interface
- 1-channel SD card interface
- 1- channel 40-pin expansion port
- JTAG debugging interface
- 2 independent buttons
- 5 user LED lights

2.2 Gigabit Ethernet interface

The AX7015B baseboard has two Gigabit Ethernet interfaces. One interface connects to the PS system, and the other connects to the PL's logic I/O port. The Gigabit Ethernet interface connected to the PL needs to be programmed to be attached to the ZYNQ's AXI bus system via IP address.

The Ethernet chip uses JL Semiconductor's industrial-grade Ethernet GPHY chip (JL2121-N040I) to provide network communication services. The Ethernet PHY chip on the PS side connects to the GPIO interface of the ZYNQ's PS-side BANK501. The Ethernet PHY chip on the PL side connects to the BANK35's I/O port. The JL2121 chip supports 10/100/1000 Mbps network transmission rates and communicates with the Zynq7000 system's MAC layer via the RGMII interface. The JL2121 supports MDI/MDX auto-adaptation, various speed auto-adaptation, Master/Slave auto-adaptation, and supports PHY register management via the MDIO bus.

Upon power-up, the JL2121 detects the voltage levels of certain I/O pins to determine its operating mode. Table 2.2.1 describes the default settings of the GPHY chip after power-up.

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Configure Pin	illustrate	Configuration value
RXD3_ADR0 RXC_ADR1 RXCTL_ADR2	PHY address in MDIO/MDC mode	PHY Address is 001
RXD1_TXDLY	TX clock 2ns delay	Delay
RXD0_RXDLY	RX clock 2ns delay	Delay

Table 2.2.1 - Default Configuration Values for PHY Chip

When the network is connected to Gigabit Ethernet, data transmission between the ZYNQ and the JL2121 PHY chip is conducted via the RGMII bus, with a transmission clock of 125MHz. Data is sampled on both the rising and falling edges of the clock.

When the network is connected to 100Mbps Ethernet, data transmission between the ZYNQ and the JL2121 PHY chip is conducted via the RMII bus, with a transmission clock of 25MHz. Data is sampled on both the rising and falling edges of the clock. Figure 2.2.1 shows a schematic diagram of a single-channel Ethernet PHY chip connection on the ZYNQ PS side.

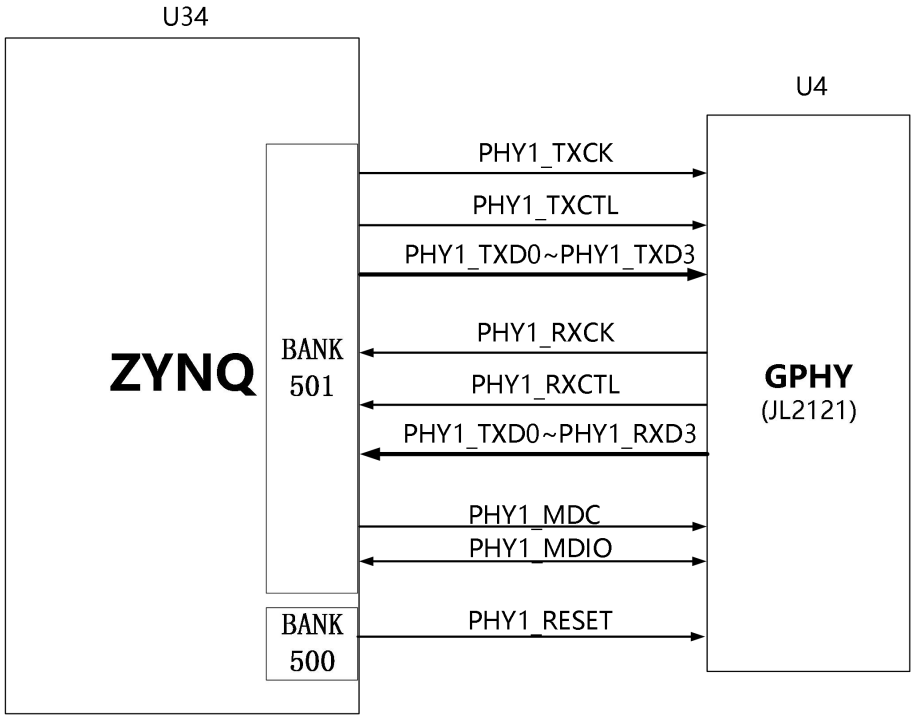


Figure 2.2.1 - Schematic diagram of ZYNQ PS system and GPHY connection

Figure 2.2.2 shows a schematic diagram of the connection of a single Ethernet PHY chip on the ZYNQ PL terminal:

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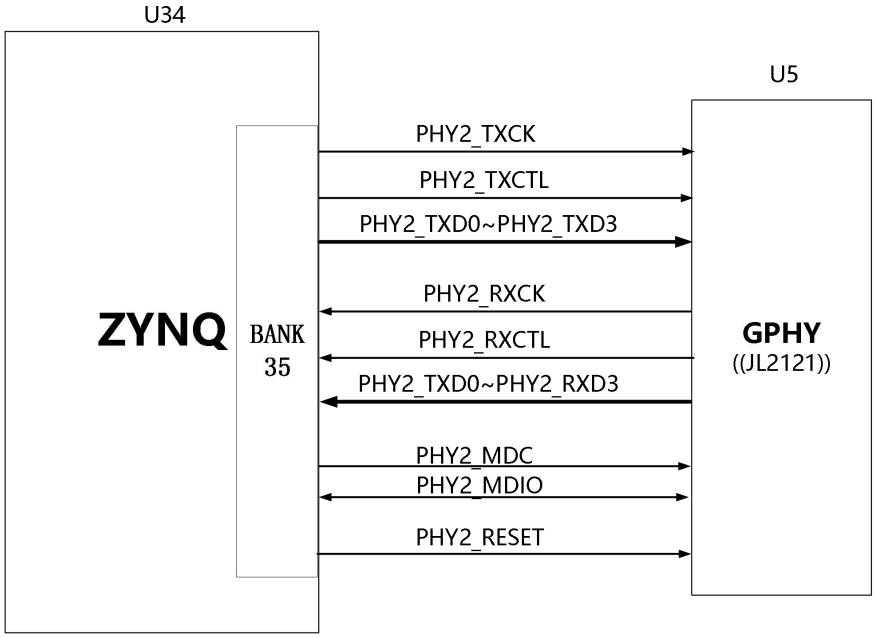


Figure 2.2.2 - Schematic diagram of ZYNQ PL terminal connection to 4 GPHY

The pin assignments for Gigabit Ethernet on the PS side are as follows:

Signal name	ZYNQ pin name	ZYNQ pin number	Remark
PHY1_TXCK	PS_MIO16_501	D17	RGMII Transmit Clock
PHY1_TXD0	PS_MIO1 7_501	E14	Send data bit0
PHY1_TXD1	PS_MIO1 8_501	A16	Send data bit1
PHY1_TXD2	PS_MIO1 9_501	E13	Send data bit2
PHY1_TXD3	PS_MIO 20_501	A15	Send data bit 3
PHY1_TXCTL	PS_MIO 21_501	F12	Send enable signal
PHY1_RXCK	PS_MIO 22_501	A9	RGMII Receive Clock
PHY1_RXD0	PS_MIO 23_501	E12	Receive data Bit0
PHY1_RXD1	PS_MIO 24_501	B16	Receive data Bit1
PHY1_RXD2	PS_MIO 25_501	F11	Receive data Bit2
PHY1_RXD3	PS_MIO 26_501	A10	Receive data Bit3
PHY1_RXCTL	PS_MIO 27_501	D16	Received data valid signal
PHY1_MDC	PS_MIO 52_501	D13	MDIO manages the clock

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PHY1_MDIO	PS_MIO 53_501	C11	MDIO Management Data
PHY1_RESET	PS_MIO7	D18	Reset signal

Table 2.2.2 - PS-side Gigabit Ethernet Pin Assignment

The Gigabit Ethernet pin assignments for the PL side are as follows:

Signal name	ZYNQ pin name	ZYNQ pin number	Remark
PHY2_TXCK	B35_L16_P	D1	RGMII Transmit Clock
PHY2_TXD0	B35_L23_P	F2	Send data bit0
PHY2_TXD1	B35_L23_N	F1	Send data bit1
PHY2_TXD2	B35_L17_P	E2	Send data bit2
PHY2_TXD3	B35_L17_N	D2	Send data bit 3
PHY2_TXCTL	B35_L16_N	C1	Send enable signal
PHY2_RXCK	B35_L13_P	B4	RGMII Receive Clock
PHY2_RXD0	B35_L15_P	A2	Receive data Bit0
PHY2_RXD1	B35_L15_N	A1	Receive data Bit1
PHY2_RXD2	B35_L18_P	B2	Receive data Bit2
PHY2_RXD3	B35_L18_N	B1	Receive data Bit3
PHY2_RXCTL	B35_L13_N	B3	Received data valid signal
PHY2_MDC	B35_L7_P	C8	MDIO manages the clock
PHY2_MDIO	B35_L 8 _ N	B8	MDIO Management Data
PHY2_RESET	B35_L8_P	B7	Reset signal

Table 2.2.3 - Gigabit Ethernet Pin Assignment for PL Terminal

2.3 USB 2.0 Host Interface

The AX7015B baseboard has four USB 2.0 host ports. The USB 2.0 transceiver uses a 1.8V, high-speed USB3320C-EZK chip that supports the ULPI standard interface. This is further expanded into four USB host ports via a USB2514 USB hub chip . The ZYNQ's USB bus interface connects to the USB3320C-EZK transceiver , enabling high-speed USB 2.0 host mode data communication . The USB3320C 's data and control signals are connected to the BANK501 I/O port on the ZYNQ chip's PS side. The USB interface differential signals (DP/DM) are connected to the USB2514 chip to expand into four USB ports. Two 24MHz crystal oscillators provide the system clock for both the

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USB3320C and USB2514 chips .

The baseboard provides four USB HOST ports , all of which are flat USB Type A connectors , allowing users to connect different USB Slave peripherals (such as USB mice and USB keyboards) simultaneously . Additionally , the baseboard provides +5V power to each USB port. A schematic diagram of the connection between the ZYNQ processor , the USB3320C-EZK chip, and the USB2514 chip is shown in Figure 2.3.1 .

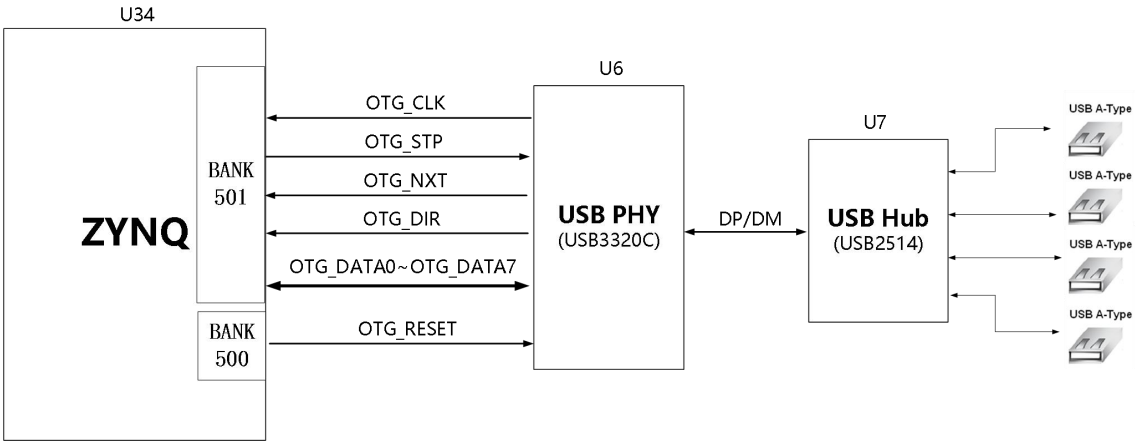


Figure 2.3.1 - Schematic diagram of the connection between Zynq7000 and USB chip

USB 2.0 pin assignment:

Signal name	ZYNQ pin name	ZYNQ pin number	Remark
OTG_DATA4	PS_MIO28_501	A11	USB data bit 4
OTG_DIR	PS_MIO29_501	E15	USB data direction signal
OTG_STP	PS_MIO30_501	A12	USB stop signal
OTG_NXT	PS_MIO31_501	F14	USB next data signal
OTG_DATA0	PS_MIO32_501	C16	USB data bit 0
OTG_DATA1	PS_MIO33_501	G11	USB data bit 1
OTG_DATA2	PS_MIO34_501	B11	USB data bit 2
OTG_DATA3	PS_MIO35_501	F9	USB data bit 3
OTG_CLK	PS_MIO36_501	A14	USB clock signal
OTG_DATA5	PS_MIO37_501	B9	USB data bit 5
OTG_DATA6	PS_MIO38_501	F10	USB data bit 6
OTG_DATA7	PS_MIO39_501	C10	USB data bit 7

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OTG_RESETN	PS_MIO8_500	E18	USB reset signal

Table 2.3.1 - USB 2.0 Pin Assignment

2.4 HDMI output interface

The HDMI output interface is implemented using the SIL9134 HDMI (DVI) encoding chip from Silion Image, which supports up to 1080P@60Hz output and 3D output.

The SIL9134's video digital interface, audio digital interface, and I2C configuration interface are connected to the BANK34/35 IO pins of the ZYNQ7000 PL section. The ZYNQ7000 system uses the I2C pins to initialize and control the SIL9134. A schematic diagram of the hardware connection between the SIL9134 chip and the ZYNQ7000 is shown in Figure 2.4.1 below .

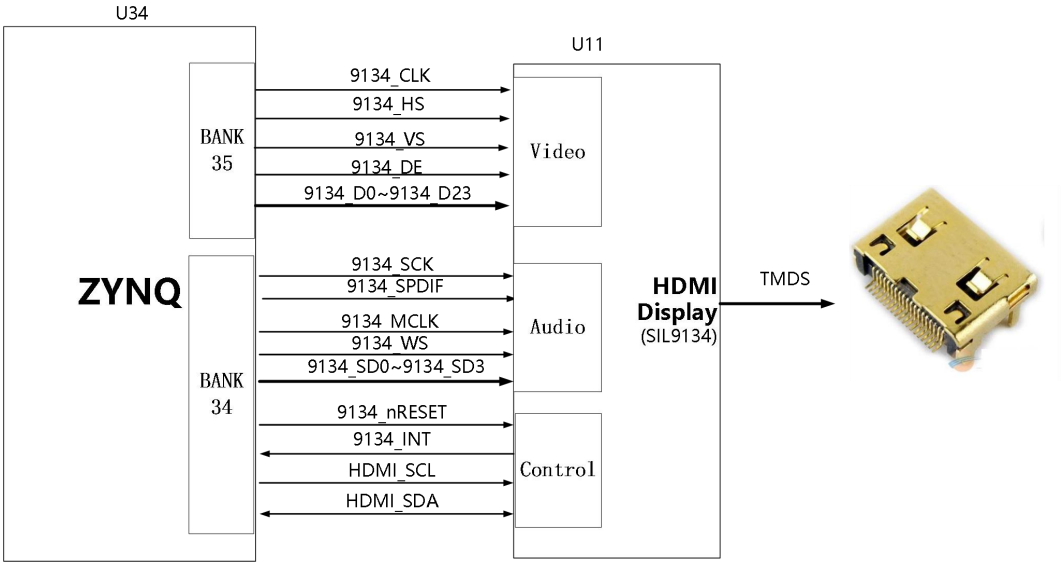


Figure 2.4.1 - Schematic diagram of HDMI interface design

ZYNQ pin assignment:

Signal name	ZYNQ pin name	ZYNQ pin number	Remark
9134_CLK	B35_L24_P	H1	9134 Video Signal Clock
9134_HS	B35_L21_P	E4	9134 Video Horizontal Sync
9134_VS	B35_L21_N	E3	9134 Video Vertical Sync
9134_DE	B35_L22_N	G2	9134 Video Data Enable
9134_D[0]	B35_L22_P	G3	9134 Video Data 0
9134_D[1]	B35_L19_N	H3	9134 Video Data 1
9134_D[2]	B35_L19_P	H4	9134 Video Data 2

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9134_D[3]	B35_L4_N	G7	9134 Video Data 3
9134_D[4]	B35_L4_P	G8	9134 Video Data 4
9134_D[5]	B35_L24_N	G1	9134 Video Data 5
9134_D[6]	B35_IO25	H5	9134 Video Data 6
9134_D[7]	B35_IO0	H6	9134 Video Data 7
9134_D[8]	B35_L20_P	G4	9134 Video Data 8
9134_D[9]	B35_L20_N	F4	9134 Video Data 9
9134_D[10]	B35_L5_P	F5	9134 Video Data 10
9134_D[11]	B35_L5_N	E5	9134 Video Data 11
9134_D[12]	B35_L6_P	G6	9134 Video Data 12
9134_D[13]	B35_L6_N	F6	9134 Video Data 13
9134_D[14]	B35_L1_N	E7	9134 Video Data 14
9134_D[15]	B35_L1_P	F7	9134 Video Data 15
9134_D[16]	B35_L14_P	D3	9134 Video Data 16
9134_D[17]	B35_L14_N	C3	9134 Video Data 17
9134_D[18]	B35_L12_N	C4	9134 Video Data 18
9134_D[19]	B35_L12_P	D5	9134 Video Data 19
9134_D[20]	B35_L11_N	C5	9134 Video Data 20
9134_D[21]	B35_L11_P	C6	9134 Video Data 21
9134_D[22]	B35_L3_P	E8	9134 Video Data 22
9134_D[23]	B35_L3_N	D8	9134 Video Data 23
9134_SCK	B34_L2_N	J6	9134 Audio I2S Clock
9134_SPDIF	B34_L21_N	N3	9134 Audio S/PDIF Input
9134_MCLK	B34_L21_P	N4	9134 Audio Master Clock Input
9134_WS	B34_L2_P	J7	9134 Audio I2S Word Select
9134_SD0	B34_L19_N	N5	9134 Audio I2S Data
9134_SD1	B34_L19_P	N6	9134 Audio I2S Data

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9134_SD2	B34_L13_N	T1	9134 Audio I2S Data
9134_SD3	B34_L13_P	T2	9134 Audio I2S Data
9134_nRESET	B34_L12_N	L4	9134 Reset Signal
9134_INT	B34_L12_P	L5	9134 Interrupt Signal
HDMI_SCL	B34_L1_P	J8	9134 I2C Control Clock
HDMI_SDA	B34_L1_N	K8	9134 I2C Control Data

Table 2.4.1 - HDMI Interface Pin Assignment

2.5 HDMI Input Port

For the HDMI input interface, we used the SIL9013 HDMI decoding chip from Silion Image, which supports up to 1080P@60Hz input and supports data output in different formats.

The SIL9013's IIC configuration interface is also connected to the BANK13 IO of the FPGA. ZYNQ initializes and controls the SIL9013 through I2C bus programming. The hardware connection of the HDMI input interface is shown in Figure 2.5.1 .

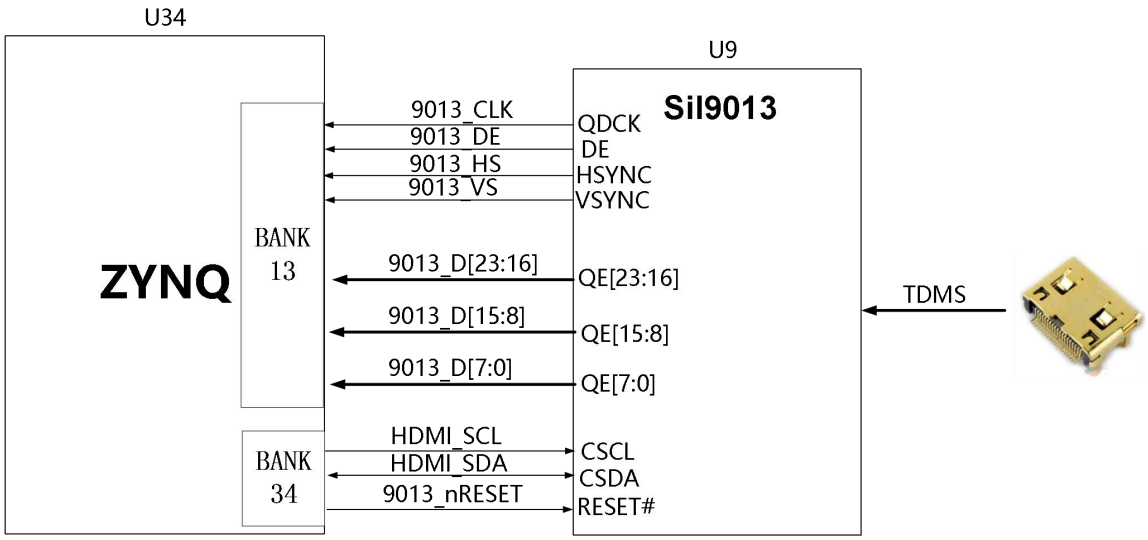


Figure 2.5.1 - HDMI Input Schematic Diagram

ZYNQ pin assignment:

Signal name	ZYNQ pin name	ZYNQ pin number	Remark
9013_nRESET	B34_L16_N	P1	9013 reset signal
9013_CLK	B13_L14_P	AA16	9013 Video Signal Clock
9013_HS	B13_L20_P	U19	9013 Video Signal Horizontal Synchronization

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9013_VS	B13_L22_N	U18	9013 Video Signal Column Synchronization
9013_DE	B13_L20_N	V19	9013 video signal valid
9013_D [0]	B13_L22_P	U17	9013 Video signal data 0
9013_D [1]	B13_L23_P	V16	9013 Video Signal Data 1
9013_D [2]	B13_L23_N	W16	9013 Video Signal Data 2
9013_D [3]	B13_L14_N	AA17	9013 Video Signal Data 3
9013_D [4]	B13_L13_N	Y19	9013 Video Signal Data 4
9013_D [5]	B13_L13_P	Y18	9013 video signal data 5
9013_D [6]	B13_L11_N	AA15	9013 video signal data 6
9013_D [7]	B13_L11_P	AA14	9013 Video Signal Data 7
9013_D [8]	B13_L17_P	AB16	9013 video signal data 8
9013_D [9]	B13_L17_N	AB17	9013 video signal data 9
9013_D [10]	B13_L16_N	AB19	9013 video signal data 10
9013_D [11]	B13_L16_P	AB18	9013 Video Signal Data 11
9013_D [12]	B13_L12_N	Y15	9013 Video Signal Data 12
9013_D [13]	B13_IO25	U16	9013 video signal data 13
9013_D [14]	B13_L1_N	V14	9013 video signal data 14
9013_D [15]	B13_L1_P	V13	9013 video signal data 15
9013_D [16]	B13_L7_N	AB11	9013 video signal data 16
9013_D [17]	B13_L7_P	AA11	9013 Video Signal Data 17
9013_D [18]	B13_L4_P	V11	9013 Video Signal Data 18
9013_D [19]	B13_L4_N	W11	9013 Video Signal Data 19
9013_D [20]	B13_L3_P	W12	9013 video signal data 20
9013_D [21]	B13_L3_N	W13	9013 Video Signal Data 21
9013_D [22]	B13_L5_N	U12	9013 Video Signal Data 22
9013_D [23]	B13_L5_P	U11	9013 Video Signal Data 23
HDMI_SCL	B34_L1_P	J8	9013 IIC Control Clock

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HDMI _SDA	B34_L1_N	K8	9013 IIC Control Data

Table 2.5.1 - HDMI Interface Pin Assignment

2.6 Fiber Optic Interface

The AX7015B expansion board has two fiber optic interfaces. Users can purchase optical modules (1.25G and 2.5G optical modules available on the market) and insert them into these two interfaces for fiber optic data communication. The two fiber optic interfaces are connected to the two RX/TX channels of the ZYNQ GTP transceiver. The TX and RX signals are differentially connected to the ZYNQ and the optical modules via DC blocking capacitors. Each TX transmit and RX receive data rate reaches up to 6.125Gb/s. The reference clock for the GTP transceiver is provided by a 125MHz differential crystal oscillator on the core board. The FPGA and fiber optic design schematic is shown in Figure 2.6.1 below .

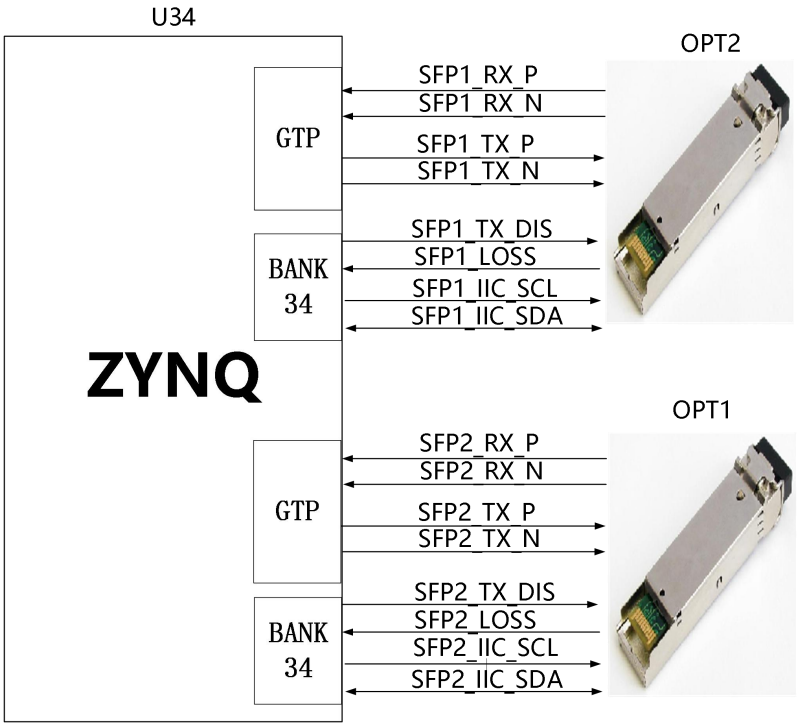


Figure 2.6.1 - Schematic diagram of fiber optic design

The pin assignments for the OPT2 fiber optic interface ZYNQ are as follows:

Network Name	ZYNQ pin	Remark
SFP 1_TX_P	W2	SFP optical module data transmission Positive
SFP 1_TX_N	Y2	SFP optical module data transmission Negative
SFP 1_R X_P	W6	Positive data reception for SFP optical modules
SFP 1_R X_N	Y6	SFP optical module data reception Negative

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SFP 1_TX_DIS	U1	SFP optical module light emission inhibited,active high
SFP 1_LOSS	U2	SFP optical receiver LOSS signal,high indicates no optical signal received.
SFP1_IIC_SCL	K7	I2C clock for SFP optical module DDMI
SFP1_IIC_SDA	L7	SFP optical module DDMI I2C data

Note: The above pin definitions are for the OPT2 fiber optic interface silkscreened on the AX7015B baseboard PCB.

Table 2.6.1 - POPT2 Fiber Optic Interface ZYNQ Pin Assignment

The pin assignments for the OPT1 fiber optic interface ZYNQ are as follows:

Network Name	ZYNQ pin	Remark
SFP 2_TX_P	AA5	SFP optical module data transmission Positive
SFP 2_TX_N	AB5	SFP optical module data transmission Negative
SFP 2_RX_P	AA9	SFP optical module data reception Positive
SFP 2_RX_N	AB9	SFP optical module data reception Negative
SFP 2_TX_DIS	K2	SFP optical module light emission inhibited,high efficiency
SFP 2_LOSS	K5	SFP optical receiver LOSS signal,high indicates no optical signal received.
SFP 2_IIC_SCL	J5	I2C clock for SFP optical module DDMI
SFP 2_IIC_S DA	J3	SFP optical module DDMI I2C data

Note: The above pin definitions are for the OPT1 fiber optic interface silkscreened on the AX7015B baseboard PCB.

Table 2.6.2 - OPT1 Fiber Optic Interface ZYNQ Pin Assignment

2.7 PCIe x2 Interface

The AX7015B expansion board provides an industrial-grade high-speed data transmission PCIe x2 interface. The PCIe card's form factor conforms to the standard PCIe card electrical specifications and can be used directly in a standard desktop PCIe slot.

The PCIe interface's transmit and receive signals are directly connected to the FPGA's GTP transceiver. The TX and RX signals of both channels are connected to the FPGA in a differential signal configuration, allowing for a single-channel communication rate of up to 5Gbit bandwidth. The PCIe reference clock is provided to the development board by the computer's PCIe slot, with a reference clock frequency of 100MHz.

The design schematic of the PCIe interface of the development board is shown in Figure 2.7.1 below , where the TX transmit signal and the reference clock CLK signal are connected in AC coupling mode.

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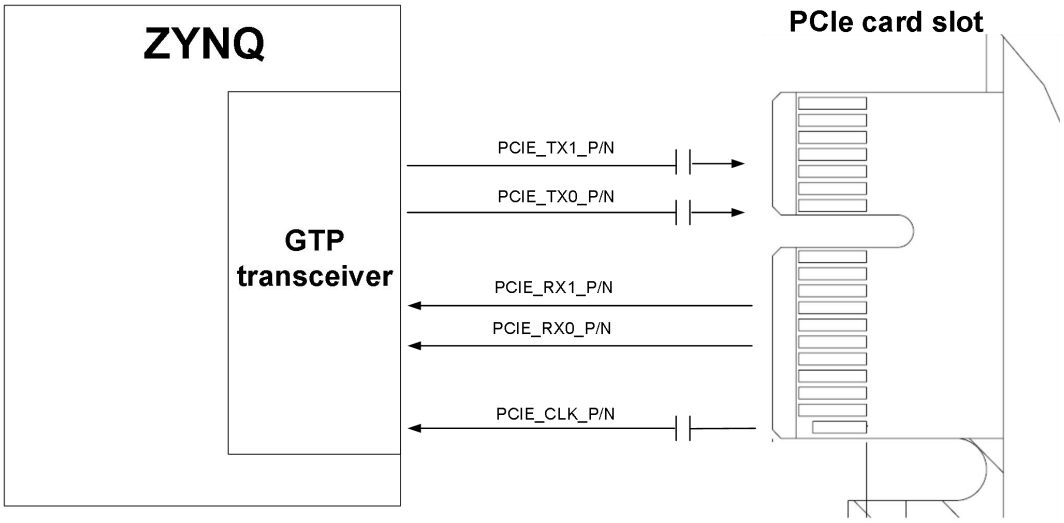


Figure 2.7.1 - PCIe x2 design schematic

The pin assignments for the PCIe x2 interface FPGA are as follows:

Network Name	FPGA pins	Remark
PCIE_RX0_P	W8	PCIe Channel 0 Data Receive Positive
PCIE_RX0_N	Y8	PCIe channel 0 data reception(Negative)
PCIe_RX1_P	AA7	PCIe Channel 1 Data Receive Positive
PCIE_RX1_N	AB7	PCIe Channel 1 Data Receiver(Negative)
PCIE_TX0_P	W4	PCIe Channel 0 Data Sending Positive
PCIE_TX0_N	Y4	PCIe channel 0 data transmission Negative
PCIe_TX1_P	AA3	PCIe Channel 1 Data Transmission Positive
PCIE_TX1_N	AB3	PCIe Channel 1 Data Transmission Negative
PCIE_CLK_P	U9	PCIe reference clock Positive
PCIE_CLK_N	V9	PCIe reference clock Negative

Table 2.7.1 - PCIe x2 Interface Pin Assignment

2.8 USB to Serial Port

The AX7015B baseboard also features a serial port interface for overall debugging of the ZYNQ7000 system. The conversion chip is a Silicon Labs CP2102GM USB-UART chip , and the USB interface is a MINI USB interface. It can be connected to the PC 's USB port using a single USB cable for independent power supply and serial data communication for the core board. A schematic

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diagram of the USB UART circuit design is shown in Figure 2.8.1 below .

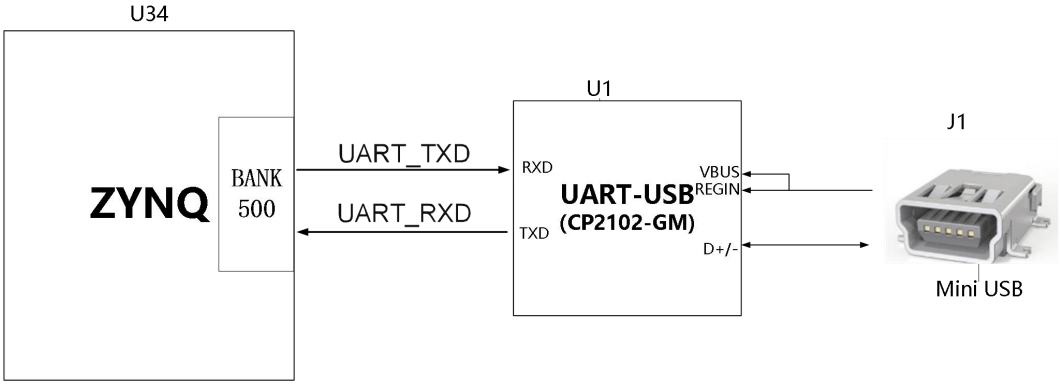


Figure 2.8.1 - Schematic diagram of USB to serial port

ZYNQ pin assignments for UART to serial port conversion:

Signal name	ZYNQ pin name	ZYNQ pin number	Remark
UART_RXD	PS_MIO 13_500	A17	UART data input
UART_TXD	PS_MIO 12_500	C18	UART data output

Table 2.8.1 - ZYNQ Pin Assignment for UART to Serial Port

2.9 SD Card Slot

The AX7015B baseboard includes a MicroSD card interface, providing users with access to SD card storage for storing the ZYNQ chip's boot program, Linux operating system kernel, file system, and other user data files.

The SDIO signals are connected to the I/O signals of the ZYNQ's PS BANK501. Since the VCCMIO of this BANK is set to 1.8V, but the SD card data level is 3.3V, we use a TXS02612 level converter for this connection. The schematic diagram of the Zynq7000 PS and SD card connector is shown in Figure 2.9.1 .

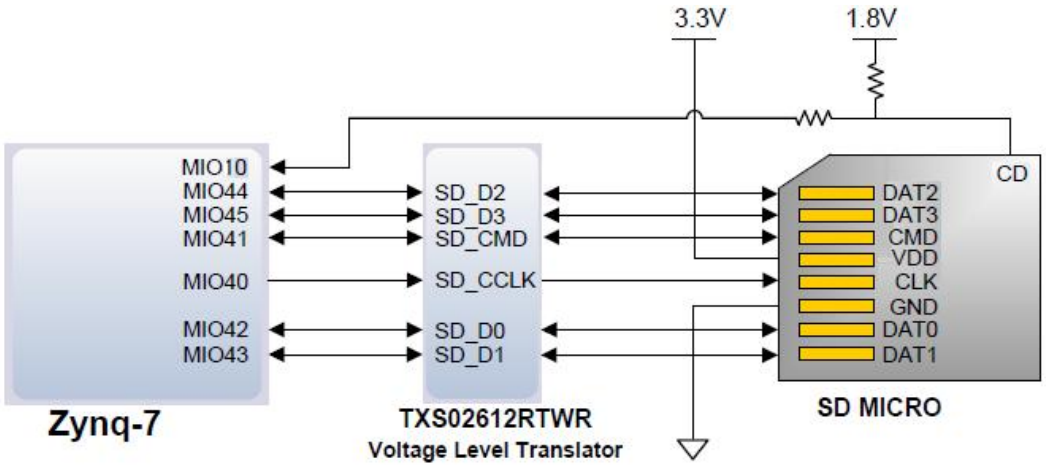


Figure 2.9.1 - SD Card Connection Diagram

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SD card slot pin assignment

Signal name	ZYNQ pin name	ZYNQ pin number	Remark
SD_CLK	PS_MIO40	E9	SD clock signal
SD_CMD	PS_MIO41	C15	SD command signals
SD_D0	PS_MIO42	D15	SD Data0
SD_D1	PS_MIO43	B12	SD Data 1
SD_D2	PS_MIO44	E10	SD Data 2
SD_D3	PS_MIO45	B14	SD Data 3
SD_CD	PS_MIO 10	G16	SD card insertion signal

Table 2.9.1 - SD Card Slot Pin Assignment

2.10 JTAG Interface

A JTAG interface is provided on the AX7015B baseboard for downloading FPGA programs or firmware to the FLASH memory. To prevent damage to the FPGA chip from hot-plugging, a protection diode has been added to the JTAG signal to ensure that the signal voltage remains within the FPGA's acceptable range, thus preventing FPGA damage.

Users can connect a PC to the JTAG interface using the provided USB programmer for ZYNQ system debugging. When plugging and unplugging the JTAG cable, avoid hot-plugging..

2.11 LED lights

The AX7015B baseboard has six red LEDs: one power indicator (PWR) and five user LEDs. The power indicator lights up when the baseboard is powered on. One user LED is connected to the PS's MIO, and the other four are connected to the PL's I/O. Users can control the LEDs' on/off state via a program. When the voltage on the I/O connected to a user LED is high, the LED is off; when the voltage is low, the LED is on. A schematic diagram of the LED hardware connection is shown in Figure 2.11.1 .

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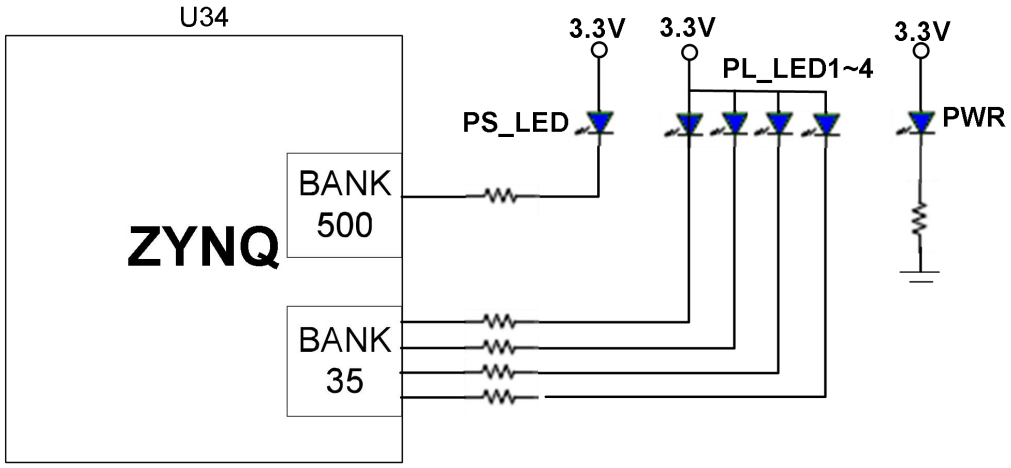


Figure 2.11.1 - Hardware connection diagram of the base plate LED light

Pin assignment for user LED lights on the baseboard

Signal name	ZYNQ pin name	ZYNQ pin number	Remark
PS_LED	PS_MIO9_500	C19	PS user LED lights
PL_LED1	B35_L10_P	A5	LED1 light for PL end users
PL_LED2	B35_L9_P	A7	LED2 lights for PL end users
PL_LED3	B35_L9_N	A6	LED 3 lights for PL end users
PL_LED4	B35_L7_N	B8	PL end user LED 4 lights

Table 2.11.1 - Pin Assignments for User LEDs

2.12 User Button

The AX7015B baseboard has two user buttons, PS KEY and PL KEY. PS KEY is connected to the MIO pin of the ZYNQ chip PS, and PL KEY is connected to the IO pin of the ZYNQ chip PL. When a button is pressed, the signal is low, and the ZYNQ chip detects this low level to determine if the button is pressed. A schematic diagram of the user button connections is shown in Figure 2.12.1 .

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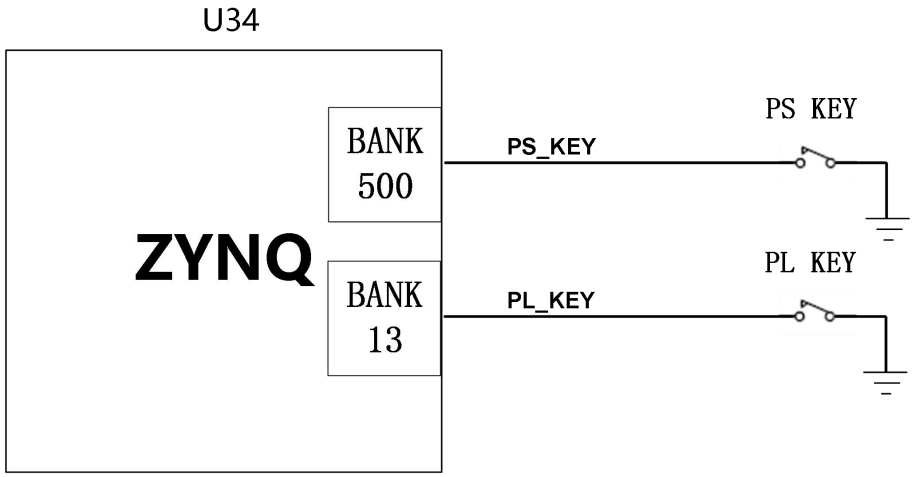


Figure 2.12.1 - Schematic diagram of user button connection

ZYNQ pin assignment for user buttons

Signal name	ZYNQ pin name	ZYNQ pin number	Remark
PS_KEY	PS_MIO11_500	B19	ZYNQ system reset signal
PL_KEY	B13_L8_N	AB12	User buttons on the PL end

Table 2.12.1 - ZYNQ Pin Assignment for User Buttons

2.13 Expansion Port

The AX7015B baseboard has a pre-installed 40-pin expansion port J12 with a standard 2.54mm pitch, for connecting various Alinx modules or user-designed external circuits. The expansion port has 40 signals: one 5V power supply, two 3.3V power supply, three ground lines, and 34 I/O ports. **Do not connect the I/O ports directly to 5V devices, as this may damage the ZYNQ7000 chip. If you need to connect 5V devices, you will need to use a level converter chip.**

Pin assignment of J12 expansion port ZYNQ

Pin number	ZYNQ pin	Pin number	ZYNQ pin
1	GND	2	+5V (output)
3	M1	4	M2
5	Y13	6	Y12
7	P2	8	P3
9	R7	10	P7

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11	P8	12	N8
13	R2	14	R3
15	R4	16	R5
17	M7	18	M8
19	M3	20	M4
21	U14	22	U13
23	AB14	24	AB13
25	W15	26	V15
27	Y17	28	W17
29	W18	30	V18
31	AB22	32	AB21
33	AA20	34	AA19
35	T17	36	R17
37	GND	38	GND
39	+3.3V (output)	40	+3.3V (output)

Table 2.13.1 - Pin Assignment for the J12 Expansion Port ZYNQ

2.14 Power Supply

The development board's power input voltage is DC 12V, which can be supplied via a PCIe slot or an external +12V power supply. When using an external power supply, please use the power supply that comes with the development board; do not use other power supplies to avoid damaging the board. The baseboard uses a 3-channel DC/DC power chip ETA1471FT2G to convert the power into four channels: +5V, +3.3V, and 1.8V. The power supply design for the expansion circuitry is shown in Figure 2.14.1 .

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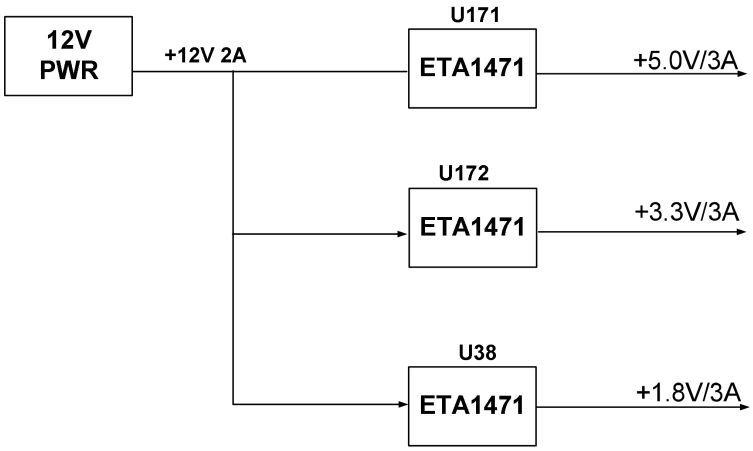


Figure 2.14.1 - Schematic diagram of the base plate power supply

2.15 Baseboard Structure Diagram

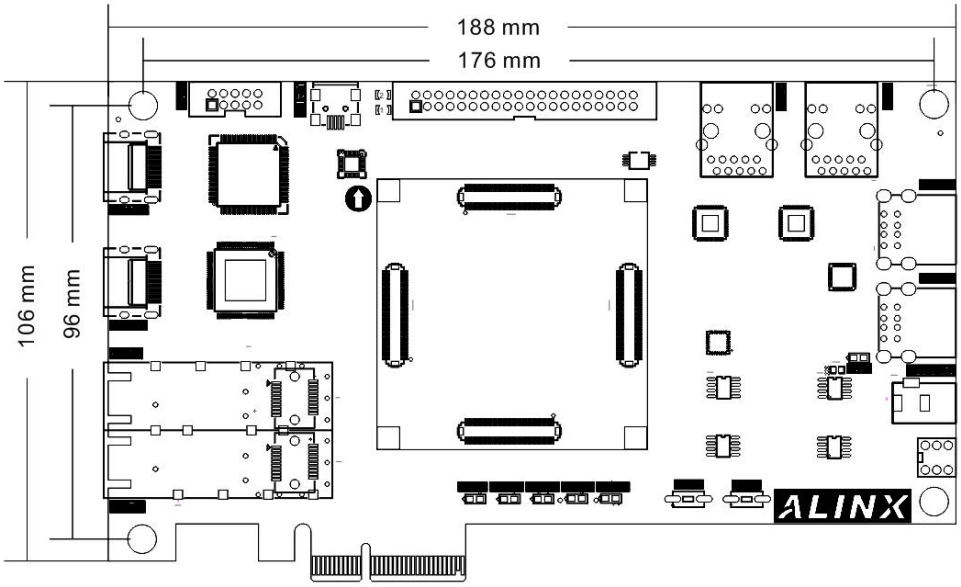


Figure 2.15.1 - Top View of the Development Board

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