phyFLEX®-i.MX 6

Hardware Manual

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List of Figures ..... **iv**
List of Tables ..... **vi**
Conventions, Abbreviations and Acronyms ..... **ix**
Preface ..... **xii**
1 Introduction **1**
1.1 Features of the phyFLEX-i.MX 6 2
1.2 Block Diagram 3
1.3 phyFLEX-i.MX 6 Component Placement 4
1.4 Minimum Requirements to operate the phyFLEX-i.MX 6 6
2 Pin Description **7**
3 Jumpers **22**
4 Power **27**
4.1 Primary System Power (VDD_5V_IN_R) 27
4.2 Power Management IC (PMIC) (U14) 27
4.2.1 Power Domains 28
4.3 Supply Voltage for external Logic 30
4.4 Backup Power (PMIC_VBAT/VDD_MX6_SNVS) 30
4.5 Control Management IC (CMIC) (U17)) 30
4.5.1 Power On/Off Control 31
4.5.2 Reset Control 31
4.5.3 Boot Control 31
5 System Configuration and Booting **32**
6 System Memory **36**
6.1 DDR3-SDRAM (U2-U9) 36
6.2 NAND Flash Memory (U13) 37
6.3 I²C EEPROM (U10) 37
6.3.1 EEPROM Write Protection Control (J3) 38
6.4 SPI Flash Memory (U25)) 38
7 SD / MM Card Interfaces **39**
8 Serial Interfaces **41**
8.1 Universal Asynchronous Interface 42
8.2 USB OTG Interface 43
8.3 USB Host Interface 43
8.4 Ethernet Interface 44
8.4.1 Ethernet PHY (U11) 44
8.4.2 Software Reset of the Ethernet Controller 45
8.4.3 MAC Address 45
8.5 I^2C Interface 46
8.6 SPI Interface 47
8.7 I^2S Audio Interface (SSI)) 48
8.8 CAN Interface 49
8.9 PCI Express Interface 49
8.10 SATA Interface 50
8.11 Media Local Bus 50

9 General Purpose I/Os 51
10 User LEDs 52
11 Debug Interface (X1, X4) 53
12 LVDS Display Interface 57
12.1 Supplementary Signals 58
12.2 LVDS Display Interface pixel mapping 58
13 High-Definition Multimedia Interface (HDMI) 59
14 Camera Interfaces 60
14.1 Camera_0 Interface (CSI0 of IPU#1) 62
14.1.1 Camera_0 as LVDS Interface 62
14.1.1.1 Signal Configuration (J31) 63
14.1.2 Camera_0 as Parallel Interface (Parallel 0) 63
14.2 Camera_1 Interface (CSI1 of IPU#2) 65
14.2.1 Camera_1 as LVDS Interface 65
14.2.1.1 Signal Configuration (J9), (J26) 66
14.2.2 Camera_1 as Parallel Interface (Parallel 1) 66
14.3 Camera_2 Camera Interface (MIPI/CSI-2) 68
15 Tamper Detection 69
16 Environment Management IC (EMIC) (U19) 70
17 Technical Specifications 73
17.1 Product Temperature Grades 74
17.2 Connectors on the phyFLEX-i.MX 6 76
18 Hints for Integrating and Handling the phyFLEX-i.MX 6 77
18.1 Integrating the phyFLEX-i.MX 6 77
18.2 Handling the phyFLEX-i.MX 6 77
19 The phyFLEX- i.MX 6 on the phyFLEX Carrier Board 79
19.1 Concept of the phyFLEX Carrier Board 80
19.2 Overview of the phyFLEX Carrier Board Peripherals 81
19.2.1 Connectors and Pin Header 83
19.2.2 Switches 85
19.2.3 LEDs 86
19.2.4 Jumpers 88
19.3 Functional Components on the phyFLEX Carrier Board 93
19.3.1 phyFLEX- i.MX 6 SOM Connectivity (X1, X2) 77 93
19.3.2 Power (X12, X55, X28) 94
19.3.2.1 Wall Adapter Input (X12) 96
19.3.2.2 Power over Ethernet Plus (PoE+) (X28) 98
19.3.2.3 Power Management Connector (X22) 99
19.3.2.3.1 Power States 99
19.3.3 RS-232 Connectivity (X50, X51) 100
19.3.4 CAN Connectivity (X52) 102
19.3.5 Ethernet Connectivity (X28) 104
19.3.6 USB Host Connectivity (X65, X66, X69, X70) 105
19.3.7 USB OTG Connectivity (X26) 108

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19.3.8 Display / Touch Connectivity (X65) 109
19.3.8.1 Display Data Connector (X65) 110
19.3.8.2 Display Power Connector (X65) 112
19.3.8.3 Touch Screen Connectivity 112
19.3.9 High-Definition Multimedia Interface (HDMI) (X40) 113
19.3.10 Camera Interface (X63, X64) 115
19.3.10.1 phyCAM-S(+) (LVDS) Camera Interfaces on the phyFLEX Carrier Board 116
19.3.10.2 phyCAM-P or Parallel Camera Interfaces on the phyFLEX Mapper Board 118
19.3.10.3 MIPI/CSI-2 (Camera_2) Interface on the phyFLEX Mapper Board 119
19.3.11 Audio Interface (X7, X8, X9, X10, X11) 120
19.3.12 I^2C Connectivity 122
19.3.13 SPI Connectivity (X30, X53, X65) 123
19.3.14 User programmable GPIOs (X54) 125
19.3.15 User programmable LEDs 126
19.3.16 Secure Digital Memory Card/ MultiMedia Card (X57, X56) 127
19.3.17 PCIe Connectivity (X59) 128
19.3.18 SATA (X62, X61) 130
19.3.19 CPU Fan Connector (X41) 131
19.3.20 Wi-Fi/Bluetooth Connector (X58) 132
19.3.21 Boot Mode Selection (S3) 134
19.3.22 System Reset Button (S1) 134
19.3.23 System Power On/Off/Wake Button (S2) 135
19.3.24 JTAG Interface (X4) 135
19.3.25 RTC at U28 136
19.3.26 Environment Management IC (EMIC) (U59) 138
20 Revision History 142
Index 144

List of Figures

Figure 1: Block Diagram of the phyFLEX-i.MX 6 3
Figure 2: phyFLEX-i.MX 6 Component Placement (top view) 4
Figure 3: phyFLEX-i.MX 6 Component Placement (bottom view) 5
Figure 4: Pinout of the phyFLEX-Connector (top view) 8
Figure 5: Typical Jumper Pad Numbering Scheme 22
Figure 6: Jumper Locations (top view) 23
Figure 7: Jumper Locations (bottom view) 24
Figure 8: Powering Scheme of phyFLEX- i.MX 6 29
Figure 9: JTAG Interface at X4 (top view) 54
Figure 10: JTAG Interface at X4 (bottom view) 55
Figure 11: Camera Connectivity of the i.MX 6 (Solo/DualLite) 60
Figure 12: Camera Connectivity of the i.MX 6 (Dual Core/Quad Core) 60
Figure 13: Camera Connectivity of the phyFLEX-i.MX 6 with Dual Core/Quad Core 61
Figure 14: EMIC and supporting Components (top view) 71
Figure 15: EMIC and supporting Components (bottom view) 72
Figure 16: Physical Dimensions (top view) 73
Figure 17: Footprint of the phyFLEX-i.MX 6 78
Figure 18: phyFLEX Carrier Board Overview of Connectors, LEDs and Buttons (bottom view) 81
Figure 19: phyFLEX Carrier Board Overview of Connectors, LEDs and Buttons (top view) 82
Figure 20: Typical Jumper Numbering Scheme 88
Figure 21: phyFLEX Carrier Board Jumper Locations (top view) 89
Figure 22: phyFLEX Carrier Board Jumper Locations (bottom view) 90
Figure 23: phyFLEX- i.MX 6 SOM Connectivity to the Carrier Board 93
Figure 24: Powering Scheme 94
Figure 25: Power Connector corresponding to Wall Adapter Input X12 97
Figure 26: RS-232 Interface Connectors X50 and X51 100
Figure 27: RS-232 Connector X50 Signal Mapping (UART1) 101
Figure 28: RS-232 Connector X51 Signal Mapping (UART0) 101
Figure 29: CAN Interface Connector X52 102
Figure 30: CAN Connector X52 Signal Mapping 103
Figure 31: Ethernet Interface at Connector X28 104
Figure 32: Components supporting the USB Host Interface 105

Figure 33: USB OTG Interface at Connector X26 108
Figure 34: Phytec Display Interface (PDI) at Connector X65 109
Figure 35: HDMI Interface at Connector X40 113
Figure 36: Camera Interface at Connector X63, X64 115
Figure 37: Use of Camera_0 (CSI0 of IPU#1) as phyCAM-S+ Interface 116
Figure 38: Use of Camera_1 (CSI1 of IPU#2) as phyCAM-S+ Interface 117
Figure 39: Use of Camera_0 (CSI0 of IPU#1) as phyCAM-P Interface, or Customized 118
Figure 40: Use of Camera_1 (CSI1 of IPU#2) as phyCAM-P Interface, or Customized 118
Figure 41: Audio Interface at Connectors X7, X8, X9, X10, X11 120
Figure 42: SPI Connectivity at Connectors X30, X53 and X65 123
Figure 43: User programmable GPIOs and LEDs 125
Figure 44: SD / MM Card Interfaces at Connector X57 and X56 127
Figure 45: CPU Fan Connector X41 131
Figure 46: Wi-Fi/Bluetooth Connector X58 132
Figure 47: RTC with Battery Buffer 136
Figure 48: EMIC and supporting Components (top view) 138

List of Tables

Table 1: Signal Types used in this Manual x
Table 2: Abbreviations and Acronyms used in this Manual xi
Table 3: Pinout of the phyFLEX-fix Connector X1, Row A 10
Table 4: Pinout of the phyFLEX-fix Connector X1, Row B 12
Table 5: Pinout of the phyFLEX-optional Connector X2, Row A 15
Table 6: Pinout of the phyFLEX-optional Connector X2, Row B 16
Table 7: Pinout of the phyFLEX-flex Connector X3, Row A 18
Table 8: Pinout of the phyFLEX-flex Connector X3, Row B 19
Table 9: Jumper Settings 25
Table 10: Standard phyFLEX Boot Options 33
Table 11: phyFLEX-i.MX 6 specific Boot Options 33
Table 12: Boot Configuration Pins at phyFLEX-flex Connector X3 and X1 34
Table 13: Boot Configuration Signals generated by the CMIC 35
Table 14: EEPROM Write Protection States via J3 38
Table 15: Location of the SD / MM Card Interface Signals 39
Table 16: Location of the UART Signals 42
Table 17: Location of the USB OTG Signals 43
Table 18: Location of the USB-Host Signals 43
Table 19: Location of the Ethernet Signals 44
Table 20: I^2C Interface Signal Location 46
Table 21: SPI Interface Signal Location 47
Table 22: I^2S Interface Signal Location 48
Table 23: CAN Interface Signal Location 49
Table 24: PCIe Interface Signal Location 49
Table 25: SATA Interface Signal Location 50
Table 26: Media Local Bus Interface Signal Location 50
Table 27: Location of GPIO Pins 51
Table 28: Debug Interface Signal Location at phyFLEX-Connector X1 53
Table 29: JTAG Connector X4 Signal Assignment 56
Table 30: Display Interface Signal Location 57
Table 31: Supplementary Signals to support the Display Connectivity 58
Table 32: Pixel Mapping of 18-bit LVDS Display Interface 58
Table 33: Pixel Mapping of 24-bit LVDS Display Interface 58
Table 34: HDMI Interface Signal Location at X2 59

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Table 35: Camera_0 LVDS Interface Signal Location at phyFLEX Connector X2 62
Table 36: LVDS Signal Configuration for Camera_0 Interface (J31) 63
Table 37: Parallel 0 Camera Interface Signal Location at the phyFLEX-Connector 64
Table 38: Camera_1 LVDS Interface Signal Location at phyFLEX Connector X2 65
Table 39: LVDS Signal Configuration for Camera_1 Interface (J9) 66
Table 40: Clock Configuration for Camera_1 Interface (J26) 66
Table 41: Parallel 1 Camera Interface Signal Location at the phyFLEX-Connector 67
Table 42: Camera_2 Signal Location at phyFLEX Connector X3 68
Table 43: Environment Management IC (EMIC) IO Signals 70
Table 44: I^2C Addresses of the optional Temperature Sensors 70
Table 45: Technical Specifications 74
Table 46: Product Temperature Grades 75
Table 47: phyFLEX Carrier Board Connectors and Pin Headers 83
Table 48: phyFLEX Carrier Board Push Buttons Descriptions 85
Table 49: phyFLEX Carrier Board LEDs Descriptins 86
Table 50: phyFLEX Carrier Board Jumper Descriptions 91
Table 51: Voltage Domains on the Carrier Board 95
Table 52: Power LEDs 95
Table 53: Power Jumper JP11 and DIP switch S9 96
Table 54: Power Management Connector X22 99
Table 55: phyFLEX Carrier Board DIP Switch S5 Descriptions 103
Table 56: Distribution of the USB Hub's (U66) Ports 106
Table 57: USB Hub's Status LEDs D93 – D96 106
Table 58: USB VBUS Indicator LEDs 106
Table 59: USB Hub's Feature Configuration DIP switch S8 107
Table 60: PDI Data Connector X65 Signal Description 110
Table 61: Auxiliary Interfaces at PDI Data Connector X65 111
Table 62: PDI Power Connector X65 Signal Description 112
Table 63: HDMI/DVI Connector X40 Pinout 114
Table 64: Phytec phyCAM-S+ Camera Connector X63 116
Table 65: Phytec phyCAM-S+ Camera Connector X64 117
Table 66: I^2C Connectivity 122
Table 67: I2C0 Addresses in Use 122
Table 68: SPI0 Connector Selection 123
Table 69: SPI0 Pin Header X53 Pinout 124

Table 70: SPI Buffer U63 Mode of Operation 124
Table 71: SPI1 Pin Header X30 Pinout 124
Table 72: GPIOs used on the phyFLEX Carrier Board 125
Table 73: GPIO Pin Header X54 Pinout 126
Table 74: User Programmable LEDs on the Carrier Board 126
Table 75: PCIe0 Connector X59 128
Table 76: SATA Data Connector X62 130
Table 77: Molex Disk Power Connector X61 130
Table 78: CPU Fan Connector X41 131
Table 79: Wi-Fi/Bluetooth Connector X58 133
Table 80: phyFLEX Carrier Board DIP Switch S3 Descriptions 134
Table 81: JTAG Connector X4 135
Table 82: RTC Interrupt Configuration JP1 137
Table 83: Environment Management IC (EMIC) Measured Variables 139
Table 84: Environment Management IC (EMIC) Measured Data via I^2C Interface 140
Table 85: EMIC JTAG Connector X49 140
Table 86: Environment Management IC (EMIC) UART Interface Connector X67 141
Table 87: EMIC Boot Mode Selection S4 141

Conventions, Abbreviations and Acronyms

This hardware manual describes the PFL-A-XL1 System on Module in the following referred to as phyFLEX®-i.MX 6. The manual specifies the phyFLEX®-i.MX 6's design and function. Precise specifications for the Freescale Semiconductor i.MX 6 microcontrollers can be found in the enclosed microcontroller Data Sheet/User's Manual.

Note:
We refrain from providing detailed part specific information within this manual, which can be subject to continuous changes, due to part maintenance for our products. Please read the paragraph "**Product Change Management and information in this manual on parts populated on the SOM"** within the *Preface*.

Note:
The BSP delivered with the phyFLEX®-i.MX 6 usually includes drivers and/or software for controlling all components such as interfaces, memory, etc. Therefore programming close to hardware at register level is not necessary in most cases. For this reason, this manual contains no detailed description of the controller's registers, or information relevant for software development. Please refer to the *i.MX 6 Reference Manual*, if such information is needed to connect customer designed applications.

Conventions

The conventions used in this manual are as follows:

- Signals that are preceded by an "n", "/", or "#"character (e.g.: nRD, /RD, or #RD), or that have a dash on top of the signal name (e.g.: $\overline{\text{RD}}$) are designated as active low signals. That is, their active state is when they are driven low, or are driving low.
- A "0" indicates a logic zero or low-level signal, while a "1" represents a logic one or high-level signal.
- The hex-numbers given for addresses of I^2C devices always represent the 7 MSB of the address byte. The correct value of the LSB which depends on the desired command (read (1), or write (0)) must be added to get the complete address byte. E.g. given address in this manual 0x41 => complete address byte = 0x83 to read from the device and 0x82 to write to the device
- Tables which describe jumper settings show the default position in **bold, blue text.**
- Text in *blue italic* indicates a hyperlink within, or external to the document. Click these links to quickly jump to the applicable URL, part, chapter, table, or figure.
- References made to the phyFLEX-Connector always refer to the high density Samtec connectors on the undersides of the phyFLEX-i.MX 6 System on Module.

Types of Signals

Different types of signals (ST) are brought out at the phyFLEX-Connector. The following table lists the abbreviations used to specify the type of a signal.

Signal Type (ST)	Description	Abbr.
Power In	Supply voltage input	PWR_I
Power Out	Supply voltage output	PWR_O
Ref-Voltage	Reference voltage output	REF_O
Input	Digital input	I
Output	Digital output	O
IO	Bidirectional input/output	I/O
IPU	Digital input with pull-up resistor, must only be connected to GND. (jumper or open collector output)	IPU
OC-Bidir PU	Open collector input/output with pull-up resistor	OC-BI
OC-Output	Open collector output without pull-up resistor, requires an external pull-up resistor	OC
5V Input PD	5 V tolerant input with pull-down resistor	5V_PD
LVDS Input	Differential line pairs 100 Ohm LVDS level input	LVDS_I
LVDS Output	Differential line pairs 100 Ohm LVDS level output	LVDS_O
LVDS IO	Differential line pairs 100 Ohm LVDS level bidirectional input/output	LVDS_I/O
TMDS Output	Differential line pairs 100 Ohm TMDS level output	TMDS_O
USB IO	Differential line pairs 90 Ohm USB level bidirectional input/output	USB_I/O
ETHERNET Input	Differential line pairs 100 Ohm Ethernet level input	ETH_I
ETHERNET Output	Differential line pairs 100 Ohm Ethernet level output	ETH_O
ETHERNET IO	Differential line pairs 100 Ohm Ethernet level bidirectional input/output	ETH_I/O
PCIe Input	Differential line pairs 100 Ohm PCIe level input	PCIe_I
PCIe Output	Differential line pairs 100 Ohm PCIe level output	PCIe_O
MLB Output	Differential line pairs 100 Ohm Media local bus output	MLB_O
MLB IO	Differential line pairs 100 Ohm Media local bus bidirectional input/output	MLB_I/O
MIPI CSI-2 Input	Differential line pairs 100 Ohm MIPI CSI-2 level input	CSI-2_I

Table 1: Signal Types used in this Manual

Abbreviations and Acronyms

Many acronyms and abbreviations are used throughout this manual. Use the table below to navigate unfamiliar terms used in this document.

Abbreviation	Definition
BSP	Board Support Package (Software delivered with the Development Kit including an operating system (Windows, or Linux) preinstalled on the module and Development Tools).
CB	Carrier Board; used in reference to the phyFLEX Development Kit Carrier Board.
DFF	D flip-flop.
EMB	External memory bus.
EMI	Electromagnetic Interference.
GPI	General purpose input.
GPIO	General purpose input and output.
GPO	General purpose output.
IRAM	Internal RAM; the internal static RAM on the Freescale Semiconductor i.MX 6 microcontroller.
J	Solder jumper; these types of jumpers require solder equipment to remove and place.
JP	Solderless jumper; these types of jumpers can be removed and placed by hand with no special tools.
PCB	Printed circuit board.
PDI	Phytec Display Interface; defined to connect Phytec display adapter boards, or custom adapters
PEB	Phytec Extension Board
PMIC	Power management IC
PoE	Power over Ethernet
POR	Power-on reset
RTC	Real-time clock.
SMT	Surface mount technology.
SOM	System on Module; used in reference to the PFL-A-XL1 /phyFLEX®-i.MX 6 module
Sx	User button Sx (e.g. S1, S2, etc.) used in reference to the available user buttons, or DIP switches on the carrier board.
Sx_y	Switch y of DIP switch Sx; used in reference to the DIP switch on the carrier board.

Table 2: Abbreviations and Acronyms used in this Manual

Preface

As a member of Phytec's new phyFLEX® product family the phyFLEX-i.MX 6 is one of a series of Phytec System on Modules (SOMs) that can be populated with different controllers and, hence, offers various functions and configurations. Phytec supports a variety of 8-/16- and 32-bit controllers in two ways:

(1) as the basis for Rapid Development Kits which serve as a reference and evaluation platform

(2) as insert-ready, fully functional phyFLEX® OEM modules, which can be embedded directly into the user's peripheral hardware design.

Implementation of an OEM-able SOM subassembly as the "core" of your embedded design allows you to focus on hardware peripherals and firmware without expending resources to "re-invent" microcontroller circuitry. Furthermore, much of the value of the phyFLEX® module lies in its layout and test.

Phytec's new phyFLEX® product family consists of a series of extremely compact embedded control engines featuring various processing performance classes while using the newly developed phyFLEX® embedded bus standard. The standardized connector footprint and pin assignment of the phyFLEX® bus makes this new SOM generation extremely scalable and flexible. This also allows to use the same carrier board to create different applications depending on the required processing power. With this new SOM concept it is possible to design entire embedded product families around vastly different processor performances while optimizing overall system cost. In addition, future advances in processor technology are already considered with this new embedded bus standard making product upgrades very easy. Another major advantage is the forgone risk of potential system hardware redesign steps caused by processor or other critical component discontinuation. Just use one of Phytec's other phyFLEX® SOMs thereby ensuring an extended product life cycle of your embedded application.

Production-ready Board Support Packages (BSPs) and Design Services for our hardware will further reduce your development time and risk and allow you to focus on your product expertise. Take advantage of Phytec products to shorten time-to-market, reduce development costs, and avoid substantial design issues and risks. With this new innovative full system solution you will be able to bring your new ideas to market in the most timely and cost-efficient manner.

For more information go to:

http://www.phytec.de/de/leistungen/entwicklungsunterstuetzung.html or
www.phytec.eu/europe/oem-integration/evaluation-start-up.html

Ordering Information

The part numbering of the phyFLEX has the following structure:

PFL-*A*-*xx*-*xxxxxx*.*Ay*

Generation

A = First Generation
B = Second Generation

Product number (consecutive)

Assembly options (depending on model) [1]

Version number

Product Specific Information and Technical Support

In order to receive product specific information on changes and updates in the best way also in the future, we recommend to register at

http://www.phytec.de/de/support/registrierung.html or
http://www.phytec.eu/europe/support/registration.html

For technical support and additional information concerning your product, please visit the support section of our web site which provides product specific information, such as errata sheets, application notes, FAQs, etc.

http://www.phytec.de/de/support/faq/faq-phyFLEX-i.MX6.html or
http://www.phytec.eu/europe/support/faq/faq-phyFLEX-i.MX6.html

[1]: Assembly options include choice of Controller; RAM (Size/Type); Size of NAND Flash, etc.; Interfaces available; Vanishing; Temperature Range; and other features. Please contact our sales team to get more information on the ordering options available.

Declaration of Electro Magnetic Conformity of the Phytec phyFLEX®-i.MX 6

Phytec System on Module (henceforth products) are designed for installation in electrical appliances or as dedicated Evaluation Boards (i.e.: for use as a test and prototype platform for hardware/software development) in laboratory environments.

Caution!
Phytec products lacking protective enclosures are subject to damage by ESD and, hence, may only be unpacked, handled or operated in environments in which sufficient precautionary measures have been taken in respect to ESD-dangers. It is also necessary that only appropriately trained personnel (such as electricians, technicians and engineers) handle and/or operate these products. Moreover, Phytec products should not be operated without protection circuitry if connections to the product's pin header rows are longer than 3 m.

Phytec products fulfill the norms of the European Union's Directive for Electro Magnetic Conformity only in accordance to the descriptions and rules of usage indicated in this hardware manual (particularly in respect to the pin header row connectors, power connector and serial interface to a host-PC).

Implementation of Phytec products into target devices, as well as user modifications and extensions of Phytec products, is subject to renewed establishment of conformity to, and certification of, Electro Magnetic Directives. Users should ensure conformance following any modifications to the products as well as implementation of the products into target systems.

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Product Change Management and information in this manual on parts populated on the SOM / SBC

When buying a Phytec SOM / SBC, you will, in addition to our HW and SW offerings, receive a free obsolescence maintenance service for the HW we provide.

Our PCM (Product Change Management) Team of developers, is continuously processing, all incoming PCN's (Product Change Notifications) from vendors and distributors concerning parts which are being used in our products.

Possible impacts to the functionality of our products, due to changes of functionality or obsolesce of a certain part, are being evaluated in order to take the right masseurs in purchasing or within our HW/SW design.

Our general philosophy here is: **We never discontinue a product as long as there is demand for it.**

Therefore we have established a set of methods to fulfill our philosophy:

Avoiding strategies

- Avoid changes by evaluating long-livety of parts during design in phase.
- Ensure availability of equivalent second source parts.
- Stay in close contact with part vendors to be aware of roadmap strategies.

Change management in rare event of an obsolete and non replaceable part

- Ensure long term availability by stocking parts through last time buy management according to product forecasts.
- Offer long term frame contract to customers.

Change management in case of functional changes

- Avoid impacts on product functionality by choosing equivalent replacement parts.
- Avoid impacts on product functionality by compensating changes through HW redesign or backward compatible SW maintenance.
- Provide early change notifications concerning functional relevant changes of our products.

Therefore we refrain from providing detailed part specific information within this manual, which can be subject to continuous changes, due to part maintenance for our products.

In order to receive reliable, up to date and detailed information concerning parts used for our product, please contact our support team through the contact information given within this manual.

1 Introduction

The phyFLEX-i.MX 6 belongs to Phytec's phyFLEX System on Module family. The phyFLEX SOMs represent the continuous development of Phytec System on Module technology. Like its mini-, micro- and nanoMODUL predecessors, the phyFLEX boards integrate all core elements of a microcontroller system on a subminiature board and are designed in a manner that ensures their easy expansion and embedding in peripheral hardware developments.

Phytec's phyFLEX family introduces the newly developed phyFLEX embedded bus standard. Apart from processor performance, a large number of embedded solutions require a corresponding number of standard interfaces. Among these process interfaces are for example Ethernet, USB, UART, SPI, I^2C, PCIe, audio, and display connectivity. The phyFLEX bus exactly meets this requirement with the phyFLEX-fix connector. As well the location of the commonly used interfaces as the mechanical specifications are clearly defined. Beside this, the phyFLEX concept also considers, that different controllers have many different interfaces. To take this into account, the phyFLEX concept allows two more connectors: the phyFLEX-optional connector, which has optional, but defined interfaces at fixed positions (e.g. SATA, CAN, camera) and the phyFLEX-flex connector, which has only fixed Ground signals. All other signals of the phyFLEX-flex connector are module specific. All interface signals of Phytec's new phyFLEX bus are available on up to three, high-density pitch (0.5 mm) connectors, allowing the phyFLEXs to be plugged like a "big chip" into a target application.

As independent research indicates that approximately 70 % of all EMI (Electro Magnetic Interference) problems stem from insufficient supply voltage grounding of electronic components in high frequency environments approximately 20 % of all pin header connectors on the phyFLEX bus are dedicated to Ground. This improves EMI and EMC characteristics and makes it easier to design complex applications meeting EMI and EMC guidelines using phyFLEX boards even in high noise environments.

phyFLEX boards achieve their small size through modern SMD technology and multi-layer design. In accordance with the complexity of the module, 0402-packaged SMD components and laser-drilled microvias are used on the boards, providing phyFLEX users with access to this cutting edge miniaturization technology for integration into their own design.

The phyFLEX-i.MX 6 is a subminiature (60 mm x 70 mm) insert-ready System on Module populated with the Freescale Semiconductor i.MX 6 microcontroller. Its universal design enables its insertion in a wide range of embedded applications.

Precise specifications for the controller populating the board can be found in the applicable controller reference manual or datasheet. The descriptions in this manual are based on the Freescale Semiconductor i.MX 6. No description of compatible microcontroller derivative functions is included, as such functions are not relevant for the basic functioning of the phyFLEX-i.MX 6.

1.1 Features of the phyFLEX-i.MX 6

The phyFLEX-i.MX 6 offers the following features:

- Subminiature System on Module (60 mm x 70 mm) achieved through modern SMD technology
- Populated with the Freescale Semiconductor i.MX 6 microcontroller (BGA624 packaging)
- Max. 1.2 GHz core clock frequency
- Boot from different memory devices (NAND Flash (standard))
- phyFLEX bus. Commonly used interfaces such as Ethernet, USB, UART, SPI, I^2C, audio, PCIe, SATA, CAN, display and camera connectivity (both LVDS) are available at up to three high-density (0.5 mm) Samtec connectors, enabling the phyFLEX-i.MX 6 to be plugged like a "big chip" into target application
- Single supply voltage of 5 V
- All controller required supplies are generated on board
- Improved interference safety achieved through multi-layer PCB technology and dedicated ground pins
- 512 MB (up to 4 GB[2]) DDR3 SDRAM
- 256 MB (up to 16 GB[2]) on-board NAND Flash
- Up to 16 MB[2] on-board serial Flash (bootable)
- Up to 4 kB[2] I^2C EEPROM
- Two Serial interface (one with 4 lines (TTL) allowing simple hardware handshake)
- High-Speed USB OTG interface
- High-Speed USB host interface
- 10/100/1000 Mbit Ethernet interface
- Two I^2C interfaces
- Two SPI interfaces
- PCIe interface
- I^2S interface
- CAN interface
- Media Local Bus (MLB) interface
- SATA interface
- Two 4 channel LVDS (24 Bit) LCD-interface
- HDMI interface
- Two LVDS camera interface; useable as phyCAM-S(+) compatible interface
- Two parallel camera interfaces; useable as phyCAM-P compatible interface
- MIPI/CS-2 camera interface
- Two SD/MMC card interfaces (1 x 8 bit, 1 x 4 bit)
- Support of standard 20 pin debug interface through JTAG connector
- Eleven dedicated GPIO/IRQ[3] ports at the phyFLEX-fix connector

[2]: The maximum memory size listed is as of the printing of this manual. Please contact Phytec for more information about additional, or new module configurations available.

- Additional GPIOs[3] available at the phyFLEX-flex connector[4]
- Two user programmable LEDs
- Power Management IC (PMIC)
- Control Management IC (CMIC)
- Optional Environment Management IC (EMIC) to monitor voltage, current and temperature, and for fan control
- One Wake Up input
- Available for different temperature grades (*section 17.1*)

1.2 Block Diagram

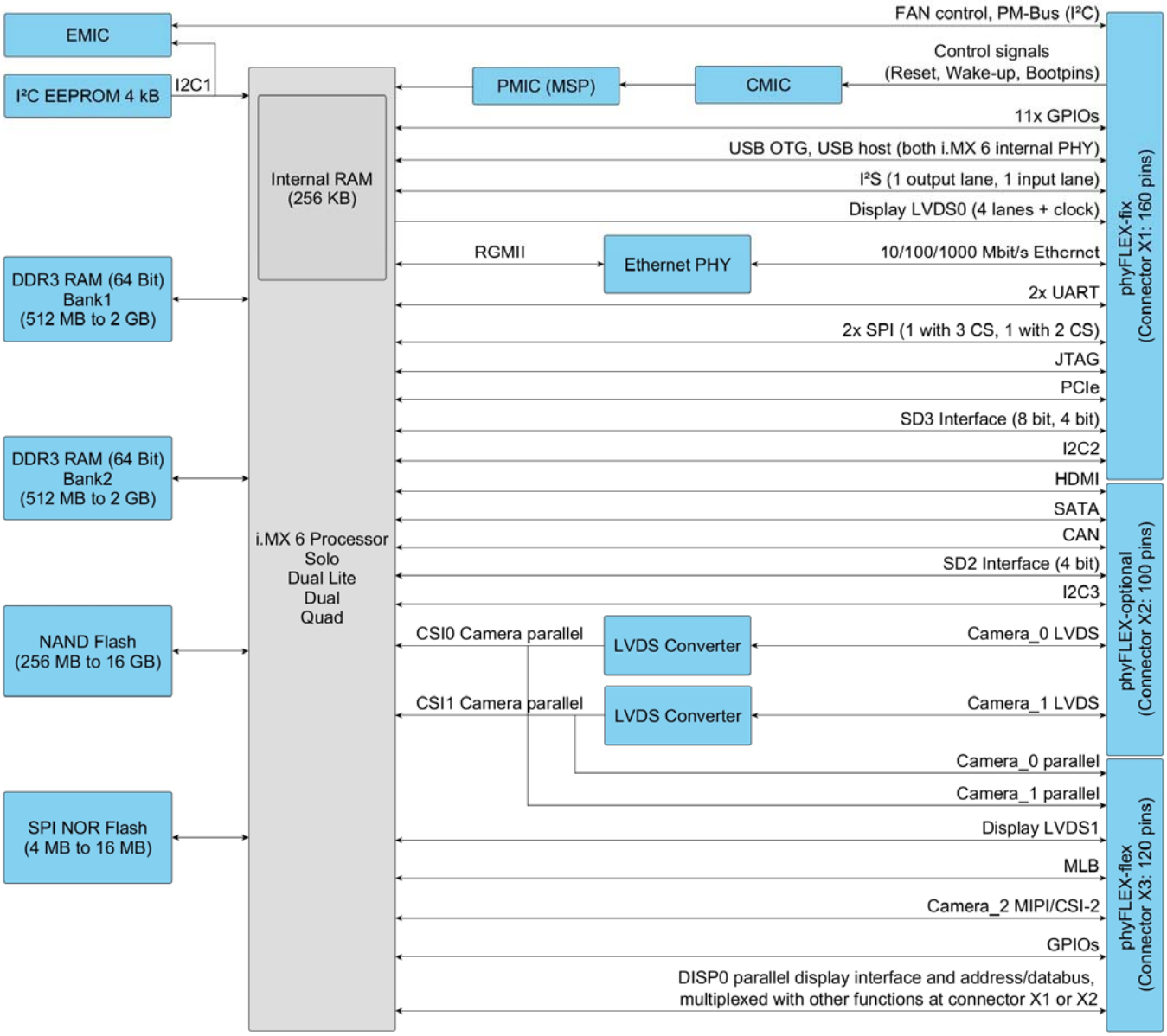


Figure 1: Block Diagram of the phyFLEX-i.MX 6

[3]: Almost every controller port which connects directly to the phyCFLEX-Connector may be used as GPIO by using the i.MX 6's pin muxing options.

[4]: The phyFLEX-flex connector is reserved to carry signals for controller specific features which are not part of the phyFLEX specification. This means that they are not present on all phyFLEX modules. Thus use of these signals should be carefully elaborated to avoid limitation of the compatibility across the phyFLEX module family.

1.3 phyFLEX-i.MX 6 Component Placement

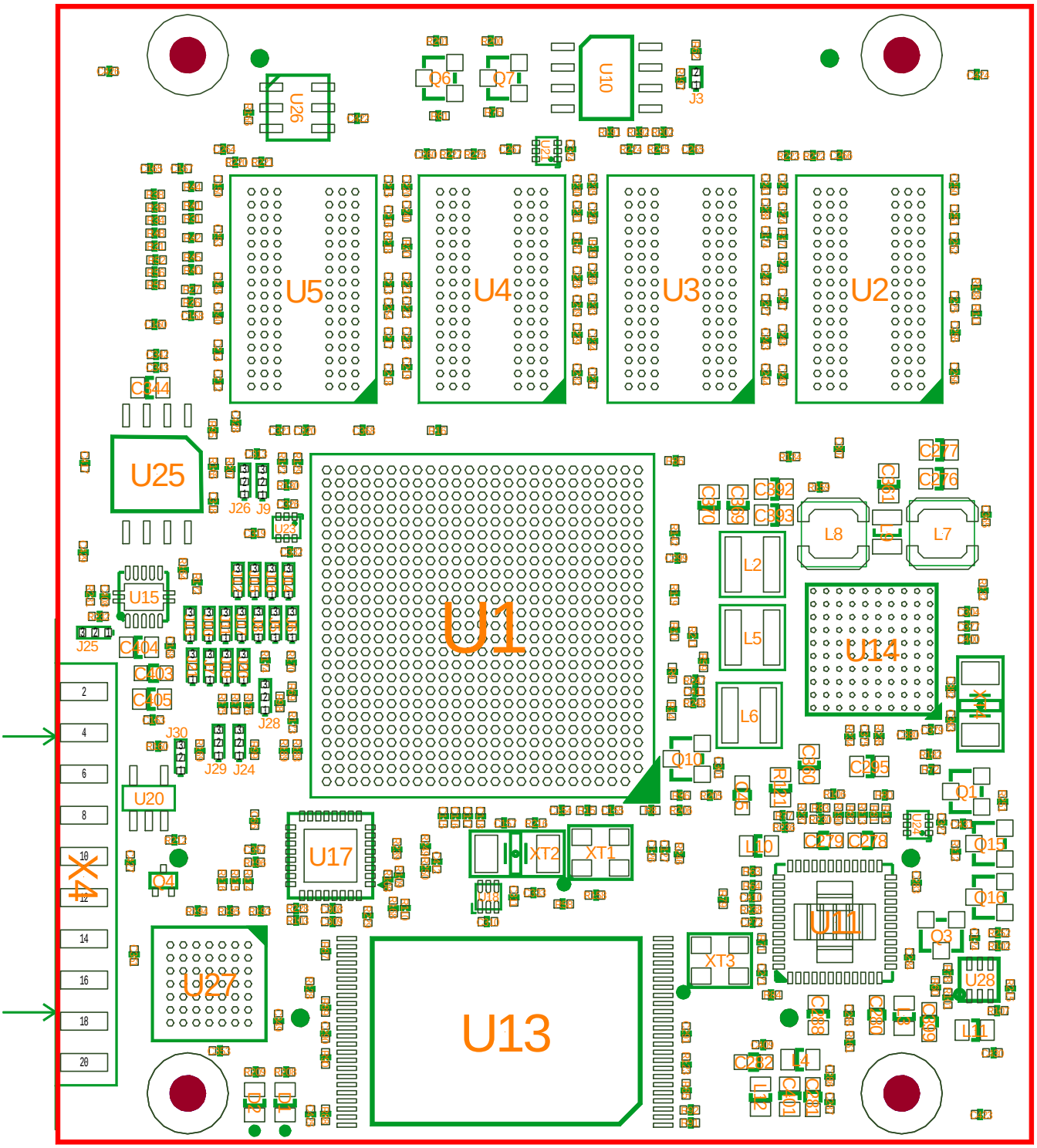


Figure 2: phyFLEX-i.MX 6 Component Placement (top view)

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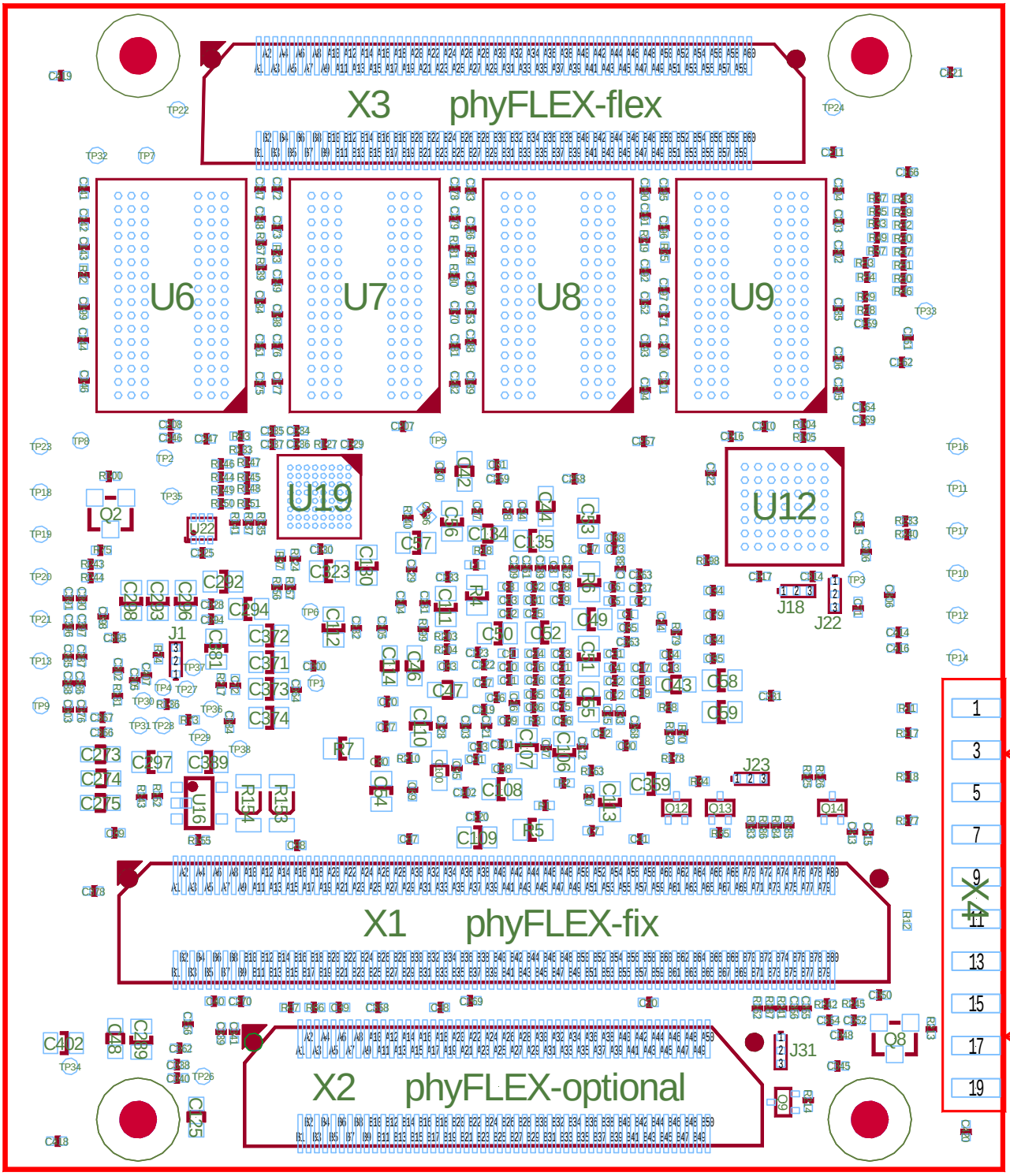


Figure 3: phyFLEX-i.MX 6 Component Placement (bottom view)

1.4 Minimum Requirements to operate the phyFLEX-i.MX 6

Basic operation of the phyFLEX-i.MX 6 only requires supply of a +5 V input voltage with 2 A load and the corresponding GND connection.

These supply pins are located at the phyFLEX-Connector X1:

VDD_5V_IN_R: X1 A1, A2, A3, B1, B2, B3

Connect all +5 V VCC input pins to your power supply and at least the matching number of GND pins.

Corresponding GND: X1 A4, A10, A16, B4, B7, B13

Please refer to *section 2* for information on additional GND Pins located at the phyFLEX-Connector X1.

Caution!
We recommend connecting all available +5 V input pins to the power supply system on a custom carrier board housing the phyFLEX-i.MX 6 and at least the matching number of GND pins neighboring the +5 V pins.

In addition, proper implementation of the phyFLEX-i.MX 6 module into a target application also requires connecting all GND pins neighboring signals that are being used in the application circuitry.

Please refer to *section 4* for more information.

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2 Pin Description

Please note that all module connections are not to exceed their expressed maximum voltage or current. Maximum signal input values are indicated in the corresponding controller manuals/data sheets. As damage from improper connections varies according to use and application, it is the user's responsibility to take appropriate safety measures to ensure that the module connections are protected from overloading through connected peripherals.

All phyFLEX bus signals extend to up to three surface mount technology (SMT) connectors (0.5 mm) (referred to as phyFLEX-Connector). The phyFLEX-i.MX 6 is equipped with three connectors (phyFLEX-fix, phyFLEX-optional, and phyFLEX-flex) as *Figure 4* indicates. This allows the phyFLEX-i.MX 6 to be plugged into any target application like a "big chip". As well the location of the commonly used interfaces as the mechanical specifications of the connectors are clearly defined.

The first connector X1 is called phyFLEX-fix connector. All phyFLEX SOMs support all interfaces specified for this connector at the same locations. The second connector X2, called phyFLEX-optional connector, has optional, but defined interfaces at fixed positions (e.g. SATA[5], CAN[5], camera[5]). phyFLEX SOMs can, but do not have to support the interfaces at the phyFLEX-optional connector. The third connector, phyFLEX-flex connector X3, has only fixed Ground signals. All other signals of the phyFLEX-flex connector are module specific and depend on the features of the controller populating the SOM.

The numbering scheme for the phyFLEX-Connector is based on a two dimensional matrix in which column positions are identified by a letter and row position by a number with prefixed Connector Reference (X1=phyFLEX-fix, X2=phyFLEX-optional, X3=phyFLEX-flex). Pin X1A1, for example, is always located in the upper left hand corner of the matrix of connector X1. The pin numbering values increase moving down on the board. Lettering of the pin connector rows progresses alphabetically from left to right (*Figure 4*).

The numbered matrix can be aligned with the phyFLEX-i.MX 6 (viewed from above; phyFLEX-Connector pointing down) or with the socket of the corresponding phyFLEX Carrier Board/user target circuitry. The upper left-hand corner of the numbered matrix (pin X1A1) is thus covered with the corner of the phyFLEX-i.MX 6. The numbering scheme is always in relation to the PCB as viewed from above, even if all connector contacts extend to the bottom of the module.

The numbering scheme is thus consistent for both the module's phyFLEX-Connector as well as the mating connector on the phyFLEX Carrier Board or target hardware, thereby considerably reducing the risk of pin identification errors.

[5]: If supported by the SOM

The following figure illustrates the numbered matrix system. It shows a phyFLEX-i.MX 6 with all three SMT phyFLEX-Connectors on its underside (defined as dotted lines) mounted on a carrier board. In order to facilitate understanding of the pin assignment scheme, the diagram presents a cross-view of the phyFLEX-i.MX 6 module showing the phyFLEX-Connector mounted on the underside of the module's PCB.

Table 3 to *Table 8* provide an overview of the pinout of the different phyFLEX-Connectors X1, X2, and X3 with signal names and descriptions specific to the phyFLEX-i.MX 6. It also provides the appropriate voltage domain, signal type (ST) and a functional grouping of the signals. The signal type includes also information about the signal direction[6]. A description of the signal types can be found in *Table 1*.

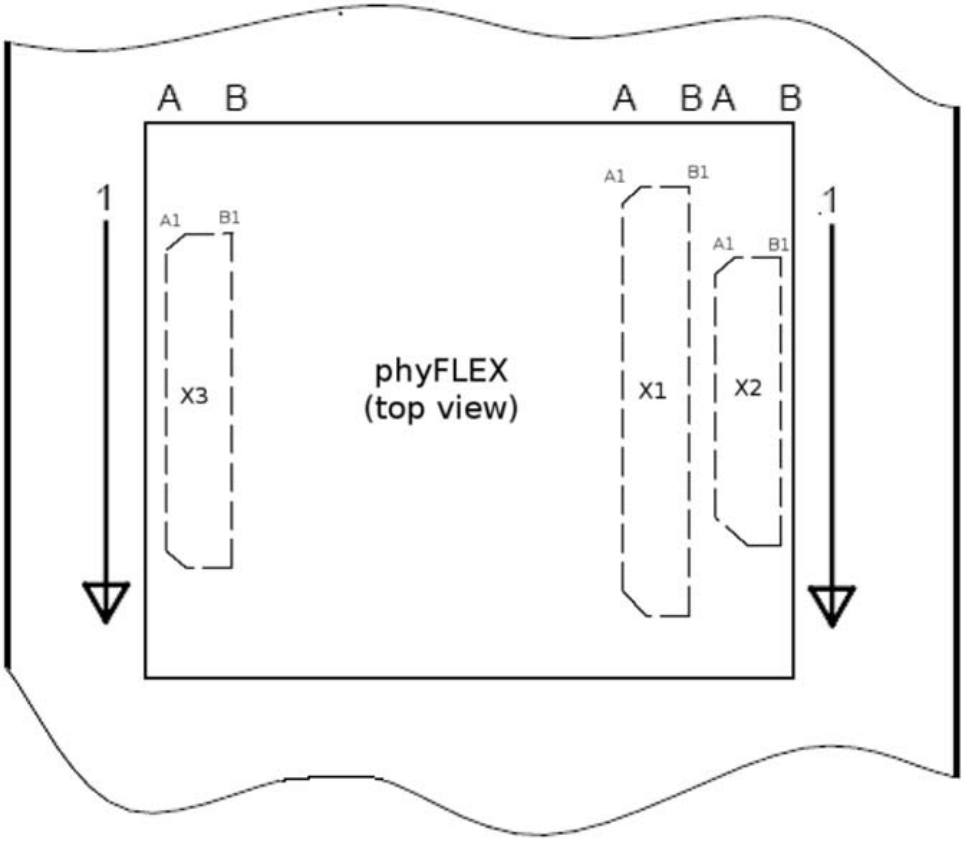


Figure 4: Pinout of the phyFLEX-Connector (top view)

Caution!

- The Freescale Semiconductor i.MX 6 is a multi-voltage operated microcontroller and as such special attention should be paid to the interface voltage levels to avoid unintentional damage to the microcontroller and other on-board components. Please refer to the Freescale Semiconductor *i.MX 6 Reference Manual* for details on the functions and features of controller signals and port pins.
- As some of the signals which are brought out on the phyFLEX-Connector are used to configure the boot mode for specific boot options, please make sure that these signals are not driven by any device on the baseboard during reset. The signals which may affect the boot configuration are shown in *Table 12*.

[6]: The specified direction indicated refers to the standard phyFLEX use of the pin.

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Caution!

- It is mandatory to avoid voltages at the IO pins of the phyFLEX-i.MX 6 which are sourced from the supply voltage of peripheral devices attached to the SOM during power-up, or power–down. These voltages can cause a current flow into the controller especially if peripheral devices attached to the interfaces of the i.MX 6 are supposed to be powered while the phyFLEX-i.MX 6 is in suspend mode, or turned off. To avoid this bus switches either supplied by VDD_3V3_LOGIC on the phyFLEX side, or having their output enable to the SOM controlled by the X_PM_PWR_GOOD signal (*section 4.3*) must be used.

Note:

- Signals on the phyFLEX-fix (X1) and phyFLEX-optional (X2) connectors have fixed positions equal for all phyFLEX SOMs. Furthermore all phyFLEX SOMs support all interfaces specified for the phyFLEX-fix connector (X1). As opposed to this, the phyFLEX-optional connector (X2) has optional, but defined interfaces at fixed positions (e.g. SATA, CAN, camera). Other phyFLEX SOMs might have more, or less interfaces.
- The following tables describe the full set of signals available at the phyFLEX-Connector according to the phyFLEX specification. However, the availability of some interfaces is order-specific (e.g. Camera_0). Thus, some signals might not be available on your module.
- Most of the controller pins have multiple multiplexed functions. As most of these pins are connected directly to the phyFLEX-Connector the alternative functions are available by using the i.MX 6's pin muxing options. Signal names and descriptions in *Table 3* to *Table 8* however, are in regard to the specification of the phyFLEX-i.MX 6 and the functions defined therein. Please refer to the *i.MX 6 Reference Manual*, or the schematic to get to know about alternative functions. In order to utilize a specific pin's alternative function the corresponding registers must be configured within the appropriate driver of the BSP.
- The numbering in the signal names of the various interfaces is in compliance with the phyFLEX specification, it might not correspond to the numbering in the controller's documentation. The numbering from the controller's perspective can be found in the *Description* column. E.g. the signals of the phyFLEX's UART0 interface (X1A18 and X1A20) are derived from the controller's UART 4.
- If the phyFLEX-i.MX 6 is delivered with a carrier board (e.g. the phyFLEX Carrier Board) the pin muxing might be changed within the appropriate BSP in order to support all features of the carrier board. If so, information on the differences from the pinout given in the following tables can be found in the carrier board's documentation.

Pin #	Signal	ST	Voltage domain	Description
X1A1	VDD_5V_IN_R	PWR_I	5V	5 V Primary Voltage Supply Input
X1A2	VDD_5V_IN_R	PWR_I	5V	5 V Primary Voltage Supply Input
X1A3	VDD_5V_IN_R	PWR_I	5V	5 V Primary Voltage Supply Input
X1A4	GND	-	-	Ground 0 V
X1A5	X_JTAG_TRSTB	I	VDD_3V3_LOGIC	JTAG reset input (low active)
X1A6	X_JTAG_TDI	I	VDD_3V3_LOGIC	JTAG TDI
X1A7	X_JTAG_TMS	I	VDD_3V3_LOGIC	JTAG TMS
X1A8	X_JTAG_TDO	O	VDD_3V3_LOGIC	JTAG TDO
X1A9	X_JTAG_TCK	I	VDD_3V3_LOGIC	JTAG clock input
X1A10	GND	-	-	Ground 0 V
X1A11	N.C.	-	-	Not connected
X1A12	X_UART1_TxD_TTL	O	VDD_3V3_LOGIC	UART3 serial transmit signal
X1A13	X_UART1_RxD_TTL	I	VDD_3V3_LOGIC	UART3 serial data receive signal
X1A14	X_UART1_RTS_TTL	O	VDD_3V3_LOGIC	UART3 request to send
X1A15	X_UART1_CTS_TTL	I	VDD_3V3_LOGIC	UART3 clear to send
X1A16	GND	-	-	Ground 0 V
X1A17	reference-voltage	REF_O	VDD_3V3_LOGIC	UART3 reference voltage
X1A18	X_UART0_TxD_TTL	O	VDD_3V3_LOGIC	UART4 serial transmit signal
X1A19	reference-voltage	REF_O	VDD_3V3_LOGIC	UART4 reference voltage
X1A20	X_UART0_RxD_TTL	I	VDD_3V3_LOGIC	UART4 serial data receive signal
X1A21	X_SPI0_MOSI	O	VDD_3V3_LOGIC	eCSPI3 master output/slave input
X1A22	GND	-	-	Ground 0 V
X1A23	X_SPI0_MISO	I	VDD_3V3_LOGIC	eCSPI3 master input/slave output
X1A24	X_SPI0_CSBOOT	O	VDD_3V3_LOGIC	eCSPI3 chip select 0 (BOOT)
X1A25	X_SPI0_CS0	O	VDD_3V3_LOGIC	eCSPI3 chip select 1
X1A26	X_SPI0_CS1	O	VDD_3V3_LOGIC	eCSPI3 chip select 2
X1A27	reference-voltage	REF_O	VDD_3V3_LOGIC	SPI0 reference voltage
X1A28	GND	-	-	Ground 0 V
X1A29	X_SPI0_CLK	O	VDD_3V3_LOGIC	eCSPI3 clock signal
X1A30	X_SPI1_CS0[7]	O	VDD_3V3_LOGIC	eCSPI5 chip select 0
X1A31	X_SPI1_MOSI[7]	O	VDD_3V3_LOGIC	eCSPI5 master output/slave input

Table 3: Pinout of the phyFLEX-fix Connector X1, Row A

[7]: SPI1 is not available for i.MX 6 Solo and i.MX 6 Dual Lite

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Pin #	Signal	ST	Voltage domain	Description
X1A32	X_SPI1_MISO[7]	I	VDD_3V3_LOGIC	eCSPI5 master input/slave output
X1A33	reference-voltage	REF_O	VDD_3V3_LOGIC	SPI1 reference voltage
X1A34	GND	-	-	Ground 0 V
X1A35	X_SPI1_CLK[7]	O	VDD_3V3_LOGIC	eCSPI5 clock signal
X1A36	X_SPI1_CS1[7]	O	VDD_3V3_LOGIC	eCSPI5 chip select 1
X1A37	X_USB0_nVBUSEN	O	VDD_3V3_LOGIC	USB OTG VBUS enable (active low)
X1A38	X_USB0_VBUS	PWR_I	5V	USB OTG VBUS input
X1A39	X_USB0_nOC	IPU	VDD_3V3_LOGIC	USB OTG overcurrent input
X1A40	GND	-	-	Ground 0 V
X1A41	reference-voltage	REF_O	VDD_3V3_LOGIC	USB0 reference voltage
X1A42	X_USB0_CHGDET	O	VDD_3V3_LOGIC	USB OTG charger detection
X1A43	X_USB1_nVBUSEN	O	VDD_3V3_LOGIC	USB host 1 VBUS enable (active low)
X1A44	X_USB1_VBUS	PWR_I	5V	USB host 1 VBUS input
X1A45	X_USB1_nOC	IPU	VDD_3V3_LOGIC	USB host 1 overcurrent input
X1A46	GND	-	-	Ground 0 V
X1A47	reference-voltage	REF_O	VDD_3V3_LOGIC	USB1 reference voltage
X1A48	X_I2S0_CLK	O	VDD_3V3_LOGIC	I^2S AUD5 receive clock
X1A49	X_I2S0_FRM	O	VDD_3V3_LOGIC	I^2S AUD5 receive frame
X1A50	X_I2S0_ADC	I	VDD_3V3_LOGIC	I^2S AUD5 receive data
X1A51	reference-voltage	REF_O	VDD_3V3_LOGIC	I^2S reference voltage
X1A52	GND	-	-	Ground 0 V
X1A53	X_I2S0_DAC	O	VDD_3V3_LOGIC	I^2S AUD5 transmit data
X1A54	X_GPIO0	I/O	VDD_3V3_LOGIC	General purpose input/output 0 (GPIO5_8 of i.MX 6)
X1A55	X_GPIO1	I/O	VDD_3V3_LOGIC	General purpose input/output 1 (GPIO5_7 of i.MX 6)
X1A56	X_GPIO2	I/O	VDD_3V3_LOGIC	General purpose input/output 2 (GPIO4_18 of i.MX 6)
X1A57	reference-voltage	REF_O	VDD_3V3_LOGIC	GPIO reference voltage
X1A58	GND	-	-	Ground 0 V
X1A59	X_GPIO3	I/O	VDD_3V3_LOGIC	General purpose input/output 3 (GPIO4_19 of i.MX 6)
X1A60	X_GPIO4	I/O	VDD_3V3_LOGIC	General purpose input/output 4 (GPIO1_6 of i.MX 6)
X1A61	X_GPIO5	I/O	VDD_3V3_LOGIC	General purpose input/output 5 (GPIO1_9 of i.MX 6)
X1A62	X_GPIO6	I/O	VDD_3V3_LOGIC	General purpose input/output 6 (GPIO7_12 of i.MX 6)
X1A63	X_GPIO7	I/O	VDD_3V3_LOGIC	General purpose input/output 7 (GPIO7_13 of i.MX 6)

Table 3: Pinout of the phyFLEX-fix Connector X1, Row A (continued)

Pin #	Signal	ST	Voltage domain	Description
X1A64	GND	-	-	Ground 0 V
X1A65	X_GPIO8	I/O	VDD_3V3_LOGIC	General purpose input/output 8 (GPIO4_5 of i.MX 6)
X1A66	X_GPIO9	I/O	VDD_3V3_LOGIC	General purpose input/output 9 (GPIO2_23 of i.MX 6)
X1A67	X_GPIO10	I/O	VDD_3V3_LOGIC	General purpose input/output 10 (GPIO2_24 of i.MX 6)
X1A68	X_I2C0_SDA	OC-BI	VDD_3V3_LOGIC	I2C2 data
X1A69	X_I2C0_SCL	OC-BI	VDD_3V3_LOGIC	I2C2 clock[11]
X1A70	GND	-	-	Ground 0 V
X1A71	reference-voltage	REF_O	VDD_3V3_LOGIC	I2C0 reference voltage
X1A72	X_PM_nRESET_IN	IPU	VDD_PM	Reset input
X1A73	X_PM_nRESET_OUT	OC	-	Reset output
X1A74	X_PM_SDA	OC-BI	VDD_3V3_LOGIC	Power management bus data (EMIC)
X1A75	X_PM_SCL	OC-BI	VDD_3V3_LOGIC	Power management bus clock (EMIC)
X1A76	GND	-	-	Ground 0 V
X1A77	X_PM_nON/WAKEUP/OFF	IPU	VDD_PM	Power on/wakeup/power off input
X1A78	X_PM_PWR_GOOD	OC	-	Power good output
X1A79	X_PM_PWM	OC	-	Fan PWM output
X1A80	X_PM_TACHO	OC	-	Fan tacho input

Table 3: Pinout of the phyFLEX-fix Connector X1, Row A (continued)

Pin #	Signal	ST	Voltage Domain	Description
X1B1	VDD_5V_IN_R	PWR_I	5V	5 V Primary Voltage Supply Input
X1B2	VDD_5V_IN_R	PWR_I	5V	5 V Primary Voltage Supply Input
X1B3	VDD_5V_IN_R	PWR_I	5V	5 V Primary Voltage Supply Input
X1B4	GND	-	-	Ground 0 V
X1B5	reference-voltage	REF_O	VDD_3V3_LOGIC	JTAG reference voltage
X1B6	RSVD	-	-	Reserved
X1B7	GND	-	-	Ground 0 V
X1B8	reference-voltage	REF_O	VDD_SD0	SD0 reference voltage
X1B9	X_SD0_WP	IPU	VDD_SD0	SD0 write protection (GPIO1_29)
X1B10	X_SD0_nCD	IPU	VDD_SD0	SD0 card detection (active low) (GPIO1_27)
X1B11	X_SD0_D3	I/O	VDD_SD0	uSDHC3 data 3
X1B12	X_SD0_CMD	O	VDD_SD0	uSDHC3 command
X1B13	GND	-	-	Ground 0 V
X1B14	X_SD0_CLK	O	VDD_SD0	uSDHC3 clock
X1B15	X_SD0_D0	I/O	VDD_SD0	uSDHC3 data 0

Table 4: Pinout of the phyFLEX-fix Connector X1, Row B

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Pin #	Signal	ST	Voltage Domain	Description
X1B16	X_SD0_D1	I/O	VDD_SD0	uSDHC3 data 1
X1B17	X_SD0_D2	I/O	VDD_SD0	uSDHC3 data 2
X1B18	X_SD0_D4	I/O	VDD_SD0	uSDHC3 data 4
X1B19	GND	-	-	Ground 0 V
X1B20	X_SD0_D5	I/O	VDD_SD0	uSDHC3 data 5
X1B21	X_SD0_D6	I/O	VDD_SD0	uSDHC3 data 6
X1B22	X_SD0_D7	I/O	VDD_SD0	uSDHC3 data 7
X1B23	RSVD	-	-	reserved
X1B24	X_ETH0_ANALOG_ VOLTAGE	REF_O	VDD_3V3_LOGIC	ETH0 reference voltage for 10/100 Mbit
X1B25	GND	-	-	Ground 0 V
X1B26	X_ETH0_A+/TX0+	ETH_O	VDD_3V3_LOGIC	ETH0 data A+ /transmit+
X1B27	X_ETH0_A-/TX0-	ETH_O	VDD_3V3_LOGIC	ETH0 data A-/transmit-
X1B28	X_ETH0_LED0	OC	VDD_3V3_LOGIC	ETH0 link LED output
X1B29	X_ETH0_B+/RX0+	ETH_I	VDD_3V3_LOGIC	ETH0 data B+/receive+
X1B30	X_ETH0_B-/RX0-	ETH_I	VDD_3V3_LOGIC	ETH0 data B-/receive-
X1B31	GND	-	-	Ground 0 V
X1B32	X_ETH0_C+	ETH_I/O	VDD_3V3_LOGIC	ETH0 data C+ (only GbE)
X1B33	X_ETH0_C-	ETH_I/O	VDD_3V3_LOGIC	ETH0 data C- (only GbE)
X1B34	X_ETH0_LED1	OC	VDD_3V3_LOGIC	ETH0 traffic LED output
X1B35	X_ETH0_D+	ETH_I/O	VDD_3V3_LOGIC	ETH0 data D+ (only GbE)
X1B36	X_ETH0_D-	ETH_I/O	VDD_3V3_LOGIC	ETH0 data D- (only GbE)
X1B37	GND	-	-	Ground 0 V
X1B38	X_USB0_D-	USB_I/O	i.MX 6 internal	USB OTG data-
X1B39	X_USB0_D+	USB_I/O	i.MX 6 internal	USB OTG data+
X1B40	X_USB0_ID	I	VDD_3V3_LOGIC	USB OTG ID Pin
X1B41	N.C.	-	-	Not connected
X1B42	N.C.	-	-	Not connected
X1B43	GND	-	-	Ground 0 V
X1B44	X_USB1_D-	USB_/IO	i.MX 6 internal	USB host 1 data-
X1B45	X_USB1_D+	USB_I/O	i.MX 6 internal	USB host 1 data+
X1B46	X_nPCIe0_PERST	I/O	VDD_3V3_LOGIC	PCIe0 reset signal (active low) (GPIO4_17 of i.MX 6)
X1B47	N.C.	-	-	Not connected
X1B48	N.C.	-	-	Not connected
X1B49	GND		-	Ground 0 V
X1B50	X_LVDS0_L0+	LVDS_O	i.MX 6 internal	LVDS0 data 0+
X1B51	X_LVDS0_L0-	LVDS_O	i.MX 6 internal	LVDS0 data 0-

Table 4: Pinout of the phyFLEX-fix Connector X1, Row B (continued)

Pin #	Signal	ST	Voltage Domain	Description
X1B52	X_LVDS0_nDISP_EN	I/O	VDD_3V3_LOGIC	LVDS0 display enable (low active) (GPIO1_8 of i.MX 6)
X1B53	X_LVDS0_L1+	LVDS_O	i.MX 6 internal	LVDS0 data 1+
X1B54	X_LVDS0_L1-	LVDS_O	i.MX 6 internal	LVDS0 data 1-
X1B55	GND	-	-	Ground 0 V
X1B56	X_LVDS0_L2+	LVDS_O	i.MX 6 internal	LVDS0 data 2+
X1B57	X_LVDS0_L2-	LVDS_O	i.MX 6 internal	LVDS0 data 2-
X1B58	X_LVDS0_DISP_BL_PWM	I/O	VDD_3V3_LOGIC	LVDS0 backlight PWM output (PWM1_OUT of i.MX 6)
X1B59	X_LVDS0_L3+	LVDS_O	i.MX 6 internal	LVDS0 data 3+
X1B60	X_LVDS0_L3-	LVDS_O	i.MX 6 internal	LVDS0 data 3-
X1B61	GND	-	-	Ground 0 V
X1B62	X_LVDS0_CLK+	LVDS_O	i.MX 6 internal	LVDS0 clock+
X1B63	X_LVDS0_CLK-	LVDS_O	i.MX 6 internal	LVDS0 clock-
X1B64	reference-voltage	REF_O	VDD_3V3_LOGIC	LVDS0 reference voltage
X1B65	X_PCIe0_nPRSNT	I/O	VDD_3V3_LOGIC	PCIe0 present signal (low active) (GPIO1_21 of i.MX 6)
X1B66	reference-voltage	REF_O	VDD_3V3_LOGIC	PCIe0 reference voltage
X1B67	GND	-	-	Ground 0 V
X1B68	X_PCIe0_TX+	PCIe_O	i.MX 6 internal	PCIe0 transmit lane+
X1B69	X_PCIe0_TX-	PCIe_O	i.MX 6 internal	PCIe0 transmit lane-
X1B70	X_PCIe0_nWAKE	I/O	VDD_3V3_LOGIC	PCIe0 wake signal (low active) (GPIO1_7 of i.MX 6)
X1B71	X_PCIe0_RX+	PCIe_I	i.MX 6 internal	PCIe0 receive lane+
X1B72	X_PCIe0_RX-	PCIe_I	i.MX 6 internal	PCIe0 receive lane-
X1B73	GND	-	-	Ground 0 V
X1B74	X_PCIe0_CLK+	PCIe_O	i.MX 6 internal	PCIe0 clock lane+ (XTALOSC_CLK1)
X1B75	X_PCIe0_CLK-	PCIe_O	i.MX 6 internal	PCIe0 clock lane- (XTALOSC_CLK1)
X1B76	X_BOOT0	IPU	VDD_PM	Boot configuration 0
X1B77	X_BOOT1	IPU	VDD_PM	Boot configuration 1
X1B78	X_BOOT2	IPU	VDD_PM	Boot configuration 2
X1B79	GND	-	-	Ground 0 V
X1B80	RSVD	-	-	reserved

Table 4: Pinout of the phyFLEX-fix Connector X1, Row B (continued)

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Pin #	Signal	ST	Voltage Domain	Description
X2A1	X_I2C1_SDA	OC-BI	VDD_3V3_LOGIC	I2C3 data
X2A2	X_I2C1_SCL	OC-BI	VDD_3V3_LOGIC	I2C3 clock
X2A3	reference-voltage	REF_O	VDD_3V3_LOGIC	I2C1 reference voltage
X2A4	X_CAN0_TXD	O	VDD_3V3_LOGIC	FlexCAN1 transmit
X2A5	X_CAN0_RXD	I	VDD_3V3_LOGIC	FlexCAN1 receive
X2A6	GND	-	-	Ground 0 V
X2A7	reference-voltage	REF_O	VDD_3V3_LOGIC	CAN0 reference voltage
X2A8	X_HDMI0_SDA	I/O	VDD_3V3_LOGIC	HDMI I^2C data
X2A9	X_HDMI0_SCL	I/O	VDD_3V3_LOGIC	HDMI I^2C clock
X2A10	X_SATA0_TX+	LVDS_O	i.MX 6 internal	SATA PHY transmit lane+
X2A11	X_SATA0_TX-	LVDS_O	i.MX 6 internal	SATA PHY transmit lane-
X2A12	GND	-	-	Ground 0 V
X2A13	X_SATA0_RX+	LVDS_I	i.MX 6 internal	SATA PHY receive lane+
X2A14	X_SATA0_RX-	LVDS_I	i.MX 6 internal	SATA PHY receive lane-
X2A15	X_SD1_D3	I/O	VDD_SD1	uSDHC2 data 3
X2A16	X_SD1_CMD	O	VDD_SD1	uSDHC2 command
X2A17	X_SD1_CLK	O	VDD_SD1	uSDHC2 clock
X2A18	GND	-	-	Ground 0 V
X2A19	reference-voltage	REF_O	VDD_SD1	SD1 reference voltage
X2A20	X_SD1_WP	IPU	VDD_SD1	SD1 write protection(GPIO1_2)
X2A21	X_SD1_nCD	IPU	VDD_SD1	SD1 card detection (active low) (GPIO1_4)
X2A22	X_SD1_D0	I/O	VDD_SD1	uSDHC2 data 0
X2A23	X_SD1_D1	I/O	VDD_SD1	uSDHC2 data 1
X2A24	GND	-	-	Ground 0 V
X2A25	X_SD1_D2	I/O	VDD_SD1	uSDHC2 data 2
X2A26	N.C.	-	-	Not connected
X2A27	N.C.	-	-	Not connected
X2A28	N.C.	-	-	Not connected
X2A29	N.C.	-	-	Not connected
X2A30	GND	-	-	Ground 0 V
X2A31	N.C.	-	-	Not connected
X2A32	N.C.	-	-	Not connected
X2A33	N.C.	-	-	Not connected
X2A34	N.C.	-	-	Not connected
X2A35	N.C.	-	-	Not connected
X2A36	GND	-	-	Ground 0 V
X2A37	N.C.	-	-	Not connected
X2A38	N.C.	-	-	Not connected

Table 5: Pinout of the phyFLEX-optional Connector X2, Row A

Pin #	Signal	ST	Voltage Domain	Description
X2A39	N.C.	-	-	Not connected
X2A40	X_CAMERA0_LO+	LVDS_I	VDD_3V3_LOGIC	Camera_0 data+
X2A41	X_CAMERA0_LO-	LVDS_I	VDD_3V3_LOGIC	Camera_0 data-
X2A42	GND	-	-	Ground 0 V
X2A43	X_CAMERA0_CLK	O	VDD_3V3_LOGIC	Camera_0 master clock (CCM_CLKO1 of i.MX 6)
X2A44	reference-voltage	REF_O	VDD_3V3_LOGIC	Camera_0 reference voltage
X2A45	RSVD	-	-	reserved
X2A46	X_CAMERA_1_LO+	LVDS_I	VDD_3V3_LOGIC	Camera_1 data+
X2A47	X_CAMERA1_LO-	LVDS_I	VDD_3V3_LOGIC	Camera_1 data-
X2A48	GND	-	-	Ground 0 V
X2A49	X_CAMERA1_CLK	O	VDD_3V3_LOGIC	Camera_1 master clock (CCM_CLKO2[8] of i.MX 6)
X2A50	reference-voltage	REF_O	VDD_3V3_LOGIC	Camera_1 reference voltage

Table 5: Pinout of the phyFLEX-optional Connector X2, Row A (continued)

Pin #	Signal	ST	Voltage Domain	Description
X2B1	X_HDMI0_TMDS_DATA2+	TMDS_O	i.MX 6 internal	HDMI data 2+
X2B2	X_HDMI0_TMDS_DATA2-	TMDS_O	i.MX 6 internal	HDMI data 2-
X2B3	GND	-	-	Ground 0 V
X2B4	X_HDMI0_TMDS_DATA1+	TMDS_O	i.MX 6 internal	HDMI data 1+
X2B5	X_HDMI0_TMDS_DATA1-	TMDS_O	i.MX 6 internal	HDMI data 1-
X2B6	reference-voltage	REF_O	VDD_3V3_LOGIC	HDMI0 reference voltage
X2B7	X_HDMI0_TMDS_DATA0+	TMDS_O	i.MX 6 internal	HDMI data 0+
X2B8	X_HDMI0_TMDS_DATA0-	TMDS_O	i.MX 6 internal	HDMI data 0-
X2B9	GND	-	-	Ground 0 V
X2B10	X_HDMI0_TMDS_CLOCK+	TMDS_O	i.MX 6 internal	HDMI clock+
X2B11	X_HDMI0_TMDS_CLOCK-	TMDS_O	i.MX 6 internal	HDMI clock-
X2B12	X_HDMI0_CEC	I/O	VDD_3V3_LOGIC	HDMI CEC
X2B13	X_HDMI0_nHPD	I	VDD_3V3_LOGIC	HDMI hot plug detect
X2B14	N.C.	-	-	Not connected
X2B15	GND	-	-	Ground 0 V
X2B16	N.C.	-	-	Not connected
X2B17	N.C.	-	-	Not connected
X2B18	N.C.	-	-	Not connected
X2B19	N.C.	-	-	Not connected
X2B20	N.C.	-	-	Not connected
X2B21	GND	-	-	Ground 0 V

Table 6: Pinout of the phyFLEX-optional Connector X2, Row B

[8]: Or CCM_CLKO1 if jumper J26 is closed between 2+3 (*section 14.2.1.1*)

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Pin #	Signal	ST	Voltage Domain	Description
X2B22	N.C.	-	-	Not connected
X2B23	N.C.	-	-	Not connected
X2B24	N.C.	-	-	Not connected
X2B25	N.C.	-	-	Not connected
X2B26	N.C.	-	-	Not connected
X2B27	GND	-	-	Ground 0 V
X2B28	N.C.	-	-	Not connected
X2B29	N.C.	-	-	Not connected
X2B30	RSVD	-	-	reserved
X2B31	N.C.	-	-	Not connected
X2B32	N.C.	-	-	Not connected
X2B33	GND	-	-	Ground 0 V
X2B34	N.C.	-	-	Not connected
X2B35	N.C.	-	-	Not connected
X2B36	RSVD	-	-	reserved
X2B37	N.C.	-	-	Not connected
X2B38	N.C.	-	-	Not connected
X2B39	GND	-	-	Ground 0 V
X2B40	N.C.	-	-	Not connected
X2B41	N.C.	-	-	Not connected
X2B42	N.C.	-	-	Not connected
X2B43	N.C.	-	-	Not connected
X2B44	N.C.	-	-	Not connected
X2B45	GND	-	-	Ground 0 V
X2B46	N.C.	-	-	Not connected
X2B47	N.C.	-	-	Not connected
X2B48	N.C.	-	-	Not connected
X2B49	N.C.	-	-	Not connected
X2B50	N.C.	-	-	Not connected

Table 6: Pinout of the phyFLEX-optional Connector X2, Row B (continued)

Caution!
Signals on the phyFLEX-flex connector X3 are module specific and depend on the features of the controller populating the SOM. This means that they are not present on all phyFLEX modules. Thus use of these signals should be carefully elaborated to avoid limitation of the compatibility across the phyFLEX module family.
Please make sure that signals of the phyFLEX-flex connector used on a custom specific carrier board are not already in use for other functions on the SOM (e.g. signals X_CSI0_x are used for the Camera_0 interface, if U27 is populated).

Pin #	Signal	ST	Voltage Domain	Description
X3A1	X_CSI_CLK0P	CSI-2_I	i.MX 6 internal	MIPI/CSI-2 clock+
X3A2	X_CSI_CLK0M	CSI-2_I	i.MX 6 internal	MIPI/CSI-2 clock-
X3A3	X_CSI0_DAT10	I	VDD_3V3_LOGIC	IPU1_CSI0 data 10
X3A4	X_CSI_D0P	CSI-2_I	i.MX 6 internal	MIPI/CSI-2 data 0+
X3A5	X_CSI_D0M	CSI-2_I	i.MX 6 internal	MIPI/CSI-2 data 0-
X3A6	GND	-	-	Ground 0 V
X3A7	X_CSI_D1P	CSI-2_I	i.MX 6 internal	MIPI/CSI-2 data 1+
X3A8	X_CSI_D1M	CSI-2_I	i.MX 6 internal	MIPI/CSI-2 data 1-
X3A9	X_CSI0_DAT11	I	VDD_3V3_LOGIC	IPU1_CSI0 data 11
X3A10	X_CSI_D2P	CSI-2_I	i.MX 6 internal	MIPI/CSI-2 data 2+
X3A11	X_CSI_D2M	CSI-2_I	i.MX 6 internal	MIPI/CSI-2 data 2-
X3A12	GND	-	-	Ground 0 V
X3A13	X_CSI_D3P	CSI-2_I	i.MX 6 internal	MIPI/CSI-2 data 3+
X3A14	X_CSI_D3M	CSI-2_I	i.MX 6 internal	MIPI/CSI-2 data 3-
X3A15	X_CSI0_DAT12	I	VDD_3V3_LOGIC	IPU1_CSI0 data 12
X3A16	X_CSI0_DAT13	I	VDD_3V3_LOGIC	IPU1_CSI0 data 13
X3A17	X_CSI0_DAT14	I	VDD_3V3_LOGIC	IPU1_CSI0 data 14
X3A18	GND	-	-	Ground 0 V
X3A19	X_CSI0_DAT15	I	VDD_3V3_LOGIC	IPU1_CSI0 data 15
X3A20	X_CSI0_DAT16	I	VDD_3V3_LOGIC	IPU1_CSI0 data 16
X3A21	X_CSI0_DAT17	I	VDD_3V3_LOGIC	IPU1_CSI0 data 17
X3A22	X_CSI0_DAT18	I	VDD_3V3_LOGIC	IPU1_CSI0 data 18
X3A23	X_CSI0_DAT19	I	VDD_3V3_LOGIC	IPU1_CSI0 data 19
X3A24	GND	-	-	Ground 0 V
X3A25	X_CSI0_MCLK	I	VDD_3V3_LOGIC	IPU1_CSI0 horizontal sync
X3A26	X_CSI0_PIXCLK	I	VDD_3V3_LOGIC	IPU1_CSI0 pixel clock
X3A27	X_CSI0_VSYNC	I	VDD_3V3_LOGIC	IPU1_CSI0 vertical sync
X3A28	X_CSI0_DATA_EN	O	VDD_3V3_LOGIC	IPU1_CSI0 data enable
X3A29	X_TAMPER	I	VDD_3V3_LOGIC	Tamper
X3A30	GND	-	-	Ground 0 V
X3A31	X_EIM_WAIT	I	VDD_3V3_LOGIC	EIM wait[11]
X3A32	X_EIM_A24	O	VDD_3V3_LOGIC	IPU2_CSI1 data 19[11]
X3A33	X_EIM_A23	O	VDD_3V3_LOGIC	IPU2_CSI1 data 18[11]
X3A34	X_EIM_A22	O	VDD_3V3_LOGIC	IPU2_CSI1 data 17[11]
X3A35	X_EIM_A21	O	VDD_3V3_LOGIC	IPU2_CSI1 data 16[11]
X3A36	GND	-	-	Ground 0 V
X3A37	X_EIM_A20	O	VDD_3V3_LOGIC	IPU2_CSI1 data 15[11]
X3A38	X_EIM_A19	O	VDD_3V3_LOGIC	IPU2_CSI1 data 14[11]
X3A39	X_EIM_A18	O	VDD_3V3_LOGIC	IPU2_CSI1 data 13[11]

Table 7: Pinout of the phyFLEX-flex Connector X3, Row A

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Pin #	Signal	ST	Voltage Domain	Description
X3A40	X_EIM_A17	O	VDD_3V3_LOGIC	IPU2_CSI1 data 12[11]
X3A41	X_EIM_EB0	O	VDD_3V3_LOGIC	IPU2_CSI1 data 11[9; 11]
X3A42	GND	-	-	Ground 0 V
X3A43	X_EIM_EB1	O	VDD_3V3_LOGIC	IPU2_CSI1 data 10[11]
X3A44	X_EIM_DA0	I/O	VDD_3V3_LOGIC	IPU2_CSI1 data 9[11]
X3A45	X_EIM_DA1	I/O	VDD_3V3_LOGIC	IPU2_CSI1 data 8[11]
X3A46	X_EIM_DA2	I/O	VDD_3V3_LOGIC	IPU2_CSI1 data 7[11]
X3A47	X_EIM_DA3	I/O	VDD_3V3_LOGIC	IPU2_CSI1 data 6[11]
X3A48	GND	-	-	Ground 0 V
X3A49	X_EIM_DA4	I/O	VDD_3V3_LOGIC	IPU2_CSI1 data 5[11]
X3A50	X_EIM_DA5	I/O	VDD_3V3_LOGIC	IPU2_CSI1 data 4[11]
X3A51	X_EIM_DA6	I/O	VDD_3V3_LOGIC	IPU2_CSI1 data 3[11]
X3A52	X_EIM_DA7	I/O	VDD_3V3_LOGIC	IPU2_CSI1 data 2[11]
X3A53	X_EIM_DA8	I/O	VDD_3V3_LOGIC	IPU2_CSI1 data 1[11]
X3A54	GND	-	-	Ground 0 V
X3A55	X_EIM_DA9	I/O	VDD_3V3_LOGIC	IPU2_CSI1 data 0[11]
X3A56	X_EIM_DA10	I/O	VDD_3V3_LOGIC	EIM address/data 10[10; 11]
X3A57	X_EIM_DA11	I/O	VDD_3V3_LOGIC	IPU2_CSI1 horizontal sync[11]
X3A58	X_EIM_DA12	I/O	VDD_3V3_LOGIC	IPU2_CSI1 vertical sync[11]
X3A59	X_EIM_A16	O	VDD_3V3_LOGIC	IPU2_CSI1 pixel clock[11]
X3A60	GND	-	-	Ground 0 V

Table 7: Pinout of the phyFLEX-flex Connector X3, Row A (continued)

Pin #	Signal	ST	Votlage domain	Description
X3B1	X_LVDS1_TX0_P	LVDS_O	i.MX 6 internal	LVDS1 data 0+
X3B2	X_LVDS1_TX0_N	LVDS_O	i.MX 6 internal	LVDS1 data 0-
X3B3	GND	-	-	Ground 0 V
X3B4	X_LVDS1_TX1_P	LVDS_O	i.MX 6 internal	LVDS1 data 1+
X3B5	X_LVDS1_TX1_N	LVDS_O	i.MX 6 internal	LVDS1 data 1-
X3B6	X_DISP0_DAT9/ PWM2_PWMO	O	VDD_3V3_LOGIC	IPU1_DISP0 data 9/PWM2 output
X3B7	X_LVDS1_TX2_P	LVDS_O	i.MX 6 internal	LVDS1 data 2+
X3B8	X_LVDS1_TX2_N	LVDS_O	i.MX 6 internal	LVDS1 data 2-
X3B9	GND	-	-	Ground 0 V
X3B10	X_LVDS1_TX3_P	LVDS_O	i.MX 6 internal	LVDS1 data 3+

Table 8: Pinout of the phyFLEX-flex Connector X3, Row B

[9]: **Note:** Signal X_EIM_EB0 is used to control the power down mode of the deserializer at U12. It should only be used as data signal of the parallel camera interface if U12 is not mounted.

[10]: **Note:** Signal X_EIM_DA10 is used as enable signal for the deserializer at U12. It should only be used as data signal of the parallel camera interface if U12 is not mounted.

Pin #	Signal	ST	Votlage domain	Description
X3B11	X_LVDS1_TX3_N	LVDS_O	i.MX 6 internal	LVDS1 data 3-
X3B12	X_CSI0_DAT4	I	VDD_3V3_LOGIC	IPU1_CSI0 data 4
X3B13	X_LVDS1_CLK_P	LVDS_O	i.MX 6 internal	LVDS1 clock+
X3B14	X_LVDS1_CLK_N	LVDS_O	i.MX 6 internal	LVDS1 clock-
X3B15	GND	-	-	Ground 0 V
X3B16	X_MLB_DP	MLB_I/O	i.MX 6 internal	Media local bus data line+
X3B17	X_MLB_DN	MLB_I/O	i.MX 6 internal	Media local bus data line-
X3B18	X_CSI0_DAT5	I	VDD_3V3_LOGIC	IPU1_CSI0 data 5
X3B19	X_MLB_SP	MLB_I/O	i.MX 6 internal	Media local bus signal line+
X3B20	X_MLB_SN	MLB_I/O	i.MX 6 internal	Media local bus signal line-
X3B21	GND	-	-	Ground 0 V
X3B22	X_MLB_CP	MLB_O	i.MX 6 internal	Media local bus clock+
X3B23	X_MLB_CN	MLB_O	i.MX 6 internal	Media local bus clock-
X3B24	X_CSI0_DAT9	I	VDD_3V3_LOGIC	IPU1_CSI0 data 9
X3B25	X_EIM_LBA	O	VDD_3V3_LOGIC	EIM load burst address[11]
X3B26	X_EIM_RW	O	VDD_3V3_LOGIC	EIM Read/write[11]
X3B27	GND	-	-	Ground 0 V
X3B28	X_CSI0_DAT8	I	VDD_3V3_LOGIC	IPU1_CSI0 data 8
X3B29	X_EIM_OE	O	VDD_3V3_LOGIC	EIM output enable
X3B30	X_EIM_BCLK	O	VDD_3V3_LOGIC	EIM burst clock
X3B31	X_EIM_DA13	I/O	VDD_3V3_LOGIC	EIM address/data 13[11]
X3B32	X_EIM_DA14	I/O	VDD_3V3_LOGIC	EIM address/data 14[11]
X3B33	GND	-	-	Ground 0 V
X3B34	X_EIM_DA15	I/O	VDD_3V3_LOGIC	EIM address/data 15[11]
X3B35	X_CLK2_P	LVDS_I/O	i.MX 6 internal	Differential clock 2+ (XTALOSC_CLK2)
X3B36	X_CLK2_N	LVDS_I/O	i.MX 6 internal	Differential clock 2- (XTALOSC_CLK2)
X3B37	X_GPIO_16	I/O	VDD_3V3_LOGIC	GPIO16
X3B38	X_EIM_D22	I/O	VDD_3V3_LOGIC	EIM data 22
X3B39	GND	-	-	Ground 0 V
X3B40	X_CSI0_DAT7	I	VDD_3V3_LOGIC	IPU1_CSI0 data 7
X3B41	X_CSI0_DAT6	I	VDD_3V3_LOGIC	IPU1_CSI0 data 6
X3B42	X_KEY_COL1	I/O	VDD_3V3_LOGIC	Keypad column 1
X3B43	X_KEY_ROW1	I/O	VDD_3V3_LOGIC	Keypad row 1
X3B44	PMIC_VBBAT	PWR_I	2 V – 5 V	PMIC Backup power supply
X3B45	GND	-	-	Ground 0 V
X3B46	VDD_MX6_SNVS	PWR_I	3 V	i.MX 6 Backup power supply (normally generated by PMIC)

Table 8: Pinout of the phyFLEX-flex Connector X3, Row B (continued)

[11]: **Caution!** These pins are also used as boot mode pins by the i.MX 6.. Special care must be taken not to override the device configuration when using this pin as input (*section 5*).

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Pin #	Signal	ST	Votlage domain	Description
X3B47	X_DIO_DISP_CLK	O	VDD_3V3_LOGIC	DIO display clock
X3B48	X_DIO_PIN4	O	VDD_3V3_LOGIC	DIO pin 4
X3B49	X_DISP0_DAT6	O	VDD_3V3_LOGIC	DISP0 data 6
X3B50	X_DISP0_DAT7	O	VDD_3V3_LOGIC	DISP0 data 7
X3B51	GND	-	-	Ground 0 V
X3B52	X_DISP0_DAT10	O	VDD_3V3_LOGIC	DISP0 data 10
X3B53	X_DISP0_DAT11	O	VDD_3V3_LOGIC	DISP0 data 11
X3B54	X_DISP0_DAT12	O	VDD_3V3_LOGIC	DISP0 data 12
X3B55	X_DISP0_DAT15	O	VDD_3V3_LOGIC	DISP0 data 15
X3B56	X_DISP0_DAT20	O	VDD_3V3_LOGIC	DISP0 data 20
X3B57	GND	-	-	Ground 0 V
X3B58	X_DISP0_DAT21	O	VDD_3V3_LOGIC	DISP0 data 21
X3B59	X_DISP0_DAT22	O	VDD_3V3_LOGIC	DISP0 data 22
X3B60	X_DISP0_DAT23	O	VDD_3V3_LOGIC	DISP0 data 23

Table 8: Pinout of the phyFLEX-flex Connector X3, Row B (continued)

3 Jumpers

For configuration purposes, the phyFLEX-i.MX 6 has several solder jumpers, some of which have been installed prior to delivery. *Figure 5* illustrates the numbering of the solder jumper pads, while *Figure 6* and *Figure 7* indicate the location and the default configuration of the solder jumpers on the board.

Table 9 below provides a functional summary of the solder jumpers which can be changed to adapt the phyFLEX-i.MX 6 to your needs. It shows their default positions, and possible alternative positions and functions. A detailed description of each solder jumper can be found in the applicable chapter listed in the table.

Note:
Jumpers not listed should not be changed as they are installed with regard to the configuration of the phyFLEX-i.MX 6.

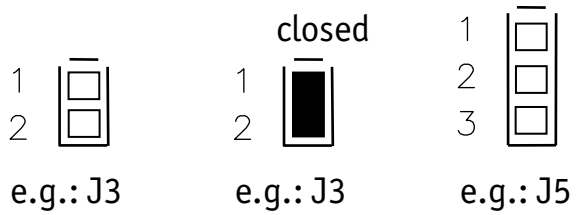


Figure 5: Typical Jumper Pad Numbering Scheme

If manual jumper modification is required please ensure that the board as well as surrounding components and sockets remain undamaged while de-soldering. Overheating the board can cause the solder pads to loosen, rendering the module inoperable. Carefully heat neighboring connections in pairs. After a few alternations, components can be removed with the solder-iron tip. Alternatively, a hot air gun can be used to heat and loosen the bonds.

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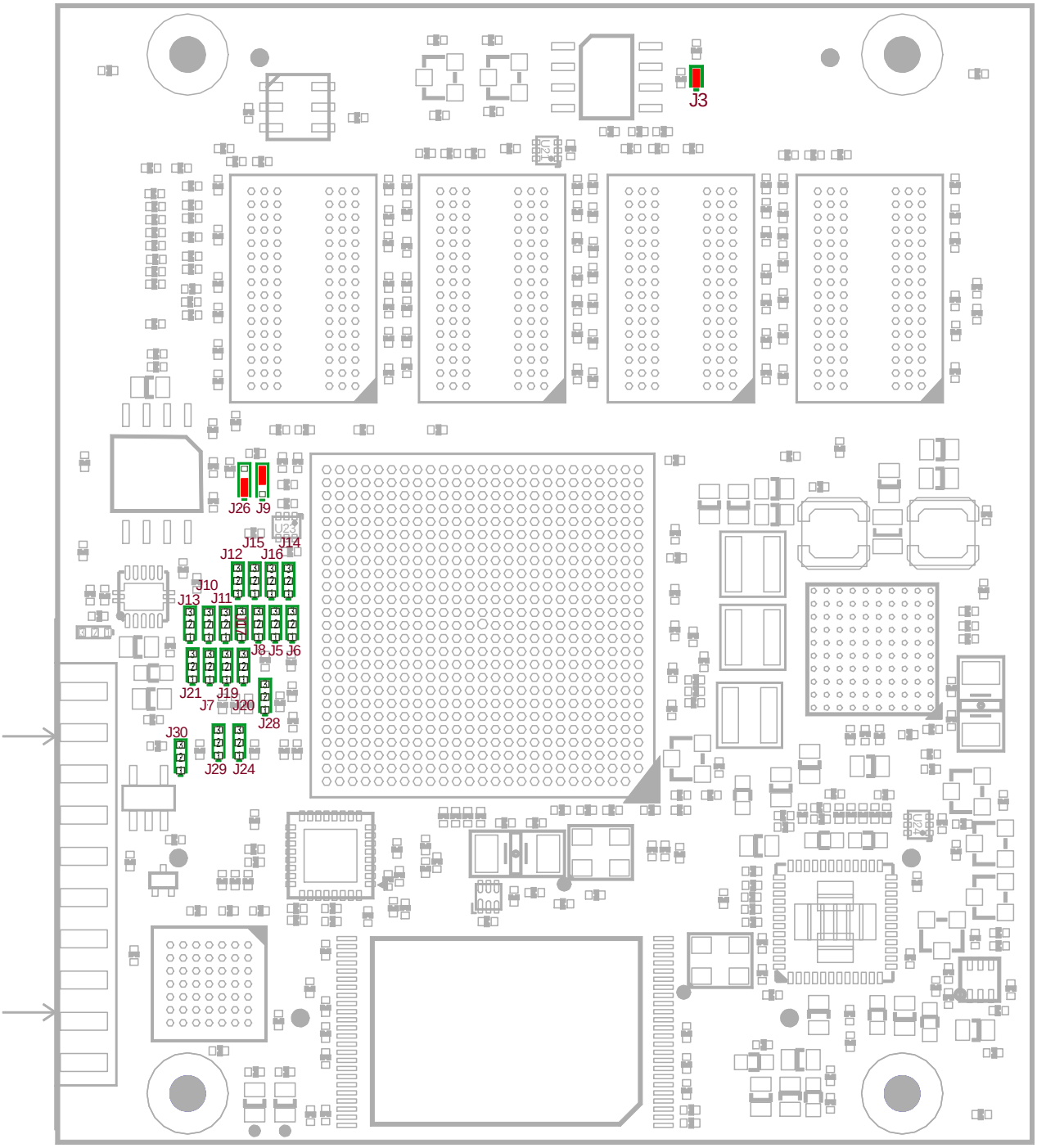


Figure 6: Jumper Locations (top view)

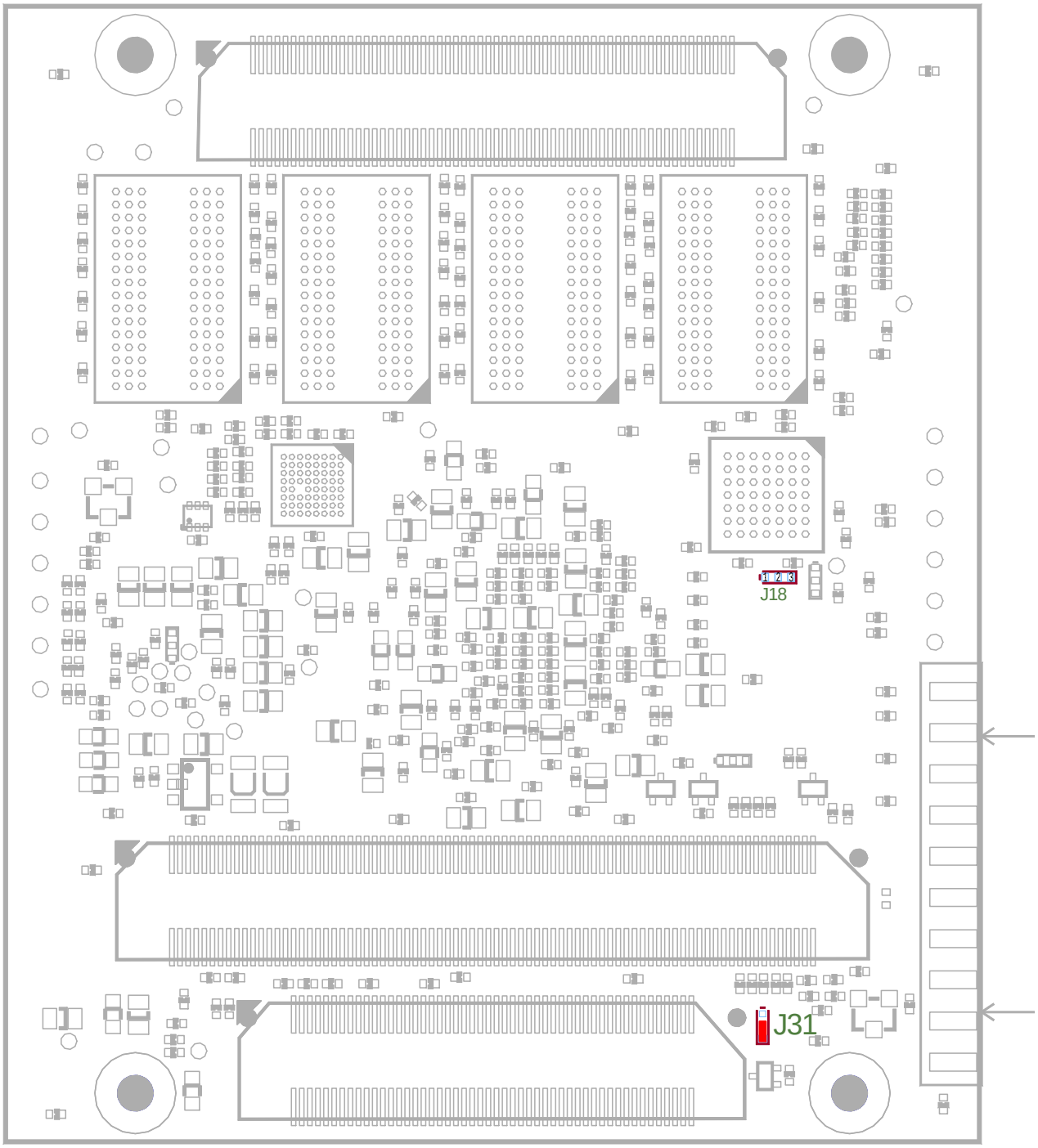


Figure 7: Jumper Locations (bottom view)

Please pay special attention to the “TYPE” column to ensure you are using the correct type of jumper (0 Ohms, 10k Ohms, etc...). The jumpers are either 0805 package or 0402 package with a 1/8 W or better power rating.

The jumpers (J = solder jumper) have the following functions:

Jumper	Description	Type	Chapter
J3	J3 connects the write protect input of the on board EEPROM with GND. If this jumper is not populated, the EEPROM is write protected.	0R (0402)	6.3.1
closed	**EEPROM is not write protected**		
open	EEPROM is write protected. The protection can be changed by the EEPROM_WP signal (GPIO3_19)		
J5-J8, J10-J21, J24,J28-J30	These jumpers are connected to the boot configuration inputs of the i.MX 6. They can be used to change the boot settings according to the i.MX 6 datasheet. *Please refer to the i.MX 6 data sheet for more detailed information.*	10 kΩ (0402)	5
J9	J9 selects rising, or falling edge strobe for the LVDS Deserializer at U12 used for the camera connectivity of the phyFLEX-i.MX 6 (Camera_1; IPU2_CSI1)	0 Ω (0402)	14.2.1.1
2+3	**rising edge strobe used for the LVDS camera signals**		
1+2	falling edge strobe used for the LVDS camera signals		
J26	Jumper J26 selects the clock signal used for camera interface Camera_1. Either a separate clock signal, or the clock signal of Camera_0 can be used. The later configuration is useful to have both camera interfaces synchronized		
1+2	**Interface Camera_1 operates with dedicated clock signal X_CAMERA1_CLK**		
2+3	Interface Camera_1 operates with the same clock signal as interface Camera_0		
J31	J31 selects rising, or falling edge strobe for the LVDS Deserializer at U27 used for the camera connectivity of the phyFLEX-i.MX 6 (Camera_0; IPU1_CSI0)	0 Ω (0402)	14.1.1.1
2+3	**rising edge strobe used for the LVDS camera signals**		
1+2	falling edge strobe used for the LVDS camera signals		

Table 9: Jumper Settings[12]

[12]: Default settings are in **bold blue** text

Jumper	Description	Type	Chapter
J26	Jumper J26 selects the clock signal used for camera interface Camera_1. Either a separate clock signal, or the clock signal of Camera_0 can be used. The later configuration is useful to have both camera interfaces synchronized	0 Ω (0402)	*14.2.1.1*
1+2	**Interface Camera_1 operates with dedicated clock signal X_CAMERA1_CLK**		
2+3	Interface Camera_1 operates with the same clock signal as interface Camera_0		

Table 9: Jumper Settings (continued)[13]

[13]: Default settings are in **bold blue** text

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4 Power

The phyFLEX-i.MX 6 operates off of a single power supply voltage.

The following sections of this chapter discuss the primary power pins on the phyFLEX-Connector X1 in detail.

4.1 Primary System Power (VDD_5V_IN_R)

The phyFLEX-i.MX 6 operates off of a primary voltage supply with a nominal value of +5 V. On-board switching regulators generate the 3.3 V, 2.5 V, 1.375 V, 1.5 V, 0.75 V, 1.2 V and 3 V voltage supplies required by the i.MX 6 MCU and on-board components from the primary 5 V supplied to the SOM.

For proper operation the phyFLEX-i.MX 6 must be supplied with a voltage source of 5 V ±5 % with 2 A load at the VCC pins on the phyFLEX-Connector X1.

VDD_5V_IN_R: X1 A1, A2, A3, B1, B2, B3

Connect all +5 V VCC input pins to your power supply and at least the matching number of GND pins.

Corresponding GND: X1 A4, A10, A16, B4, B7, B13

Please refer to *section 2* for information on additional GND Pins located at the phyFLEX-Connector X1.

Caution!
As a general design rule we recommend connecting all GND pins neighboring signals which are being used in the application circuitry. For maximum EMI performance all GND pins should be connected to a solid ground plane.

4.2 Power Management IC (PMIC) (U14)

The phyFLEX-i.MX 6 provides an on-board Power Management IC (PMIC) at position U14 to generate different voltages required by the microcontroller and the on-board components. *Figure 8* presents a graphical depiction of the powering scheme.

The PMIC supports many functions like on-chip RTC and different power management functionalities like dynamic voltage control, different low power modes and regulator supervision. It is connected to the i.MX 6 via the on-board I^2C bus (I2C1). The I^2C address of the PMIC is 0x58 (page 0 and 1) and 0x59 (page 2 and 3).

4.2.1 Power Domains

External voltages:

- VDD_5V_IN_R 5 V main supply voltage
- USB0_VBUS USB0 Bus voltage, must be supplied with 5 V if USB0 is used
- USB1_VBUS USB1 Bus voltage, must be supplied with 5 V if USB1 is used
- PMIC_VBBAT PMIC Backup supply

Internal voltages:
VDD_5V_IN[14] : only used to generate other voltages

Internally generated voltages: VDD_MX6_ARM (1.375 V), VDD_MX6_SOC (1.375 V), VDD_3V3_LOGIC (3.3 V), VDD_3V3_PMIC_IO (3.3V), VDD_SD0 and VDD_SD1 (3.3 V), VDD_ETH_IO (2.5 V) VDD_MX6_SNVS (3.0 V), VDD_MX6_HIGH (3.0 V), VDD_PM (3.3 V), VDD_ETH_1V2 (1.2 V), VDD_DDR3_1V5 (1.5 V), DDR3_VTT (0.75 V), DDR3_VREF (0.75 V)

- VDD_MX6_ARM: (1.375 V) i.MX 6 core (VDDARM_IN, VDDARM23_IN)
- VDD_MX6_SOC: (1.375 V) i.MX 6 SOC (VDDSOC_IN)
- VDD_MX6_HIGH: (3.0 V) i.MX 6 internal regulator (VDDHIGH_IN)
- VDD_MX6_SNVS: (3.0 V) i.MX 6 backup supply (VDD_SNVS_IN)
- VDD_ETH_IO: (2.5 V) i.MX 6 RGMII supply (NVCC_RGMII, NVCC_ENET), RGMII IO Ethernet PHY supply
- VDD_ETH_1V2: (1.2 V) Ethernet PHY core voltage
- VDD_SD0: (3.3 V) i.MX 6 SD3 supply (NVCC_SD3)
- VDD_SD1: (3.3 V) i.MX 6 SD2 supply (NVCC_SD2)
- VDD_PM: (3.3 V) CMIC supply
- VDD_3V3_PMIC_IO: (3.3 V) PMIC IO supply
- VDD_DDR3_1V5: (1.5 V) i.MX 6 DDR (NVCC_DRAM), RAM devices

[14]: derived from VDD_5V_IN_R via current sense amplifier at U16

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- DDR3_VTT: (0.75 V) RAM devices termination voltage
- DDR3_VREF: (0.75 V) i.MX 6 DDR3 reference voltage (DRAM_VREF), RAM devices reference voltage
- VDD_3V3_LOGIC: (3.3 V) i.MX 6 pad supply (NVCC_NANDF, NVCC_JTAG, NVCC_LCD, NVCC_CSI, NVCC_EIM, NVCC_GPIO), I^2C EEPROM, SPI Flash, NAND Flash, Camera Deserializer, Ethernet PHY, EMIC

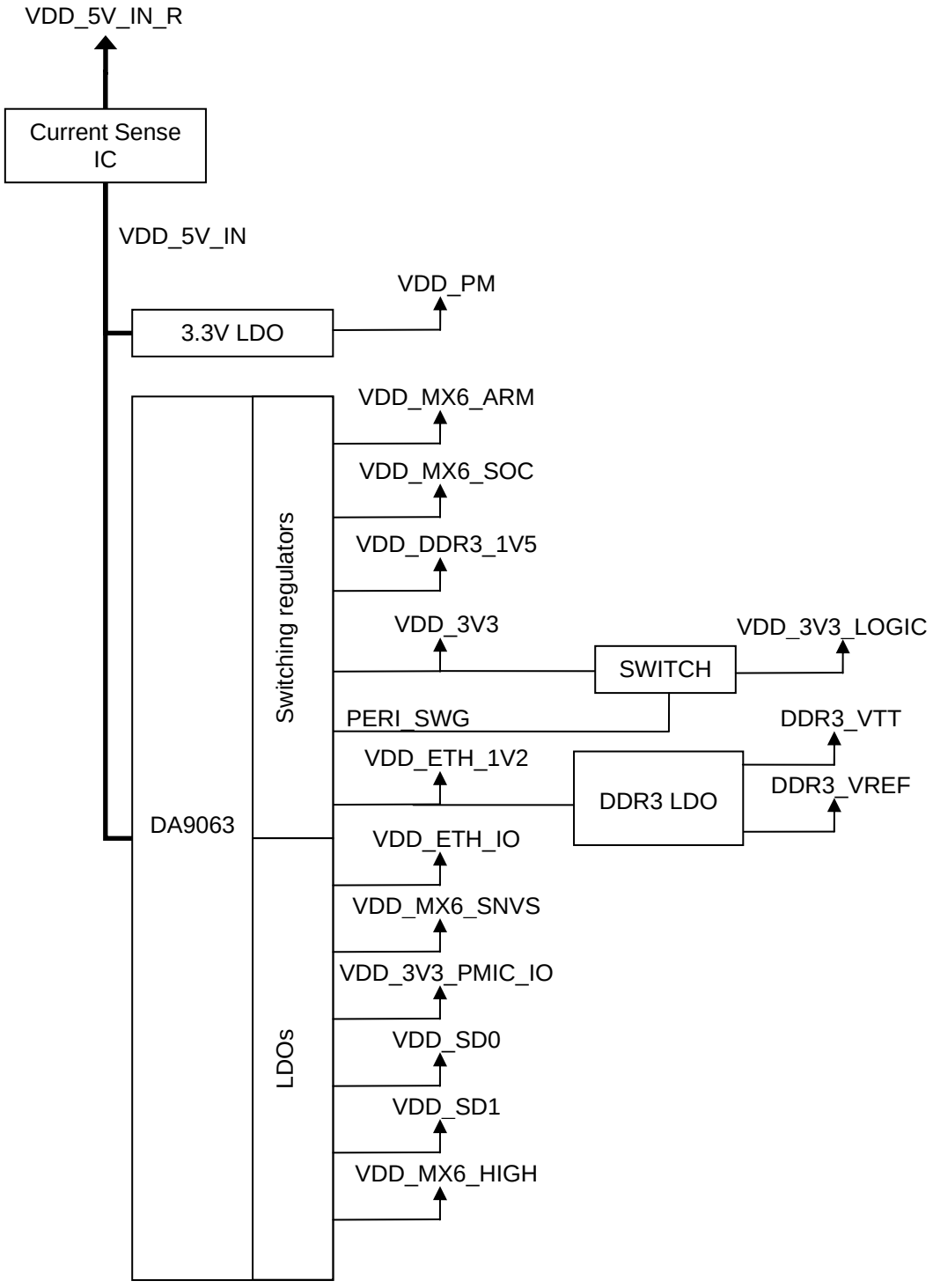


Figure 8: Powering Scheme of phyFLEX- i.MX 6

4.3 Supply Voltage for external Logic

The voltage level of the phyFLEX's logic circuitry is VDD_3V3_LOGIC (3.3 V) which is generated on-board. In order to allow connecting external devices to the phyFLEX-i.MX 6 with a different voltage level this voltage is brought out at the different reference voltage pins of the phyFLEX-Connector.

Use of level shifters supplied with VDD_3V3_LOGIC allows converting the signals according to the needs on the custom target hardware. Alternatively signals can be connected to an open drain circuitry with a pull-up resistor attached to VDD_3V3_LOGIC.

Caution!

- The maximum load for VDD_3V3_LOGIC is, according to the phyFLEX specification 50 mA. Consequently this voltage should only be used as reference, or supply voltage for level shifters, and not for supplying other external devices.
- It is mandatory to avoid voltages at the IO pins of the phyFLEX-i.MX 6 which are sourced from the supply voltage of peripheral devices attached to the SOM during power-up, or power–down. These voltages can cause a current flow into the controller especially if peripheral devices attached to the interfaces of the i.MX 6 are supposed to be powered while the phyFLEX-i.MX 6 is in suspend mode, or turned off. To avoid this bus switches either supplied by VDD_3V3_LOGIC on the phyFLEX side, or having their output enable to the SOM controlled by the X_PM_PWR_GOOD signal must be used. Also other external devices should be switched on and off by use of the X_PM_PWR_GOOD signal. This way the power-up and power–down sequencing will be considered even if the devices are not supplied directly by VDD_3V3_LOGIC.
  Not taking this into account might also lead to problems with booting the module.

4.4 Backup Power (PMIC_VBAT/VDD_MX6_SNVS)

To backup the PMIC's RTC and some of its critical registers, or the i.MX 6's low power domain (SNVS_LP) and its RTC, a secondary voltage source of 3 V can be attached to the phyFLEX-i.MX 6 at pin X3B44.

4.5 Control Management IC (CMIC) (U17))

The Control Management IC (MSP430G2253I) at U17 monitors the supply voltage and generates necessary control signals for the i.MX 6 processor as a result of different input signals. The CMIC also manages the boot, reset, wakeup and poweroff signals.

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4.5.1 Power On/Off Control

Input signal X_PM_nON/WAKEUP/OFF (X1A77) allows to turn the phyFLEX-i.MX 6 on and off. Pulling this signal low for less than 5 seconds will wake up the phyFLEX-i.MX 6 module, or will turn on the system, if it is powered off. Pulling this signal low for more than 5 seconds will turn off the system without proper shut down of the operating system.

4.5.2 Reset Control

U17 generates a reset if a reset is applied at pin X1A72 of the phyFLEX-Connector, or if the PMIC at U14 senses a voltage drop on the primary supply voltage and generates a reset signal which is available at pin X1A73 to reset peripheral devices on a carrier board.

4.5.3 Boot Control

The CMIC controls the two boot mode pins BOOT_MODE[1:0] of the i-MX 6, and is also able to overwrite the default configuration of the pull-up/pull-down circuitry of BCG1[7:4] and BCFG2[1] depending on the external boot mode inputs X_BOOT[2:0] (X1B78, X1B77 and X1B76). *Table 13* shows to which level the CMIC sets the different configuration signals for the boot modes. Please refer to *section 5* for further details.

Please refer to the phyFLEX specification for further information.

5 System Configuration and Booting

Although most features of the i.MX 6 microcontroller are configured and/or programmed during the initialization routine, other features, which impact program execution, must be configured prior to initialization via pin termination.

The system start-up configuration includes:

- Boot device order configuration

During the reset cycle the operational system boot mode of the i.MX 6 microcontroller is determined by the configuration of two BOOTMODE pins BOOT_MODE[1:0]. These pins select the boot type. If the boot type is set to “Internal boot” (BOOT_MODE[1:0]=10, BOOT_CFGx[7:0] are used to configure further boot options. You can find further information about these boot pins in the *i.MX 6 Reference Manual*.

The internal ROM code is the first code executed during the initialization process of the i.MX 6 after POR. The ROM code detects which boot devices the controller has to check by using the BOOT_MODE[1:0] and particular BOOT_CFGx[7:0] pin configuration. For serial boot devices, the ROM code polls the communication interface selected, initiates the download of the code into the internal RAM and triggers its execution from there. For memory booting, the ROM code finds the bootstrap in permanent memories such as NAND-Flash or SD-Cards and executes it. Please refer to the *i.MX 6 Reference Manual* for more information.

The phyFLEX-i.MX 6 provides three boot configuration pins BOOT[2:0]. The setting of these pins configures the boot device which is selected by the microcontroller. The standard phyFLEX boot options are shown in *Table 10*. Boot options specific for the i.MX 6 controller ar e shown in *Table 11*.

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Boot Mode	X_BOOT2	X_BOOT1	X_BOOT0	Boot Source
0	**1**	**1**	**1**	**On board memory (e.g. NAND, SSD, eMMC)**
1 (optional)	1	1	0	SPI0
2 (optional)	1	0	1	alternative on board memory (e.g. SSD, eMMC)
3 (optional)	1	0	0	SD0 external
4 (optional)	0	1	1	Serial (UART or USB)
5 (optional)	0	1	0	SATA0
6 (optional)	0	0	1	USB0
7 (optional)	0	0	0	specific (e.g. PCIe, I2C, Ethernet……)

Table 10: Standard phyFLEX Boot Options

The phyFLEX-i.MX 6 specific boot options are shown in the following table.

Boot Mode	X_BOOT2	X_BOOT1	X_BOOT0	Boot Source
0	**1**	**1**	**1**	**NAND**
1	1	1	0	SPI3, CS0 (on board SPI Flash if populated, same as mode 2)
2	1	0	1	SPI3, CS0 (on board SPI Flash if populated, same as mode 1)
3	1	0	0	SD0 external
4	0	1	1	Serial USB OTG (USB0, same as mode 6)
5	0	1	0	SATA
6	0	0	1	Serial USB OTG (USB0, same as mode 4)
7	0	0	0	Bootconfig from eFUSE

Table 11: phyFLEX-i.MX 6 specific Boot Options

The BOOT[2:0] lines have 10 kΩ pull-up resistors populated on the module. Hence leaving the three pins unconnected sets the controller to boot mode 0, NAND boot.

Note:
As some of the signals which are brought out on the phyFLEX-flex connector are used to configure the boot mode for specific boot options, please make sure that these signals are not driven by any device on the baseboard during reset. The signals which may affect the boot configuration are shown in *Table 12*.

Configuration Pin	Pin #	Signal	ST	SL	Description
BCFG1[0]	X3A44	X_EIM_DA0	I/O	3.3 V	IPU2_CSI1 data 9
BCFG1[1]	X3A45	X_EIM_DA1	I/O	3.3 V	IPU2_CSI1 data 8
BCFG1[2]	X3A46	X_EIM_DA2	I/O	3.3 V	IPU2_CSI1 data 7
BCFG1[3]	X3A47	X_EIM_DA3	I/O	3.3 V	IPU2_CSI1 data 6
BCFG1[4]	X3A49	X_EIM_DA4	I/O	3.3 V	IPU2_CSI1 data 5
BCFG1[5]	X3A50	X_EIM_DA5	I/O	3.3 V	IPU2_CSI1 data 4
BCFG1[6]	X3A51	X_EIM_DA6	I/O	3.3 V	IPU2_CSI1 data 3
BCFG1[7]	X3A52	X_EIM_DA7	I/O	3.3 V	IPU2_CSI1 data 2
BCFG2[0]	X3A53	X_EIM_DA8	I/O	3.3 V	IPU2_CSI1 data 1
BCFG2[1]	X3A55	X_EIM_DA9	I/O	3.3 V	IPU2_CSI1 data 0
BCFG2[2]	X3A56	X_EIM_DA10	I/O	3.3 V	EIM address/data10
BCFG2[3]	X3A57	X_EIM_DA11	I/O	3.3 V	IPU2_CSI1 horizontal sync
BCFG2[4]	X3A58	X_EIM_DA12	I/O	3.3 V	IPU2_CSI1 vertical sync
BCFG2[5]	X3B31	X_EIM_DA13	I/O	3.3 V	EIM address/data13
BCFG2[6]	X3B32	X_EIM_DA14	I/O	3.3 V	EIM address/data14
BCFG2[7]	X3B34	X_EIM_DA15	I/O	3.3 V	EIM address/data15
BCFG3[0]	X3A59	X_EIM_A16	O	3.3 V	IPU2_CSI1 pixel clock
BCFG3[1]	X3A40	X_EIM_A17	O	3.3 V	IPU2_CSI1 data 12
BCFG3[2]	X3A39	X_EIM_A18	O	3.3 V	IPU2_CSI1 data 13
BCFG3[3]	X3A38	X_EIM_A19	O	3.3 V	IPU2_CSI1 data 14
BCFG3[4]	X3A37	X_EIM_A20	O	3.3 V	IPU2_CSI1 data 15
BCFG3[5]	X3A35	X_EIM_A21	O	3.3 V	IPU2_CSI1 data 16
BCFG3[6]	X3A34	X_EIM_A22	O	3.3 V	IPU2_CSI1 data 17
BCFG3[7]	X3A33	X_EIM_A23	O	3.3 V	IPU2_CSI1 data 18
BCFG4[0]	X3A32	X_EIM_A24	O	3.3 V	IPU2_CSI1 data 19
BCFG4[1]	X3A31	X_EIM_WAIT	I	3.3 V	EIM wait
BCFG4[2]	X3B25	X_EIM_LBA	O	3.3 V	EIM load burst address
BCFG4[3]	X3A41	X_EIM_EB0	O	3.3 V	IPU2_CSI1 data 11
BCFG4[4]	X3A43	X_EIM_EB1	O	3.3 V	IPU2_CSI1 data 10
BCFG4[5]	X3B26	X_EIM_RW	O	3.3 V	EIM Read/write
BCFG4[6]	X1A69	X_EIM_RW	OC-BI	3.3 V	I2C2 clock
BCFG4[7]		LED_RED	not available at phyFLEX-Connector[15]		

Table 12: Boot Configuration Pins at phyFLEX-flex Connector X3 and X1

[15]: Connected to GND for the standard module configuration

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By setting the desired boot mode with the phyFLEX boot configuration pins BOOT[2:0], the CMIC, which is populated on the module, sets some of the appropriate BCFG pins and the BOOT_MODE[1:0] pins of the i.MX 6 controller. Only BCFG1[7:4], BCFG2[1], and BOOT_MODE[1:0] can be set by the CMIC. All other BCFG pins are set to a fixed value by 10 kΩ configuration resistors which are located on the phyFLEX module. Furthermore BCFG1[4], BCFG2[1] and BCFG4[2] have 10 kΩ on board configuration resistors, too.

The specific boot configuration settings, which are set by the on board configuration resistors, can be changed by modifying the resistors on the module or by connecting a configuration resistor (e.g. 10 kΩ) to the configuration signal. Please consider that any change of the default BCFG configuration can also influence other boot modes, which might result in faulty boot behavior.

For further information about the different boot modes and the influence of the BCFG pins please see the *i.MX 6 Reference Manual*.

Table 13 shows to which level the CMIC sets the different configuration signals for the boot modes. "Z" means that the CMIC sets the signal to high impedance, and thus the value of the configuration resistor is used.

Boot mode	Description	BOOT_MODE[1:0]	BCFG1[7:4]	BCFG2[1]
0	NAND	0b10	0b1000	depends on NAND size
1	SPI	0b10	0b0011	0bZ
2	SPI	0b10	0b0011	0bZ
3	SD0	0b10	0b010Z	0bZ
4	USB OTG	0b01	0bZZZZ	0bZ
5	SATA	0b10	0b0010	0bZ
6	USB OTG	0b01	0bZZZZ	0bZ
7	eFUSE	0b00	0bZZZZ	0bZ

Table 13: Boot Configuration Signals generated by the CMIC

6 System Memory

The phyFLEX-i.MX 6 provides four types of on-board memory:

- 2 Banks DDR3 RAM: 512 MB DDR3 SDRAM (up to 4 GB)[16]
- NAND Flash (VFBGA): 256 MB (up to 16 GB)[1]
- I²C-EEPROM: 4 kB[1]
- SPI Flash: 16 MB[1]

The following sections of this chapter detail each memory type used on the phyFLEX-i.MX 6.

6.1 DDR3-SDRAM (U2-U9)

The RAM memory of the phyFLEX-i.MX 6 is comprised of up to two 64 bit wide banks each of four 16-bit wide DDR3-SDRAM chips (Bank 1: U2-U5, Bank 2: U6-U9). The chips are connected to the special DDR interface called Multi Mode DDR Controller (MMDC) of the i.MX 6 microcontroller.

The DDR3 memory is accessed via the second AHB port starting at 0x1000 0000.

Typically the DDR3-SDRAM initialization is performed by a boot loader or operating system following a power-on reset and must not be changed at a later point by any application code. When writing custom code independent of an operating system or boot loader, SDRAM must be initialized by accessing the appropriate SDRAM configuration registers on the i.MX 6 controller. Refer to the *i.MX 6 Reference Manual* for accessing and configuring these registers.

[16]: Please contact Phytec for more information about additional module configurations.

6.2 NAND Flash Memory (U13)

Use of Flash as non-volatile memory on the phyFLEX-i.MX 6 provides an easily reprogrammable means of code storage.

The NAND Flash memory at U13 is connected to the General Purpose Media Interface (GPMI). Dependent on the memory size one or more of the chip enable signals NANDF_CS0, NANDF_CS1, NANDF_CS2 and NANDF_CS3 of the GPMI interface select the NAND Flash.

The Flash devices are programmable with 3.3 V. No dedicated programming voltage is required.

As of the printing of this manual these NAND Flash devices generally have a life expectancy of at least 100,000 erase/program cycles and a data retention rate of 10 years.

Any parts that are footprint (TSOP-48-50-C3) and functionally compatible may be used with the phyFLEX-i.MX 6.

6.3 I²C EEPROM (U10)

The phyFLEX-i.MX 6 is populated with a non-volatile 4 kB I^2C[17] EEPROM at U10. This memory can be used to store configuration data or other general purpose data. This device is accessed through I^2C port 1 on the i.MX 6. The control registers for I^2C port 1 are mapped between addresses 0x021A 0000 and 0x021A 3FFF. Please see the *i.MX 6 Reference Manual* for detailed information on the registers.

The three lower address bits are fixed to zero which means that the EEPROM can be accessed at I^2C address 0x50.

Write protection to the device is accomplished via jumper J3. Refer to *section 6.3.1* for further details.

[17]: See the manufacturer's data sheet for interfacing and operation.

6.3.1 EEPROM Write Protection Control (J3)

Jumper J3 controls write access to the EEPROM (U10) device. Closing this jumper allows write access to the device, while removing this jumper will cause the EEPROM to enter write protect mode, thereby disabling write access to the device.

The following configurations are possible:

EEPROM Write Protection State	J3
Write access allowed	**closed**
EEPROM is write protected. The protection can be changed by the EEPROM_WP signal (GPIO3_19)	open

Table 14: EEPROM Write Protection States via J3[18]

6.4 SPI Flash Memory (U25))

The optional SPI Flash Memory of the phyFLEX-i.MX 6 at U25 can be used to store configuration data or any other general purpose data. Beside this it can also be used as boot device[19] and recovery boot device[19]. The device is accessed through eCSPI3 SS0 on the i.MX 6. The control registers for eCSPI3 are mapped between addresses 0x0201 0000 and 0x0201 3FFF. Please see the *i.MX 6 Reference Manual* for detailed information on the registers.

The SPI Flash can be write protected. The active low signal SPI_NOR_$\overline{\text{WP}}$/GPIO3_29 connects to GPIO3_29 of the i.MX 6 and allows to control the SPI Flash's write-protection.

As of the printing of this manual these SPI Flash devices generally have a life expectancy of at least 100,000+ erase/program cycles and a data retention rate of 20 years. This makes the SPI Flash a reliable and secure solution to store the first and second level bootloaders.

[18]: Defaults are in **bold blue** text

[19]: The standard boot configuration selects the SPI Flash as recovery boot device. To use it as boot device the boot configuration, or the eFUSEs must be changed.

7 SD / MM Card Interfaces

The phyFLEX bus features one fixed and one optional SD / MM Card interface. On the phyFLEX-i.MX 6 the interface signals extend from the controllers third and second Ultra Secured Digital (uSDHC3 / uSDHC2) Host Controller to the phyFLEX-Connector. *Table 15* shows the location of the different interface signals on the phyFLEX-Connector. The MMC/SD/SDIO Host Controller is fully compatible with the SD Memory Card Specification 3.0 and SD I/O Specification, Part E1, v1.10. SDC / MMC interface SD0 (uSDHC3 of the i.MX 6), supports 8 data channels and SD1 (uSDHC2 of the i.MX 6) 4 data channels. Both interfaces have a maximum data rate of up to 104 MB/s (refer to the *i.MX 6 Reference Manual* for more information).

Pin #	Signal	ST	Voltage Domain	Description
X2A15	X_SD1_D3	I/O	VDD_SD1	uSDHC2 data 3
X2A16	X_SD1_CMD	O	VDD_SD1	uSDHC2 command
X2A17	X_SD1_CLK	O	VDD_SD1	uSDHC2 clock
X2A19	reference-voltage	REF_O	VDD_SD1	SD1 reference voltage
X2A20	X_SD1_WP	IPU	VDD_SD1	SD1 write protection; using GPIO1_2
X2A21	X_SD1_nCD	IPU	VDD_SD1	SD1 card detection (active low); using GPIO1_4
X2A22	X_SD1_D0	I/O	VDD_SD1	uSDHC2 data 0
X2A23	X_SD1_D1	I/O	VDD_SD1	uSDHC2 data 1
X2A25	X_SD1_D2	I/O	VDD_SD1	uSDHC2 data 2

Table 15: Location of the SD / MM Card Interface Signals

Pin #	Signal	ST	Voltage Domain	Description
X1B8	reference-voltage	REF_O	VDD_SDO	SDO reference voltage
X1B9	X_SDO_WP	IPU	VDD_SDO	SDO write protecttion; using GPIO1_29
X1B10	X_SDO_nCD	IPU	VDD_SDO	SDO card detection (active low); using GPIO1_27
X1B11	X_SDO_D3	I/O	VDD_SDO	uSDHC3 data 3
X1B12	X_SDO_CMD	O	VDD_SDO	uSDHC3 command
X1B13	GND	-	-	Ground 0 V
X1B14	X_SDO_CLK	O	VDD_SDO	uSDHC3 clock
X1B15	X_SDO_DO	I/O	VDD_SDO	uSDHC3 data 0
X1B16	X_SDO_D1	I/O	VDD_SDO	uSDHC3 data 1
X1B17	X_SDO_D2	I/O	VDD_SDO	uSDHC3 data 2
X1B18	X_SDO_D4	I/O	VDD_SDO	uSDHC3 data 4
X1B20	X_SDO_D5	I/O	VDD_SDO	uSDHC3 data 5
X1B21	X_SDO_D6	I/O	VDD_SDO	uSDHC3 data 6
X1B22	X_SDO_D7	I/O	VDD_SDO	uSDHC3 data 7

Table 15: Location of the SD / MM Card Interface Signals (continued)

Because of compatibility reasons a card detect and a write protect signal is added to each SDC / MMC interface (X_SDx_nCD and X_SDx_WP). The card detect and write protect function is implemented by using four GPIOs of the i.MX 6 (see tables above).

Note:
If X_SDx_WP of the interface is not used (e.g. because a micro SD-Card slot is used) you should connect this signal to GND.

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8 Serial Interfaces

The phyFLEX-i.MX 6 provides numerous serial interfaces some of which are equipped with a transceiver to allow direct connection to external devices:

1. Two High speed UARTs (TTL, derived from UART3 and UART4 of the i.MX 6) with up to 4 MHz and one with hardware flow control (RTS and CTS signals)
2. High speed USB OTG interface (extended directly from the i.MX 6's USB OTG PHY (USBPHY1))
3. High speed USB host interface (extended directly from the i.MX 6 USB host PHY (USBPHY2))
4. Auto-MDIX enabled 10/100/1000 Mbit Ethernet interface
5. Two I^2C interface (derived from I^2C port 2 and port 3 of the i.MX 6)
6. Two Serial Peripheral Interface (SPI) interface (extended from the third and fifth SPI module (eCSPI3 and eCSPI5) of the i.MX 6)
7. I^2S audio interface (originating from the fifth module of the i.MX 6's Synchronous Serial Interface (SSI5))
8. CAN 2.0B interface (extended directly from the i.MX 6 FlexCAN1 module)
9. PCI Express Gen. 2.0 (extended directly from the i.MX 6 PCIe PHY)
10. SATA II, 3.0 Gbps (extended directly from the i.MX 6 SATA PHY)
11. Media Local Bus (MLB) interface (connecting to the i.MX 6's MediaLB 150 block)

The following sections of this chapter detail each of these serial interfaces and any applicable configuration jumpers.

Note:
The numbering in the signal names of the various interfaces is in compliance with the phyFLEX specification, it might not correspond to the numbering in the controller's documentation. The numbering from the controller's perspective can be found in the Description column.

8.1 Universal Asynchronous Interface

The phyFLEX-i.MX 6 provides two high speed universal asynchronous interfaces with up to 4 MHz and one with additional hardware flow control (RTS and CTS signals). The following table shows the location of the signals on the phyFLEX-Connector.

Pin #	Signal	ST	Voltage Domain	Description
X1A12	X_UART1_TxD_TTL	O	VDD_3V3_LOGIC	UART3 serial transmit signal
X1A13	X_UART1_RxD_TTL	I	VDD_3V3_LOGIC	UART3 serial data receive signal
X1A14	X_UART1_RTS_TTL	O	VDD_3V3_LOGIC	UART3 request to send
X1A15	X_UART1_CTS_TTL	I	VDD_3V3_LOGIC	UART3 clear to send
X1A17	reference-voltage	REF_O	VDD_3V3_LOGIC	UART3 reference voltage
X1A18	X_UART0_TxD_TTL	O	VDD_3V3_LOGIC	UART4 serial transmit signal
X1A19	reference-voltage	REF_O	VDD_3V3_LOGIC	UART4 reference voltage
X1A20	X_UART0_RxD_TTL	I	VDD_3V3_LOGIC	UART4 serial data receive signal

Table 16: Location of the UART Signals

The signals extend from UART3 respectively UART4 of the i.MX 6 directly to the phyFLEX-Connector without conversion to RS-232 level. External RS-232 transceivers must be attached by the user if RS-232 levels are required.

8.2 USB OTG Interface

The phyFLEX-i.MX 6 provides a high speed USB OTG interface which uses the i.MX 6 embedded HS USB OTG PHY. An external USB Standard-A (for USB host), USB Standard-B (for USB device), or USB mini-AB (for USB OTG) connector is all that is needed to interface the phyFLEX-i.MX 6 USB OTG functionality. The applicable interface signals can be found on the phyFLEX-fix Connector X1 as shown in *Table 17*.

Pin #	Signal	ST	Voltage Domain	Description
X1A37	X_USB0_nVBUSEN	O	VDD_3V3_LOGIC	USB OTG VBUS enable (active low)
X1A38	X_USB0_VBUS	PWR_I	5 V	USB OTG VBUS input
X1A39	X_USB0_nOC	IPU	VDD_3V3_LOGIC	USB OTG overcurrent pin
X1A41	reference-voltage	REF_O	VDD_3V3_LOGIC	USB0 reference voltage
X1A42	X_USB0_CHGDET	O	VDD_3V3_LOGIC	USB OTG charger detection
X1B38	X_USB0_D-	USB_I/O	i.MX 6 internal	USB OTG data-
X1B39	X_USB0_D+	USB_I/O	i.MX 6 internal	USB OTG data+
X1B40	X_USB0_ID	I	VDD_3V3_LOGIC	USB OTG ID Pin

Table 17: Location of the USB OTG Signals

Caution!
X_USB0_VBUS must be supplied with 5 V for proper USB functionality.

8.3 USB Host Interface

The phyFLEX-i.MX 6 provides a high speed USB host interface which uses the i.MX 6 embedded HS USBhost PHY.

An external USB Standard-A (for USB host) connector is all that is needed to interface the phyFLEX-i.MX 6 USB host functionality. The applicable interface signals (D+/D-/ PWR/OC) can be found on the phyFLEX-fix Connector X1.

Pin #	Signal	ST	Voltage Domain	Description
X1A43	X_USB1_nVBUSEN	O	VDD_3V3_LOGIC	USB host 1 VBUS enable (active low)
X1A44	X_USB1_VBUS	PWR_I	5 V	USB host 1 VBUS input
X1A45	X_USB1_nOC	IPU	VDD_3V3_LOGIC	USB host 1 overcurrent pin
X1A47	reference-voltage	REF_O	VDD_3V3_LOGIC	USB1 reference voltage
X1B44	X_USB1_D-	USB_I/O	i.MX 6 internal	USB host 1 data-
X1B45	X_USB1_D+	USB_I/O	i.MX 6 internal	USB host 1 data+

Table 18: Location of the USB-Host Signals

Caution!
X_USB1_VBUS must be supplied with 5 V for proper USB functionality.

8.4 Ethernet Interface

Connection of the phyFLEX-i.MX 6 to the world wide web or a local area network (LAN) is possible using the on-board GbE PHY at U11. It is connected to the RGMII interface of the i.MX 6. The PHY operates with a data transmission speed of 10 Mbit/s, 100 Mbit/s or 1000 Mbit/s.

8.4.1 Ethernet PHY (U11)

With an Ethernet PHY mounted at U11 the phyFLEX-i.MX 6 has been designed for use in 10Base-T, 100Base-T and 1000Base-T networks. The 10/100/1000Base-T interface with its LED signals extends to the phyFLEX-fix Connector X1.

Pin #	Signal	ST	Voltage Domain	Description
X1B24	X_ETH0_ANALOG_ VOLTAGE	REF_O	VDD_3V3_LOGIC	ETH0 reference voltage for 10/100Mbit , for phyFLEX-i.MX 6 this pin is only connected to a 100 nF capacitor tied to ground
X1B26	X_ETH0_A+/TX0+	ETH_O	VDD_3V3_LOGIC	ETH0 data A+ /transmit+
X1B27	X_ETH0_A-/TX0-	ETH_O	VDD_3V3_LOGIC	ETH0 data A-/transmit-
X1B28	X_ETH0_LED0	OC	VDD_3V3_LOGIC	ETH0 link LED output
X1B29	X_ETH0_B+/RX0+	ETH_I	VDD_3V3_LOGIC	ETH0 data B+/receive+
X1B30	X_ETH0_B-/RX0-	ETH_I	VDD_3V3_LOGIC	ETH0 data B-/receive-
X1B32	X_ETH0_C+	ETH_I/O	VDD_3V3_LOGIC	ETH0 data C+ (only GbE)
X1B33	X_ETH0_C-	ETH_I/O	VDD_3V3_LOGIC	ETH0 data C- (only GbE)
X1B34	X_ETH0_LED1	OC	VDD_3V3_LOGIC	ETH0 traffic LED output
X1B35	X_ETH0_D+	ETH_I/O	VDD_3V3_LOGIC	ETH0 data D+ (only GbE)
X1B36	X_ETH0_D-	ETH_I/O	VDD_3V3_LOGIC	ETH0 data D- (only GbE)

Table 19: Location of the Ethernet Signals

The on board GbE PHY supports HP Auto-MDIX technology, eliminating the need for the consideration of a direct connect LAN cable, or a cross-over patch cable. It detects the TX and RX pins of the connected device and automatically configures the PHY TX and RX pins accordingly. The Ethernet PHY also features an Auto-negotiation to automatically determine the best speed and duplex mode.

The Ethernet PHY is connected to the RGMII interface of the i.MX 6. Please refer to the *i.MX 6 Reference Manual* for more information about this interface.

In order to connect the module to an existing 10/100/1000Base-T network some external circuitry is required. The required termination resistors on the analog signals (ETH0_A±, ETH0_B±, ETH0_C±, ETH0_D±) are integrated in the chip, so there is no need to connect external termination resistors to these signals. Connection to an external Ethernet magnetics should be done using very short signal traces. The A+/A-, B+/B-, C+,C- and D+/D- signals should be routed as 100 Ohm differential pairs. The same applies for the signal lines after the transformer circuit. The carrier board layout should avoid any other signal lines crossing the Ethernet signals.

If you are using the applicable carrier board for the phyFLEX-i.MX 6 (part number PBA-B-01), the external circuitry mentioned above is already integrated on the board (*section 19.3.5*).

Caution!
Please see the datasheet of the Ethernet PHY when designing the Ethernet transformer circuitry or refer to the schematic of the applicable carrier board (PBA-B-01) as reference.

8.4.2 Software Reset of the Ethernet Controller

The Ethernet PHY at U11 can be reset by software. The reset input of the Ethernet PHY is permanently connected to pad EIM_D23 (GPIO3_23) of the i.MX 6.

8.4.3 MAC Address

In a computer network such as a local area network (LAN), the MAC (Media Access Control) address is a unique computer hardware number. For a connection to the Internet, a table is used to convert the assigned IP number to the hardware's MAC address.

In order to guarantee that the MAC address is unique, all addresses are managed in a central location. Phytec has acquired a pool of MAC addresses. The MAC address of the phyFLEX-i.MX 6 is located on the bar code sticker attached to the module. This number is a 12-digit HEX value.

8.5 I²C Interface

The Inter-Integrated Circuit (I²C) interface is a two-wire, bidirectional serial bus that provides a simple and efficient method for data exchange among devices. The i.MX 6 contains three identical and independent multimaster fast-mode I²C modules. The interface of the second and third module (I2C2 and I2C3) are available on the phyFLEX-Connectors. The first module connects to the on-board EEPROM (*section 6.3*), the PMIC (*section 4.2*) and to the EMIC at U19 (*section 15*). Both I²C interfaces which are brought out on the connector have on board resistors which are laid-out for a capacitive load of max. 150 pF in fast mode. The following table lists the I²C ports on the phyFLEX-Connector:

Pin #	Signal	ST	Voltage Domain	Description
X1A68	X_I2C0_SDA	I/O	VDD_3V3_LOGIC	I2C2 data
X1A69	X_I2C0_SCL	I/O	VDD_3V3_LOGIC	I2C2 clock
X1A71	reference-voltage	REF_O	VDD_3V3_LOGIC	I2C0 reference voltage
X2A1	X_I2C1_SDA	I/O	VDD_3V3_LOGIC	I2C3 data
X2A2	X_I2C1_SCL	I/O	VDD_3V3_LOGIC	I2C3 clock
X2A3	reference-voltage	REF_O	VDD_3V3_LOGIC	I2C1 reference voltage

Table 20: I²C Interface Signal Location

As I²C devices on the SOM connect to I2C1 of the i.MX 6 both I²C interfaces are fully available for connecting external I²C devices to the phyFLEX-i.MX 6.

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8.6 SPI Interface

The Serial Peripheral Interface (SPI) interface is a four-wire, bidirectional serial bus that provides a simple and efficient method for data exchange among devices. The phyFLEX provides two SPI interfaces on the phyFLEX-fix connector X1. The SPI interfaces provide three respectively two chip select signals. The Enhanced Configurable SPI (eCSPI) of the i.MX 6 has five separate modules (eCSPI1, eCSPI2, eCSPI3, eCSPI4 and eCSPI5) which support data rates of up to 20 Mbit/s. The interface signals of the third and fifth module (eCSPI3, eCSPI5) are made available on the phyFLEX-Connector. This module is master/slave configurable. The following table lists the SPI signals on the phyFLEX-Connector:

Pin #	Signal	ST	Voltage Domain	Description
X1A21	X_SPI0_MOSI	I/O	VDD_3V3_LOGIC	eCSPI3 master output/slave input
X1A23	X_SPI0_MISO	I/O	VDD_3V3_LOGIC	eCSPI3 master input/slave output
X1A24	X_SPI0_CSBOOT	O	VDD_3V3_LOGIC	eCSPI3 chip select 0 (BOOT) (SS0)
X1A25	X_SPI0_CS0	O	VDD_3V3_LOGIC	eCSPI3 chip select 1 (SS1)
X1A26	X_SPI0_CS1	O	VDD_3V3_LOGIC	eCSPI3 chip select 2 (SS2)
X1A27	reference-voltage	REF_O	VDD_3V3_LOGIC	SPI0 reference voltage
X1A29	X_SPI0_CLK	O	VDD_3V3_LOGIC	eCSPI3 clock signal
X1A30	X_SPI1_CS0[20]	O	VDD_3V3_LOGIC	eCSPI5 chip select 0 (SS0)
X1A31	X_SPI1_MOSI[20]	I/O	VDD_3V3_LOGIC	eCSPI5 master output/slave input
X1A32	X_SPI1_MISO[20]	I/O	VDD_3V3_LOGIC	eCSPI5 master input/slave output
X1A33	reference-voltage	REF_O	VDD_3V3_LOGIC	SPI1 reference voltage
X1A35	X_SPI1_CLK[20]	O	VDD_3V3_LOGIC	eCSPI5 clock signal
X1A36	X_SPI1_CS1[20]	O	VDD_3V3_LOGIC	eCSPI5 chip select 1 (SS1)

Table 21: SPI Interface Signal Location

Note:
If an SPI Flash is mounted at U25 it will be selected by X_SPI0_CSBOOT. In this case X_SPI0_CSBOOT can not be used on a custom carrier board.

[20]: SPI1 is not available for i.MX 6 Solo and i.MX 6 Dual Lite

8.7 I²S Audio Interface (SSI))

The Synchronous Serial Interface (SSI) of the phyFLEX-i.MX 6 is a full-duplex, serial interface that allows to communicate with a variety of serial devices, such as standard codecs, digital signal processors (DSPs), microprocessors, peripherals, and popular industry audio codecs that implement the inter-IC sound bus standard (I^2S) and Intel AC'97 standard. The i.MX 6 provides three instances of the SSI module. On the phyFLEX-i.MX 6 SSI is brought out to the phyFLEX-Connector through port 5 of the i.MX 6's Digital Audio Multiplexer (AUDMUX5).

With reference to the phyFLEX specification, the main purpose of this interface is to connect to an external codec, such as I^2S. Four signals extend from the i.MX 6 SSI module to the phyFLEX-Connector (I2S0_CLK, I2S0_FRM, I2S0_ADC, I2S0_DAC).

Pin #	Signal	ST	Voltage Domain	Description
X1A48	X_I2S0_CLK	I/O	VDD_3V3_LOGIC	I^2S AUD5 transmit clock
X1A49	X_I2S0_FRM	I/O	VDD_3V3_LOGIC	I^2S AUD5 frame
X1A50	X_I2S0_ADC	I	VDD_3V3_LOGIC	I^2S AUD5 receive data
X1A51	reference-voltage	REF_O	VDD_3V3_LOGIC	I^2S reference voltage
X1A53	X_I2S0_DAC	O	VDD_3V3_LOGIC	I^2S AUD5 transmit data

Table 22: I^2S Interface Signal Location

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8.8 CAN Interface

The CAN interface of the phyFLEX-i.MX 6 is connected to the first FlexCAN module (FlexCAN1) of the i.MX 6 which is a full implementation of the CAN protocol specification Version 2.0B. It supports standard and extended message frames and programmable bit rates of up to 1 Mb/s.

The signals of the CAN interface are brought out on the phyFLEX-optional connector X2. The following table shows the position of the signals.

Pin #	Signal	ST	Voltage Domain	Description
X2A4	X_CAN0_TXD	O	VDD_3V3_LOGIC	FlexCAN1 transmit
X2A5	X_CAN0_RXD	I	VDD_3V3_LOGIC	FlexCAN1 receive
X2A7	reference-voltage	REF	VDD_3V3_LOGIC	CAN0 reference voltage

Table 23: CAN Interface Signal Location

8.9 PCI Express Interface

The 1-lane PCI Express interface of the phyFLEX-i.MX 6 provides PCIe Gen. 2.0 functionality which supports 5 Gbit/s operation. Furthermore the interface is fully backwards compatible to the 2.5 Gbit/s Gen. 1.1 specification. The control signals (reset, present and wake) are realized by GPIOs.

Table 24 shows the position of the PCIe signals on the phyFLEX-fix connector X1.

Pin #	Signal	ST	Voltage Domain	Description
X1B46	X_nPCIe0_PERST	I/O	VDD_3V3_LOGIC	PCIe0 reset signal (active low) (GPIO4_17 of i.MX 6)
X1B65	X_PCIe0_nPRSNT	I/O	VDD_3V3_LOGIC	PCIe0 present signal (active low) (GPIO1_21 of i.MX 6)
X1B66	reference-voltage	REF_0	VDD_3V3_LOGIC	PCIe0 reference voltage
X1B68	X_PCIe0_TX+	PCIe_0	i.MX 6 internal	PCIe0 transmit lane+
X1B69	X_PCIe0_TX-	PCIe_0	i.MX 6 internal	PCIe0 transmit lane-
X1B70	X_PCIe0_nWAKE	I/O	VDD_3V3_LOGIC	PCIe0 wake signal (low active) (GPIO1_7 of i.MX 6)
X1B71	X_PCIe0_RX+	PCIe_I	i.MX 6 internal	PCIe0 receive lane+
X1B72	X_PCIe0_RX-	PCIe_I	i.MX 6 internal	PCIe0 receive lane-
X1B74	X_PCIe0_CLK+	PCIe_0	i.MX 6 internal	PCIe0 clock lane+ (XTALOSC_CLK1)
X1B75	X_PCIe0_CLK-	PCIe_0	i.MX 6 internal	PCIe0 clock lane- (XTALOSC_CLK1)

Table 24: PCIe Interface Signal Location

8.10 SATA Interface

The SATA II interface of the phyFLEX-i.MX 6 is a high-speed serialized ATA data link interface compliant with SATA Revision 3.0 (physical layer complies with SATA Revision 2.5) which supports data rates of up to 3.0 Gbit/s. The interface includes an internal DMA engine, command layer, transport layer, link layer and the physical layer. The interface itself supports only one SATA device.

The phyFLEX-i.MX 6 provides an SATA II Interface at the phyFLEX-optional connector X2 at the following locations:

Pin #	Signal	ST	Voltage Domain	Description
X2A10	X_SATA0_TX+	LVDS_O	i.MX 6 internal	SATA PHY transmit lane+
X2A11	X_SATA0_TX-	LVDS_O	i.MX 6 internal	SATA PHY transmit lane-
X2A13	X_SATA0_RX+	LVDS_I	i.MX 6 internal	SATA PHY receive lane+
X2A14	X_SATA0_RX-	LVDS_I	i.MX 6 internal	SATA PHY receive lane-

Table 25: SATA Interface Signal Location

As the signals extend directly from the i.MX 6's SATA PHY a standard SATA connector is all that is needed to interface the phyFLEX-i.MX 6's SATA functionality.

8.11 Media Local Bus

The Media Local Bus (MLB) interface provides a link to a MOST® data network, using the standardized Media Local Bus protocol (up to 150 Mbit/s) for inter-chip communication. The Media Local Bus interface is implemented as MediaLB 6-pin interface (differential) which supports the MediaLB protocol for high-speed differential 6-pin mode, with a maximum data rate of 6144xFs (294.912 MHz at Fs=48 kHz). The module is backward compatible to MLB-50. The MLB interface is only available on the not standardized phyFLEX-flex connector X3. The following table shows the position of the signals on the connector.

Pin #	Signal	ST	Voltage Domain	Description
X3B16	X_MLB_DP	MLB_I/O	i.MX 6 internal	Media local bus data line+
X3B17	X_MLB_DN	MLB_I/O	i.MX 6 internal	Media local bus data line-
X3B19	X_MLB_SP	MLB_I/O	i.MX 6 internal	Media local bus signal line+
X3B20	X_MLB_SN	MLB_I/O	i.MX 6 internal	Media local bus signal line-
X3B22	X_MLB_CP	MLB_O	i.MX 6 internal	Media local bus clock+
X3B23	X_MLB_CN	MLB_O	i.MX 6 internal	Media local bus clock-

Table 26: Media Local Bus Interface Signal Location

9 General Purpose I/Os

The phyFLEX bus provides 11 GPIO signals. *Table 27* shows the location of the GPIO pins on the phyFLEX-Connector, as well as the corresponding ports of the i.MX 6.

Pin #	Signal	ST	Voltage Domain	Description
X1A54	X_GPIO0	I/O	VDD_3V3_LOGIC	General purpose input/output 0 (GPIO5_8 of i.MX 6)
X1A55	X_GPIO1	I/O	VDD_3V3_LOGIC	General purpose input/output 1 (GPIO5_7 of i.MX 6)
X1A56	X_GPIO2	I/O	VDD_3V3_LOGIC	General purpose input/output 2 (GPIO4_18 of i.MX 6)
X1A57	reference-voltage	REF_O	VDD_3V3_LOGIC	GPIO reference voltage
X1A59	X_GPIO3	I/O	VDD_3V3_LOGIC	General purpose input/output 3 (GPIO4_19 of i.MX 6)
X1A60	X_GPIO4	I/O	VDD_3V3_LOGIC	General purpose input/output 4 (GPIO1_6 of i.MX 6)
X1A61	X_GPIO5	I/O	VDD_3V3_LOGIC	General purpose input/output 5 (GPIO1_9 of i.MX 6)
X1A62	X_GPIO6	I/O	VDD_3V3_LOGIC	General purpose input/output 6 (GPIO7_12 of i.MX 6)
X1A63	X_GPIO7	I/O	VDD_3V3_LOGIC	General purpose input/output 7 (GPIO7_13 of i.MX 6)
X1A65	X_GPIO8	I/O	VDD_3V3_LOGIC	General purpose input/output 8 (GPIO4_5 of i.MX 6)
X1A66	X_GPIO9	I/O	VDD_3V3_LOGIC	General purpose input/output 9 (GPIO2_23 of i.MX 6)
X1A67	X_GPIO10	I/O	VDD_3V3_LOGIC	General purpose input/output 10 (GPIO2_24 of i.MX 6)
X3B37	X_GPIO_16	I/O	VDD_3V3_LOGIC	General purpose input/output 16 (GPIO7_11 of i.MX 6)[21]

Table 27: Location of GPIO Pins

Beside these 11 dedicated GPIOs, most of the i.MX 6 signals which are connected directly to the module connector can be configured to act as GPIOs, due to the multiplexing functionality of most controller pins.

[21]: **Note:** GPIO16 is located on the phyFLEX-flex connector which is module specific. Hence, this GPIO might not be available on other phyFLEX modules.

10 User LEDs

The phyFLEX-i.MX 6 provides two user LEDs on board, a red (D2) and a green (D1). D2 can be controlled by setting GPIO2_31 (pad EIM_EB3) and D1 can by controlled by setting GPIO1_30 (pad ENET_TXD0) to the desired output level. A high-level turns the LED on, a low-level turns it off.

11 Debug Interface (X1, X4)

The phyFLEX-i.MX 6 is equipped with a JTAG interface for downloading program code into the external flash, internal controller RAM or for debugging programs currently executing. The JTAG interface extends to the phyFLEX-fix connector X1 and also to a 2.0 mm pitch pin header at X4 on the edge of the module PCB.

Table 28 shows the location of the JTAG pins on the phyFLEX-fix connector X1.

Pin #	Signal	ST	Voltage Domain	Description
X1A5	X_JTAG_TRSTB	I	VDD_3V3_LOGIC	JTAG reset input (low active)
X1A6	X_JTAG_TDI	I	VDD_3V3_LOGIC	JTAG TDI
X1A7	X_JTAG_TMS	I	VDD_3V3_LOGIC	JTAG TMS
X1A8	X_JTAG_TDO	O	VDD_3V3_LOGIC	JTAG TDO
X1A9	X_JTAG_TCK	I	VDD_3V3_LOGIC	JTAG clock input
X1A10	GND	-	-	Ground 0 V
X1B5	reference-voltage	REF_O	VDD_3V3_LOGIC	JTAG reference voltage

Table 28: Debug Interface Signal Location at phyFLEX-Connector X1

Figure 9 and *Figure 10* show the position of the phyFLEX-i.MX 6 module's debug interface at JTAG connector X4 and at the JTAG pins of phyFLEX-fix connector X1.

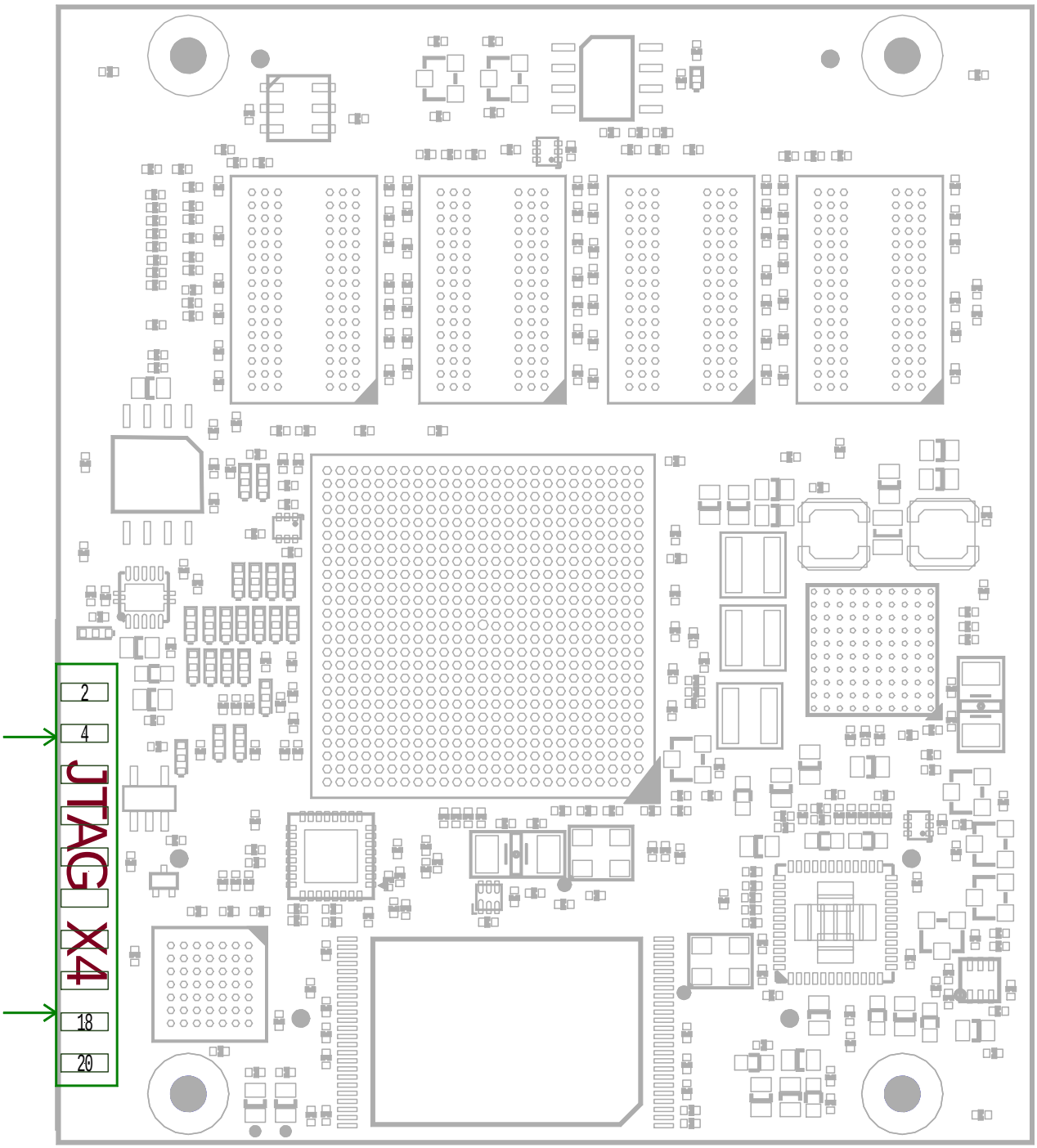


Figure 9: JTAG Interface at X4 (top view)

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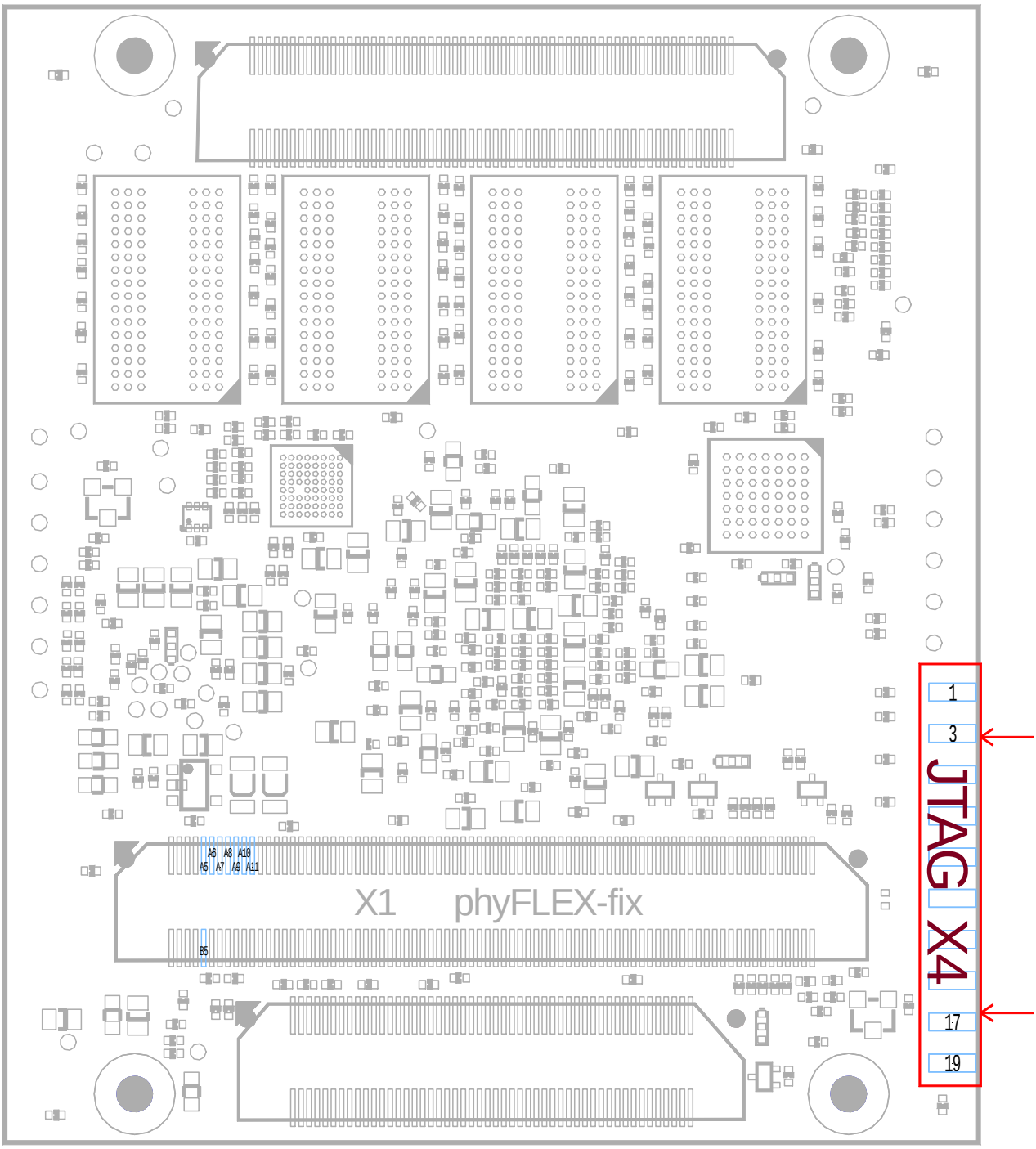


Figure 10: JTAG Interface at X4 (bottom view)

Pin 1 of the JTAG connector X4 is on the connector side of the module. Pin 2 of the JTAG connector is on the controller side of the module.

Table 29 shows details on the JTAG signal pin assignment.

Note:
The JTAG connector X4 only populates phyFLEX-i.MX 6 modules with a specific order option. We recommend integration of a standard (2 mm pitch) pin header connector in the user target circuitry to allow easy program updates via the JTAG interface.

Signal	Pin Row*		Signal
	A	B	
VSUPPLY (VDD_3V3_LOGIC)	2	1	TREF (VDD_3V3_LOGIC via 0 Ohms)
GND	4	3	X_JTAG_TRSTB (low active)
GND	6	5	X_JTAG_TDI
GND	8	7	X_JTAG_TMS
GND	10	9	X_JTAG_TCK
GND	12	11	X_JTAG_RTCK (connected via 0 Ohms to X_JTAG_TCK)
GND	14	13	X_JTAG_TDO
GND	16	15	X_PM_nRESET_IN
GND	18	17	not connected
GND	20	19	not connected

Table 29: JTAG Connector X4 Signal Assignment

***Note:** Row A is on the controller side of the module and row B is on the connector side of the module

Phytec offers a JTAG-Emulator adapter (order code JA-002) for connecting the phyFLEX-i.MX 6 to a standard emulator. The JTAG-Emulator adapter extends the signals of the module's JTAG connector to a standard ARM connector with 2 mm pin pitch. The JA-002 therefore functions as an adapter for connecting the module's non-ARM-compatible JTAG connector X4 to standard Emulator connectors.

12 LVDS Display Interface

The LVDS-Signals from both channels of the on-chip LVDS Display Bridge (LDB) on the i.MX 6 are brought out at the phyFLEX-Connector.
The signals from the first display interface (LVDS0) are brought out at the phyFLEX-fix connector X1, while the signals from the second display interface (LVDS1) are available at the non standardized phyFLEX-flex connector X3. Thus an LVDS-Display can connect directly to the phyFLEX-i.MX 6. The location of the applicable interface signals can be found in the table below.

Pin #	Signal	ST	Voltage Domain	Description
X1B50	X_LVDS0_L0+	LVDS_O	i.MX 6 internal	LVDS0 data0+
X1B51	X_LVDS0_L0-	LVDS_O	i.MX 6 internal	LVDS0 data0-
X1B53	X_LVDS0_L1+	LVDS_O	i.MX 6 internal	LVDS0 data1+
X1B54	X_LVDS0_L1-	LVDS_O	i.MX 6 internal	LVDS0 data1-
X1B56	X_LVDS0_L2+	LVDS_O	i.MX 6 internal	LVDS0 data2+
X1B57	X_LVDS0_L2-	LVDS_O	i.MX 6 internal	LVDS0 data2-
X1B59	X_LVDS0_L3+	LVDS_O	i.MX 6 internal	LVDS0 data3+
X1B60	X_LVDS0_L3-	LVDS_O	i.MX 6 internal	LVDS0 data3-
X1B62	X_LVDS0_CLK+	LVDS_O	i.MX 6 internal	LVDS0 clock+
X1B63	X_LVDS0_CLK-	LVDS_O	i.MX 6 internal	LVDS0 clock-
X1B64	reference-voltage	REF_O	VDD_3V3_LOGIC	LVDS0 reference voltage
X3B1	X_LVDS1_TX0_P	LVDS_O	i.MX 6 internal	LVDS1 data0+
X3B2	X_LVDS1_TX0_N	LVDS_O	i.MX 6 internal	LVDS1 data0-
X3B4	X_LVDS1_TX1_P	LVDS_O	i.MX 6 internal	LVDS1 data1+
X3B5	X_LVDS1_TX1_N	LVDS_O	i.MX 6 internal	LVDS1 data1-
X3B7	X_LVDS1_TX2_P	LVDS_O	i.MX 6 internal	LVDS1 data2+
X3B8	X_LVDS1_TX2_N	LVDS_O	i.MX 6 internal	LVDS1 data2-
X3B10	X_LVDS1_TX3_P	LVDS_O	i.MX 6 internal	LVDS1 data3+
X3B11	X_LVDS1_TX3_N	LVDS_O	i.MX 6 internal	LVDS1 data3-
X3B13	X_LVDS1_CLK_P	LVDS_O	i.MX 6 internal	LVDS1 clock+
X3B14	X_LVDS1_CLK_N	LVDS_O	i.MX 6 internal	LVDS1 clock-

Table 30: Display Interface Signal Location

12.1 Supplementary Signals

Two control signals display enable and backlight PWM (X_LVDS0_nDISP_EN and X_LVDS0_DISP_BL_PWM) are provided to support the display connectivity of the phyFLEX-i.MX 6.

Pin #	Signal	ST	Voltage Domain	Description
X1B52	X_LVDS0_nDISP_EN	O	VDD_3V3_LOGIC	LVDS0 display enable (low active) (GPIO1_8 of i.MX 6)
X1B58	X_LVDS0_DISP_BL_PWM	O	VDD_3V3_LOGIC	LVDS0 backlight PWM output (PWM1_OUT of i.MX 6)

Table 31: Supplementary Signals to support the Display Connectivity

12.2 LVDS Display Interface pixel mapping

The phyFLEX specification defines the pixel mapping of the LVDS display interface. The pixel mapping equates to the OpenLDI respectively Intel 24.0 or JEIDA standard. Thus you can connect 18-bit as well as 24-bit LVDS displays to the phyFLEX. *Table 32* and *Table 33* show the recommended pixel mapping of the LVDS display.
However since the i.MX 6 LDB Module supports also the SPWG pixel mapping, this one can be used as well by setting the appropriated configuration bit.

Note:
To be fully compatible to the phyFLEX specification, make sure that the LVDS display you want to use provides the same pin mapping as the phyFLEX (JEIDA respectively OpenLDI). Normally this is only important for 24-bit LVDS displays because due to the organization of the LVDS pixel mapping all common 18-bit LVDS displays should work.

18-bit LVDS Display

	1	2	3	4	5	6	7
CLK	1	1	0	0	0	1	1
A0	G0	R5	R4	R3	R2	R1	R0
A1	B1	B0	G5	G4	G3	G2	G1
A2	DE	VSYNC	HSYNC	B5	B4	B3	B2
A3	0	0	0	0	0	0	0

Table 32: Pixel Mapping of 18-bit LVDS Display Interface

24-bit LVDS Display

	1	2	3	4	5	6	7
CLK	1	1	0	0	0	1	1
A0	G2	R7	R6	R5	R4	R3	R2
A1	B3	B2	G7	G6	G5	G4	G3
A2	DE	VSYNC	HSYNC	B7	B6	B5	B4
A3	0	B1	B0	G1	G0	R1	R0

Table 33: Pixel Mapping of 24-bit LVDS Display Interface

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13 High-Definition Multimedia Interface (HDMI)

The High-Definition Multimedia Interface (HDMI) of the phyFLEX-i.MX 6 is compliant to HDMI 1.4 and DVI 1.0. It supports a maximum pixel clock of up to 340 MHz for up to 720p at 100 Hz and 720i at 200 Hz, or 1080p at 60 Hz and 1080i/720i at 120 Hz HDTV display resolutions, and a graphic display resolution of up to 2048x1536 (QXGA). Please refer to the *i.MX 6 Reference Manual* for more information.

The following table shows the location of the HDMI signals on the phyFLEX-optional connector X2.

Pin #	Signal	ST	Voltage Domain	Description
X2A8	X_HDMI0_SDA	I/O	VDD_3V3_LOGIC	HDMI I2C data
X2A9	X_HDMI0_SCL	I/O	VDD_3V3_LOGIC	HDMI I2C clock
X2B1	X_HDMI0_TMDS_DATA2+	TMDS_0	i.MX 6 internal	HDMI data2+
X2B2	X_HDMI0_TMDS_DATA2-	TMDS_0	i.MX 6 internal	HDMI data2-
X2B4	X_HDMI0_TMDS_DATA1+	TMDS_0	i.MX 6 internal	HDMI data1+
X2B5	X_HDMI0_TMDS_DATA1-	TMDS_0	i.MX 6 internal	HDMI data1-
X2B6	reference-voltage	REF_0	VDD_3V3_LOGIC	HDMI0 reference voltage
X2B7	X_HDMI0_TMDS_DATA0+	TMDS_0	i.MX 6 internal	HDMI data0+
X2B8	X_HDMI0_TMDS_DATA0-	TMDS_0	i.MX 6 internal	HDMI data0-
X2B10	X_HDMI0_TMDS_CLOCK+	TMDS_0	i.MX 6 internal	HDMI clock+
X2B11	X_HDMI0_TMDS_CLOCK-	TMDS_0	i.MX 6 internal	HDMI clock-
X2B12	X_HDMI0_CEC	I/O	VDD_3V3_LOGIC	HDMI CEC
X2B13	X_HDMI0_nHPD	I	VDD_3V3_LOGIC	HDMI hot plug detect

Table 34: HDMI Interface Signal Location at X2

14 Camera Interfaces

The phyFLEX-i.MX 6 SOM offers various interfaces to connect digital cameras. Up to two parallel camera interfaces (IPU1_CSI0 and IPU2_CSI1[22]) as well as the interface to the MIPI/CSI-2 Host Controller are supported and brought out in different ways. All signals (including control signals and an I^2C interface) to use the camera interfaces according to Phytec's phyCAM-S+, or phyCAM-P standard are available at the phyFLEX-Connector.

The i.MX 6 (Solo), and i.MX 6 (DualLite) microcontrollers are equipped with one parallel camera port (IPU1_CSI0) and one image processing units (version 3H) (IPU#1) to process the signals from the parallel, or the MIPI camera interface (*Figure 11)*. The i.MX 6D (dual core), and i.MX 6Q (quad core) provide an additional parallel camera port (IPU2_CSI1) and a second image processing unit (IPU#2[22]) (*Figure 12*). The second, independent image processing unit of the i.MX 6D (dual core), and the i.MX 6Q (quad core) allows to operate two cameras at the same time.

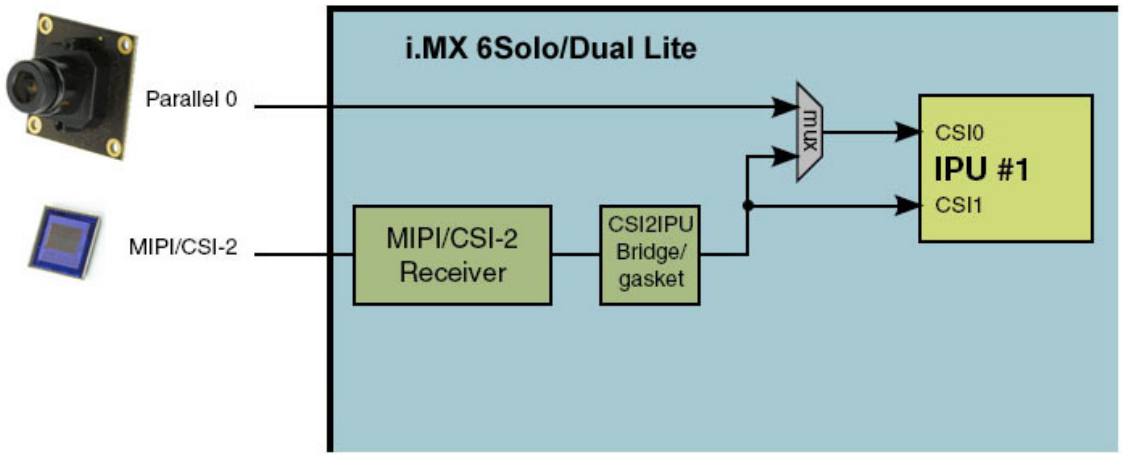


Figure 11: Camera Connectivity of the i.MX 6 (Solo/DualLite)

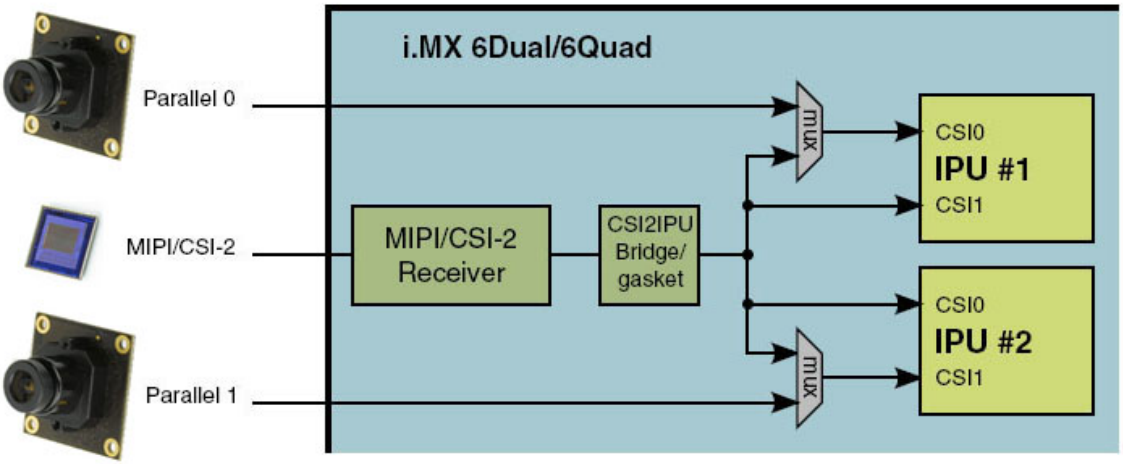


Figure 12: Camera Connectivity of the i.MX 6 (Dual Core/Quad Core)

[22]: Only i.MX 6 with Dual-. or Quad core. i.MX 6 with Solo-, or DualLite core provide only one parallel camera interface and one IPU.

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On the phyFLEX-i.MX 6 SOM camera ports IPU1_CSI0 and IPU2_CSI1 are brought out as parallel interfaces, and, through the use of deserializers, also as LVDS interfaces. Connectivity to the MIPI/CSI-2 interface is possible on the phyFLEX-i.MX 6, too. Hence, the i.MX 6's camera interfaces are supported as follows:

IPU1_CS0 (denoted as Camera_0):

- as parallel interface (Parallel 0) with 16 data bits, HSYNC, VSYNC and PIXCLK at phyFLEX-flex connector X3
- as LVDS interface allowing to connect serial camera modules to the phyFLEX-optional connector X2 (via deserializer at U27)

IPU2_CS1 (denoted as Camera_1):

- as parallel interface (Parallel 1) with 20 data bits, HSYNC, VSYNC and PIXCLK at phyFLEX-flex connector X3
- as LVDS interface allowing to connect serial camera modules to the phyFLEX-optional connector X2 (via deserializer at U12)

MIPI/CSI-2 (denoted as Camera_2):

- as MIPI/CSI-2 interface with 5-lanes at phyFLEX-flex connector X3

Figure 13 depicts the different options to connect a camera modul to the phyFLEX-i.MX 6.

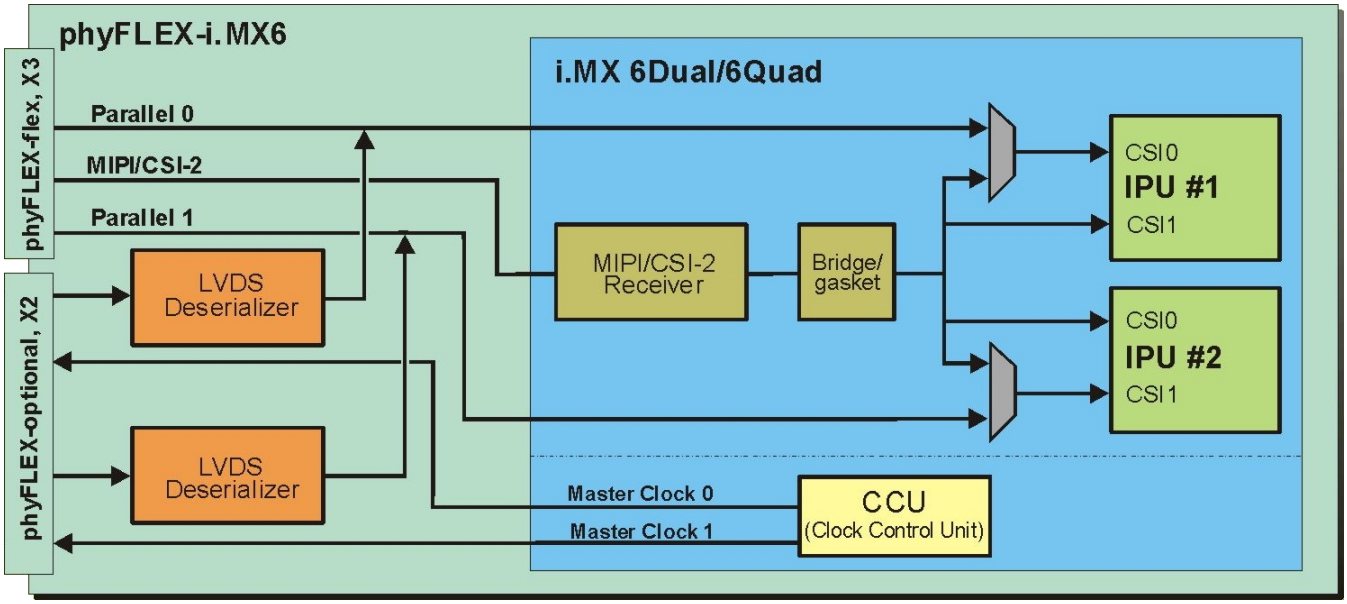


Figure 13: Camera Connectivity of the phyFLEX-i.MX 6 with Dual Core/Quad Core

The camera interfaces of the phyFLEX-i.MX 6 include all signals and are prepared to be used as phyCAM-S(+), phyCAM-P, or MIPI/CSI-2 interface on an appropriate carrier board.

Please refer to section *19.3.10* for more information on how to connect a camera to the Phytec carrier board (PBA-B-01), the Phytec Mapper Board[23] (FLM-A-XL1), or a custom application using the different interface options.

[23]: The Phytec Mapper Board (FLM-A-XL1) is not included in all kits. Pleas contact our sales team for more information.

14.1 Camera_0 Interface (CSI0 of IPU#1)

14.1.1 Camera_0 as LVDS Interface

The phyFLEX-i.MX 6 uses a 1-channel 10-Bit LVDS random lock deserializer (U27), to receive LVDS-signals from an LVDS camera interface. The LVDS deserializer converts the LVDS Signals to a 10-bit wide parallel data bus and separate clock which can be used as inputs for the i.MX 6 camera sensor interfaces connected to CSI0 of IPU#1. The 10-bit wide data bus consists of 8 data bits and 2 sync bits (HSYNC/VSYNC).

Caution! The deserializer needs the same clock frequency, as the source serializer on the camera board. This can be achieved, by either adjusting the clock sources for deserializer and serializer to the same frequency, or by using the clock of the deserializer for the serializer as well. Therefor the clock of the deserializer is available at connector X2.

The following table shows the location of the signals:

Pin #	Signal	ST	Voltage Domain	Description
X2A40	X_CAMERA0_L0+	LVDS_I	VDD_3V3_LOGIC	Camera_0 data+
X2A41	X_CAMERA0_L0-	LVDS_I	VDD_3V3_LOGIC	Camera_0 data-
X2A43	X_CAMERA0_CLK	O	VDD_3V3_LOGIC	Camera_0 master clock
X2A44	reference-voltage	REF_O	VDD_3V3_LOGIC	Camera_0 reference voltage

Table 35: Camera_0 LVDS Interface Signal Location at phyFLEX Connector X2

In combination with an I²C bus and the master-clock-serializer on the main board, the interface can be used according to the Phytec phyCAM-S+ interface (*section 19.3.10*).

To assists the implementation of a power management the deserializer's REN input connects to the X_CSI0_DATA_EN signal (GPIO5_20 of the i.MX 6). Furthermore the power down feature of the deserializer can be used by toggling signal CAM_LVDS_PRWDN/GPIO1_24 (GPIO1_24 of the i.MX 6) connected to the nPWRDN input. Thereby the LVDS deserializer can be switched into power down state, or turned off by software.

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14.1.1.1 Signal Configuration (J31)

J31 selects rising, or falling edge strobe for the LVDS deserializer at U27 used for the camera connectivity of the phyFLEX-i.MX 6Camera_0 interface.

Position	Description	Type
2+3	**rising edge strobe used for the LVDS camera signals**	0R (0402)
1+2	falling edge strobe used for the LVDS camera signals	

Table 36: LVDS Signal Configuration for Camera_0 Interface (J31)

14.1.2 Camera_0 as Parallel Interface (Parallel 0)

The Camera_0 interface (CSI0 of IPU#1) is also brought out as parallel interfaces (Parallel 0) with 18 data bits, HSYNC, VSYNC and PIXCLK. Most of the data signals extend to the phyFLEX-flex connector X3[24], whereas the clock signal is available at connector X2 (*Table 37*).

Note:
Use of Camera_0 as parallel interface requires the LVDS deserializer at U27 to be disabled. This is done by setting signal X_CSI0_DATA_EN (GPIO5_20 of the i.MX 6) to low either by software, or using a pull-down resistor at X3A28.

[24]: The phyFLEX-flex connector X3 is not available with all assembly configurations of the phyFLEX-i.MX 6 SOM.

The following table shows the location of the Parallel 0 (CSI0 of IPU#1) camera signals at the phyFLEX-Connector:

Pin #	Signal	ST	Voltage Domain	Description
X3A23	X_CSI0_DAT19	I	VDD_3V3_LOGIC	Camera_0 data19 (IPU1_CS0 D19)
X3A22	X_CSI0_DAT18	I	VDD_3V3_LOGIC	Camera_0 data18 (IPU1_CS0 D18)
X3A21	X_CSI0_DAT17	I	VDD_3V3_LOGIC	Camera_0 data17 (IPU1_CS0 D17
X3A20	X_CSI0_DAT16	I	VDD_3V3_LOGIC	Camera_0 data16 (IPU1_CS0 D16)
X3A19	X_CSI0_DAT15	I	VDD_3V3_LOGIC	Camera_0 data15 (IPU1_CS0 D15)
X3A17	X_CSI0_DAT14	I	VDD_3V3_LOGIC	Camera_0 data14 (IPU1_CS0 D14)
X3A16	X_CSI0_DAT13	I	VDD_3V3_LOGIC	Camera_0 data13 (IPU1_CS0 D13)
X3A15	X_CSI0_DAT12	I	VDD_3V3_LOGIC	Camera_0 data12 (IPU1_CS0 D12)
X3A9	X_CSI0_DAT11	I	VDD_3V3_LOGIC	Camera_0 data11 (IPU1_CS0 D11)
X3A3	X_CSI0_DAT10	I	VDD_3V3_LOGIC	Camera_0 data10 (IPU1_CS0 D10)
X3B24	X_CSI0_DAT9	I	VDD_3V3_LOGIC	Camera_0 data9 (IPU1_CS0 D9)
X3B28	X_CSI0_DAT8	I	VDD_3V3_LOGIC	Camera_0 data8 (IPU1_CS0 D8)
X3B40	X_CSI0_DAT7	I	VDD_3V3_LOGIC	Camera_0 data7 (IPU1_CS0 D7)
X3B41	X_CSI0_DAT6	I	VDD_3V3_LOGIC	Camera_0 data6 (IPU1_CS0 D6)
X3B18	X_CSI0_DAT5	I	VDD_3V3_LOGIC	Camera_0 data5 (IPU1_CS0 D5)
X3B12	X_CSI0_DAT4	I	VDD_3V3_LOGIC	Camera_0 data4 (IPU1_CS0 D4)
X1A14	X_UART1_RTS[25]	I	VDD_3V3_LOGIC	Camera_0 data3 (IPU1_CS0 D3)
X1A15	X_UART1_CTS[25]	I	VDD_3V3_LOGIC	Camera_0 data2 (IPU1_CS0 D2)
X3A25	X_CSI0_MCLK	I	VDD_3V3_LOGIC	Camera_0 HSYNC (IPU1_CS0 HSYNC)
X3A27	X_CSI0_VSYNC	I	VDD_3V3_LOGIC	Camera_0 VSYNC (IPU1_CS0 VSYNC)
X3A26	X_CSI0_PIXCLK	I	VDD_3V3_LOGIC	Camera_0 PCLK (IPU1_CS0 PCLK)
X2A43	X_CAMERA0_CLK	O	VDD_3V3_LOGIC	Camera_0 MCLK

Table 37: Parallel 0 Camera Interface Signal Location at the phyFLEX-Connector

Using the phyFLEX's camera interface Parallel 0, together with an I²C bus facilitates easy implementation of a CMOS camera interface, e.g. a phyCAM-P interface, on a carrier board More information on how to connect to the parallel camera interface with 18 data bits, or in accordance with the Phytec phyCAM-P standard (with up to 12 data bits) can be found in *section 19.3.10*.

[25]: According to the specification of the phyFLEX-i.MX 6 this pin is used for the hardware flow control of the serial interface. Use of this pin as data signal for the Camera_0 interface requires to change the i.MX 6's pin muxing.

14.2 Camera_1 Interface (CSI1 of IPU#2)

14.2.1 Camera_1 as LVDS Interface

The phyFLEX-i.MX 6 uses a 1-channel 10-Bit LVDS random lock deserializer (U12), to receive LVDS-signals from a LVDS camera interface. The LVDS deserializer converts the LVDS Signals to a 10-bit wide parallel data bus and separate clock which can be used as inputs for the i.MX 6 camera sensor interfaces connected to CSI1 of IPU#2. The 10-bit wide data bus consists of 8 data bits and 2 sync bits (HSYNC/VSYNC).

Caution! The deserializer needs the same clock frequency, as the source serializer on the camera board. This can be achieved, by either adjusting the clock sources for deserializer and serializer to the same frequency, or by using the clock of the deserializer for the serializer as well. Therefor the clock of the deserializer is available at connector X2.

The following table shows the location of the signals:

Pin #	Signal	ST	Voltage Domain	Description
X2A46	X_CAMERA1_L0+	LVDS_I	VDD_3V3_LOGIC	Camera_1 data+
X2A47	X_CAMERA1_L0-	LVDS_I	VDD_3V3_LOGIC	Camera_1 data-
X2A49	X_CAMERA1_CLK	O	VDD_3V3_LOGIC	Camera_1 master clock
X2A50	reference-voltage	REF_O	VDD_3V3_LOGIC	Camera_1 reference voltage

Table 38: Camera_1 LVDS Interface Signal Location at phyFLEX Connector X2

In combination with an I²C bus and the master-clock-seralizer on the main board, the interface can be used according to the Phytec phyCAM-S+ interface (*section 19.3.10*).

To assists the implementation of a power management the deserializer's REN input connects to the X_EIM_DA10[26] signal (GPIO3_10 of the i.MX 6). Furthermore the power down feature of the deserializer can be used by toggling signal X_EIM_EB0[26] (GPIO2_28 of the i.MX 6) connected to the nPWRDN input. Thereby the LVDS deserializer can be switched into power down state, or turned off by software.

[26]: **Caution!** This pin is also used as boot mode pin by the i.MX 6. Special care must be taken not to override the device configuration when using this pin as input (*section 5*).

14.2.1.1 Signal Configuration (J9), (J26)

J9 selects rising, or falling edge strobe for the LVDS deserializer at U12 used for the camera connectivity of the phyFLEX-i.MX 6Camera_1 interface.

Position	Description	Type
1+2	falling edge strobe used for the LVDS camera signals	0R (0402)
2+3	**rising edge strobe used for the LVDS camera signals**	

Table 39: LVDS Signal Configuration for Camera_1 Interface (J9)

Jumper J26 selects the clock signal used for camera interface Camera_1. Either a separate clock signal, or the clock signal of Camera_0 can be used. The later configuration is useful to have both camera interfaces synchronized.

Position	Description	Type
1+2	**Interface Camera_1 operates with dedicated clock signal X_CAMERA1_CLK**	0R (0402)
2+3	Interface Camera_1 operates with the same clock signal as interface Camera_0	

Table 40: Clock Configuration for Camera_1 Interface (J26)

14.2.2 Camera_1 as Parallel Interface (Parallel 1)

The Camera_1 interface (CSI1 of IPU#2) is also brought out as parallel interfaces (Parallel 1) with 20 data bits, HSYNC, VSYNC and PIXCLK. All of the data signals extend to the phyFLEX-flex connector X3[27], whereas the clock signal is available at connector X2 (*Table 41*).

Note:
Use of Camera_1 as parallel interface requires the LVDS deserializer at U12 to be disabled. This is done by setting signal X_EIM_DA10 (GPIO3_10 of the i.MX 6) to low.

The following table shows the location of the Parallel 1 (CSI1 of IPU#2) camera signals at the phyFLEX-Connector:

[27]: The phyFLEX-flex connector X3 is not available with all assembly configurations of the phyFLEX-i.MX 6 SOM.

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The following table shows the location of IPU2_CSI1 camera signals at phyFLEX-connector:

Pin #	Signal	ST	Voltage Domain	Description
X3A32	X_EIM_A24	I	VDD_3V3_LOGIC	Camera_1 data19 (IPU2_CS1 D19)
X3A33	X_EIM_A23	I	VDD_3V3_LOGIC	Camera_1 data18 (IPU2_CS1 D18)
X3A34	X_EIM_A22	I	VDD_3V3_LOGIC	Camera_1 data17 (IPU2_CS1 D17)
X3A35	X_EIM_A21	I	VDD_3V3_LOGIC	Camera_1 data16 (IPU2_CS1 D16)
X3A37	X_EIM_A20	I	VDD_3V3_LOGIC	Camera_1 data15 (IPU2_CS1 D15)
X3A38	X_EIM_A19	I	VDD_3V3_LOGIC	Camera_1 data14 (IPU2_CS1 D14)
X3A39	X_EIM_A18	I	VDD_3V3_LOGIC	Camera_1 data13 (IPU2_CS1 D13)
X3A40	X_EIM_A17	I	VDD_3V3_LOGIC	Camera_1 data12 (IPU2_CS1 D12)
X3A41	X_EIM_EB0	I	VDD_3V3_LOGIC	Camera_1 data11 (IPU2_CS1 D11)
X3A43	X_EIM_EB1	I	VDD_3V3_LOGIC	Camera_1 data10 (IPU2_CS1 D10)
X3A44	X_EIM_DA0	I	VDD_3V3_LOGIC	Camera_1 data9 (IPU2_CS1 D9)
X3A45	X_EIM_DA1	I	VDD_3V3_LOGIC	Camera_1 data8 (IPU2_CS1 D8)
X3A46	X_EIM_DA2	I	VDD_3V3_LOGIC	Camera_1 data7 (IPU2_CS1 D7)
X3A47	X_EIM_DA3	I	VDD_3V3_LOGIC	Camera_1 data6 (IPU2_CS1 D6)
X3A49	X_EIM_DA4	I	VDD_3V3_LOGIC	Camera_1 data5 (IPU2_CS1 D5)
X3A50	X_EIM_DA5	I	VDD_3V3_LOGIC	Camera_1 data4 (IPU2_CS1 D4)
X3A51	X_EIM_DA6	I	VDD_3V3_LOGIC	Camera_1 data3 (IPU2_CS1 D3)
X3A52	X_EIM_DA7	I	VDD_3V3_LOGIC	Camera_1 data2 (IPU2_CS1 D2)
X3A53	X_EIM_DA8	I	VDD_3V3_LOGIC	Camera_1 data1 (IPU2_CS1 D1)
X3A55	X_EIM_DA9	I	VDD_3V3_LOGIC	Camera_1 data0 (IPU2_CS1 D0)
X3A57	X_EIM_DA11	I	VDD_3V3_LOGIC	Camera_1 HSYNC (IPU2_CS1 HSYNC)
X3A58	X_EIM_DA12	I	VDD_3V3_LOGIC	Camera_1 VSYNC (IPU2_CS1 VSYNC)
X3A59	X_EIM_A16	I	VDD_3V3_LOGIC	Camera_1 PCLK (IPU2_CS1 PCLK)
X2A49	X_CAMERA1_CLK	O	VDD_3V3_LOGIC	Camera_1 MCLK

Table 41: Parallel 1 Camera Interface Signal Location at the phyFLEX-Connector[28]

Using the phyFLEX's camera interface Parallel 1, together with an I²C bus facilitates easy implementation of a CMOS camera interface, e.g. a phyCAM-P interface, on a carrier board More information on how to connect to the parallel camera interface with 18 data bits, or in accordance with the Phytec phyCAM-P standard (with up to 12 data bits) can be found in *section 19.3.10*.

[28]: **Caution!** These pins are also used as boot mode pins by the i.MX 6. Special care must be taken not to override the device configuration when using this pin as camera interface (*section 5*).

14.3 Camera_2 Camera Interface (MIPI/CSI-2)

The MIPI/CSI-2 of the i.MX 6, denoted as Camera_2, is available with up to 4 data lanes and one clock at the phyFLEX-flex connector X3[29] (*Table 42*).

Note:
It is not possible to use the MIPI/CSI-2 interface and the IPU1_CSI0 or IPU2_CSI1 interface at the same time.

The following table shows the location of the Camera_2 (MIPI/CSI-2) signals at the phyFLEX-Connector:

Pin #	Signal	ST	Voltage Domain	Description
X3A1	X_CSI_CLK0P	LVDS_I	i.MX 6 internal	Camera_2 clock+
X3A2	X_CSI_CLK0M	LVDS_I	i.MX 6 internal	Camera_2 clock-
X3A4	X_CSI_D0P	LVDS_I	i.MX 6 internal	Camera_2 data0+
X3A5	X_CSI_D0M	LVDS_I	i.MX 6 internal	Camera_2 data0-
X3A7	X_CSI_D1P	LVDS_I	i.MX 6 internal	Camera_2 data1+
X3A8	X_CSI_D1M	LVDS_I	i.MX 6 internal	Camera_2 data1-
X3A10	X_CSI_D2P	LVDS_I	i.MX 6 internal	Camera_2 data2+
X3A11	X_CSI_D2M	LVDS_I	i.MX 6 internal	Camera_2 data2-
X3A13	X_CSI_D3P	LVDS_I	i.MX 6 internal	Camera_2 data3+
X3A14	X_CSI_D3M	LVDS_I	i.MX 6 internal	Camera_2 data3-

Table 42: Camera_2 Signal Location at phyFLEX Connector X3

Use of the I²C bus and the camera clock signal allows to directly connect a MIPI/CSI-2 camera module.

[29]: The phyFLEX-flex connector X3 is not available with all assembly configurations of the phyFLEX-i.MX 6 SOM.

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15 Tamper Detection

The phyFLEX-i.MX 6 supports the tamper detection feature of the i.MX 6. With the tamper detection feature it is possible to recognize when the device encounters unauthorized opening or tampering.

For this purpose, the i.MX 6's Tamper Detection signal is available at pin X3A29 of the phyFLEX-flex connector[30].

When not in use, the Tamper Detection signal is pulled-down internally. In order to implement tamper protection this signal should be connected to a Tamper Detection contact in the application which is normally closed pulling the Tamper Detection signal to the power domain VDD_MX6_SNVS on the phyFLEX-i.MX 6 (i.MX 6: VDD_SNVS_IN).

For proper operation of the tamper detection an always-ON power supply (coin cell battery, or memory backup capacitor) must be connected to the VDD_MX6_SNVS power input at pin X3B46 of the phyFLEX-flex connector[30].

If the tamper detection feature is enabled by software then opening of the tamper contact can, e.g., result in:

- switching system power ON with a Tamper Detection alarm interrupt asserted (for software reaction) , or
- activating security related hardware (e.g. automatic and immediate erasure of the Zeroizable Master Key and deny access and erase secure memory contents)

[30]: The phyFLEX-flex connector X3 is not available with all assembly configurations of the phyFLEX-i.MX 6 SOM.

16 Environment Management IC (EMIC) (U19)

The optional Environment Management IC (EMIC) at U19 gives the possibility to detect, monitor and record particular physical parameter such as current consumption, temperature und voltages. Furthermore the Environment Management IC comes with a PWM output and a tacho input for fan controlling and an I^2C Management bus.

The following table shows the signals of the EMIC available at phyFLEX Connector X1.

Pin #	Signal	ST	Voltage Domain	Description
X1A74	X_PM_SDA	I/O	VMMC_3P3V	EMIC I^2C bus data
X1A75	X_PM_SCL	O	VMMC_3P3V	EMIC I^2C bus clock
X1A79	X_PM_PWM	O		EMIC fan PWM output
X1A80	X_PM_TACHO	I		EMIC fan tacho input

Table 43: Environment Management IC (EMIC) IO Signals

In addition to the signals brought out at the phyFLEX Connector, four temperature sensors and a current sense amplifier are optionally available on the phyFLEX-i.MX 6. The temperature sensors can be used to monitor the temperature of the Core Power Supply (U22), the RAM (U21), the Controller/PCB (U23), and the Ethernet PHY (U24). The current sense amplifier at U16 serves to monitor the current consumption of the SOM

The table below lists the I^2C addresses of the four temperature sensors, while *Figure 14* and *Figure 15* show the location of the sensors.

Temperature Sensor	Address
RAM (U21)	0x49
Core Power Supply (U22)	0x48
Controller/PCB (U23)	0x4A
Ethernet PHY (U24)	0x4B

Table 44: I^2C Addresses of the optional Temperature Sensors

Note:
As the software required for the EMIC depends much on the individual use case the EMIC is not programmed upon delivery. Hence, usage of the EMIC requires additional software development. Programming and debugging of the EMIC is possible via test points TP13 and TP18 – TP21. Please contact our sales team for additional information.

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Note:
To avoid any conflicts when connecting external I^2C devices to the EMIC's I^2C bus at X1A74 (X_PM_SDA) and X1A75 (X_PM_SCL) the addresses of the on-board temperature sensors must be considered.

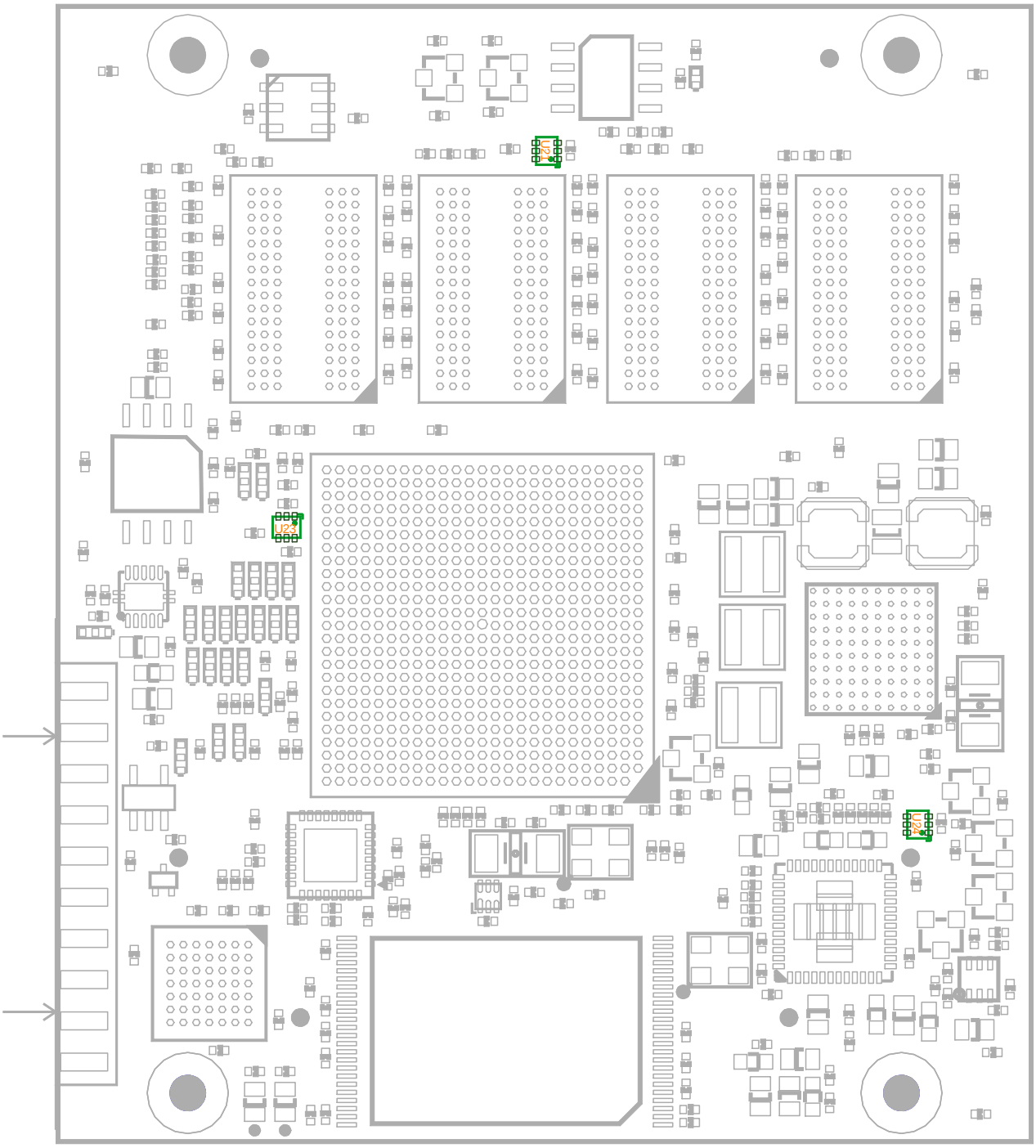


Figure 14: EMIC and supporting Components (top view)

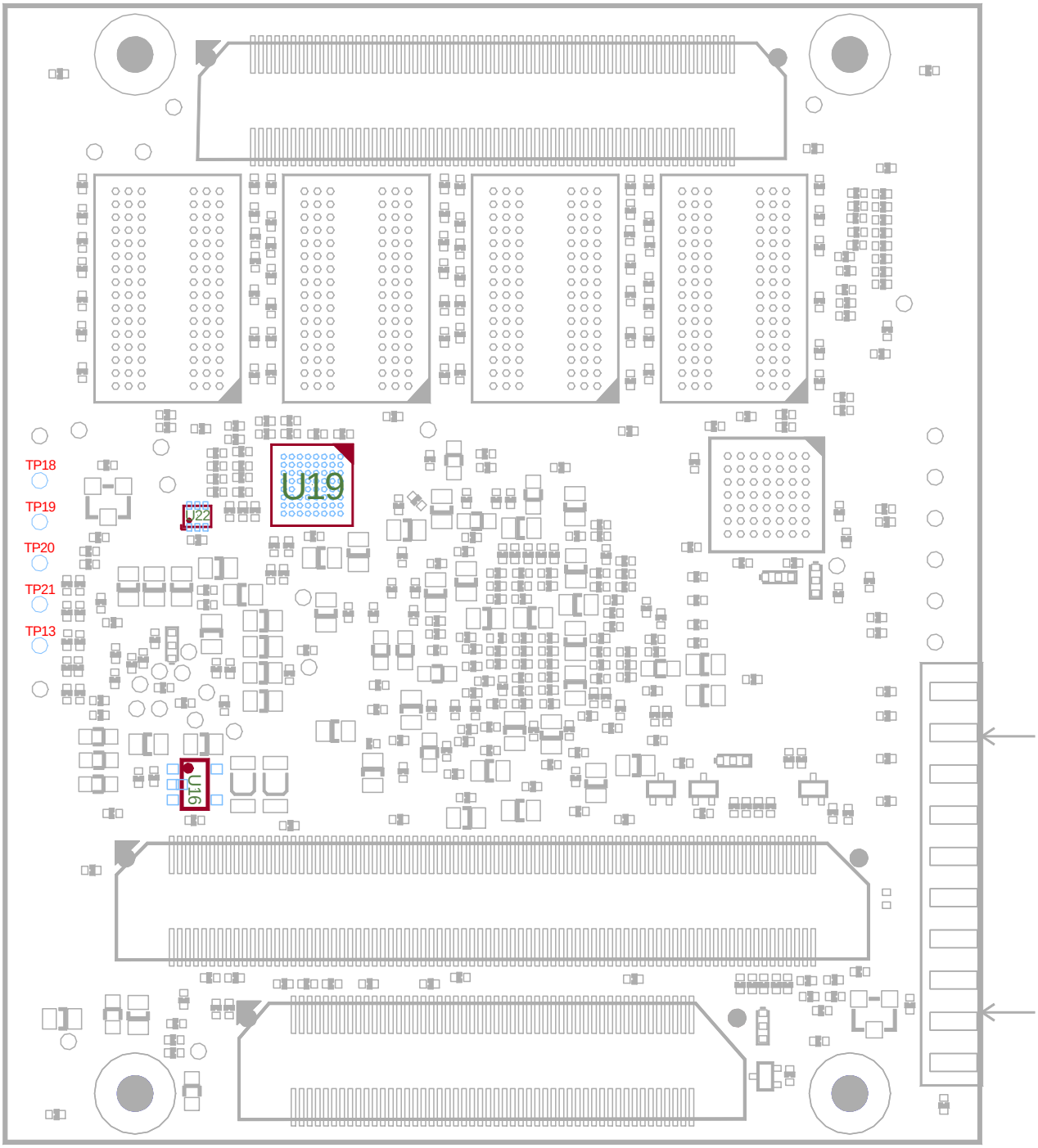


Figure 15: EMIC and supporting Components (bottom view)

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17 Technical Specifications

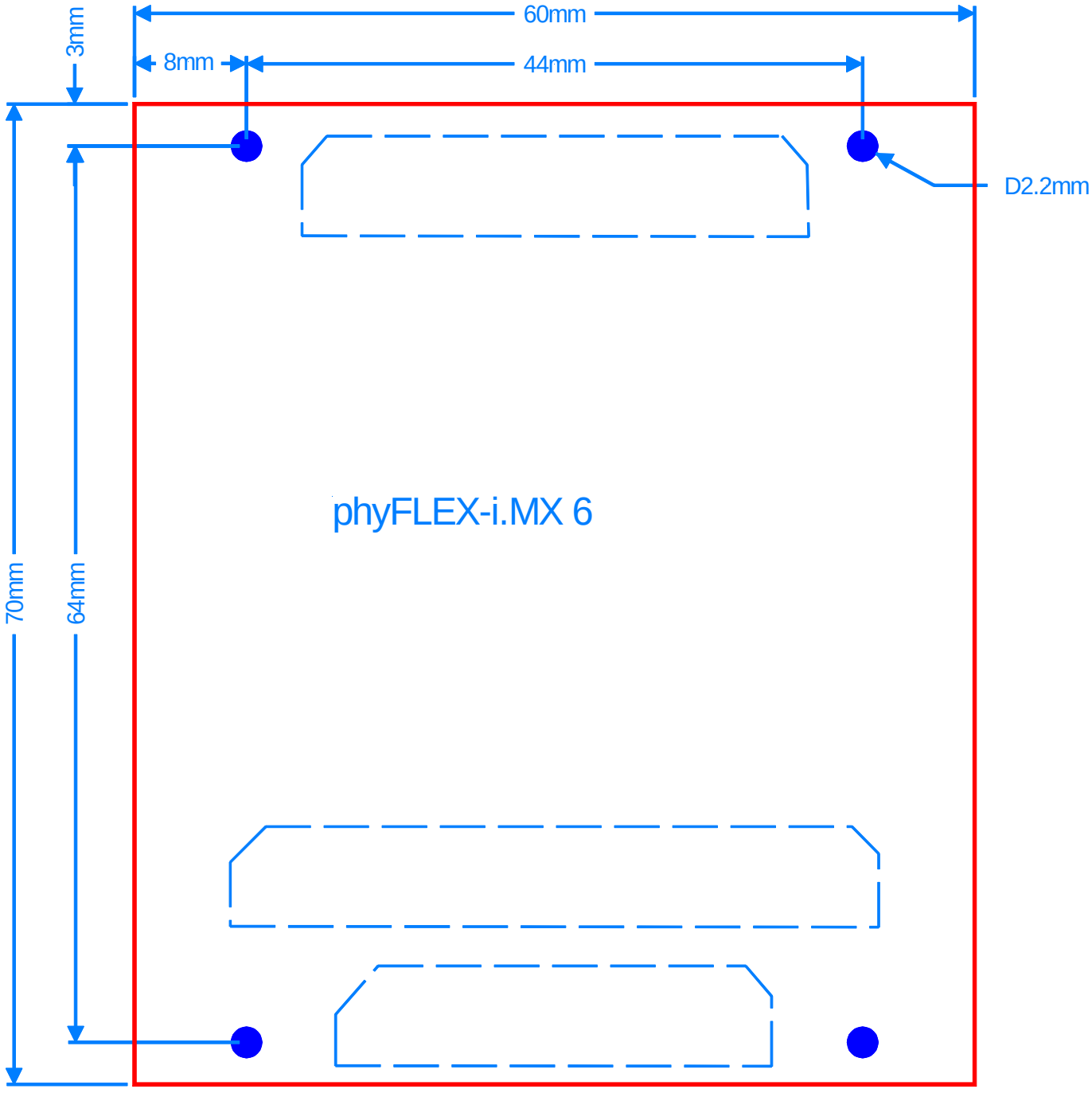


Figure 16: Physical Dimensions (top view)

The physical dimensions of the phyFLEX-i.MX 6 are represented in *Figure 16*. The module's profile is max. 10 mm thick, with a maximum component height of 3.0 mm on the bottom (connector) side of the PCB and approximately 5.0 mm on the top (microcontroller) side. The board itself is approximately 1.4 mm thick.

Note:
To facilitate the integration of the phyFLEX-i.MX 6 into your design, the footprint of the phyFLEX-i.MX 6 is available for download (*section 18.1*).

Additional specifications:

Dimensions:	60 mm x 70 mm
Weight:	TBD
Storage temperature:	-40 °C to +125 °C
Operating temperature:	refer to *section 17.1*
Humidity:	95 % r.F. not condensed
Operating voltage:	VCC 5 V +/- 5 %
Power consumption:	TBD

Table 45: Technical Specifications

These specifications describe the standard configuration of the phyFLEX-i.MX 6 as of the printing of this manual.

17.1 Product Temperature Grades

Caution!
The right temperature grade of the Module depends very much on the use case. It is mandatory to determine if the use case suites the temperature range of the chosen module (see below). If necessary a heat spreader can be used for temperature compensation

The feasible operating temperature of the SOM highly depends on the use case of your software application. Modern high performance microcontrollers and other active parts as the ones described within this manual are usually rated by qualifications based on tolerable junction or case temperatures. Therefore, making a general statement about maximum or minimum ambient temperature ratings for the described SOM is not possible. However, the above mentioned parts are available still in different temperature qualification levels by the producers. We offer our SOM's in different configurations making use of those temperature qualifications. To indicate which level of temperature qualification is used for active and passive parts of a SOM configuration we have categorized our SOM's in three temperature grades. The table below describes these grades in detail. These grades describe a set of components which in combination add up to a useful set of product options with different temperature grades. This enables us to make use of cost optimizations depending on the required temperature range.

In order to determine the right temperature grade and whether the maximum or minimum qualification levels are met within an application the following conditions must be defined by considering the use case:

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- Determined processing load for the given software use case
- Maximum temperature ranges of components (see table below)
- Power consumption resulting from a base load and the calculating power required (in consideration of peak loads as well as time periods for system cool down)
- Surrounding temperatures and existing airflow in case the system is mounted into a housing
- Heat resistance of the heat dissipation paths within the system along with the considered usage of a heat spreader or a heat sink to optimize heat dissipation

Product Temp. Grade	Controller Temp Range (Junction Temp)	RAM (Case Temp)	Others (Ambient)
I	Industrial -40 °C to +105 °C / Automotive -40 °C to+125 °C	Industrial -40 °C to +95 °C	Industrial -40 °C to +85 °C
X	Extended Commercial -20 °C to +105 °C	Industrial -40 °C to +95 °C	Industrial -40 °C to +85 °C
C	Commercial 0 °C to +95 °C	Consumer 0 °C to +95 °C	Consumer 0 °C to +70 °C

Table 46: Product Temperature Grades

17.2 Connectors on the phyFLEX-i.MX 6

Manufacturer	Samtec
	phyFLEX-fix (X1):
Number of pins per contact rows	160 pins (2 rows of 80 pins each)
Samtec part number (lead free)	BSH-080-01-L-D-A-K-TR
	phyFLEX-optional (X2):
Number of pins per contact rows	100 pins (2 rows of 50 pins each)
Samtec part number (lead free)	BSH-050-01-L-D-A-K-TR
	phyFLEX-flex (X3):
Number of pins per contact rows	120 pins (2 rows of 60 pins each)
Samtec part number (lead free)	BSH-060-01-L-D-A

The following list shows the receptacle sockets that correspond to the connectors populating the underside of the phyFLEX—i.MX 6. The given connector height indicates the distance between the two connected PCBs when the module is mounted on the corresponding carrier board. In order to get the exact spacing, the maximum component height (3 mm) on the bottom side of the phyFLEX must be subtracted.

Connector height 5 mm

Manufacturer	Samtec
Number of pins per contact row	160 pins (2 rows of 80 pins each)
Samtec part number (lead free)	ASP-167037-01 (BTH-080-01-L-D-A-K-TR)
Phytec part number (lead free)	VM245
Number of pins per contact row	100 pins (2 rows of 50 pins each)
Samtec part number (lead free)	BTH-050-01-L-D-A-K-TR
Phytec part number (lead free)	VM247
Number of pins per contact row	120 pins (2 rows of 60 pins each)
Samtec part number (lead free)	BTH-060-01-L-D-A
Phytec part number (lead free)	VM240

Please refer to the corresponding data sheets and mechanical specifications provided by Samtec (*www.samtec.com*).

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18 Hints for Integrating and Handling the phyFLEX-i.MX 6

18.1 Integrating the phyFLEX-i.MX 6

Besides this hardware manual much information is available to facilitate the integration of the phyFLEX-i.MX 6 into customer applications.

1. the design of the standard phyFLEX Carrier Board can be used as a reference for any customer application
2. many answers to common questions can be found at http://www.phytec.de/de/support/faq/faq-phyFLEX-i.MX 6.html, or http://www.phytec.eu/europe/support/faq/faq-phyFLEX-i.MX 6.html
3. the link "Carrier Board" within the category Dimensional Drawing leads to the layout data as shown in *Figure 17*. It is available in different file formats. Use of this data allows to integrate the phyFLEX-i.MX 6 SOM as a single component into your design.
4. different support packages are available to support you in all stages of your embedded development. Please visit http://www.phytec.de/de/support/support-pakete.html, or http://www.phytec.eu/europe/support/support-packages.html, or contact our sales team for more details.

18.2 Handling the phyFLEX-i.MX 6

- **Modifications on the phyFLEX Module**

Removal of various components, such as the microcontroller and the standard quartz, is not advisable given the compact nature of the module. Should this nonetheless be necessary, please ensure that the board as well as surrounding components and sockets remain undamaged while de-soldering. Overheating the board can cause the solder pads to loosen, rendering the module inoperable. Carefully heat neighboring connections in pairs. After a few alternations, components can be removed with the solder-iron tip. Alternatively, a hot air gun can be used to heat and loosen the bonds.

Caution!
If any modifications to the module are performed, regardless of their nature, the manufacturer guarantee is voided.

- **Integrating the phyFLEX into a Target Application**

Successful integration in user target circuitry greatly depends on the adherence to the layout design rules for the GND connections of the phyFLEX module. For maximum EMI performance we recommend as a general design rule to connect all GND pins to a solid ground plane. But at least all GND pins neighboring signals which are being used in the application circuitry should be connected to GND.

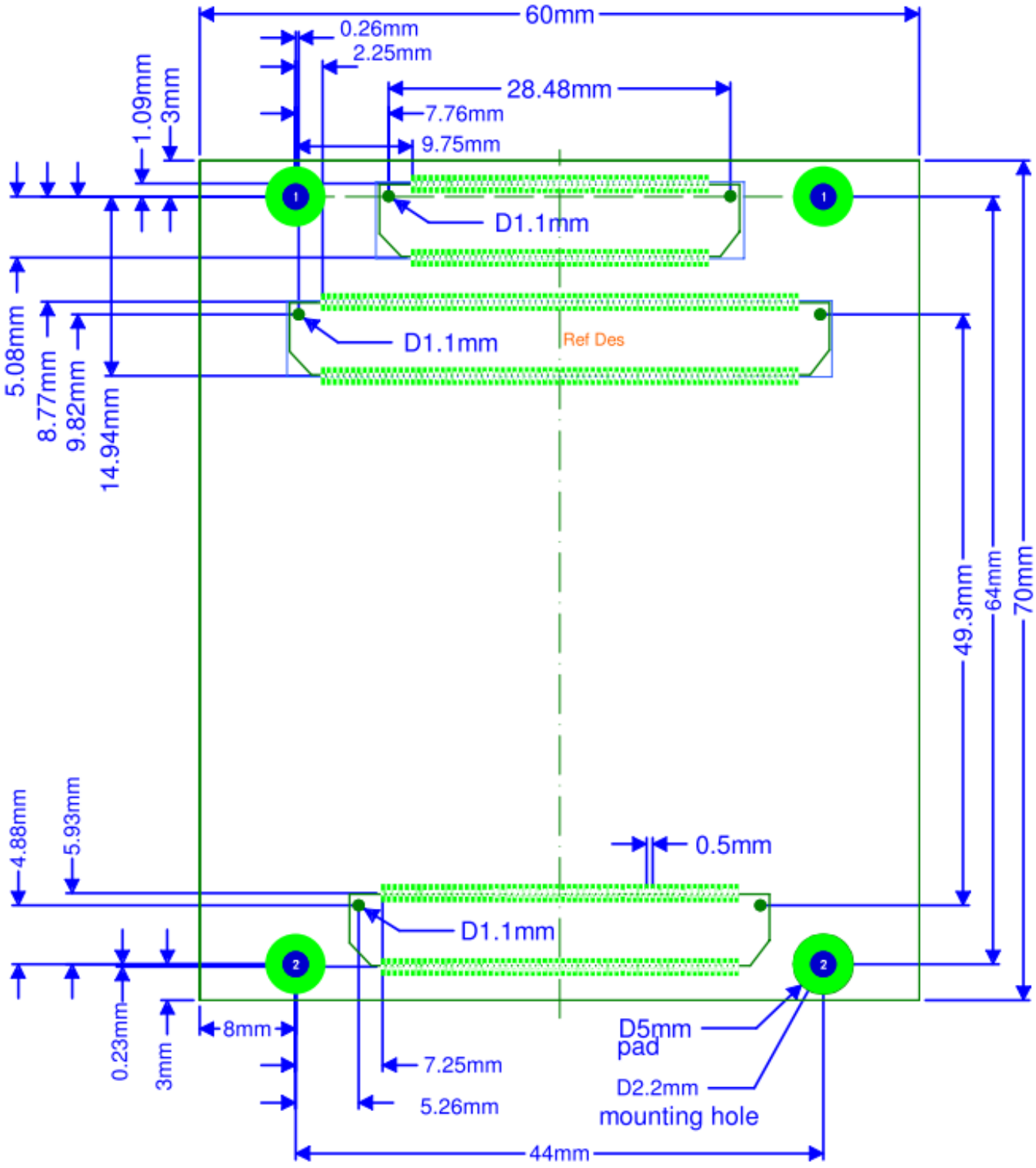


Figure 17: Footprint of the phyFLEX-i.MX 6

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19 The phyFLEX- i.MX 6 on the phyFLEX Carrier Board

Phytec phyFLEX Carrier Boards are fully equipped with all mechanical and electrical components necessary for the speedy and secure start-up and subsequent communication to and programming of applicable Phytec System on Module (SOM) modules. phyFLEX Carrier Boards are designed for evaluation, testing and prototyping of Phytec System on Module in laboratory environments prior to their use in customer designed applications.

The phyFLEX Carrier Board provides a flexible development platform enabling quick and easy start-up and subsequent programming of the phyFLEX-i.MX 6 System on Module. The carrier board design allows easy connection of additional extension boards featuring various functions that support fast and convenient prototyping and software evaluation.

Note:
The following list includes all features of the phyFLEX Carrier Board. Features which are not supported by the phyFLEX-i.MX 6 are in light gray.

The phyFLEX Carrier Board supports the following features for the phyFLEX-i.MX 6 modules:

- Power supply circuits to supply the phyFLEX-i.MX 6 and the peripheral devices of the carrier board
- 12 V Power Supply
- POE+ Power over Ethernet support (25 W)
- Support of all interfaces available at the phyFLEX-fix and phyFLEX-optional Connector
- Support of different power modes of the appropriate phyFLEXs
- Switch to configure the boot order of the i.MX 6
- Full featured 4 line RS-232 transceiver supporting data rates of up to 1 Mbps, hardware handshake and RS-232 connector
- Second 2 line RS-232 transceiver supporting data rates of up to 1 Mbps
- High integrated and isolated CAN interface
- USB 3.0 hub with 4 downstream ports available at different connectors (the i.MX 6 supports only USB 2.0)
- USB-OTG interface
- Gbit Ethernet interface
- 10/100 Mbps Ethernet interface
- Support of two I^2C buses from the SOM, available at different connectors on the carrier board (the phyFLEX-i.MX 6 features only one I^2C interface (I2C0))
- Connectivity to two SPI interfaces from the phyFLEX-Module
- Complete audio interface available at four 3.5 mm audio jacks and speaker connector
- DVI interface
- Phytec Display Interface (PDI) (LVDS display with separate connectors for data lines and display / backlight supply voltage)
- Circuitry to allow dimming of a backlight

- Touch screen interface for use of 4 wire resistive touch screens
- Two LVDS camera interfaces compatible to Phytec phyCAM-S+ camera standard with I^2C for camera control
- Two Secure Digital Card / Multi Media Card Interfaces
- Phytec Wi-Fi/Bluetooth connector
- DIP switch to configure the boot options for the phyFLEX-i.MX 6 module mounted
- RTC with battery supply/backup
- SATA Power and Data connector
- PCIe port
- miniPCIe port
- Five user programmable LEDs
- Pin header connector to connect to 10 GPIOs of the phyFLEX-Module
- JTAG interface for programming and debugging
- Fan Connector
- Environment Management IC (EMIC) for custom specific monitoring of different voltages, currents and temperatures, and for fan control

19.1 Concept of the phyFLEX Carrier Board

The phyFLEX Carrier Board provides a flexible development platform enabling quick and easy start-up and subsequent programming of the phyFLEX System on Module. The carrier board design allows easy connection of additional extension boards featuring various functions that support fast and convenient prototyping and software evaluation. The carrier board is compatible with all phyFLEX SOMs.
This modular development platform concept includes the following components:

- the **phyFLEX-i.MX 6 Module** populated with the i.MX 6 microcontroller and all applicable SOM circuitry such as DDR SDRAM, Flash, PHYs, and transceivers to name a few.

- the **phyFLEX Carrier Board** which offers all essential components and connectors for start-up including: a power socket which enables connection to an **external power adapter**, interface connectors such as **DB-9**, **USB** and **Ethernet** allowing for use of the SOM's interfaces with standard cable.

The following sections contain specific information relevant to the operation of the phyFLEX-i.MX 6 mounted on the phyFLEX Carrier Board.

Note:
Only features of the phyFLEX Carrier Board which are supported by the phyFLEX-i.MX 6 are described. Jumper settings and configurations which are not suitable for the phyFLEX-i.MX 6 are not described in the following chapters.

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19.2 Overview of the phyFLEX Carrier Board Peripherals

The phyFLEX Carrier Board is depicted in *Figure 18* and *Figure 19*. It is equipped with the components and peripherals listed in *Table 47, Table 48, Table 49* and *Table 50*. For a more detailed description of each peripheral refer to the appropriate chapter listed in the applicable table. The following figures highlight the location of each peripheral for easy identification.

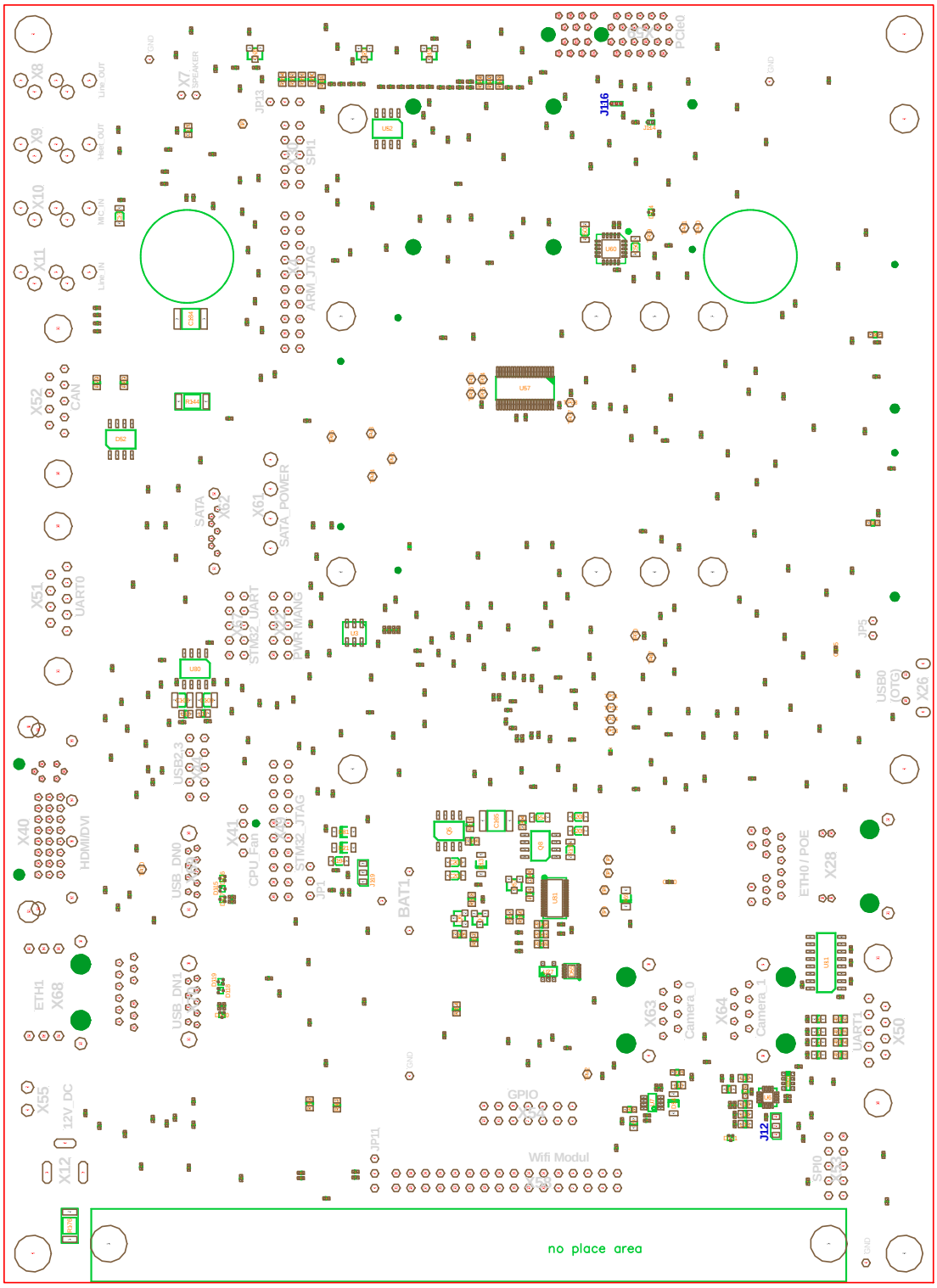


Figure 18: phyFLEX Carrier Board Overview of Connectors, LEDs and Buttons (bottom view)

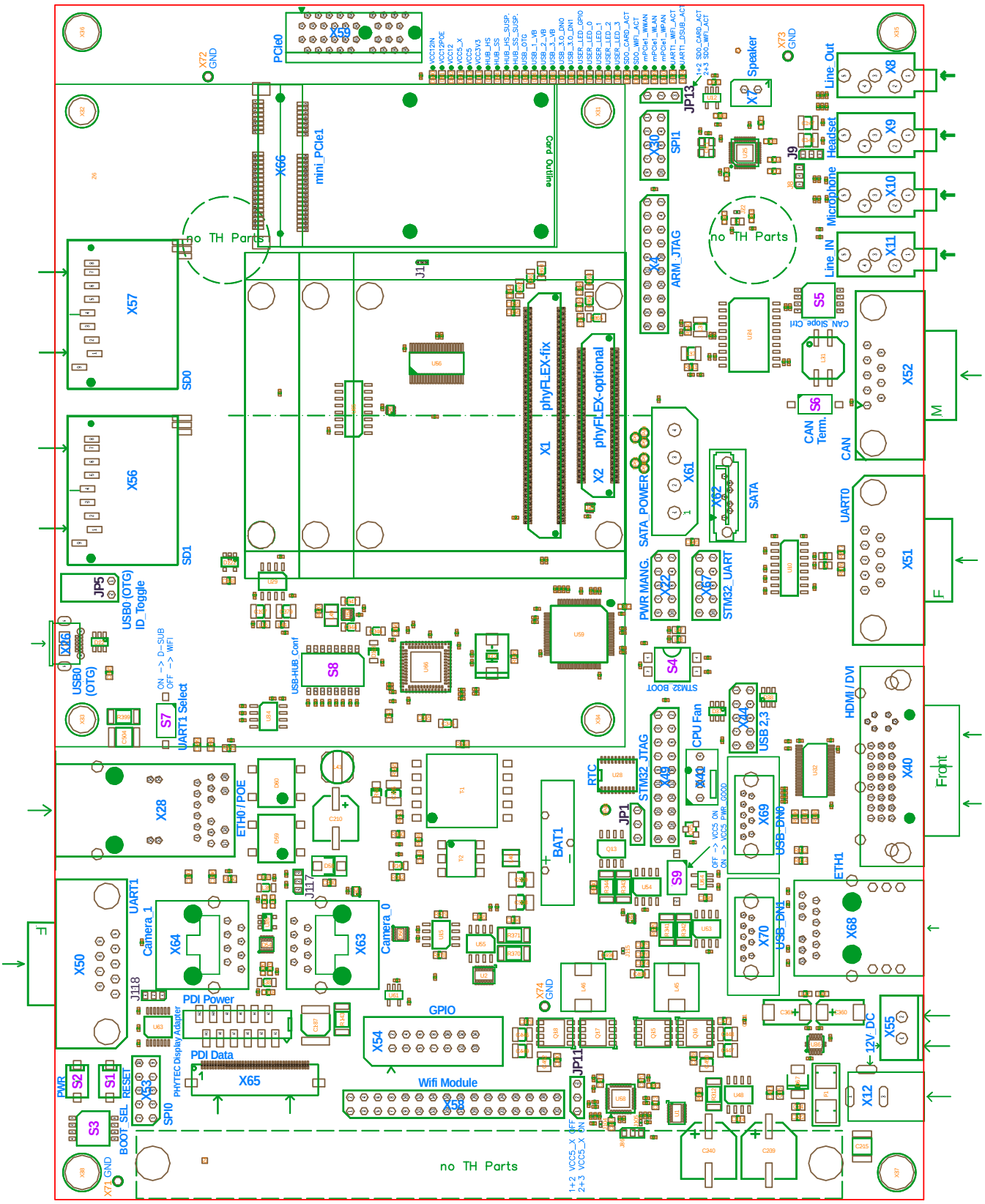


Figure 19: phyFLEX Carrier Board Overview of Connectors, LEDs and Buttons (top view)

Note:
Descriptions printed in light gray in the following tables *Table 47, Table 48, Table 49,* and *Table 50* indicate that the specific feature is not available with the phyFLEX-i.MX 6.

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Note:
The numbering in the signal names of the various interfaces is in compliance with the phyFLEX specification, it might not correspond to the numbering in the controller's documentation. The numbering from the controller's perspective can be found in *Table* 3 to *Table 8*. E.g. the signals of the UART0 interface are derived from the controller's UART 4.

19.2.1 Connectors and Pin Header

Table 47 lists all available connectors on the phyFLEX Carrier Board. *Figure 19* highlights the location of each connector for easy identification.

Reference Designator	Description	See Section
X1	phyFLEX-fix connector for mounting the phyFLEX-i.MX 6	*19.3.1*
X2	phyFLEX-optional connector for mounting the phyFLEX-i.MX 6	
X4	JTAG (2x10-pin header connector; 2.54 mm pitch)	*19.3.24*
X7	Speaker connector (molex connector; 2.5 mm pitch)	*19.3.11*
X8	Line out connector (3.5 mm stereo jack)	
X9	Headset out connector (3.5 mm stereo jack)	
X10	Microphone in connector (3.5 mm stereo jack)	
X11	Line in connector (3.5 mm stereo jack)	
X12	Wall adapter input power jack to supply main board power (12 V, max. 5 A)	*19.3.2.1*
X22	Power Management signal connector (2x5-pin header connector; 2.54 mm pitch)	*19.3.2.3*
X26	USB OTG connector (USB Micro-AB)	*19.3.7*
X28	Ethernet0/POE connector (RJ45 with speed and link LED)	*19.3.2.2 and 19.3.5*
X30	SPI1 interface (2x5-pin header connector; 2.54 mm pitch)	*19.3.13*
X40	DVI connector	*19.3.9*
X41	CPU fan connector	*19.3.19*
X44	Connector for second and third USB host interface (USB2, USB3) from the SOM (2x5-pin header connector; 2.54 mm pitch)	*Not supported*
X49	JTAG interface of the Environment Management IC (EMIC) (2x10-pin header connector; 2.54 mm pitch)	*19.3.26*

Table 47: phyFLEX Carrier Board Connectors and Pin Headers

Reference Designator	Description	See Section
X50	Serial interface UART1 with handshake signals (DB-9F)	19.3.3
X51	Serial interface UART0 without handshake signals (DB-9F)	
X52	CAN interface (DB-9M)	19.3.4
X53	SPI0 interface (2x5-pin header connector; 2.54 mm pitch)	19.3.13
X54	GPIO connector (2x7-pin header connector; 2.54 mm pitch)	19.3.14
X55	Alternative power connector (12 V > 5 A) (terminal block; 5.08 mm pitch)	19.3.2.1
X56	Secure Digital/MultiMedia Card slot SD1	19.3.16
X57	Secure Digital/MultiMedia Card slot SD0	
X58	Wi-Fi/Bluetooth connector (2x16-pin header connector; 2.54 mm pitch)	19.3.20
X59	PCIe0 connector (PCIe0)	19.3.17
X61	SATA power connector	19.3.18
X62	SATA data connector	
X63	Camera_0, phyCAM-S+ Connector (RJ45 connector)	19.3.10
X64	Camera_1, phyCAM-S+ Connector (RJ45 connector)	19.3.10
X65	PDI (Phytec Display Interface)	19.3.8
X66	Mini PCIe connector (PCIe1)	Not supported
X67	Serial interface of the Environment Management IC (EMIC) (2x5-pin header connector; 2.54 mm pitch)	19.3.6
X68	Ethernet1 (ETH1) connector (RJ45 with speed and link LED)	Not supported
X69	Downstream USB_DN0 of USB hub U66 (USB 3.0 standard A)	19.3.6
X70	Downstream USB_DN1 of USB hub U66 (USB 3.0 standard A)	

Table 47: phyFLEX Carrier Board Connectors and Pin Headers (continued)

Note:
Ensure that all module connections are not to exceed their expressed maximum voltage or current. Maximum signal input values are indicated in the corresponding controller User's Manual/Data Sheets. As damage from improper connections varies according to use and application, it is the user's responsibility to take appropriate safety measures to ensure that the module connections are protected from overloading through connected peripherals.

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19.2.2 Switches

The phyFLEX Carrier Board is populated with some switches which are essential for the operation of the phyFLEX-i.MX 6 module on the carrier board. *Figure 19* shows the location of the switches and push buttons.

Button	Description	See Section
S1	System Reset Button – system reset signal generation	*19.3.22*
S2	Power Button – powering on and off main supply voltages of the carrier board	*19.3.23*
S3	DIP switch – boot mode selection phyFLEX SOM	*19.3.21*
S4	DIP switch – boot mode selection EMIC	*19.3.26*
S5	DIP switch - slope control of the CAN transceiver (U24)	*19.3.4*
S6	DIP switch – CAN interface terminating	
S7	DIP switch - UART1 signal routing	*19.3.3* and *19.3.20*
S8	DIP switch USB hub configuration	*19.3.6*
S9	DIP switch Power ON Handling	*19.3.2*

Table 48: phyFLEX Carrier Board Push Buttons Descriptions

S1 Issues a **system reset** signal. Pressing this button will toggle the X_nPM_RESET_IN pin (X1A72) of the phyFLEX microcontroller LOW, causing the controller to reset.

S2 Issues a **power on/off/wake** event. Pressing this button less than 5 seconds will wake up the phyFLEX-i.MX 6 module and the peripherals on the carrier board, or will turn on the system, if it is powered off. Pressing this button more than 5 seconds will turn off the system without proper shut down of the operating system.

S3 This DIP switch allows to change the booting device order of the phyFLEX-i.MX 6.

S4 DIP switch S4 selects the boot source of the EMIC at U59.

S5 DIP switch S5 allows two select different modes of operation for the CAN transceiver at U24. To reduce EMI a slope control can be enabled at different speeds.

S6 By using DIP switch S6 a terminating resistor of 120 Ohm can be connected to the CAN interface.

S7 DIP switch S7 selects if the TTL signals of UART1 are routed either to the RS-232 transceiver at U11 (thus making UART1 available at DB-9 connector X50 at RS-232 level), or to the Wi-Fi/Bluetooth module connector X58 (at TTL level).

S8 Allows to configure the USB hub at U66.

S9 DIP switch S9 selects whether the voltage VCC5 and VCC3V3 are turned on and off by the PWR_GOOD signal (X_PM_PWR_GOOD, X1A78) of the phyFLEX-i.MX 6 or are permanently switched on.

19.2.3 LEDs

The phyFLEX Carrier Board is populated with numerous LEDs to indicate the status of the various USB host interfaces, as well as the different supply voltages. *Figure 19* shows the location of the LEDs. Their function is listed in the table below:

LED	Color	Description	See Section
D91	green	Indicates presence of 12 V input voltage VCC12_POE_X from Ethernet at connector X28	*19.3.2*
D100	green	Indicates presence of 12 V input voltage VCC12_IN at power connector X12, or X55	
D101	green	5 V supply voltage VCC5_X for the phyFLEX-i.MX 6 available	
D102	green	12 V supply voltage VCC12 available at the DC-to-DC synchronous buck controller U58 (derived from VCC12_IN or VCC12_POE)	
D111	green	3.3 V supply voltage VCC3V3_X for various peripherals on the phyFLEX Carrier Board available	*19.3.2*
D112	green	5 V supply voltage VCC5 for various peripherals on the phyFLEX Carrier Board present	
D105	green	User LED connected to GPIO10 (GPIO2_24 of the i.MX 6)	*19.3.15*
D97	red	User LED0 (port LED0 from 4-bit LED dimmer at U52)	
D98	yellow	User LED1 (port LED1 from 4-bit LED dimmer at U52)	
D99	yellow	User LED2 (port LED2 from 4-bit LED dimmer at U52)	
D86	green	User LED3(port LED3 from 4-bit LED dimmer at U52)	
D84	green	Indicates presence of VBUS at the first USB host interface (USB1, USB hub's upstream)	*19.3.6*
D87	green	VBUS indicator for USB hub downstream port USB_DN0	
D88	green	VBUS indicator for USB hub downstream port USB_DN1	
D93	yellow	High-speed indicator LED for USB hub's upstream port connection speed	
D94	yellow	Super-speed indicator LED for USB hub's upstream port connection speed	
D95	yellow	High-speed suspend status indicator LED for USB hub's upstream port	
D96	yellow	Super-speed suspend status indicator LED for USB hub's upstream port	
D85	green	Indicates presence of VBUS at the USB OTG interface (USB0)	*19.3.7*
D82	green	Indicates presence of VBUS at the module's second USB host interface (USB2)	Not supported

Table 49: phyFLEX Carrier Board LEDs Descriptins

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LED	Color	Description	See Section
D83	green	Indicates presence of VBUS at the module's third USB host interface (USB3)	Not supported
D106	yellow	SD0 Card connector X57 active	*19.3.16* *19.3.20*
D107	yellow	Wi-Fi/Bluetooth connector X58 active	
D108	yellow	Mini PCIe WWAN status LED	Not supported
D109	yellow	Mini PCIe WLAN status LED	
D110	yellow	Mini PCIe WPAN status LED	
D123	yellow	UART1 signals routed to Wi-Fi/Bluetooth connector X58 (TTL)	*19.3.20*
D124	yellow	UART1 signals available at DB-9F connector X50 (RS-232)	*19.3.3*

Table 49: phyFLEX Carrier Board LEDs Descriptions (continued)

19.2.4 Jumpers

The phyFLEX Carrier Board comes pre-configured with removable jumpers (JP) and solder jumpers (J). The jumpers allow the user flexibility of configuring a limited number of features for development constraint purposes. *Table 50* below lists the jumpers, their default positions, and their functions in each position. *Figure 20* depicts the jumper pad numbering scheme for reference when altering jumper settings on the development board.

Figure 21 provides a detailed view of the phyFLEX Carrier Board jumpers and their default settings. In these diagrams a beveled edge indicates the location of pin 1.

Before making connections to peripheral connectors it is advisable to consult the applicable section in this manual for setting the associated jumpers.

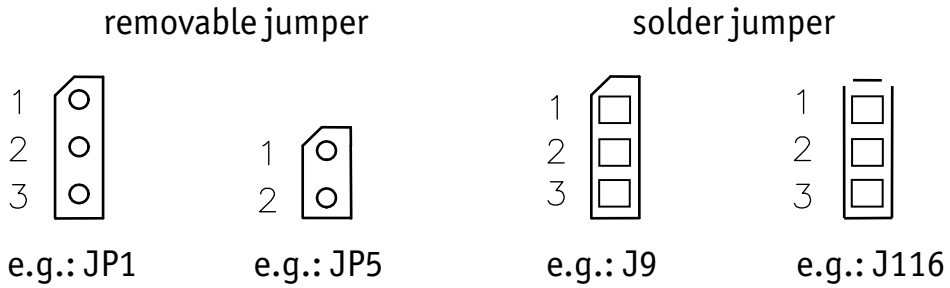


Figure 20: Typical Jumper Numbering Scheme

Table 50 provides a comprehensive list of all carrier board jumpers. The table only provides a concise summary of jumper descriptions. For a detailed description of each jumper see the applicable chapter listed in the right hand column of the table.

If manual modification of the solder jumpers is required please ensure that the board as well as surrounding components and sockets remain undamaged while de-soldering. Overheating the board can cause the solder pads to loosen, rendering the board inoperable. Carefully heat neighboring connections in pairs. After a few alternations, components can be removed with the solder-iron tip. Alternatively, a hot air gun can be used to heat and loosen the bonds.

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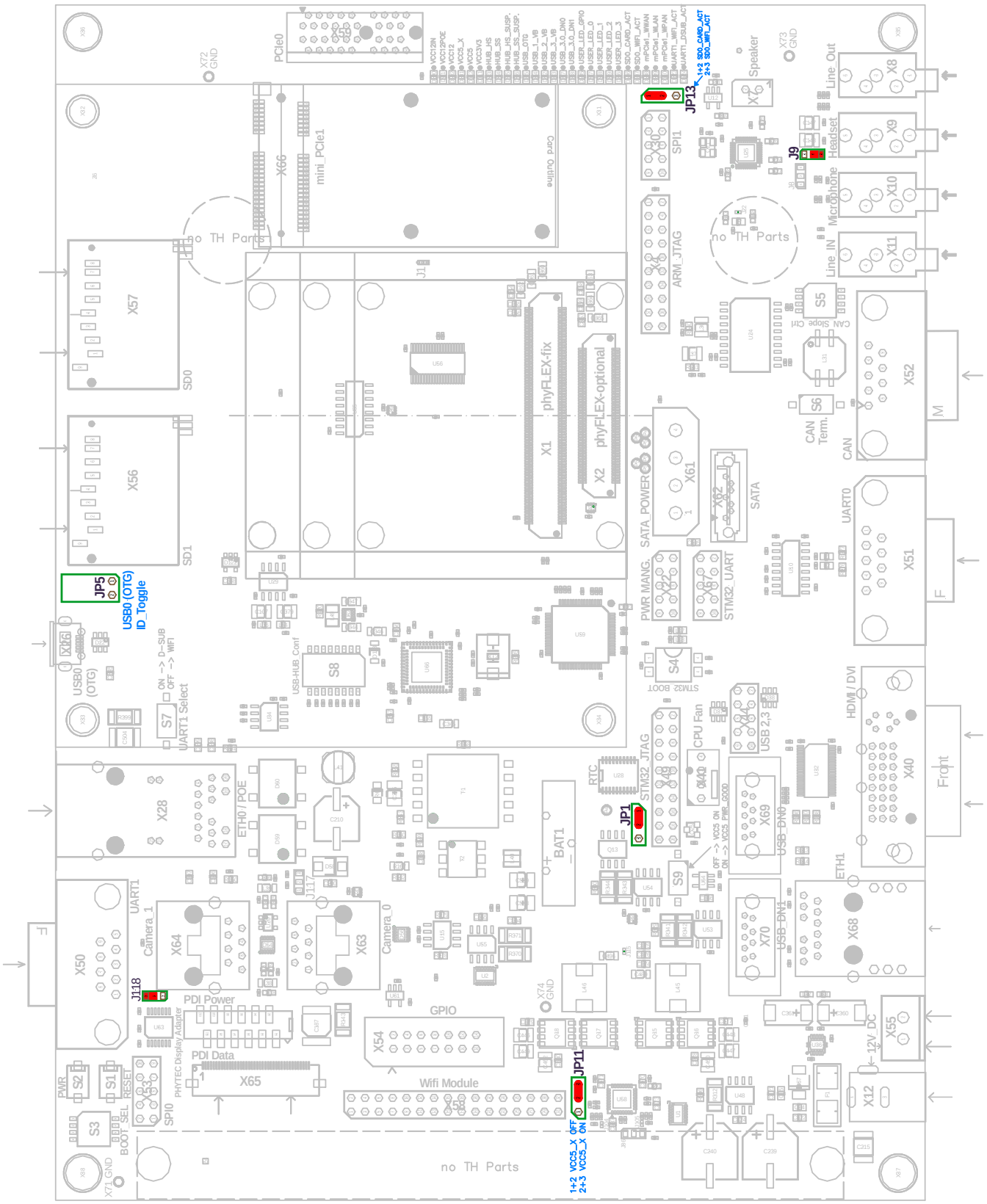


Figure 21: phyFLEX Carrier Board Jumper Locations (top view)

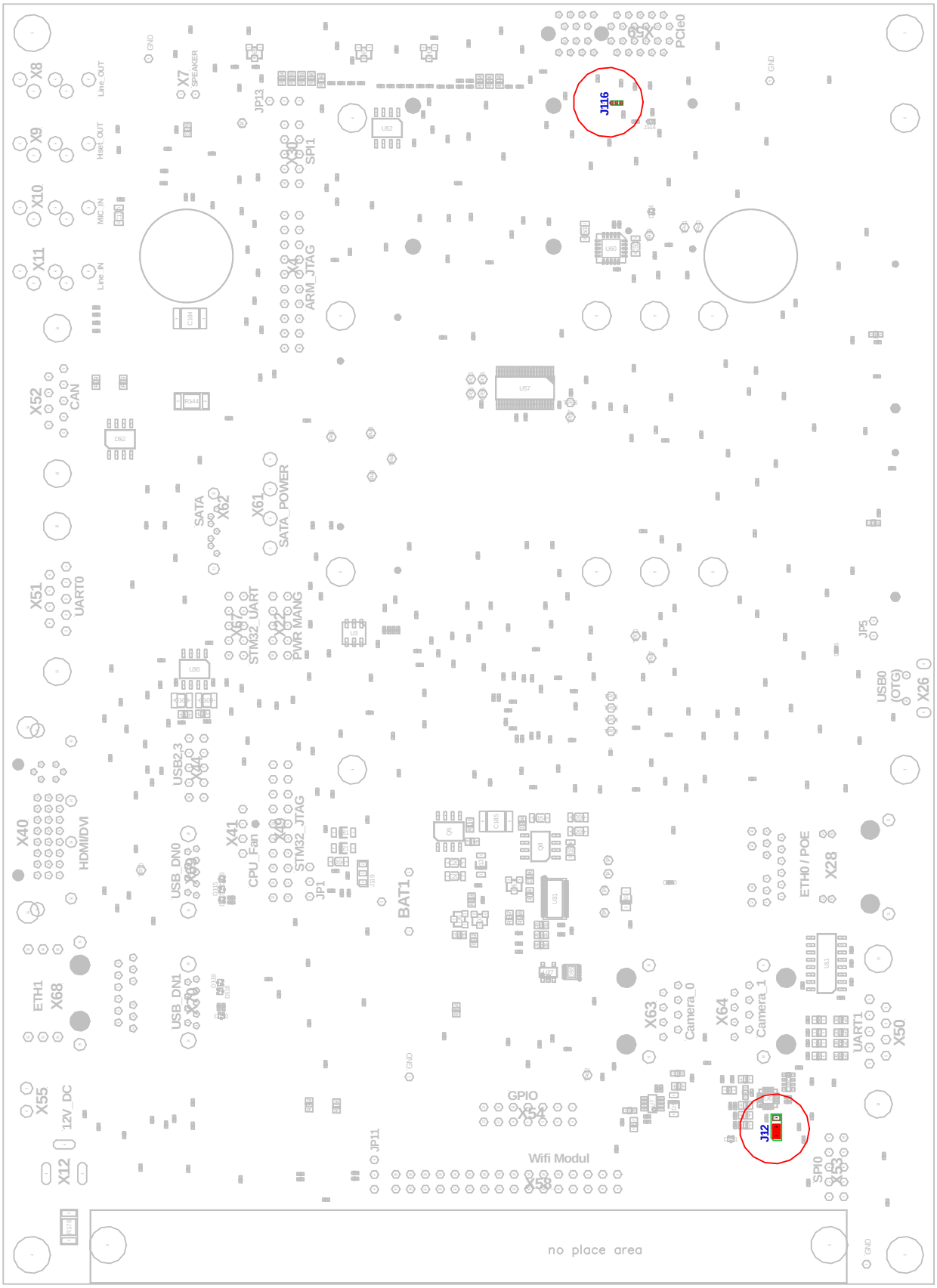


Figure 22: phyFLEX Carrier Board Jumper Locations (bottom view)

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The following conventions are used in the Jumper column of jumper *Table 50*

- J = solder jumper
- JP = removable jumper

Jumper/ Setting	Description	See Section
JP1	Jumper JP1 connects the RTC Interrupt to the Power_ON/Wake/Off Signal or to X_GPIO5 of the phyFLEX-i.MX 6 (GPIO1_09 of the i.MX 6)	*19.3.25*
1+2	**RTC interrupt connected to Power_ON/Wake/Off**	
2+3	RTC interrupt connected to X_GPIO5 (GPIO1_09 of the i.MX 6)	
JP5	Jumper JP5 forces the USB OTG interface of the phyFLEX-i.MX 6 to function either as host (master), or device (slave)	*19.3.7*
open	**USBO_ID floating, phyFLEX-i.MX 6 in slave mode, or according to the mode configured by software**	
1+2	USBO_ ID connected to GND, phyFLEX-i.MX 6 in host mode	
JP11	Jumper JP11 allows to control the supply voltage VCC5_X of the phyFLEX-i.MX 6 module	*19.3.2*
1+2	SOM supply voltage VCC5_X turned OFF	
2+3	**SOM supply voltage VCC5_X turned ON**	
JP13	Jumper JP13 allows to route the signals of SD0 either to the SD card slot X57, or to the Wi-Fi /Bluetooth connector X58	*19.3.16 and 19.3.20*
1+2	**SD0 routed to the SD card slot X57**	
2+3	SD0 routed to the Wi-Fi /Bluetooth connector X58	
J1	Jumper J1 connects either the global reset signal X_nPM_RESET_OUT to the miniPCIe connector X66, or a reset signal specifically dedicated to the PCIe1 interface (available from some phyFLEX SOMs only)	Not supported
1+2	Global reset signal X_nPM_RESET_OUT connected to miniPCIe connector X66	
2+3	**Specifically dedicated reset signal X_nPCIe1_PERST connected to X66**	

Table 50: phyFLEX Carrier Board Jumper Descriptions[31]

[31] : Default settings are in **bold blue** text

Jumper/ Setting	Description	See Section
J9	Jumper J9 connects the shield contact of audio jack X9 (headphone out) to either GND, or the HPCOM output driver of the stereo audio codec at U25. Connecting the shield contact to HPCOM allows using the jack detection function of the stereo audio codec.	*19.3.11*
1+2	Shield contact connected to GND, jack detection disabled	
2+3	**Shield contact connected to the HPCOM output driver of the stereo audio codec, jack detection enabled**	
J12	Jumper J12 configures the I²C address of the touch screen controller at U6	*19.3.8.3*
1+2	**Touch Controller (U6) Address: 0x41**	
2+3	Touch Controller (U6) Address: 0x44	
J116	Jumper J116 connects either the global reset signal X_nPM_RESET_OUT to the PCIe connector X59, or a reset signal specifically dedicated to the PCIe0 interface (available from some phyFLEX SOMs only)	*19.3.17*
1+2	Global reset signal X_nPM_RESET_OUT connected to PCIe connector X59	
2+3	**Specifically dedicated reset signal X_nPCIe0_PERST connected to X59**	
J117	Jumper J117 selects the clock signal used for camera interface Camera_1. Either a separate clock signal, or the clock signal of Camera_0 can be used. The later configuration is useful to have both camera interfaces synchronized	*19.3.10*
1+2	**Interface Camera_1 operates with dedicated clock signal X_CAMERA1_CLK**	
2+3	Interface Camera_1 operates with the same clock signal as interface Camera_0	
J118	Jumper J118 allows to switch buffer U63 (relevant for the SPI0 interface at the display data connector) into Three-State Output Mode that reduces supply current	*19.3.13* and *19.3.8.1*
1+2	Three-State Output Mode enabled	
2+3	**normal operation**	

Table 50: phyFLEX Carrier Board Jumper Descriptions[31] (continued)

Note:
Detailed descriptions of the assembled connectors, jumpers and switches can be found in the following chapters.

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19.3 Functional Components on the phyFLEX Carrier Board

This section describes the functional components of the phyFLEX Carrier Board supporting the phyFLEX-i.MX 6. Each subsection details a particular connector/interface and associated jumpers for configuring that interface.

19.3.1 phyFLEX- i.MX 6 SOM Connectivity (X1, X2) 77

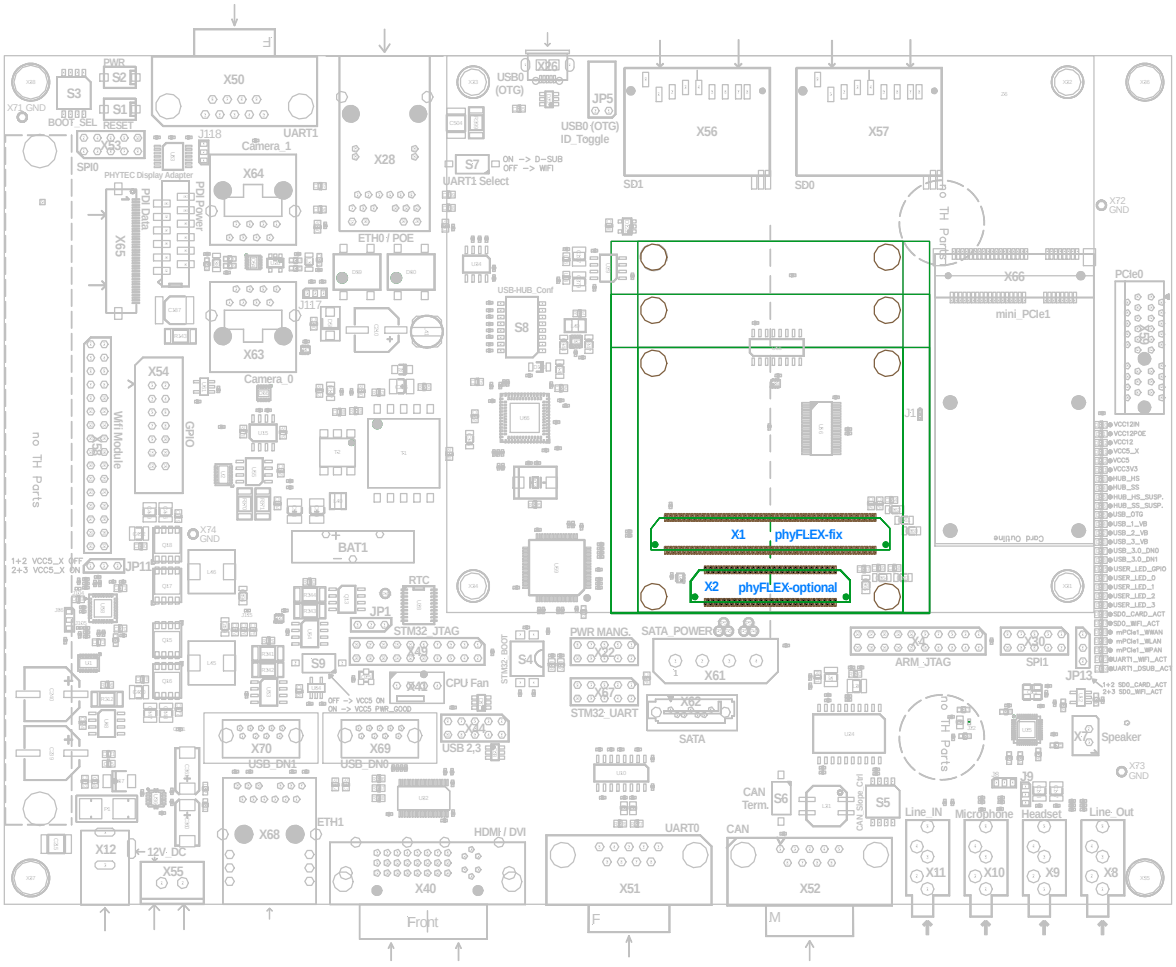


Figure 23: phyFLEX- i.MX 6 SOM Connectivity to the Carrier Board

Connectors X1 and X2 on the carrier board provide the phyFLEX System on Module connectivity. The connector is keyed for proper insertion of the SOM.

Figure 23 above shows the location of connectors X1 and X2, along with the pin numbering scheme as described in *section 2*.

Caution!
Samtec connectors guarantee optimal connection and proper insertion of the phyFLEX-i.MX 6. Please make sure that the phyFLEX-i.MX 6 is fully plugged into the matting connectors of the carrier board. Otherwise individual signals may have a bad, or no contact.

19.3.2 Power (X12, X55, X28)

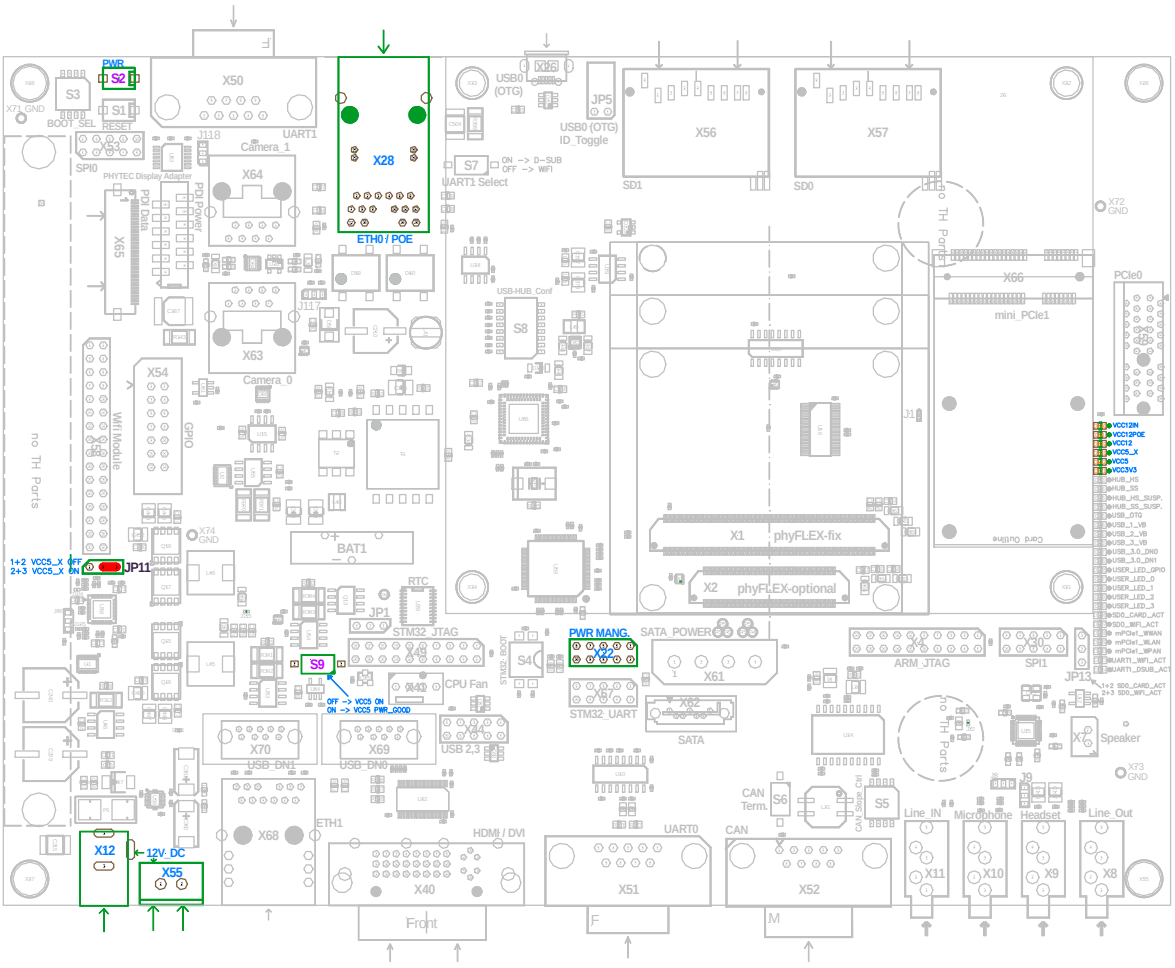


Figure 24: Powering Scheme

The primary input power of the phyFLEX-i.MX 6 Carrier Board comes from either the wall adapter jack X12 (+12 V), or connector X55 (input current > 5 A), or the Power-over-Ethernet circuit (via Ethernet jack X28).

Switching regulators on the carrier board generate seven different voltages to supply the phyFLEX-i.MX 6 and the different components of the carrier board supported by the SOM.

The following table lists the voltage domains and their main use.

Voltage domain	Description
VCC12	Supply voltage[32] (VCC5_X, VCC5, VCC3V3, buck converter, PDI interface, PCIe, SATA, CPU fan), resulting from either VCC12_IN, or VCC12_POE
VCC5	Supply voltage[32] (PDI interface, SATA, DVI, CAN, USB)
VCC5_X	Supply voltage phyFLEX SOM
VCC3V3	Supply voltage[32] (PDI, camera, CPU fan, power management, RTC, Wi-Fi/Bluetooth, SD/MMC card interface, UART interface, PCIe)
VCC1V8	Supply voltage Wi-Fi/Bluetooth
VCC1V8_Audio	Supply voltage audio codec
VCC1V5	Supply voltage[32] mini PCIe1 connector X66
VCC1V1	Supply voltage USB hub U66

Table 51: Voltage Domains on the Carrier Board

Six LEDs on the phyFLEX Carrier Board show the status of the different voltage domains. The assignment of the LEDs to the voltage domains is shown in the following table:

LEDs	Color	Description	
D91	green	VCC12_POE_X –	12 V POE voltage attached to connector X28
D100	green	VCC12_IN –	12 V supply voltage for the phyFLEX Carrier Board attached to connector X12 or X55
D101	green	VCC5_X –	5 V supply voltage for the phyFLEX module
D102	green	VCC12 –	12 V supply voltage for DC-to-DC synchronous buck controller and peripherals on the phyFLEX Carrier Board resulting from either VCC12_IN, or VCC12_POE.
D111	green	VCC_3V3_X –	3.3 V supply voltage for peripherals on the phyFLEX Carrier Board
D112	green	VCC5 –	5 V supply voltage for various peripherals on the phyFLEX Carrier Board

Table 52: Power LEDs

A jumper and a DIP switch on the phyFLEX Carrier Board allow to enable, or disable single voltage domains. The following table lists the voltage domain and the associated jumper and switch.

[32]: **Note:** Not all interfaces listed are supported by the phyFLEX-i.MX 6

Voltage domain	Jumper/ DIP switch	Description
VCC5, VCC3V3	S9	DIP switch S9 selects whether the voltage VCC5 and VCC3V3 are turned on and off by the PWR_GOOD signal (X_PM_PWR_GOOD, X1A78) of the phyFLEX-i.MX 6 or are permanently switched on.
	Off	Power_ON connected to high level. VCC5 and VCC3V3 are permanently on[33]
	On	**Power_ON connected to PWR_GOOD. If X_PM_PWR_GOOD (X1A78) is high the voltages VCC5 and VCC3V3 are switched on**
VCC5_X	JP11	Jumper JP11 allows to control the supply voltage VCC5_X of the phyFLEX-i.MX 6 module
	1+2	SOM supply voltage VCC5_X Voltage is turned Off
	2+3	**SOM supply voltage VCC5_X turned On**

Table 53: Power Jumper JP11 and DIP switch S9

Caution!
It is mandatory to avoid voltages at the IO pins of the phyFLEX-i.MX 6 which are sourced from the supply voltage of peripheral devices attached to the carrier board during power-up, or power–down. These voltages can cause a current flow into the controller especially if peripheral devices attached to the interfaces of the i.MX 6 are supposed to be powered while the phyFLEX-i.MX 6 is in suspend mode, or turned off. External devices should be switched on and off by use of the X_PM_PWR_GOOD signal (X22, pin 8). This way the power-up and power–down sequencing will be considered. Not taking this into account might also lead to problems with booting the module. Refer to *section 4.3* for additional information.

19.3.2.1 Wall Adapter Input (X12)

Caution!
Do not use a laboratory adapter to supply power to the carrier board! Power spikes during power-on could destroy the phyFLEX module mounted on the carrier board! Do not change modules or jumper settings while the carrier board is supplied with power!

Permissible input voltage at X12: 12 V DC regulated (< 5 A).

The required current load capacity of the power supply depends on the specific configuration of the phyFLEX mounted on the carrier board as well as whether optional PCIe boards, USB devices or SATA drives are connected to the carrier board. An adapter with a minimum supply of 2.0 A is recommended.

[33]: **Caution!** DIP switch S9 should be always ON. Disabling the use of the PWR_GOOD signal (X_PM_PWR_GOOD) might cause problems with some variants of the phyFLEX-i.MX 6 module.

Caution!
The power supply circuitry on the carrier board is not designed to support all connectable devices at the same time!

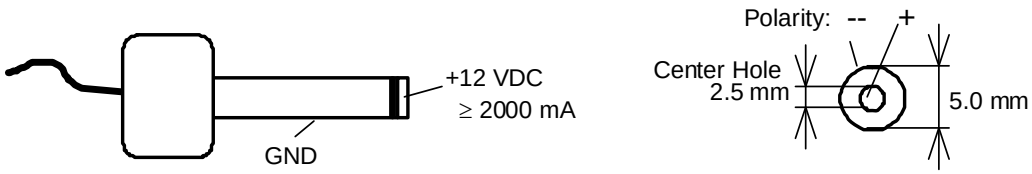


Figure 25: Power Connector corresponding to Wall Adapter Input X12

Note:
If many functions and peripherals of the phyFLEX-i.MX 6 kit are used at the same time the power consumption might exceed 60 W (5 A). Wall Adapter Input X12 is not capable to support this. In this case connector X55 must be used. This connector supports a current of up to 16 A..

19.3.2.2 Power over Ethernet Plus (PoE+) (X28)

The Power-over-Ethernet Plus (POE+) circuit provides a method of powering the board via the Ethernet interface. In this configuration the carrier board acts as the Powered Device (PD) while the connecting Ethernet interface acts as the Power Source Equipment (PSE). For applications that require Ethernet connectivity this is an extremely convenient method to also simultaneously provide power. To make use of the PoE circuit a PSE e.g. a PoE enabled router or switch is necessary. LED D91 indicates the availability of the PoE supply voltage.

The PoE+ circuit generates a supply voltage of 12 V, which is feed into the VCC12 branch through an ideal diode.

The IEEE PoE+ standard restricts the maximum amount of power a PSE must provide and therefore a PD can consume. The carrier board PoE+ circuit was designed to provide up to 25 W of power to the board.

The carrier board Ethernet connector X28 supports both PSE sourcing methods of power over the data wires, or power over the spare wires.

Caution!
The PoE+ circuit was designed to provide up to 25 W of power to the board. This is less than the board can potentially consume. Be aware that this limitation could cause board operation to fail if peak power is exceeded due to enabled peripherals. Do not supply the system over Ethernet, if the power consumption expected might exceed 25 W! Do not change modules or jumper settings while the carrier board is supplied with power over the Ethernet!

19.3.2.3 Power Management Connector (X22)

Pin header connector X22 provides the Power Management Signals generated on the phyFLEX-i.MX 6.

Pin #	Signal Name	Description
1	VCC3V3	3.3 V power supply
2	X_nPM_RESET_OUT	Reset Output
3	X_nPM_RESET_IN	Reset Input
4	X_nPM_ON/WAKEUP/OFF	Power ON/Wake/Off Signal
5	X_PM_SDA	Power Management I²C SDA[34]
6	X_PM_SCL	Power Management I²C SCL[34]
7	NC	not connected
8	X_PM_PWR_GOOD	Power Good Signal
9	NC	not connected
10	GND	Ground

Table 54: Power Management Connector X22

19.3.2.3.1 Power States

- **RUN** can be entered by pressing power button S2 less than 5 seconds. Button S2 is connected to the X_nPM_ON/WAKEUP/OFF signal.
- **OFF** can also be entered using power button S2. In this mode we have to make a distinction between two possible of OFF modes. The first is, when the system is shut down by software. In this case, the phyFLEX-i.MX 6 will stop the running processes and shutdown. If button S2 is held for a time longer than 5 seconds, OFF mode will be reached by turning off the phyFLEX-i.MX 6 internal voltages without stopping processes and shutdown.

It is also possible to control state modes from outside the carrier board with the help of the X_nPM_ON/WAKEUP/OFF signal accessible on the Power Management pin header connector X22. To enter the different power states, signal X_nPM_ON/WAKEUP/OFF must be active low for different times as described in the text above.

[34] : The function of this signal is not available yet

19.3.3 RS-232 Connectivity (X50, X51)

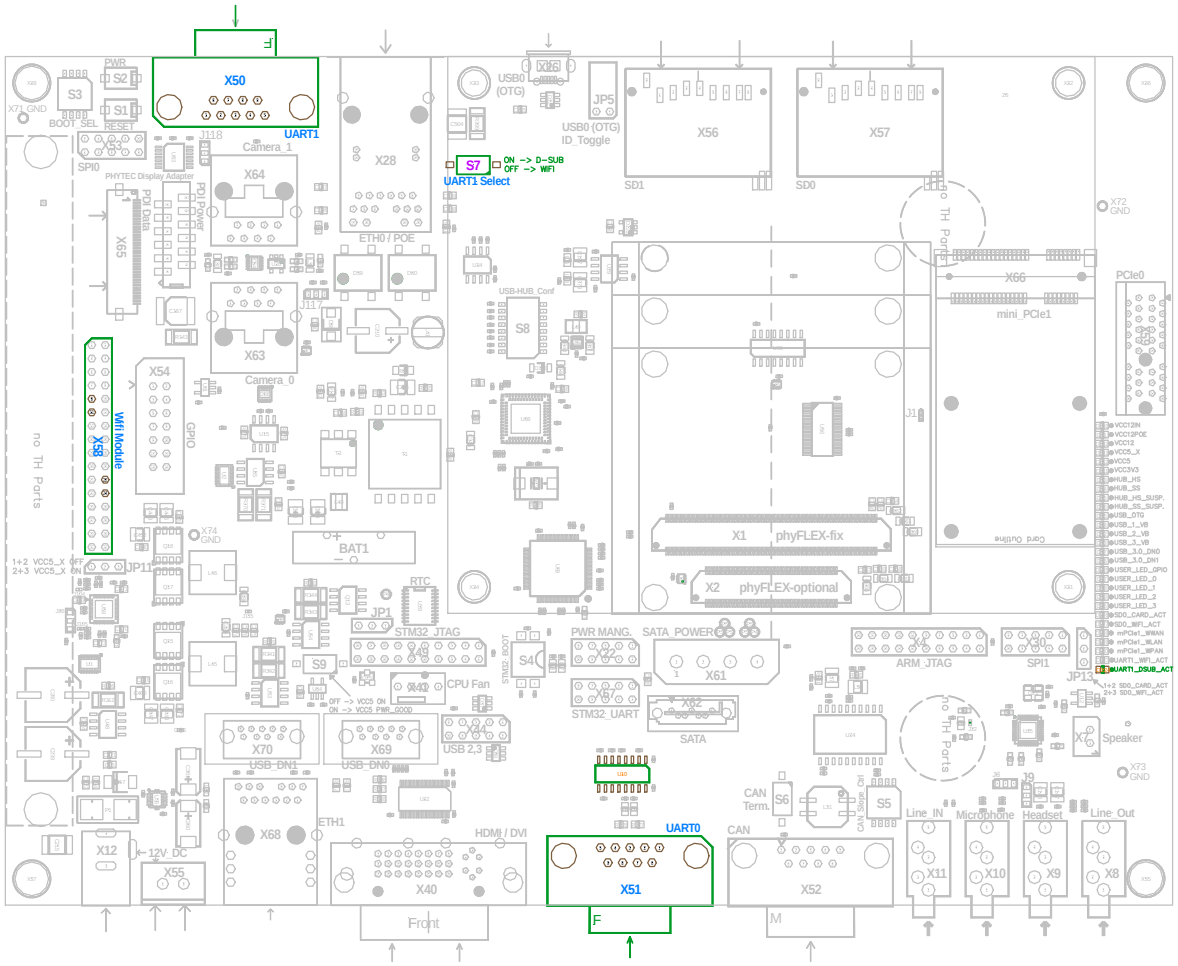


Figure 26: RS-232 Interface Connectors X50 and X51

The phyFLEX Carrier Board supports both UART interfaces (UART0 and UART1) provided by the phyFLEX Module.

Connectors X50 and X51 are DB9 sub-connectors and provide connection interfaces to UART0 (X51) and UART1 (X50) of the phyFLEX-i.MX 6. Two RS-232 transceivers (U10, U11) on the carrier board convert the TTL level signals from the phyFLEX-i.MX 6 to RS-232 level signals. The serial interface UART1 allows for a 5-wire connection including the signals RTS and CTS for hardware flow control. UART0 provides only signals TX and RX. *Figure 27* and *Figure 28* below show the signal mapping of the RS-232 level signals at connectors X50 and X51.

The RS-232 interface at connector X51 (UART0) is hard-wired and no jumpers must be configured for proper operation.

The TTL signals of UART1 can be routed either to the RS-232 transceiver at U11 and thus providing them at X50 as described above, or they can be routed to the Wi-Fi/Bluetooth connector X58. To use the RS-232 interface UART1 at DB-9F connector X50 DIP switch S7 must be ON. LED D124 (yellow) indicates that UART1 is available at connector X50.

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Please refer to section *19.3.20* for more information on how to use the signals of serial interface UART1 on the Wi-Fi/Bluetooth connector X58 at TTL level.

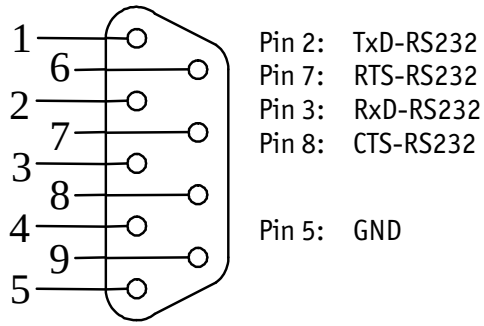


Figure 27: RS-232 Connector X50 Signal Mapping (UART1)

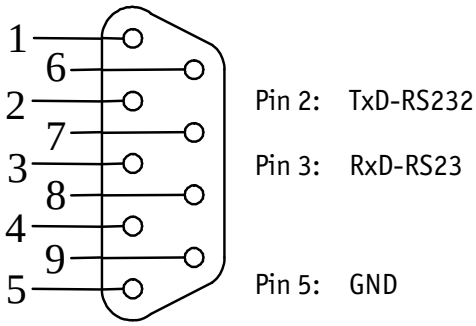


Figure 28: RS-232 Connector X51 Signal Mapping (UART0)

19.3.4 CAN Connectivity (X52)

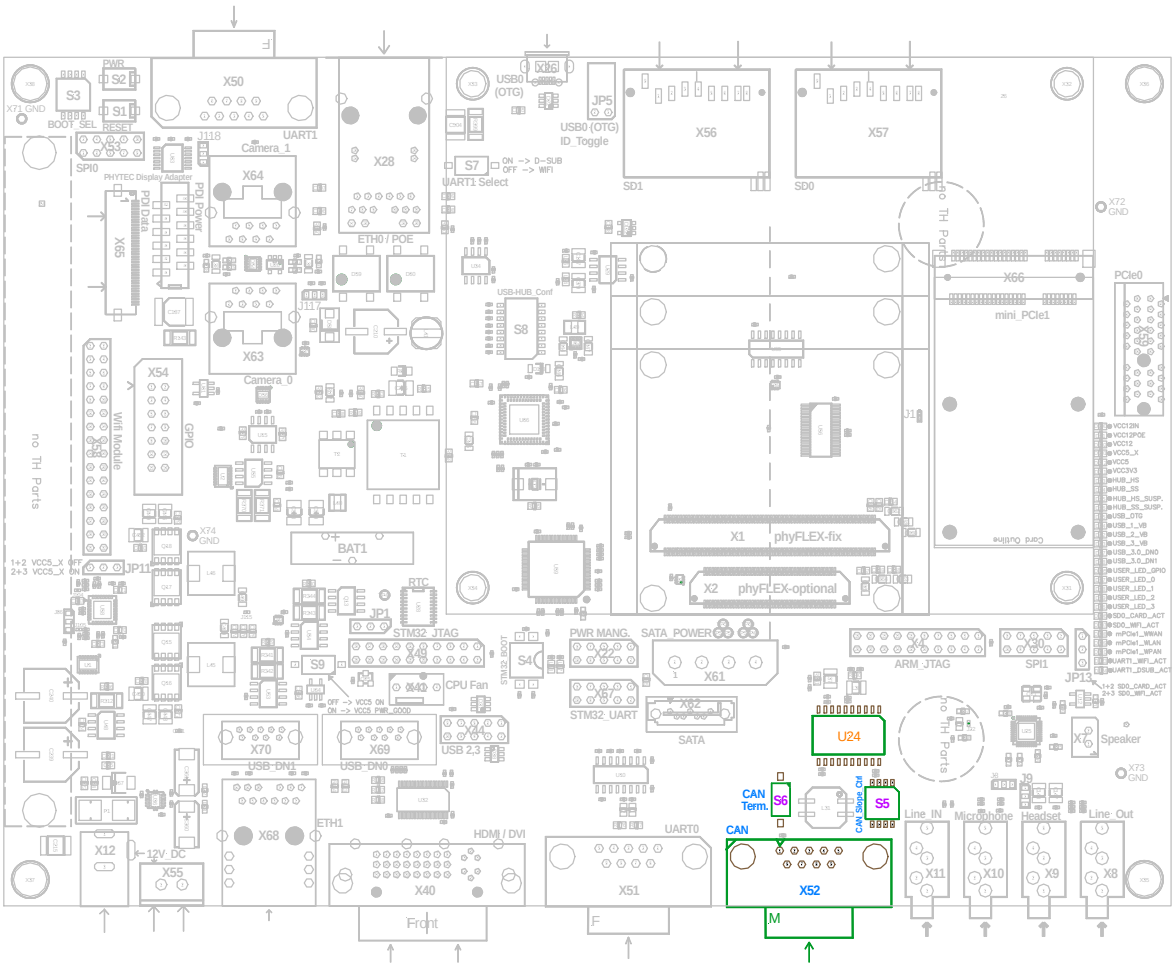


Figure 29: CAN Interface Connector X52

Connector X52 is a SUB-D9M connector and provides connection interfaces to the CAN interface of the i.MX 6. The TTL level signals from the phyFLEX-i.MX 6 are converted to differential CAN signals by the CAN transceiver at U24. This chip is completely integrated with DC/DC Switching Regulator to generate an isolated 5 V voltage.

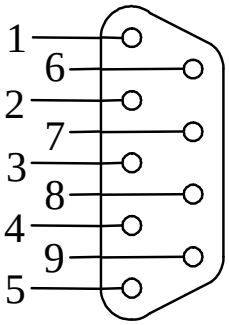
The CAN transceiver allows for slope control which can be configured by use of DIP switch S5. Four different modes of operation can be selected (high-speed and slope control with 3 different speeds). In slope control mode an unshielded twisted pair or a parallel pair of wires can be used as bus lines, while a shielded cable is recommended in high-speed mode to avoid EMI problems. *Table 55* shows the configuration of DIP switch S5 for the different modes.

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Mode of Operation	S5_1	S5_2	S5_3	S5_4
max Slope Control (Lowest Speed / Lowest Emission)	**On**	Off	Off	Off
Slope Control (Low Speed / Low Emission)	Off	**On**	Off	Off
Slope Control (High Speed / High Emission)	Off	Off	**On**	Off
High Speed Mode (Highest Speed / Highest Emission)	Off	Off	Off	**On**

Table 55: phyFLEX Carrier Board DIP Switch S5 Descriptions[35]

DIP switch S6 can be closed to add a 120 Ohm termination resistor across the CAN data lines if needed.



Pin 6: GND_CAN_ISO
Pin 2: CANL
Pin 7: CANH
Pin 3: GND_CAN_ISO

Figure 30: CAN Connector X52 Signal Mapping

[35]: Default settings are in **bold blue** text

19.3.5 Ethernet Connectivity (X28)

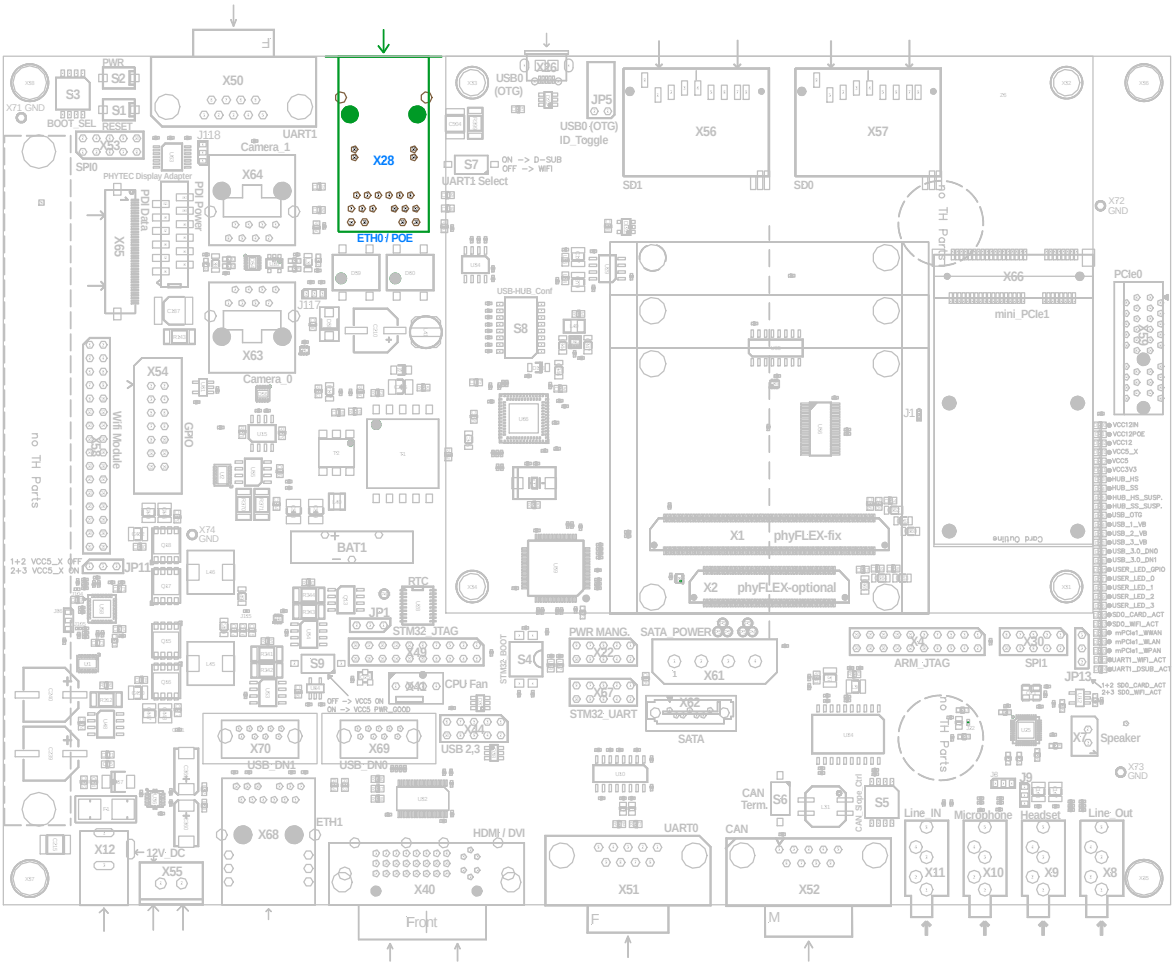


Figure 31: Ethernet Interface at Connector X28

The phyFLEX's Ethernet interface ETH0 (10/100/1000 Mbit/s) is accessible at the RJ-45 connector (X28) on the carrier board. Due to its characteristics this interface is hard-wired and can not be configured via jumpers. The LEDs for LINK (green) and SPEED (yellow) indication are integrated in the connector.

The Gigabit Ethernet interface also supports Power over Ethernet (PoE+). Please refer to *section 19.3.2.2* for more information.

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19.3.6 USB Host Connectivity (X65, X66, X69, X70)

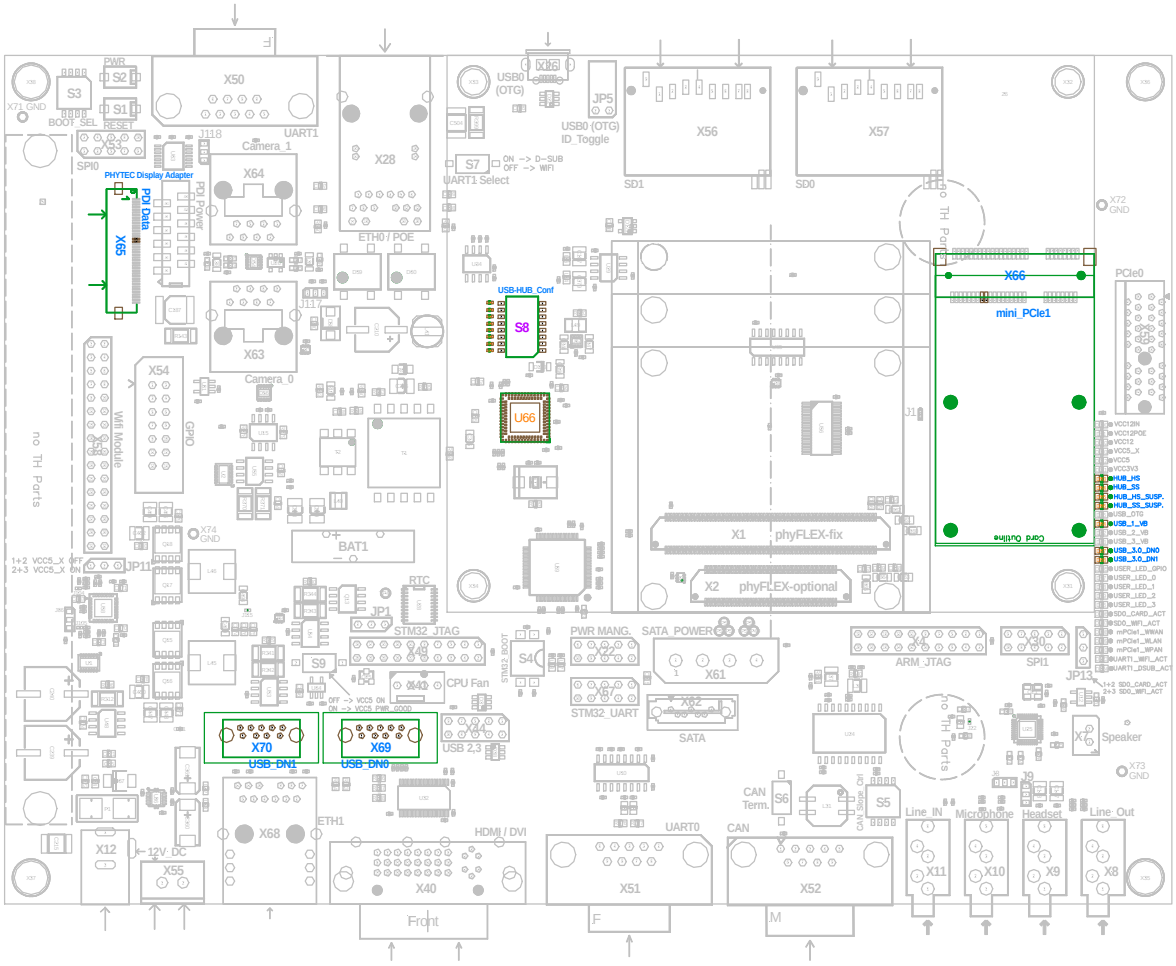


Figure 32: Components supporting the USB Host Interface

The USB host interface (USB1) of the phyFLEX is accessible via the USB hub controller U66 on the carrier board. The controller supports control of input USB devices such as keyboard, mouse or USB key. The USB hub has 4 downstream facing ports. Two ports extend to standard USB A connectors at X69 (USB_DN0) and X70 (USB_DN1). These interfaces are compliant with USB revision 3.0[36]. The remaining ports are accessible at the display data connector X65 and the mini PCIe Connector X66. These two interfaces provide only the data lines D+ and D-. They do not feature a supply line Vbus.

Table 56 shows the distribution of the four downstream facing ports to the different connectors.

[36]: Please note that the USB interfaces of the phyFLEX-i.MX 6 Module are only compliant to USB 2.0. Because of that USB 3.0 devices attached to X69and X70 will not operate at their maximum transmission rate.

USB hub port #	Connector	Connector Type
USB_DN0	X69	USB A (3.0)
USB_DN1	X70	USB A (3.0)
USB_DN2	X65	PDI data connector (40 pin FCC; pins B16 (D+) and B17 (D-))
USB_DN3	X66	Mini PCIe (pins 36 (D-) and D38 (D+))

Table 56: Distribution of the USB Hub's (U66) Ports

LEDs D93 to D96 signal the USB hub's upstream port status. The following table shows the function of the LEDs.

LED	Color	Description
D93	**yellow**	High-speed indicator LED for USB hub's upstream port connection speed
D94	**yellow**	Super-speed indicator LED for USB hub's upstream port connection speed
D95	**yellow**	High-speed suspend status indicator LED for USB hub's upstream port
D96	**yellow**	Super-speed suspend status indicator LED for USB hub's upstream port

Table 57: USB Hub's Status LEDs D93 – D96

LEDs D84, D87 and D88 indicate the presence of the VBUS supply voltage.

LED	Color	Description
D84	**green**	USB1_VBUS indicator LED (USB hub's upstream)
D87	**green**	USB30_VBUS_DN0 indicator LED (X69)
D88	**green**	USB30_VBUS_DN1 indicator LED (X70)

Table 58: USB VBUS Indicator LEDs

DIP switch S8 allows to configure different features of the USB hub controller at U66. The following table shows the different options.

DIP switch/ Setting	Description
1	Switch 1 of DIP_switch S8 configures the ability to control power to the downstream ports of the TUSB8040A1 UBS hub
OFF	**Full Power Management disabled**
ON	Full Power Management enabled
2	Switch 2 of DIP_switch S8 controls the interface mode of the TUSB8040A1 hub (I²C or SMBus)
OFF	**I²C mode selected**
ON	SMBus selected
3	Switch 3 of DIP_switch S8 controls the pull-up of the I²C SCL signal
Off	**I²C SCL pull-up disabled**
On	I²C SCL pull-up enabled
4	Switch 4 of DIP_switch S8 controls the pull-up of the I²C SDA signal
Off	**I²C SDA pull-up disabled**
On	I²C SDA pull-up enabled
5	Switch 5 of DIP_switch S8 controls the battery charging option of downstream port 0
Off	**Battery Charging Port 0 disabled**
On	Battery charging port 0 enabled
6	Switch 6 of DIP_switch S8 controls the battery charging option of downstream port 1
Off	**Battery Charging Port 1 disabled**
On	Battery charging port 1 enabled
7	Switch 7 of DIP_switch S8 controls the battery charging option of downstream port 2
Off	**Battery Charging Port 2 disabled**
Off	Battery C charging port 2 enabled
8	Switch 8 of DIP_switch S8 controls the battery charging option of downstream port 3
Off	**Battery Charging Port 3 disabled**
On	Battery charging port 3 enabled

Table 59: USB Hub's Feature Configuration DIP switch S8[37]

[37] : Default settings are in **bold blue** text

19.3.7 USB OTG Connectivity (X26)

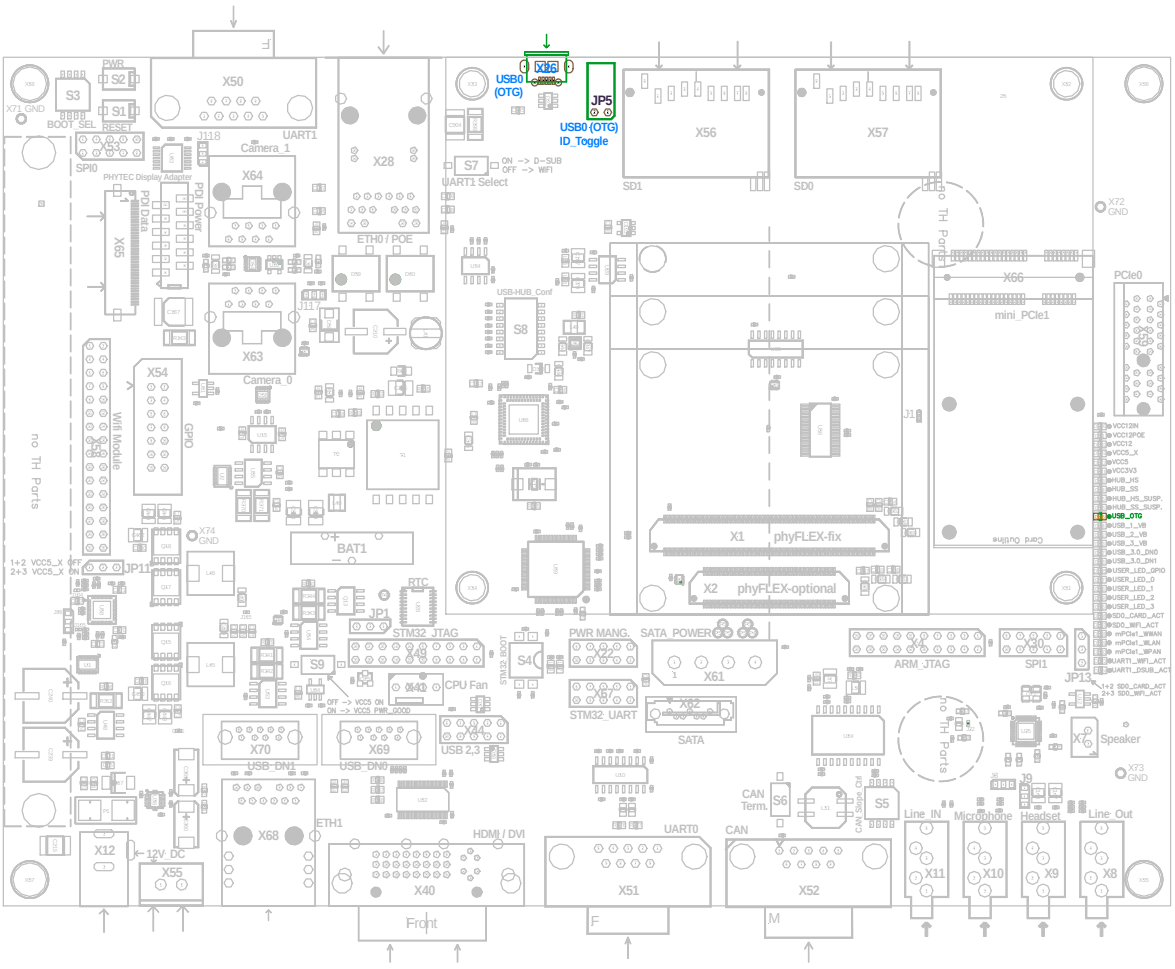


Figure 33: USB OTG Interface at Connector X26

The USB OTG interface of the phyFLEX is accessible at connector X26 (USB Micro-AB) on the carrier board. The phyFLEX-i.MX 6 supports the On-The-Go feature. The Universal Serial Bus On-The-Go is a device capable to initiate the session, control the connection and exchange Host/Peripheral roles between each other. This interface is compliant with USB revision 2.0.

Jumper JP5 configures the OTG operating mode. By default this jumper is open, which leaves the USB_OTG_ID pin floating, and thus configuring the OTG interface as slave. Alternatively this jumper can be closed, connecting USB_OTG_ID to GND, and configuring the OTG interface as host. Typically the configuration of a connecting device as host or slave is done automatically via a USB OTG cable. However, given the limited number of OTG enabled devices in the embedded market this jumper is provided to either simulate an OTG cable, or force the OTG interface into host mode when OTG operation is not required.

LED D85 (green) signals VBUS power output.

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19.3.8 Display / Touch Connectivity (X65)

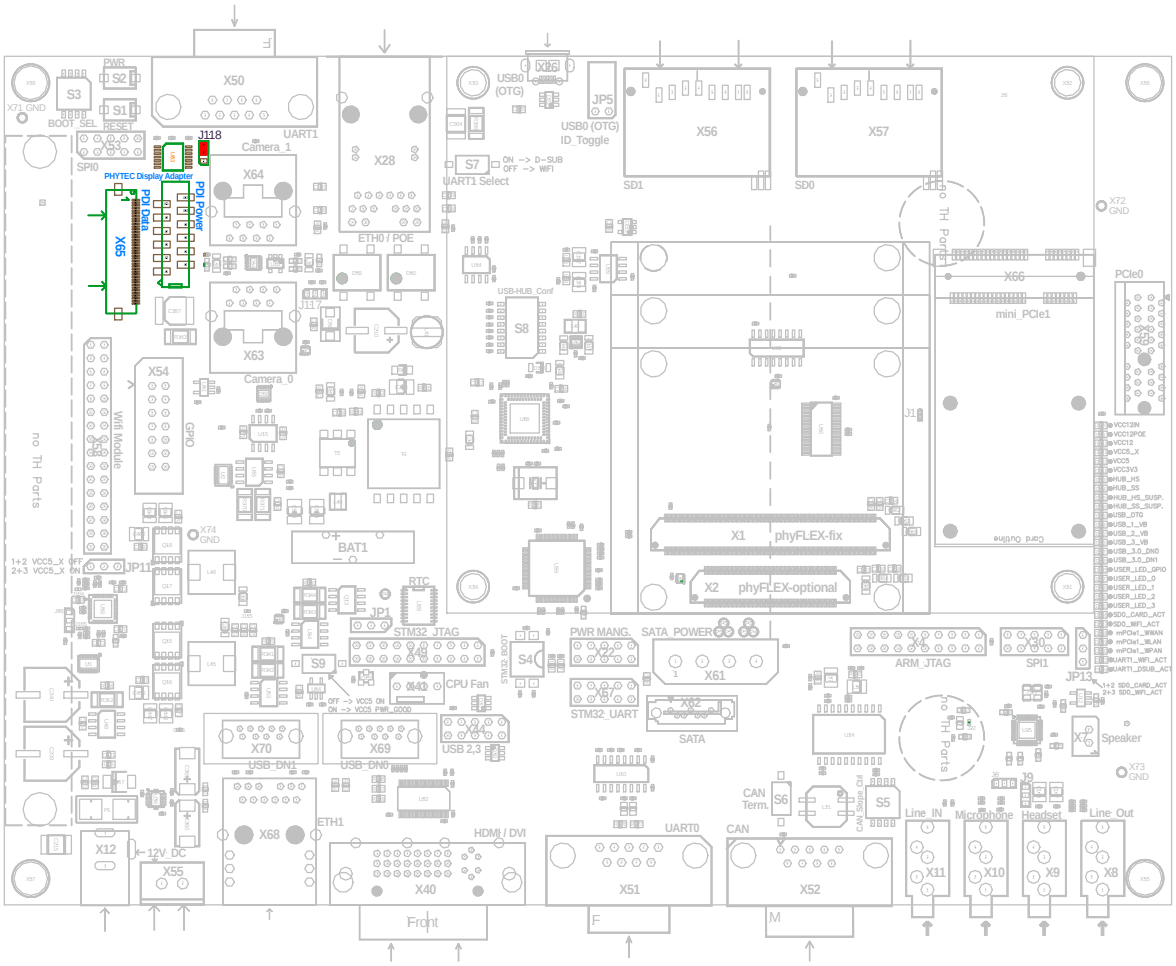


Figure 34: Phytec Display Interface (PDI) at Connector X65

The various performance classes of the phyFLEX family allow to attach a large number of different displays varying in resolution, signal level, type of the backlight, pinout, etc. In order not to limit the range of displays connectable to the phyFLEX, the phyFLEX carrier board has no special display connector suitable only for a small number of displays. The new concept intends the use of an adapter board (e.g. Phytec's LCD display adapters LCD-014, LCD-017 and LCD-018) to attach a special display, or display family to the phyFLEX. A new Phytec Display-Interface (PDI) was defined to connect the adapter board to the phyFLEX Carrier Board. It consists of two universal connectors which provide the connectivity for the display adapter. They allow easy adaption also to any customer display. One connector (40 pin FCC connector 0.5 mm pitch) at X65 is intend for connecting all data signals to the display adapter. It combines various interface signals like LVDS, USB, I^2C, etc. required to hook up a display. The second connector of the PDI (AMP microMatch 8-338069-2) at X65 provides all supply voltages needed to supply the display and a backlight, and the brightness control.

The following sections contain specific information on each connector.

19.3.8.1 Display Data Connector (X65)

PDI data connector X65 provides display data from the serial LVDS display interface of the phyFLEX-i.MX 6 (*section 12*).

In addition other useful interfaces such as USB, I²C, etc. are available at PDI data connector X65. *Table 61* lists all miscellaneous signals and gives detailed explanations. The following table shows the pin-out of the PDI's display data connectors at X65.

The display data connector at X65 is 40 pin FCC connector with 0.5 mm pitch.

Pin #	Signal name	ST	SL	Description
B1	SPI0_CLK_LCD	O	3.3 V	SPI 0 clock
B2	SPI0_MISO_LCD	I/O	3.3 V	SPI 0 master data in; slave data out
B3	SPI0_MOSI_LCD	O/I	3.3 V	SPI 0 master data out; slave data in
B4	SPI0_CS1_LCD	O	3.3 V	SPI 0 chip select display (SS2 of i.MX 6's eCSPI3 module)
B5	X_GPIO6	I	3.3 V	Display interrupt input (connects to GPIO7_12 of the i.MX 6)
B6	VCC3V3	O	3.3 V	Power supply display[38]
B7	X_I2C0_SCL	I/O	3.3 V	I²C clock signal
B8	X_I2C0_SDA	I/O	3.3 V	I²C data signal
B9	GND	-	-	Ground
B10	X_LVDS_DISP_BL_PWM	O	3.3 V	PWM brightness output
B11	VCC3V3	O	3.3 V	Logic supply voltage[1]
B12	X_nPM_ON/WAKEUP/OFF	I	3.3 V	Power on/off Button
B13	X_nLVDS_DISP_ENA	O	3.3 V	Display enable signal
B14	X_HW-Introspection	I/O	3.3 V	Hardware Introspection Interface **for internal use only**
B15	GND	-	-	Ground
B16	USB_DP_DN2	I/O	3.3 V	USB_DN2 data + (from USB hub at U66)
B17	USB_DM_DN2	I/O	3.3 V	USB_DN2 data -(from USB hub at U66)
B18	GND	-	-	Ground
B19	X_LVDS_L0-	O	3.3 V	LVDS data channel 0 negative output
B20	X_LVDS_L0+	O	3.3 V	LVDS data channel 0 positive output
B21	GND	-	-	Ground
B22	X_LVDS_L1-	O	3.3 V	LVDS data channel 1 negative output
B23	X_LVDS_L1+	O	3.3 V	LVDS data channel 1 positive output
B24	GND	-	-	Ground

Table 60: PDI Data Connector X65 Signal Description

[38]: Provided to supply any logic on the display adapter. Max. draw 100 mA

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Pin #	Signal name	ST	SL	Description
B25	X_LVDS_L2-	O	3.3 V	LVDS data channel 2 negative output
B26	X_LVDS_L2+	O	3.3 V	LVDS data channel 2 positive output
B27	GND	-	-	Ground
B28	X_LVDS_L3-	O	3.3 V	LVDS data channel 3 negative output
B29	X_LVDS_L3+	O	3.3 V	LVDS data channel 3 positive output
B30	GND	-	-	Ground
B31	X_LVDS_CLK-	O	3.3 V	LVDS clock channel negative output
B32	X_LVDS_CLK+	O	3.3 V	LVDS clock channel positive output
B33	GND	-	-	Ground
B34	TS_X+	I/O	3.3 V	Touch X+ (from touch panel controller at U6)
B35	TS_X-	I/O	3.3 V	Touch X- (from touch panel controller at U6)
B36	TS_Y+	I/O	3.3 V	Touch Y+ (from touch panel controller at U6)
B37	TS_Y-	I/O	3.3 V	Touch Y- (from touch panel controller at U6)
B38	NC	-	-	not connected
B39	GND	-	-	Ground
B40	LS_ANA	I	3.3 V	Light sensor analog input

Table 60: PDI Data Connector X65 Signal Description (continued)

The table below shows the auxiliary interfaces at display data connector X65.

Signal	Description
USBDN2	USB host interface derived form port 2 of the USB hub at U66. Suitable for optional features e.g. front USB.
I2C0	I²C interface for optional EEPROM, or other I²C devices
SPI0	SPI interface to connect optional SPI slave
1-WIRE	Hardware Introspection Interface **For internal use only**
X_nPM_ON/WAKEUP/OFF	Power on/off signal to allow for an ON/OFF switch on a front panel. It connects to the PWRON input of the CMIC on the phyFLEX-i.MX 6 and to the power management connector X22
X_nLVDS_DISP_ENA	Can be used to enable, or disable the display, or to shutdown the backlight.
X_LVDS_DISP_BL_PWM	PWM output to control the brightness of a display's backlight (0%=dark, 100%=bright).
LS_ANA	Analog light sensor input. The analog light sensor input at pin 40 extends to an 8-bit A/D converter (U7) which is connected to the I2C0 Bus at address 0x64. To get the maximum adjustment range the output voltage of an applicable light sensor should range from 0 V to VRef (VCC3V3).

Table 61: Auxiliary Interfaces at PDI Data Connector X65

All signals of the SPI interface at the display data connector are routed through a buffer at U63. Jumper J118 allows to switch the buffer into Three-State Output Mode that reduces supply current (*section 19.3.13* for more information).

19.3.8.2 Display Power Connector (X65)

The display power connector X65 (AMP microMatch 8-188275-2) provides all supply voltages needed to supply the display and a backlight.

Pin #	Signal name	ST	SL	Description
A1	GND	-		Ground
A2	VCC3V3	O	3.3 V	3.3 V power supply display
A3	GND	-		Ground
A4	VCC5	O	5 V	5V power supply display
A5	GND	-		Ground
A6	VCC5	O	5 V	5 V power supply display
A7	GND	-		Ground
A8	VCC5	O	5 V	5 V power supply display
A9	GND	-		Ground
A10	X_LVDS_DISP_BL_PWM	O	3.3 V	PWM brightness output
A11	VCC12	O	+12 V	Backlight power supply
A12	VCC12	O	+12 V	Backlight power supply

Table 62: PDI Power Connector X65 Signal Description

19.3.8.3 Touch Screen Connectivity

As many smaller applications need a touch screen as user interface, provisions are made to connect 4- wire resistive touch screens to the PDI data connector X65 (pins B34 - B37, *Table 60*). The signals from the touch screen panel are processed by a touch panel controller at U6. The touch panel controller is connected to I^2C bus I2C0 at address 0x41.

By changing jumper J12 (on the backside of the CB (*Figure 22*) the address can be set to 0x44 if needed (*Table 50*).

An additional interrupt output is connected to X_GPIO0 of the phyFLEX-i.MX 6 (X1A54 on the phyFLEX-fix Connector; GPIO5_08 of the i.MX 6).

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19.3.9 High-Definition Multimedia Interface (HDMI) (X40)

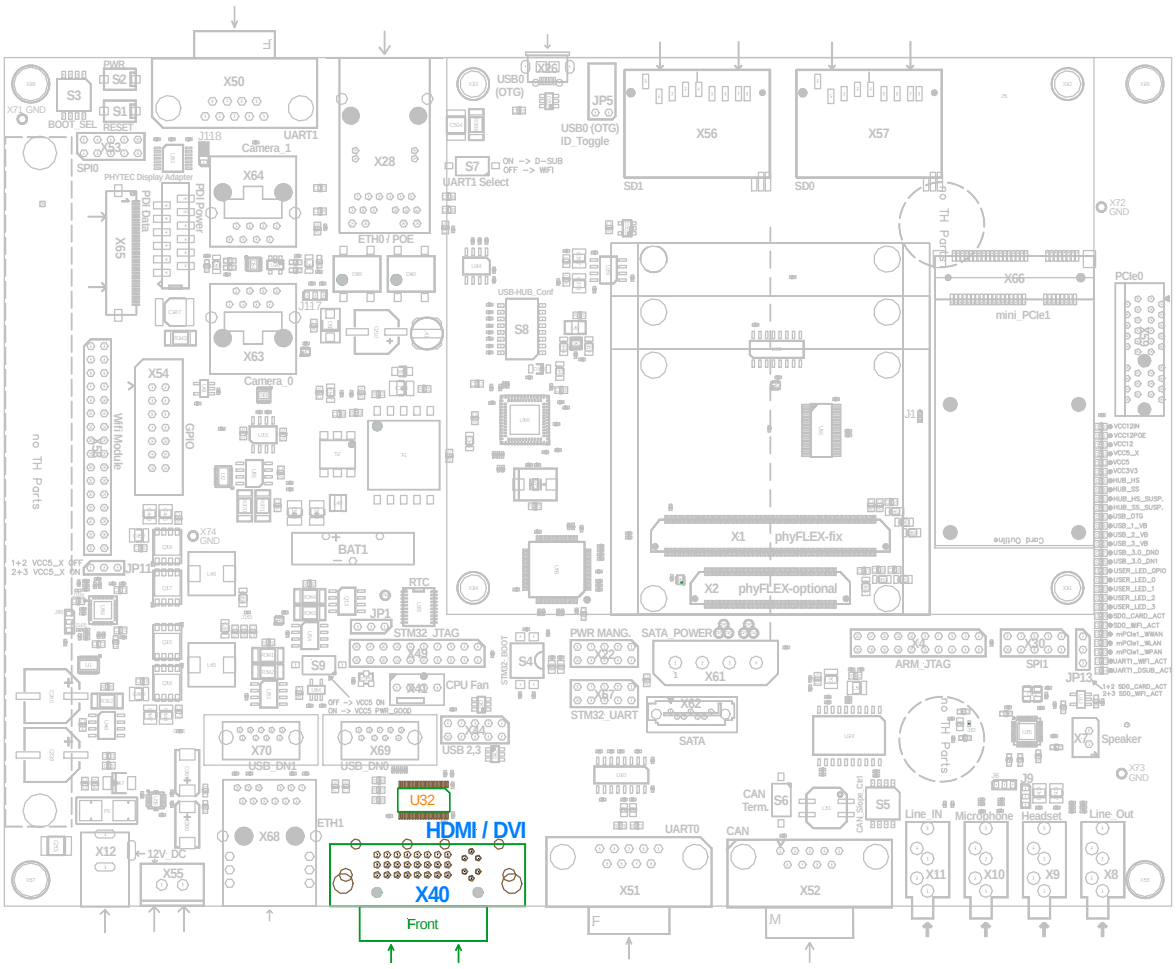


Figure 35: HDMI Interface at Connector X40

The High-Definition Multimedia Interface (HDMI) of the phyFLEX-i.MX 6 Module is compliant to HDMI 1.4, HDCP 1.4 and DVI 1.0. It supports a maximum pixel clock of 340 Mhz at a resolution of up to 1080p @ 60 Mhz and 720p/1080i @ 120 Mhz. Please refer to the *i.MX 6 Reference* Manual for more information. The HDMI interface brought out at a DVI female connector X40 on phyFLEX Carrier Board comprises the following signal groups: three pairs of data signals, one pair of clock signals, an I²C bus which is exclusively for the HDMI interface, and the hot plug detect (HPD) signal. Level shifters shift the I²C interface signals from I/O voltage (VCC3V3) to 5 V. All HDMI signals available at connector X40 extend from the phyFLEX-Connector to the DVI receptacle[39] via an HDMI transmitter port protection device at U32.

[39]: In contrast to HDMI connectors available the DVI receptacle on the phyFLEX Carrier Board is industrial-suited. Because of that and due to licensing restrictions only a DVI connector is provided, even though the phyFLEX-i.MX 6 supports HDMI.

Pin #	Signal name	ST	SL	Description
1	X_HDMI_TMDS_DATA2-	O	HDMI	HDMI data channel 2 negative output
2	X_HDMI_TMDS_DATA2+	O	HDMI	HDMI data channel 2 positive output
3	GND	-	-	Ground
4	NC	-	-	Not connected
5	NC	-	-	Not connected
6	X_HDMI_SCL	I/O	5 V	HDMI I²C clock signal
7	X_HDMI_SDA	I/O	5 V	HDMI I²C data signal
8	NC	-	-	Not connected
9	X_HDMI_TMDS_DATA1-	O	HDMI	HDMI data channel 1 negative output
10	X_HDMI_TMDS_DATA1+	O	HDMI	HDMI data channel 1 positive output
11	GND	-	-	Ground
12	NC	-	-	Not connected
13	NC	-	-	Not connected
14	V5_HDMI	O	5 V	5 V power supply
15	GND	-	-	Ground
16	X_nHDMI_HPD	I	5 V	HDMI hot plug detection
17	X_HDMI_TMDS_DATA0-	O	HDMI	HDMI data channel 0 negative output
18	X_HDMI_TMDS_DATA0+	O	HDMI	HDMI data channel 0 positive output
19	GND	-	-	Ground
20	NC	-	-	Not connected
21	NC	-	-	Not connected
22	GND	-	-	Ground
23	X_HDMI0_TMDS_CLOCK+	O	HDMI	HDMI clock positive output
24	X_HDMI0_TMDS_CLOCK-	O	HDMI	HDMI clock positive output
C1	NC	-	-	Not connected
C2	NC	-	-	Not connected
C3	NC	-	-	Not connected
C4	NC	-	-	Not connected
C5	NC	-	-	Not connected
S1	Shield	-	-	Shield
S2	Shield	-	-	Shield
S3	NC	-	-	Not connected
S4	NC	-	-	Not connected
S5	Shield	-	-	Shield
S6	Shield	-	-	Shield

Table 63: HDMI/DVI Connector X40 Pinout

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19.3.10 Camera Interface (X63, X64)

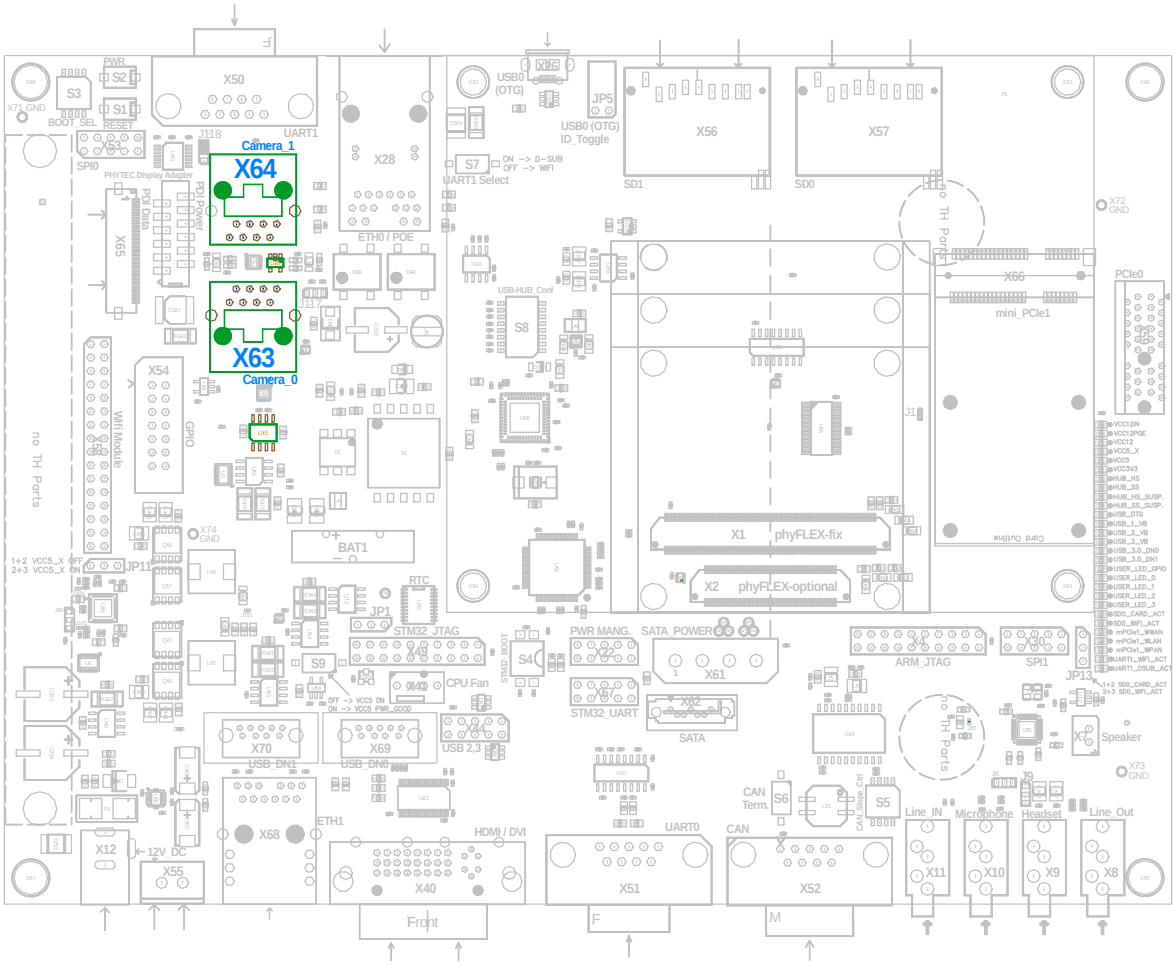


Figure 36: Camera Interface at Connector X63, X64

The phyFLEX-i.MX 6 provides three types of camera interfaces (parallel, LVDS, and MIPI/CSI-2).

On the target application the camera interfaces can thus be used to connect:

- camera modules with phyCAM-S(+) interface (*Figure 37* and *Figure 38*, circuitries "Camera_0, phyCAM-S+" and "Camera_1, phyCAM-S+" on the Phytec Carrier Board (PBA-B-01) schematic)
- camera modules with phyCAM-P interface (*Figure 39* and *Figure 40*, circuitries "Camera_0, phyCAM-P" and "Camera_1, phyCAM-P" circuitry on the Phytec Mapper Board FLM-A-XL1 schematic)
- customer camera modules with parallel interface (up to 20-Bit data) (*Figure 39* and *Figure 40*, circuitries "Camera_0, Auxiliary" and "Camera_1, Auxiliary" on the Phytec Mapper Board FLM-A-XL1 schematic)
- camera modules with MIPI/CSI-2 interface (circuitry "Camera_2, CSI-2 (MIPI)" on the Phytec Mapper Board FLM-A-XL1 schematic)

Based on the Phytec Carrier and Mapper Board (PBA-B-01 and FLM-A-XL1) the following sections give a basic overview on how to connect a camera using the different interface options. All figures show the phyFLEX-i.MX 6 equipped with the i.MX 6 dual and quad core with two parallel interfaces. Details on the position of the signals on the phyFLEX Connector and further technical details can be found in section *14.1 ff.*

19.3.10.1 phyCAM-S(+) (LVDS) Camera Interfaces on the phyFLEX Carrier Board

Camera_0 (connected to IPU1_CSI0) as phyCAM-S(+)

The 1-channel 10-Bit LVDS random lock deserializer (U27) on the phyFLEX-i.MX 6 is connected to the i.MX 6's camera sensor interfaces CSI0 of IPU#1. The LVDS deserializer converts the LVDS Signals received at the RJ45 socket X63 on the carrier board to a 10-bit wide parallel data signal and separate clock. The camera interface is compatible with the Phytec phyCAM-S+ camera interface standard. *Figure 37* depicts the signal path.

The table below shows the pinout of connector X63:

Pin #	Signal Name	Description
1	X_CAMERA0_L0+	LVDS Input+
2	X_CAMERA0_L0-	LVDS Input-
3	Camera0_RXCLK-	LVDS Clock-
4	I2C_SDA_CAMERA	I^2C Data
5	I2C_SCL_CAMERA	I^2C Clock
6	Camera0_RXCLK +	LVDS Clock+
7	VCC_CAMERA0	Power supply camera (3.3 V)
8	GND	Ground

Table 64: Phytec phyCAM-S+ Camera Connector X63

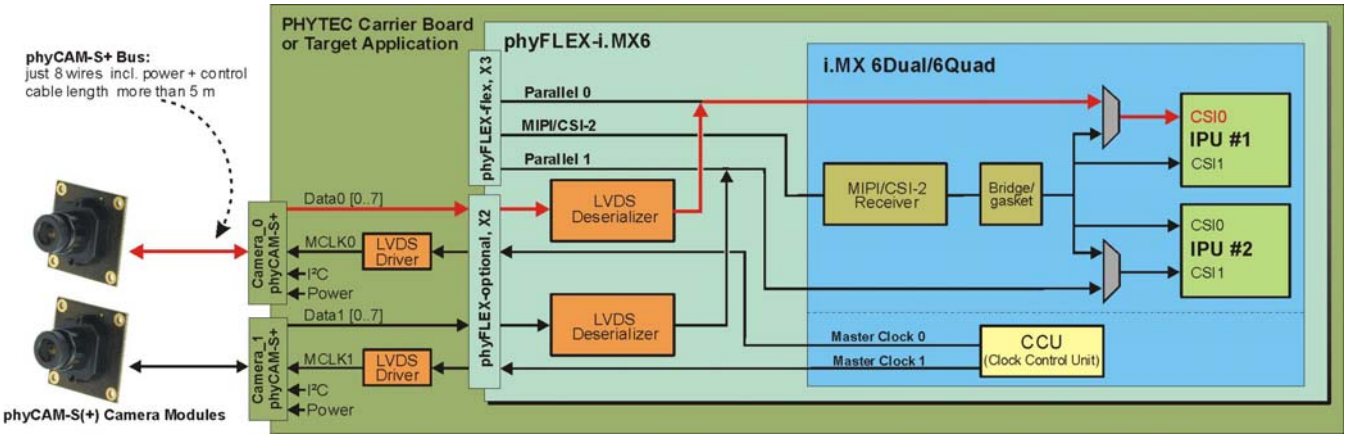


Figure 37: Use of Camera_0 (CSI0 of IPU#1) as phyCAM-S+ Interface

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Camera_1 (connected to IPU2_CSI1) as phyCAM-S(+)

The 1-channel 10-Bit LVDS random lock deserializer (U12) on the phyFLEX-i.MX 6 is connected to the i.MX 6's camera sensor interfaces CSI1 of IPU#2. The LVDS deserializer converts the LVDS Signals received at the RJ45 socket X64 on the carrier board to a 10-bit wide parallel data signal and separate clock. The camera interface is compatible with the Phytec phyCAM-S+ camera interface standard. *Figure 38* depicts the signal path.

The following table shows the pinout of connector X64:

Pin #	Signal Name	Description
1	X_CAMERA1_L0+	LVDS Input+
2	X_CAMERA1_L0-	LVDS Input-
3	Camera0_RXCLK-	LVDS Clock-
4	I2C_SDA_CAMERA	I^2C Data
5	I2C_SCL_CAMERA	I^2C Clock
6	Camera1_RXCLK +	LVDS Clock+
7	VCC_CAMERA1	Power supply camera (3.3 V)
8	GND	Ground

Table 65: Phytec phyCAM-S+ Camera Connector X64

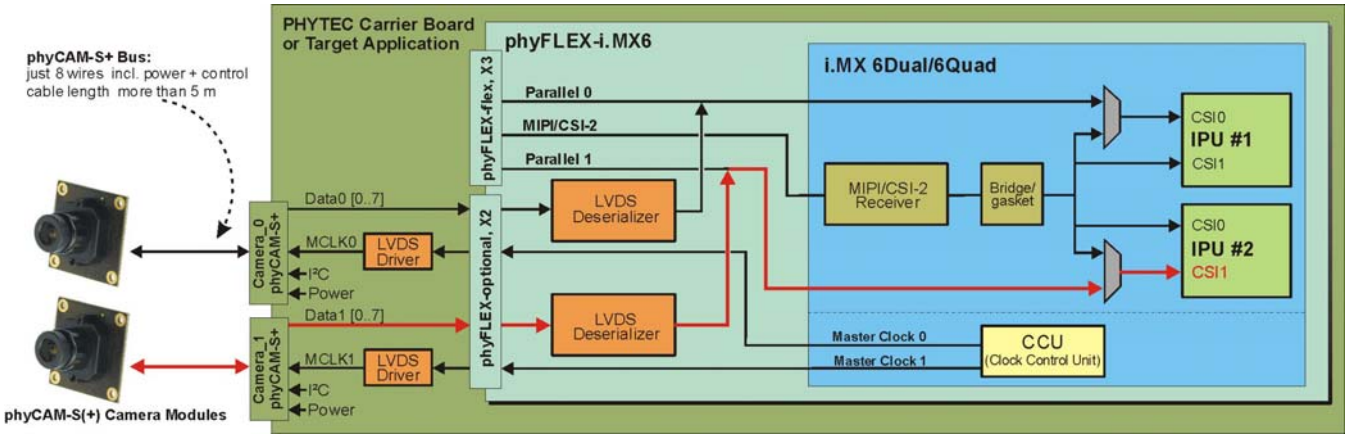


Figure 38: Use of Camera_1 (CSI1 of IPU#2) as phyCAM-S+ Interface

19.3.10.2 phyCAM-P or Parallel Camera Interfaces on the phyFLEX Mapper Board

Camera_0 (connected to IPU1_CSI0) as phyCAM-P, or parallel interface

The Parallel 0 camera interface of the i.MX 6 connects to CSI0 of IPU#1 (*Figure 11* and *Figure 12*). It is brought out as parallel interface on the phyFLEX-flex connector X3. The phyFLEX Mapper Board[40] (FLM-A-XL1) allows to connect either camera modules with phyCAM-P interface at connector X5 (33-pin FPC-connector, 0.5 mm pitch), or custom camera modules with parallel interface (up to 18-Bit data) at auxiliary connector X3 (2x20-pin header connector; 2.0 mm pitch). *Figure 39* depicts the signal path.

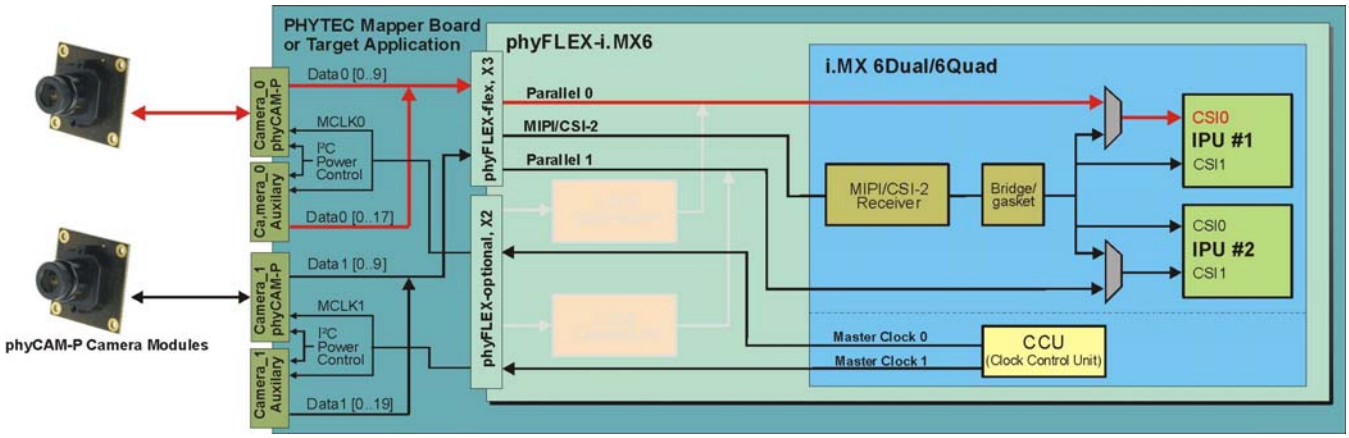


Figure 39: Use of Camera_0 (CSI0 of IPU#1) as phyCAM-P Interface, or Customized

Camera_1[41] (connected to IPU2_CSI1) as phyCAM-P, or parallel interface

The Parallel 1 camera interface of the i.MX 6 connects to CSI1 of IPU#2 (*Figure 11* and *Figure 12*). It is brought out as parallel interface on the phyFLEX-flex connector X3. The phyFLEX Mapper Board (FLM-A-XL1) allows to connect either camera modules with phyCAM-P interface at connector X6 (33-pin FPC-connector, 0.5 mm pitch), or custom camera modules with parallel interface (up to 20-Bit data) at auxiliary connector X4 (2x20-pin header connector; 2.0 mm pitch). *Figure 40* depicts the signal path.

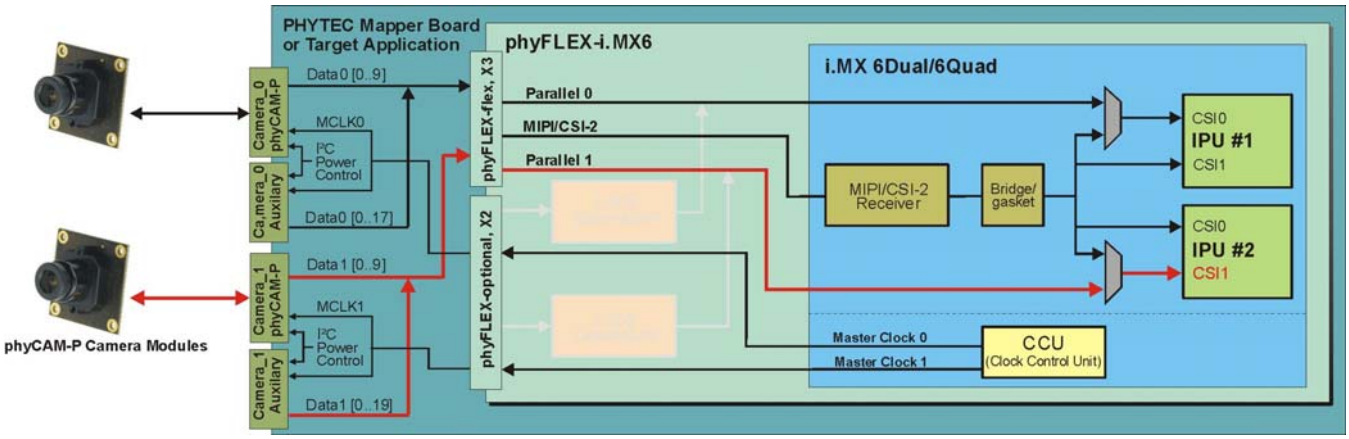


Figure 40: Use of Camera_1 (CSI1 of IPU#2) as phyCAM-P Interface, or Customized

[40]: The Phytec Mapper Board (FLM-A-XL1) is not included in all kits. Pleas contact our sales team for more information.
[41]: Only i.MX 6 with Dual-. or Quad core. i.MX 6 with Solo-, or DualLite core provide only one parallel camera interface and one IPU.

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Note:

- Simultaneously connecting a phyCAM-P and a phyCAM-S+ camera to one of the interfaces Camera_0, or Camera_1 is not possible. Selection of either phyCAM-P or phyCAM-S+ as interface type can be done in the *config* file.
- For more information on the Phytec camera interfaces phyCAM-P and phyCAM-S(+) refer also to the documentation delivered with the camera module (L-748d_x " phyCAM-P / phyCAM-S, digitale Kameraboards").

19.3.10.3 MIPI/CSI-2 (Camera_2) Interface on the phyFLEX Mapper Board

The MIPI CSI-2 camera interface is also available at the connectors of the phyFLEX-i.MX 6. It can be used alternatively to connect camera sensors with MIPI/CSI-2 interface. The phyFLEX Mapper Board[42] (FLM-A-XL1) allows to connect camera modules with MIPI/CSI-2 interface (with up to 4 data lanes and one clock) at connector X13 (30-pinMolex connector, 0.5 mm pitch).

Note:
Depending on the configuration of the CSI2IPU Bridge/gasket and the internal multiplexer(s) Camera_0 and/or Camera_1 are not available if one, or more MIPI compliant sensors are connected to the Camera_2 connector of the mapper.

[42]: The Phytec Mapper Board (FLM-A-XL1) is not included in all kits. Pleas contact our sales team for more information.

19.3.11 Audio Interface (X7, X8, X9, X10, X11)

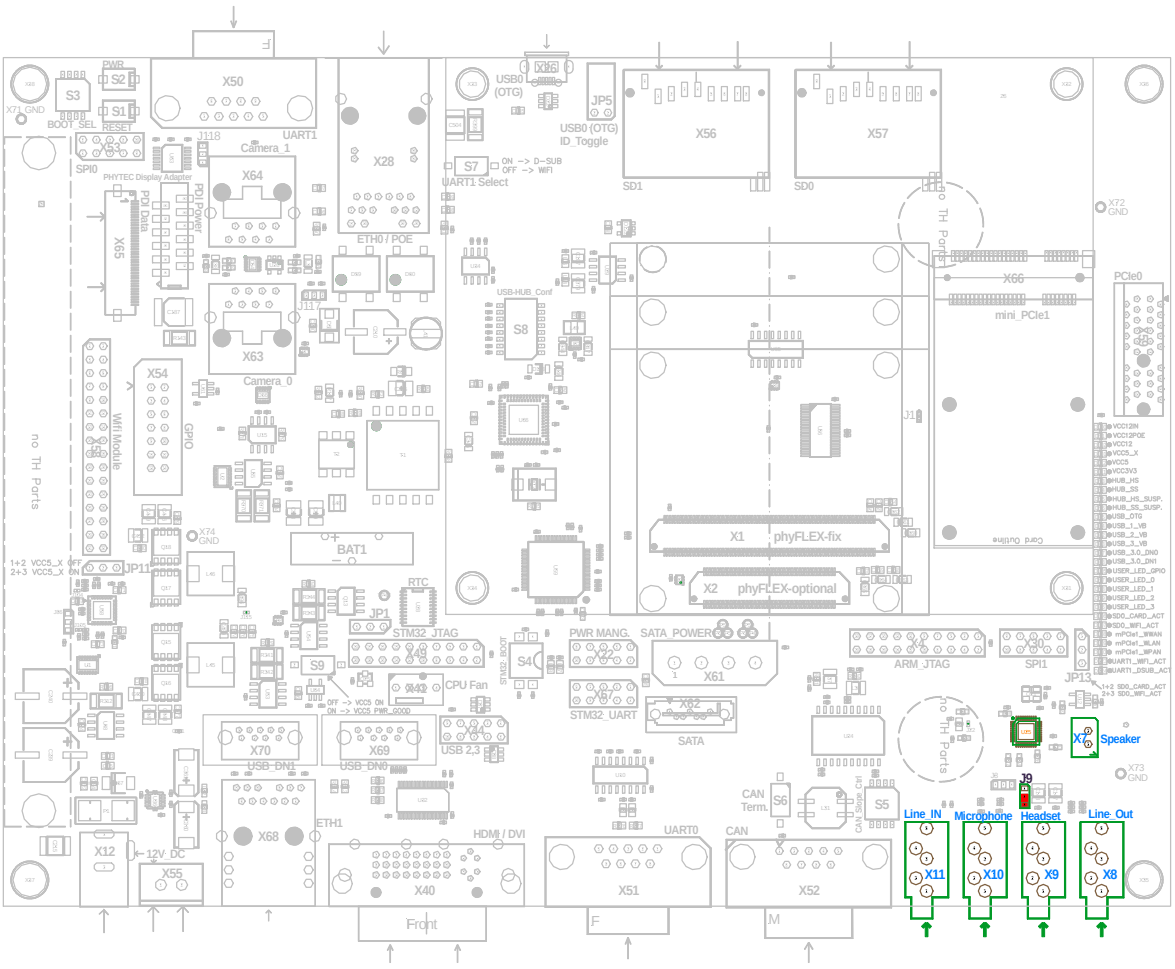


Figure 41: Audio Interface at Connectors X7, X8, X9, X10, X11

The audio interface provides a method of exploring the phyFLEX-i.MX 6 I²S capabilities. The phyFLEX Carrier Board is populated with a low-power stereo audio codec with integrated mono class-d amplifier at U25. It provides a High Performance Audio DAC and ADC with sample rates from 8 kHz to 96 kHz. It supports a stereo line input, stereo microphone input, stereo line output, stereo headphone output and direct speaker output.

The audio codec is interfaced to the phyFLEX-i.MX 6 via I²S interface for audio data and the I2C0 interface for codec configuration (I²C address 0x18). Audio devices can be connected to 3.5 mm audio jacks at X8, X9, X10 and X11. A detailed list of applicable connectors is presented below. The pin header connector at X7 allows for direct connection of a Mono Class-D 1W BTL 8 Ohm Speaker.

Audio Outputs:

X8 – Line Output
X9 – Headset Output
X7 – Speaker Output

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Audio Inputs:

X10 – Microphone In
X11 – Line In

Please refer to the audio codec's reference manual for additional information regarding the special interface specification.

The audio codec's master clock of 19.2 MHz will be generated at OZ1 on the carrier board.

The microphone input (X10) and the headset output (X9) allow jack detection. The jack detection of the microphone input is hardwired, while jack detection of the headset output can be disabled by jumper J9. In default position (2+3) jumper J9 connects the shield contact of audio jack X9 (headset out) to the HPCOM output driver of the stereo audio codec at U25. In this configuration jack detection is enabled. Connecting the shield contact to GND (J9 at 1+2) disables the jack detection function.

19.3.12 I²C Connectivity

The carrier board provides two I²C buses (I2C0 and I2C1). These are available at different connectors on the phyFLEX Carrier Board.

The following table provides a list of the connectors and pins with I²C connectivity.

Connector	Location
Camera interface X63	pin 4 (I2C_SDA_CAMERA); pin 5 (I2C_SCL_CAMERA) derived from I2C1
Camera interface X64	pin 4 (I2C_SDA_CAMERA); pin 5 (I2C_SCL_CAMERA) derived from I2C1
Display data connector X65	pin B8 (X_I2C0_SDA); pin B7 (X_I2C0_SCL) derived from I2C0

Table 66: I²C Connectivity

On the carrier board only I2C0 is used for the different devices. To avoid any conflicts when connecting external I²C devices to the phyFLEX Carrier Board at PDI data connector X65 the addresses of the on-board I²C devices must be considered. Some of the addresses can be configured by jumper. *Table 67* lists the addresses already in use.

Caution!

The use and availability of the I²C interfaces on the phyFLEX-Carrier Board are closely linked to the use of the I²C bus on the phyFLEX SOM. Because of that this section describes the I²C interfaces only in connection with the use of the phyFLEX-i.MX 6. Use of other phyFLEX SOMs might e.g. require to consider the I²C addresses of the SOMs I²C devices, too.

Device (on the Carrier Board)	Address used I2C0 (7 MSB)	Jumper
RTC (U28)	0x51	
A/D converter (U7)	0x64	
Touch screen controller (U6)	0x41 (Switchable to 0x44)	J12
Audio Controller (U25)	0x18	
LED dimmer (U52)	0x62	

Table 67: I2C0 Addresses in Use

No device on the carrier board connects to I2C1. Hence, I2C1 is fully available for connecting external I²C devices to connectors X63 and X64.

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19.3.13 SPI Connectivity (X30, X53, X65)

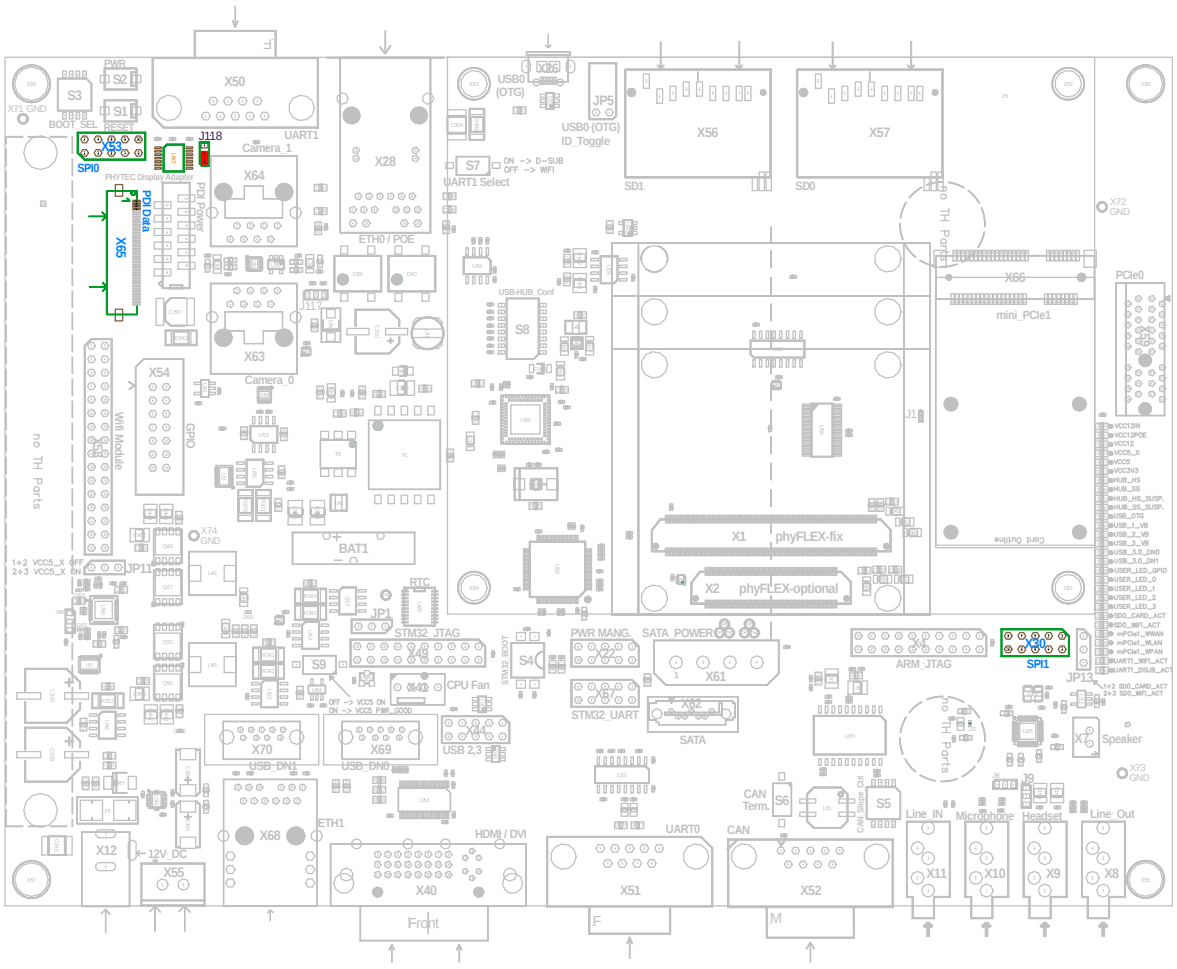


Figure 42: SPI Connectivity at Connectors X30, X53 and X65

The carrier board supports connectivity to both SPI Interfaces of the phyFLEX module.

The SPI0 interface is available at the SPI0 pin header connector X53, and display data connector X65. All signals of the SPI interface at the display data connector are routed through a buffer at U63. Jumper J118 allows to switch the buffer into Three-State Output Mode that reduces supply current (*Table 70*).

The phyFLEX-i.MX 6 supports the 3 slave select signals X_SPI0_CSBOOT, X_SPI_CS0, and X_SPI0_CS1 (*section 8.6*). X_SPI0_CSBOOT is reserved to address the SPI Flash on the module and is not available on the carrier board.

Connector	Location
PDI data connector X65	pin B1 (SPI0_CLK_LCD); pin B2 (SPI0_MISO_LCD); pin B3 (SPI0_MOSI_LCD); pin B4 (SPI0_CS1_LCD), all signals routed through buffer U63
SPI0 pin header connector X53	see *Table 69*

Table 68: SPI0 Connector Selection

Pin	ST	SL	Description
1	NC	-	not connected
2	NC	-	not connected
3	NC	-	not connected
4	O	3.3 V	X_SPI0_CS0 (SS1 of i.MX 6's eCSPI3 module)
5	O	3.3 V	X_SPI0_CS1 (SS2 of i.MX 6's eCSPI3 module)
6	I	3.3 V	X_SPI0_MISO
7	O	3.3 V	X_SPI0_MOSI
8	O	3.3 V	X_SPI0_CLK
9	-	GND	Ground
10	O	3.3 V	VREF_SPI0

Table 69: SPI0 Pin Header X53 Pinout

SPI Buffer Mode of Operation	J118
Three-State Output Mode enabled	1 + 2
normal operation	**2 + 3**

Table 70: SPI Buffer U63 Mode of Operation

The second SPI1 interface is available with two chip selects at pin header connector X30.

Pin	ST	SL	Description
1	NC	-	not connected
2	NC	-	not connected
3	NC	-	not connected
4	O	3.3 V	X_SPI1_CS1 (SS1 of i.MX 6's eCSPI5 module)
5	O	3.3 V	X_SPI1_CS0 (SS0 of i.MX 6's eCSPI5 module)
6	I	3.3 V	X_SPI1_MISO
7	O	3.3 V	X_SPI1_MOSI
8	O	3.3 V	X_SPI1_CLK
9	-	GND	Ground
10	O	3.3 V	VREF_SPI1

Table 71: SPI1 Pin Header X30 Pinout

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19.3.14 User programmable GPIOs (X54)

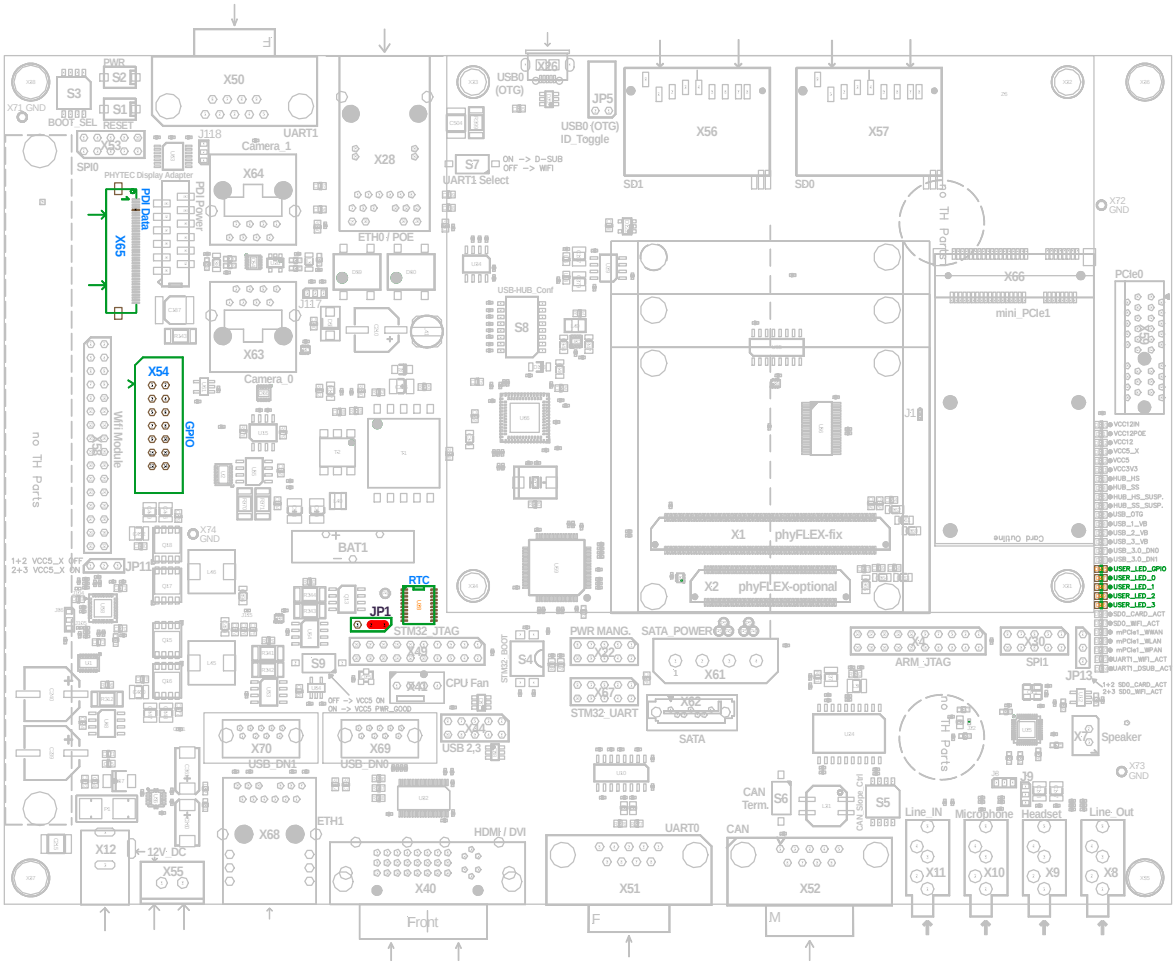


Figure 43: User programmable GPIOs and LEDs

The phyFLEX-i.MX 6 provides 11 GPIOs. All GPIOs are ports of the i.MX 6 (*section 9*). Some GPIOs are reserved for special functions on the phyFLEX Carrier Board. All GPIOs are also mapped at GPIO Connector X54. See *Table 72* which function each GPIO has.

GPIO	Function
GPIO0	Interrupt Touch Controller at U6
GPIO5	If JP1 is connected between pin 2 and 3, signal RTC_INT is connected to X_GPIO5
GPIO6	SPI_IRQ at PDI data connector X65 (pin B5)
GPIO10	Connected to User LED D105

Table 72: GPIOs used on the phyFLEX Carrier Board

Pin	ST	SL	Description
1	-	3.3 V	VREF_GPIO
2	I/O	3.3 V	X_GPIO0
3	I/O	3.3 V	X_GPIO1
4	I/O	3.3 V	X_GPIO2
5	I/O	3.3 V	X_GPIO3
6	I/O	3.3 V	X_GPIO4
7	I/O	3.3 V	X_GPIO5
8	I/O	3.3 V	X_GPIO6
9	I/O	3.3 V	X_GPIO7
10	I/O	3.3 V	X_GPIO8
11	I/O	3.3 V	X_GPIO9
12	I/O	3.3 V	X_GPIO10
13	-	GND	Ground
14	-	GND	Ground

Table 73: GPIO Pin Header X54 Pinout

19.3.15 User programmable LEDs

The phyFLEX Carrier Board provides 5 user programmable LEDs.

LED D105, is directly connected to GPIO10 of the phyFLEX-i.MX 6 (pin X1A67). A logic 1 at X_GPIO10 turns the LED on (*section 9*).

The other user programmable LEDs (D86, D97-D99) are controlled by a 4-bit LED dimmer at U52 (at the backside of the CB) which is connected to I2C0 at address 0x62.

The following table lists all user programmable LEDs.

LED	Color	Description
D105	green	User LED connected to GPIO10 (GPIO2_24 of the i.MX 6)
D97	red	User LED0 (port LED0 from 4-bit LED dimmer at U52)
D98	yellow	User LED1 (port LED1 from 4-bit LED dimmer at U52)
D99	yellow	User LED2 (port LED2 from 4-bit LED dimmer at U52)
D86	green	User LED3(port LED3 from 4-bit LED dimmer at U52)

Table 74: User Programmable LEDs on the Carrier Board

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19.3.16 Secure Digital Memory Card/ MultiMedia Card (X57, X56)

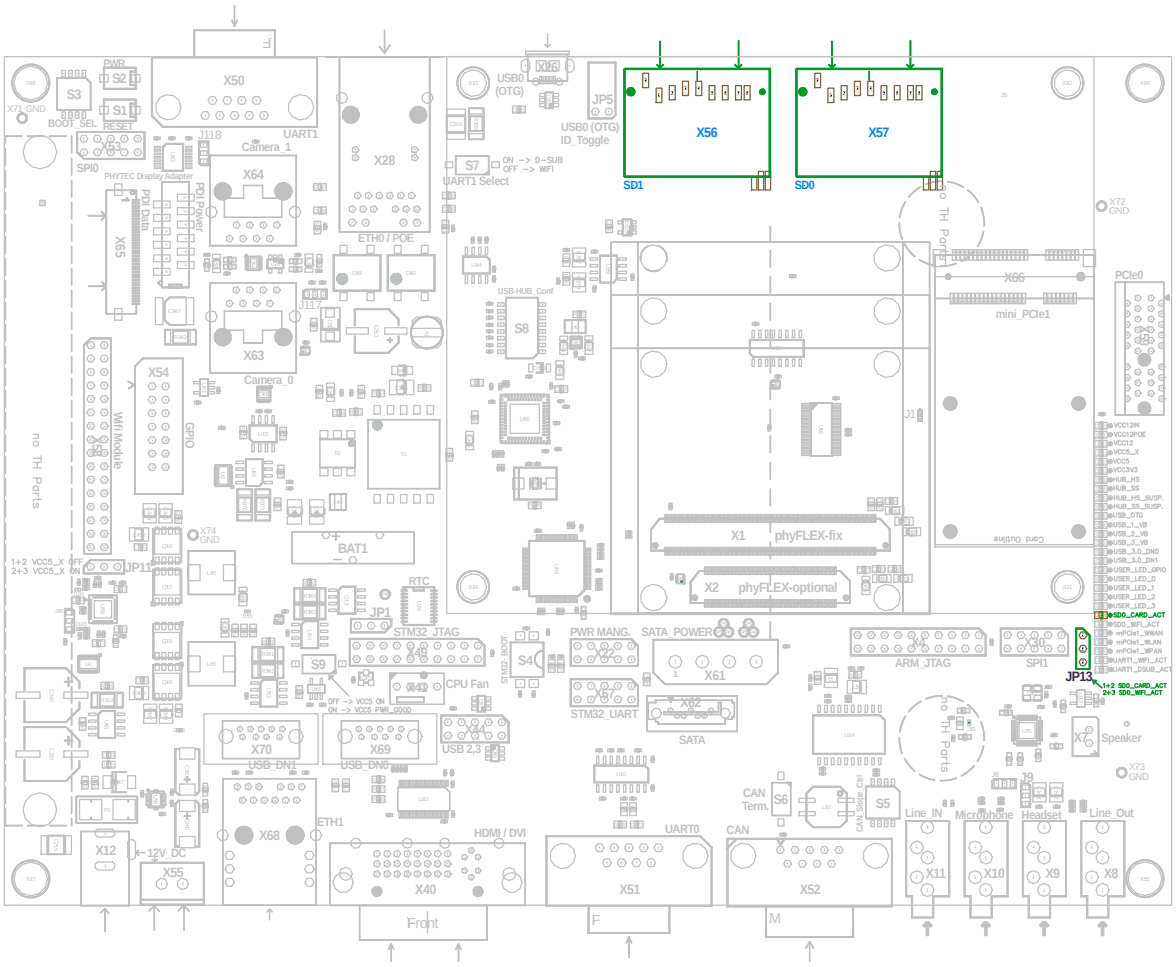


Figure 44: SD / MM Card Interfaces at Connector X57 and X56

The phyFLEX Carrier Board provides two standard SDHC card slots at X57 and X56 for connection to SD/MM cards. It allows easy and convenient connection to peripheral devices like SD- and MM cards. Power to the SD interface is supplied by inserting the appropriate card into the SD/MMC slot.

SD0 at X57 shares the SDIO signals with the Wi-Fi/Bluetooth connector X58. To use the SD0 card slot at X57, JP13 must be closed at 1 and 2. LED D106 shows that card slot SD0 (X57) is active.

SD/MMC slot X56 (SD1) is connected directly to the SD/MM card interface of the phyFLEX-i.MX 6 (*section 7*).

19.3.17 PCIe Connectivity (X59)

The phyFLEX Carrier Board provides one PCIe x1 lane at X59. PCIe0 of the phyFLEX-i.MX 6 is available at this connector.

Pin #	Signal name	ST	SL	Description
A1	GND	-	-	Hot plug presence detect connected to ground
B1	VCC12	PWR_O	12 V	12 V supply voltage output
A2	VCC12	PWR_O	12 V	12 V supply voltage output
B2	VCC12	PWR_O	12 V	12 V supply voltage output
A3	VCC12	PWR_O	12 V	12 V supply voltage output
B3	NC	-	-	Not connected
A4	GND	-	-	Ground
B4	GND	-	-	Ground
A5	NC	-	-	Not connected
B5	NC	-	-	Not connected
A6	NC	-	-	Not connected
B6	NC	-	-	Not connected
A7	NC	-	-	Not connected
B7	GND	-	-	Ground
A8	NC	-	-	Not connected
B8	VCC3V3	PWR_O	3.3 V	3.3 V supply voltage output
A9	VCC3V3	PWR_O	3.3 V	3.3 V supply voltage output
B9	NC	-	-	Not connected
A10	VCC3V3	PWR_O	3.3 V	3.3 V supply voltage output
B10	VCC3V3	PWR_O	3.3 V	3.3 V supply voltage output
A11	X_nPCIe0_PERST or X_nPM_RESET_OUT	O	3.3 V	Power Good, either global reset signal X_nPM_RESET_OUT or reset signal specifically dedicated to the PCIe0 interface (jumper J116)
B11		I/O	3.3 V	PCIe0 wake signal (low active) (GPIO1_7 of i.MX 6)
A12	GND	-	-	Ground
B12	NC	-	-	Not connected
A13	PCIe1_CLK+	PCIe_O		Reference clock lane+
B13	GND	-	-	Ground

Table 75: PCIe0 Connector X59

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Pin #	Signal name	ST	SL	Description
A14	PCIe1_CLK-	PCIe_O		Reference clock lane-
B14	X_PCIe0_TX+	PCIe_O		PCIe0 transmit lane+
A15	GND	-	-	Ground
B15	X_PCIe0_TX-	PCIe_O		PCIe0 transmit lane-
A16	X_PCIe0_RX+	PCIe_I		PCIe0 receive lane+
B16	GND	-	-	Ground
A17	X_PCIe0_RX-	PCIe_I		PCIe0 receive lane-
B17	X_PCIe0_nPRSNT	I/O		Hot plug detect signal (low active) (GPIO1_21 of i.MX 6)
A18	GND	-	-	Ground
B18	GND	-	-	Ground

Table 75: PCIe0 Connector X59 (continued)

Jumper J116 connects either the global reset signal X_nPM_RESET_OUT to the Power Good output of PCIe connector X59 (J116: 1+2), or a reset signal specifically dedicated to the PCIe0 interface available from the phyFLEX-i.MX 6 (default, J116: 2+3).

19.3.18 SATA (X62, X61)

The phyFLEX Carrier Board provides the possibility to directly connect an SATA hard disk drive. There are two connectors provided. The first connector (X62) is a Foxconn LD1807F-S51P and dedicated for data signals. The second connector (X61) is Molex Disk Drive Connector and dedicated for power supply of the hard disk drive (*Figure 19*).

Pin #	Signal name	ST	SL	Description
S1	GND	-	-	Shield1
S2	GND	-	-	Shield2
1	GND	-	-	Ground
2	X_SATA0_TX+	LVDS_O		SATA transmit lane+
3	X_SATA0_TX-	LVDS_O		SATA transmit lane-
4	GND	-	-	Ground
5	X_SATA0_RX-	LVDS_I		SATA receive lane-
6	X_SATA0_RX+	LVDS_I		SATA receive lane+
7	GND	-	-	Ground

Table 76: SATA Data Connector X62

Pin #	Signal name	ST	SL	Description
S1	VCC12	PWR_O	12 V	12 V supply voltage output
S2	GND	-	-	Ground
1	GND	-	-	Ground
2	VCC5	PWR_O	5 V	5 V supply voltage output

Table 77: Molex Disk Power Connector X61

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19.3.19 CPU Fan Connector (X41)

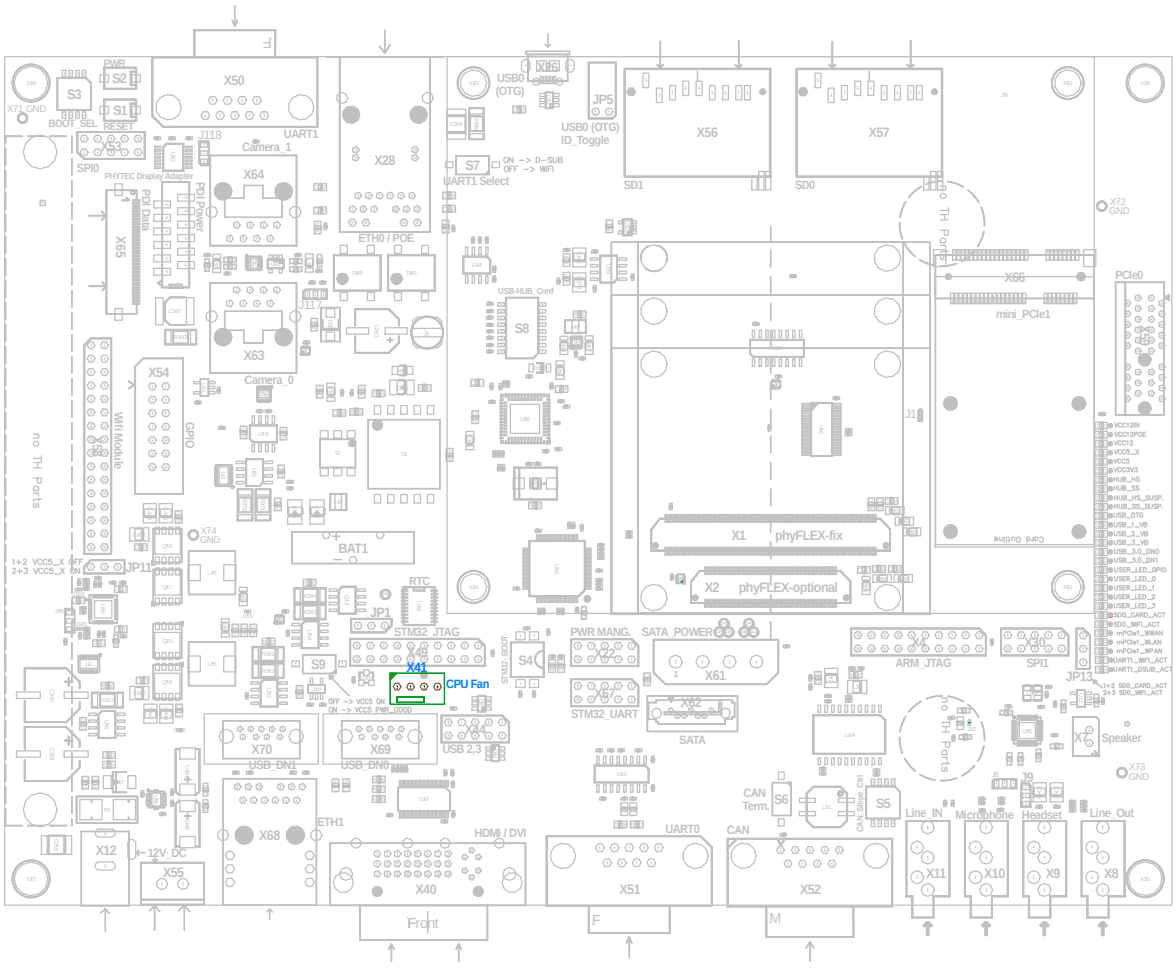


Figure 45: CPU Fan Connector X41

The carrier board supports the direct connection of a standard CPU fan with speed control at X41.

Pin #	Signal name	ST	SL	Description
1	GND	-	-	Ground
2	VCC12	PWR_O	12 V	12 V supply voltage output
3	X_PM_TACHO	OC	-	Fan tacho input
4	X_PM_PWM	OC	-	Fan PWM output

Table 78: CPU Fan Connector X41

Note:
The signals for CPU fan control are generated from the EMIC (U19) on the phyFLEX-i.MX 6 which requires custom specific programming (*section 16*).

19.3.20 Wi-Fi/Bluetooth Connector (X58)

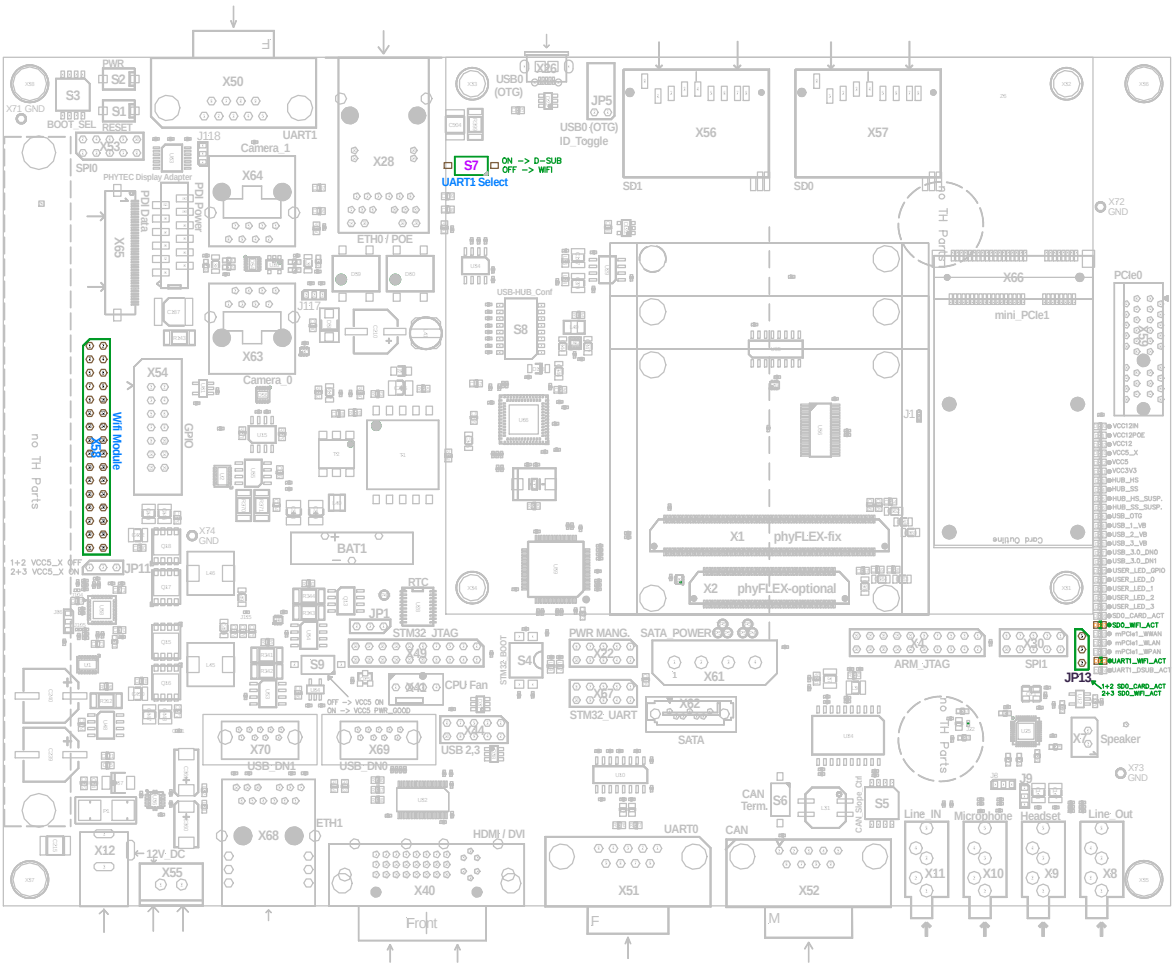


Figure 46: Wi-Fi/Bluetooth Connector X58

A Wi-Fi/Bluetooth module, such as the Phytec PCM-958, can connect to the carrier board's pin header at X58.

Two different interfaces (UART1 and SD0) connect to the Wi-Fi/Bluetooth module.

To provide the TTL signals of UART1 at the Wi-Fi/Bluetooth connector X58 DIP switch S7 must be open. LED D123 (yellow) indicates that UART1 is available at connector X58.

Use of SDIO for Wi-Fi/Bluetooth requires JP13 to be switched from position 1+2 to 2+3. LED D107 (yellow) indicates that SDIO is available at connector X58. *Table 79* shows the pinout of connector X58.

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Pin #	Signal name	ST	SL	Description
1	NC	-	-	Not connected
2	GND	-	-	Ground
3	NC	-	-	Not connected
4	VCC1V8	PWR_O	1.8 V	1.8 V supply voltage output
5	NC	-	-	Not connected
6	VCC1V8	PWR_O	1.8 V	1.8 V supply voltage output
7	GND	-	-	Ground
8	GND	-	-	Ground
9	UART1_TXD_WIFI	O	3.3 V	UART1 serial transmit signal (TTL)
10	VREF_SD0	REF_O	3.3 V	3.3 V SD0 reference voltage
11	UART1_RTS_WIFI	O	3.3 V	UART1 request to send (TTL)
12	VREF_SD0	REF_O	3.3 V	3.3 V SD0 reference voltage
13	SD0_D5_WLAN	I/O	3.3 V	SD0 data 5
14	VCC3V3	PWR_O	3.3 V	3.3 V supply voltage output
15	GND	-	-	Ground
16	VCC3V3	PWR_O	3.3 V	3.3 V supply voltage output
17	SD0_D4_WLAN	I/O	3.3 V	SD0 data 4
18	GND	-	-	Ground
19	SD0_D6_WLAN	I/O	3.3 V	SD0 data 6
20	NC	-	-	Not connected
21	SD0_D3_WLAN	I/O	3.3 V	SD0 data 3
22	UART1_RXD_WIFI	I	3.3 V	UART1 serial data receive signal (TTL)
23	GND	-	-	Ground
24	UART1_CTS_WIFI	I	3.3 V	UART1 clear to send (TTL)
25	SD0_D2_WLAN	I/O	3.3 V	SD0 data 2
26	GND	-	-	Ground
27	SD0_D1_WLAN	I/O	3.3 V	SD0 data 1
28	SD0_D7_WLAN	I/O	3.3 V	SD0 data 7
29	SD0_D0_WLAN	I/O	3.3 V	SD0 data 0
30	SD0_CMD_WLAN	O	3.3 V	SD0 command
31	GND	-	-	Ground
32	SD0_CLK_WLAN	O	3.3 V	SD0

Table 79: Wi-Fi/Bluetooth Connector X58

19.3.21 Boot Mode Selection (S3)

The boot mode DIP Switch S3 (*Figure 19*) is provided to configure the boot mode of the phyFLEX-i.MX 6 after reset. This DIP Switch allows choosing different boot sources. The following table gives an overview of the different boot sources. Refer to *sections 4.5* and *5* for more information on the boot configuration.

Note:
The following table describes only settings suitable for the phyFLEX-i.MX 6. Other settings must not be used with the phyFLEX-i.MX 6. Please refer to *Table 10* for information on the standard boot options according to the phyFLEX specification.

Caution!
The boot signals are equipped with pull-up resistors on the phyFLEX module, thus the standard signal level is high (OFF position of DIP switch S3). In order to pull a particular signal low the corresponding switch of DIP switch S3 must be set to the ON position.

Boot Mode	X_BOOT2 (S3_3)	X_BOOT1 (S3_2)	X_BOOT0 (S3_1)	BOOT Source
0	**1 (OFF)**	**1 (OFF)**	**1 (OFF)**	**NAND**
1	1 (OFF)	1 (OFF)	0 (ON)	SPI3, CS0 (on board SPI Flash if populated)
2	1 (OFF)	0 (ON)	1 (OFF)	
3	1 (OFF)	0 (ON)	0 (ON)	SD0 external
4	0 (ON)	1 (OFF)	1 (OFF)	Serial USB OTG (USB0, same as mode 6)
5	0 (ON)	1 (OFF)	0 (ON)	SATA
6	0 (ON)	0 (ON)	1 (OFF)	Serial USB OTG (USB0, same as mode 4)
7	0 (ON)	0 (ON)	0 (ON)	Bootconfig from eFUSE

Table 80: phyFLEX Carrier Board DIP Switch S3 Descriptions[43]

19.3.22 System Reset Button (S1)

The phyFLEX Carrier Board is equipped with a system reset button at S1 (*Figure 19*). Pressing the button pulls the reset input X_nPM_RESET_IN low which will reset the phyFLEX mounted on the phyFLEX Carrier Board. In the sequel the phyFLEX module generates the signal X_nPM_RESET_OUT, which resets the peripheral devices on the phyFLEX Carrier Board, such as the USB hub, etc.

System reset button S1 also connects to pin 3 of the power management connector X22.

[43]: Default settings are in **bold blue** text

19.3.23 System Power On/Off/Wake Button (S2)

The phyFLEX Carrier Board is equipped with a system Power On/Off/Wake button S2 (*Figure 19*). Pressing this button less than 5 seconds will wake up the phyFLEX-i.MX 6 module and the peripherals on the carrier board, or will turn on the system, if it is powered off. Pressing this button more than 5 seconds will turn off the system without proper shut down of the operating system.

Power On/Off/Wake button S2 also connects to pin 4 of the power management connector X22.

19.3.24 JTAG Interface (X4)

The JTAG interface of the phyFLEX-i.MX 6 is accessible at connector X4 on the carrier board (*Figure 19*). This interface is compliant with JTAG specification IEEE 1149.1 or IEEE 1149.7. No jumper settings are necessary for using the JTAG port. The following table describes the signal configuration at X4. When referencing contact numbers note that pin 1 located at the angled corner. Pins towards the labeling "ARM_JTAG" are odd numbered.

Pin #	Signal Name	ST	SL	Description
1	VREF_JTAG	O	3.3 V	JTAG reference voltage (VREF_JTAG via 100 Ohm resistor)
2	VREF_JTAG	O	3.3 V	JTAG reference voltage
3	X_nJTAG0_TRSTB	I	3.3 V	JTAG Test Reset
4, 6, 8, 10, 12, 14, 16, 18, 20	GND	-		Ground
5	X_JTAG0_TDI	I	3.3 V	JTAG Test Data Input
7	X_JTAG0_TMS	I/O	3.3 V	JTAG Test Mode Select Signal
9	X_JTAG0_TCK	I	3.3 V	JTAG Test Clock Signal
11	X_JTAG0_RTCLK	O	3.3 V	JTAG Return Test Clock Signal
13	X_JTAG0_TDO	O	3.3 V	JTAG Test Data Output
15	X_nPM_RESET_IN	I	3.3 V	System Reset
17	NC	-	-	Not connected
19	NC	-	-	Not connected

Table 81: JTAG Connector X4

19.3.25 RTC at U28

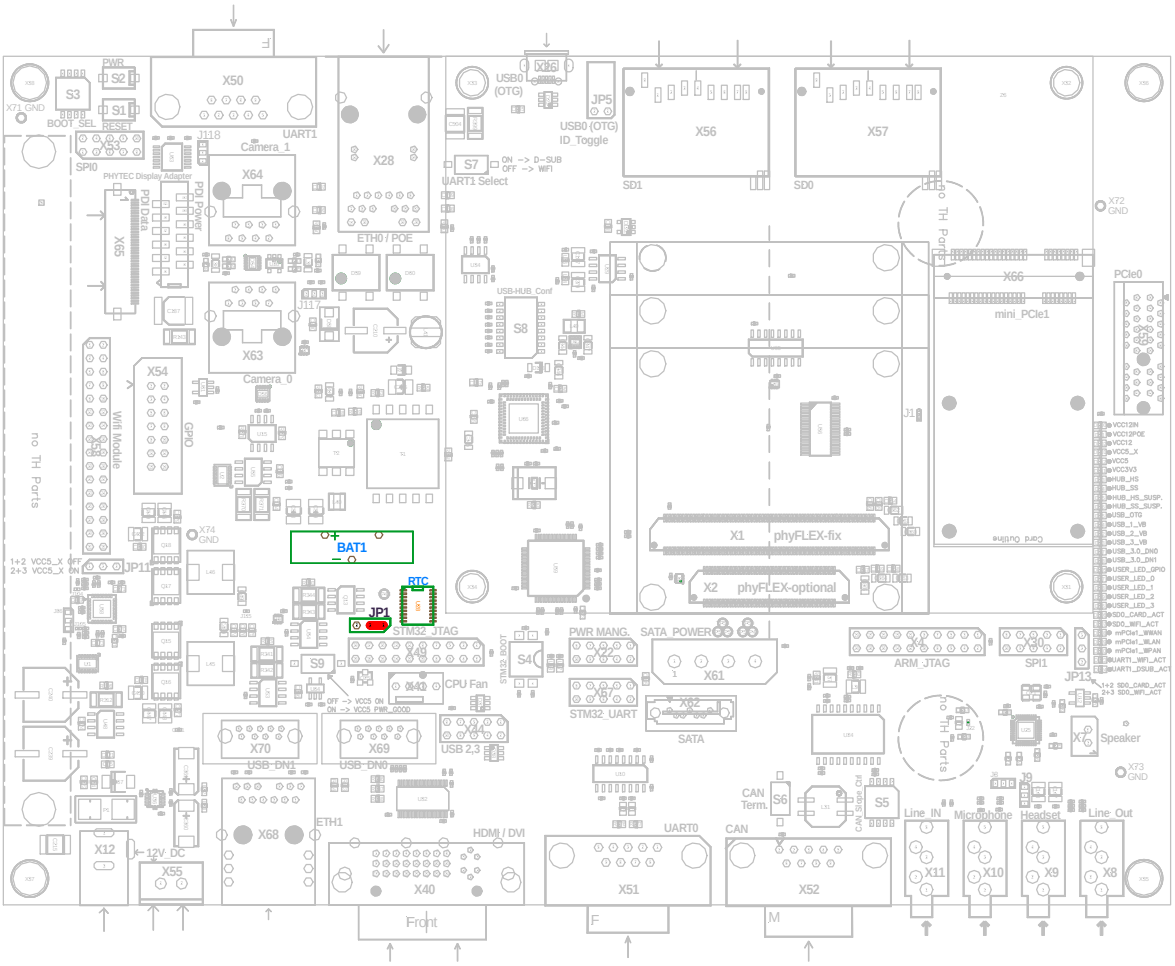


Figure 47: RTC with Battery Buffer

For real-time or time-driven applications, the phyFLEX Carrier Board is equipped with an RTC-8564 Real-Time Clock at U28. This RTC device provides the following features:

- Serial input/output bus (I^2C), address 0x51 (7 MSB)
- Power consumption
  Bus active (400 kHz): < 1 mA
  Bus inactive, CLKOUT inactive: = 275 nA
- Clock function with four year calendar
- Century bit for year 2000-compliance
- Universal timer with alarm and overflow indication
- 24-hour format
- Automatic word address incrementing
- Programmable alarm, timer and interrupt functions

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The Real-Time Clock is programmed via the I^2C bus (address 0x51). Since the phyFLEX-i.MX 6 is equipped with an internal I^2C controller, the I^2C protocol is processed very effectively without extensive processor action (*section 8.5*)

The Real-Time Clock also provides an interrupt output that extends to jumper JP1. Jumper JP1 allows to connect the RTC interrupt to the X_nPM_ ON/WAKEUP/OFF input or to X_GPIO5 of the phyFLEX-i.MX 6 (GPIO1_09 of the i.MX 6). An interrupt occurs in the event of a clock alarm, timer alarm, timer overflow and event counter alarm. It has to be cleared by software. With the interrupt function, the Real-Time Clock can be utilized in various applications.

Position JP1	Description
1+2	**RTC Interrupt connected to X_nPM_ ON/WAKEUP/OFF**
2+3	RTC Interrupt connected to X_GPIO5 (GPIO1_09 of the i.MX 6)

Table 82: RTC Interrupt Configuration JP1[44]

Note:
After connecting the supply voltage the Real-Time Clock generates no interrupt. The RTC must be first initialized (see *RTC Data Sheet* for more information).

Use of a coin cell (CR2032) at BAT1 allows to buffer the RTC.

[44]: Default settings are in **bold blue** text

19.3.26 Environment Management IC (EMIC) (U59)

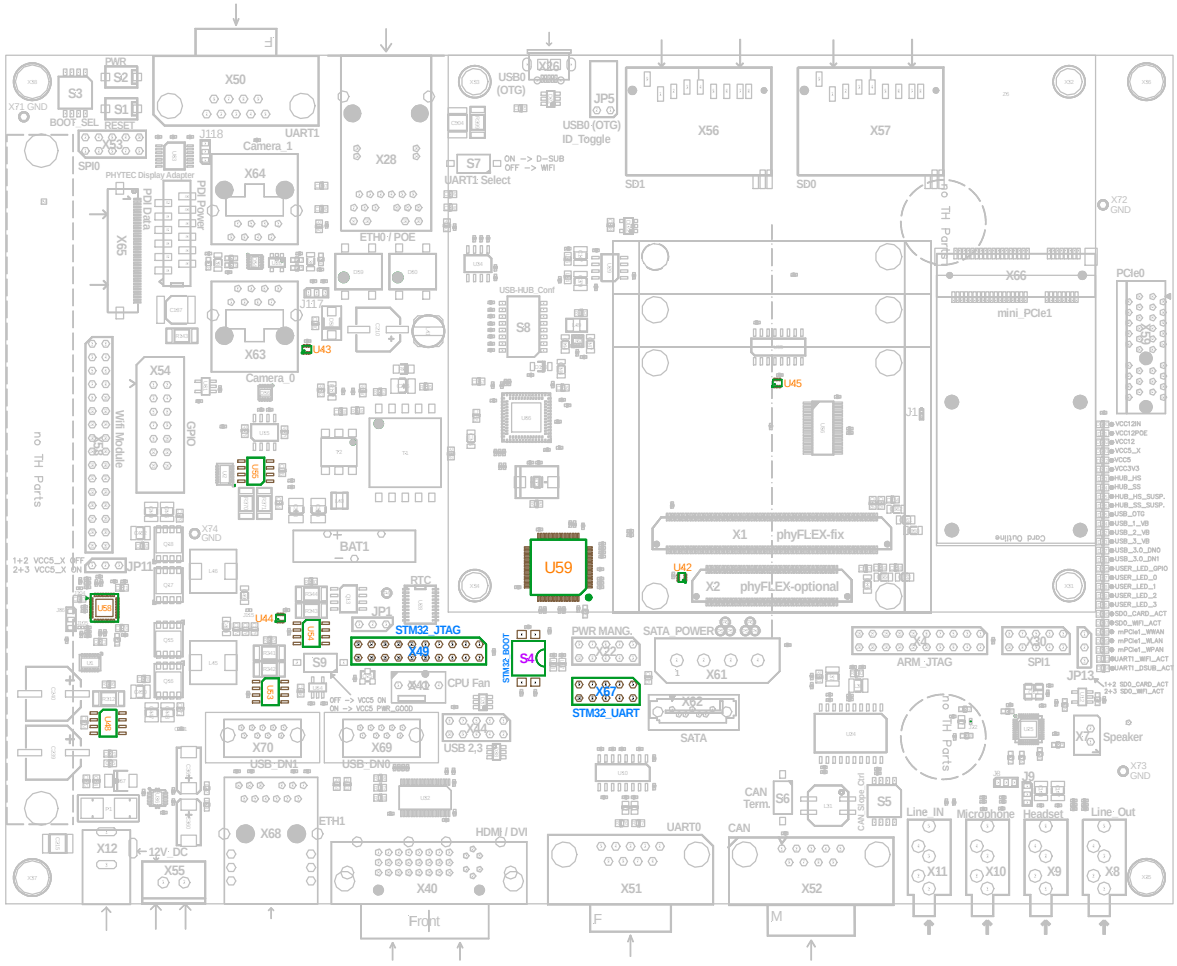


Figure 48: EMIC and supporting Components (top view)

The optional Environment Management IC (EMIC) at U59 on the carrier board gives the possibility to detect, monitor and record particular physical parameter such as current consumption, temperature und voltages. Furthermore the Environment Management IC comes with an additional serial interface and an I^2C management bus.

The Environment Management IC can be programmed via JTAG connector X49 (*Table 85*).

Note:
There is no software available for the EMIC. If you need further information, or a quotation for a custom software development, please contact Phytec at sales@phytec.de.

Data such as current consumption, voltage and state of control signals is collected via digital IOs of the EMIC, while the temperatures measured by sensors U42 – U45 is read via I^2C interface.

Table 83 shows the physical parameters which can be measured by the EMIC at U59 and the corresponding ports, whereas *Table 84* sums up the data collected via I^2C interface.

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Port	Signal	Description
		Supply Voltages
PA0	VCC12_IN_SENSE	12 V supply voltage at connector X12, or X55
PA1	VCC12_POE_SENSE	12 V supply voltage at connector X28
PA2	VCC12_SENSE	12 V supply voltage derived from either VCC12_IN, or VCC12_POE
PA3	VCC5_SENSE	5 V supply voltage for the peripherals on the carrier board
PA4	VCC3V3_SENSE	3.3 V supply voltage for the peripherals on the carrier board
PA6	VCC1V8	1.8 V supply voltage available at the Wi-Fi/Bluetooth connector X58
PA7	VCC1V1	1.1 V supply voltage of the USB hub at U66
		Supply Currents
PC0	Current_VCC12_IN	Entire supply current through X12, or X55 (U48)
PC1	Current_VCC12_POE	Entire supply current through POE at X28 (U55)
PC2	Current_VCC5	Supply current of all 5 V components on the carrier board except the phyFLEX module (U54)
PC3	Current_VCC3V3	Supply current of all 3.3 V components on the carrier board (U53)
		Control Signals
PC12	PGOOD_VCC5	Power good signal related to the 5 V supply voltage[45]
PC13	PGOOD_VCC3V3	Power good signal related to the 3.3 V supply voltage[45]
		Temperature Alerts
PC6	ALERT1	Overtemperature alert of module connectors temperature (U42)
PC7	ALERT2	Overtemperature alert of POE circuitry temperature (U43)
PC8	ALERT3	Overtemperature alert of power circuitry temperature (U44)
PC9	ALERT4	Overtemperature alert of module temperature (U45)

Table 83: Environment Management IC (EMIC) Measured Variables

The table below lists the I^2C addresses of the four temperature sensors, while *Figure 48* shows the location of the sensors.

[45]: The two Power Good inputs connect to the Power Good Outputs of the 5 V/ 3.3 V regulator at U58.

Device #	I²C Address	Position of the Temperature Sensor	Alert # (*Table 83)*
Temperature			
U42	0x49	Module connector	ALERT1
U43	0x48	POE circuitry	ALERT2
U44	0x4B	Power circuitry	ALERT3
U45	0x4A	Underneath the SOM	ALERT4

Table 84: Environment Management IC (EMIC) Measured Data via I²C Interface

Note:
To avoid any conflicts when connecting external I²C devices to the EMIC's I²C bus the addresses of the on-board temperature sensors must be considered (*Table 84*).

Pin #	Signal Name	ST	SL	Description
1	VREF_JTAG	O	3.3 V	JTAG reference voltage (VCC3V3 via 100 Ohm resistor)
2	VREF_JTAG	O	3.3 V	JTAG reference voltage (VCC3V3)
3	nJTAG_STM32_TRST	I	3.3 V	JTAG Test Reset
4, 6, 8, 10, 12, 14, 18, 20	GND	-		Ground
5	JTAG_STM32_TDI	I	3.3 V	JTAG Test Data Input
7	JTAG_STM32_TMS	I/O	3.3 V	JTAG Test Mode Select Signal
9	JTAG_STM32_TCK	I	3.3 V	JTAG Test Clock Signal
11	not connected	-	-	-
13	JTAG_STM32_TDO	O	3.3 V	JTAG Test Data Output
15	JTAG_STM32_RST	I	3.3 V	Reset
17	not connected	-	-	-
19	not connected	-	-	-

Table 85: EMIC JTAG Connector X49

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The EMIC at U59 provides an additional UART interface which is available at pin header connector X67. The following table shows the pin-out of connector X67.

Pin #	Signal Name	ST	SL	Description
1, 2, 4, 6, 7, 8, 10	not connected	-	-	-
3	EMIC_UART_TX	O	3.3 V	EMIC UART serial transmit signal
5	EMIC_UART_RX	I	3.3 V	EMIC UART serial data receive signal
9	GND	-	-	Ground 0 V

Table 86: Environment Management IC (EMIC) UART Interface Connector X67

The EMIC has different internal memory devices. The following table shows the different Boot Sources depending on the configuration of DIP switch S4

Boot Mode	PB2/BOOT1	BOOT0	DIP switch S4		Boot Source
			2	1	
0	X	0	X	Off	User Flash memory
1 (optional)	0	1	Off	On	System memory
2 (optional)	1	1	On	On	Embedded SRAM

Table 87: EMIC Boot Mode Selection S4

20 Revision History

Date	Version numbers	Changes in this manual
25.09.2012	Manual L-773e_0	First draft, Preliminary documentation. Describes the phyFLEX-i.MX 6 with phyFLEX Carrier Board.
07.12.2012	Manual L-773e_1	First Edition appropriate for the .2 PCB of the carrier board
15.03.2015	Manual L-773e_2	Second Edition information updated for the .1 PCB of the phyFLEX-i.MX 6 and the .3 PCB of the carrier board
15.10.2015	Manual L-773e_3	Third Edition information updated for the .3 and .4 PCB of the phyFLEX-i.MX 6 and the .6 PCB of the carrier board

Index

1

1000Base-T 45
100Base-T 45
10Base-T 45

A

Audio Interface 49

B

Backup Power 31
Block Diagram 3
Booting 33

C

Camera Interface 61
CAN 50
CMIC 31
Control Management IC 31

D

DDR3_1V5 29
DDR3_VREF 30
DDR3_VTT 30
DDR3-SDRAM 37
Debug Interface 54
Dimensions 75
Display Interface 58

E

EEPROM 37, 38
EEPROM Write Protection 39
EMC xiv
EMIC 71
EMIC 141
Emulator 57
Environment Management IC 71
Environment Management IC 141
Ethernet 45

F

Features 2

G

General Purpose I/Os 52
GND Connection 78

H

Humidity 75

I

I²C EEPROM 38
I²C Interface 47
I²C Memory 25
I²S 49

J

J10-J21 26
J12 115
J24 26
J26 ..... 26, 27, 67
J28-J30 26
J3 25, 39
J31 ..... 26, 64
J5-J8 26
J9 26, 67
JA-002 57
JTAG Interface 54
JTAG-Emulator Adapter 57

L

LAN 46
LED
  SOM D1 53
  SOM D2 53
LINK LED 107
LVDS
  Camera Signals 26, 64, 67

M

MAC 46
MAC Address 46

N

NAND Flash 38

O

Operating Temperature 75
Operating Voltage 75

P

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X65 108
phyFLEX Carrier Board
CAN 105
Connectors 85
Features 80
JP1 140
JTAG Interface 138
Peripherals 82
RS-232 104
RTC 139
S1 137
S2 138
S3 137
S6 106
Switches 87
Touch Screen Connectivity 115
X1 95
X10 123
X11 123
X12 97
X2 95
X26 111
X28 ..... 97, 107
X4 138
X40 116
X41 134
X50 103
X51 103
X52 105
X55 97
X56 130
X57 130
X58 135
X59 131
X61 133
X62 133
X63 118
X64 118
X65 112
X66 108
X69 108
X7 123
X70 108
X8 123
X9 123
phyFLEX-Connector 7, 8
Physical Dimensions 74
Phytec Display-Interface 112
Pin Description 7
Pinout
X1 10, 11, 12, 13, 14
X2 15, 16, 17
X3 18, 19, 20, 21
PMIC 28
PMIC_VBAT 31
Power Consumption 75
Power Domains 29
Power Supply 6

R

RS-232 Level 43
RTC 139

S

SATA Interface 51
SD / MMC Card Interfaces 40
Serial Interfaces 42
SMT Connector 7
SPEED LED 107
SPI Flash 37, 39
SPI Interface 48
Storage Temperature 75
Supply Voltage 28
System Configuration 33
System Memory 37
System Power 28

T

Tamper Detection 70
Technical Specifications 74

U

U10 38
U11 45
U12 ..... 26, 67
U13 38
U17 31
U19 71
U25 39
U27 ..... 26, 64
U2-U9 37
U59 141
UART 43
USB
OTG Interface 44
USB 2.0 111
USB 3.0 108
USB Device 44

USB Host 44
USB OTG..... 44
User LEDs 53

V

VCC_PM..... 29
VDD_5V_IN..... 29
VDD_5V_IN_R 28
VDD_MX6_SNVS..... 31
Voltage Output..... 31

W

Weight..... 75

X

X454

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