



Product Specification

M315HVR01.5

AU OPTRONICS CORPORATION

() Preliminary Specification

(V) Final Specification

Module	31.5" Color TFT-LCD
Model Name	M315HVR01.5 Open Cell

Customer

Date

Approved by

Note: This Specification is subject to change without notice.

Approved by

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Record of Revision

Version	Date	Page	Old description	New Description	Remark
1.0	2021/3/26	All			



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I Handling Precautions

- 1) Since polarizer is easily damaged, do not touch or press the surface of polarizer with hand.
- 2) Be sure to turn off power supply when inserting or disconnecting from input connector.
- 3) Wipe off water drop immediately. Long contact with water may cause discoloration or spots.
- 4) When the panel surface is soiled, wipe it with absorbent cotton or other soft cloth.
- 5) Since the panel is made of glass, it may break or crack if dropped or bumped on hard surface.
- 6) Since CMOS LSI is used in this module, take care of static electricity and insure human earth when handling.
- 7) Do not open or modify the Module Assembly.
- 8) Do not press the reflector sheet at the back of the module to any directions.
- 9) In case a TFT-LCD Module has to be put back into the packing container slot after once it was taken out from the container, do not press the center of the LED lightbar edge. Otherwise the TFT-LCD Module may be damaged.
- 10) Insert or pull out the interface connector, be sure not to rotate nor tilt it of the TFT-LCD Module.
- 11) Do not twist nor bend the TFT -LCD Module even momentary. It should be taken into consideration that no bending/twisting forces are applied to the TFT-LCD Module from outside. Otherwise the TFT-LCD Module may be damaged.
- 12) Please avoid touching COF position while you are doing mechanical design.
- 13) When storing modules as spares for a long time, the following precaution is necessary: Store them in a dark place. Do not expose the module to sunlight or fluorescent light. Keep the temperature between 5°C and 35°C at normal humidity.
- 14) Do not apply the same pattern for a long time, it will enhance relevant defect.
- 15) If the product will be used under extreme conditions such as under high temperature, humidity, display patterns or the operation time etc., it is strongly recommended to contact AUO for the advice about the application of engineering. Otherwise, its reliability and the function may not be guaranteed. Extreme conditions are commonly found at airports, transit stations, banks, stock markets, and controlling systems.
- 16) Module designer should apply adequate thermal solutions to keep the electrical components surface temperature under control limit (ex: Source Driver IC 100°C , Components on T-con PCB 85°C) Operations over the temperature can cause damages or decrease of lifetime.



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2 General Description

This specification applies to the 31.5 inch wide Color a-Si TFT-LCD Module M315HVR01.5

The display supports the FHD - 1920(H) x 1080(V) screen format and 16.7M colors (RGB 8-bits). The input interface is LVDS .

2.1 Display Characteristics

The following items are characteristics summary on the table under 25°C condition:

ITEMS	Unit	SPECIFICATIONS
Screen Diagonal	[mm]	801.3 (31.50")
Active Area	[mm]	698.4 (H) x 392.85 (V)
Pixels H x V	-	1920(x3) x 1080
Pixel Pitch	[um]	363.75 (per one triad) × 363.75
Pixel Arrangement	-	R.G.B. Vertical Stripe. Source board at bottom
Display Mode	-	VA Mode, Normally Black
Response Time	[msec]	20 (Typical, G to G)
Power Consumption	[Watt]	5.52 (Typ.) @ White pattern, Fv=60Hz
Weight	[Grams]	765.8
Electrical Interface	-	2 Port LVDS
Support Color	-	16.7M colors (RGB 8-bits)
Surface Treatment	-	SAG 40% , 3H
Temperature Range		
Operating	[°C]	0 to +50
Storage (Shipping)	[°C]	-20 to +60
Cell transmittance	[%]	4.25% (Typ.)
		3.60% (Min.)
Cell thickness	[mm]	1.24 (Thickness of polarizer film: 0.22 mm each side)



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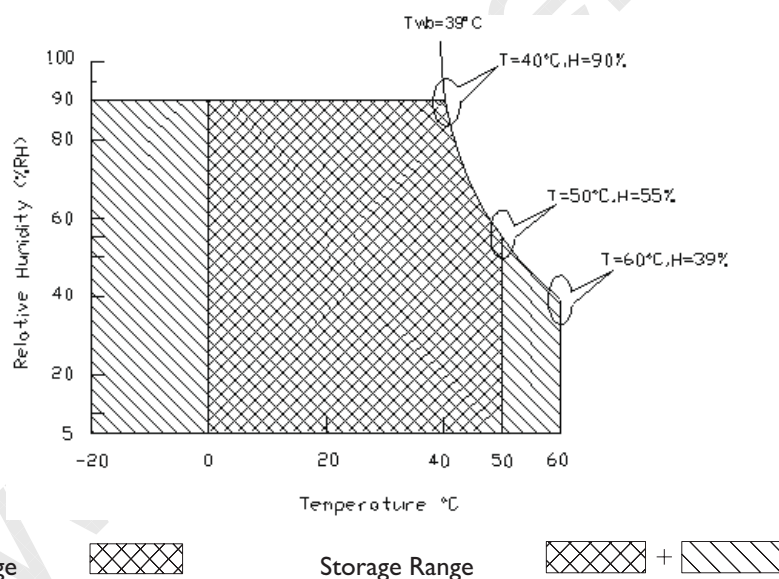
2.2 Absolute Maximum Rating of Environment

Permanent damage may occur if exceeding the following maximum rating.

Symbol	Description	Min.	Max.	Unit	Remark
TOP	Operating Temperature	0	+50	[°C]	Note 2-1
TGS	Glass surface temperature (operation)	0	+65	[°C]	Note 2-1 Function judged only
HOP	Operation Humidity	5	90	[%RH]	Note 2-1
TST	Storage Temperature	-20	+60	[°C]	
HST	Storage Humidity	5	90	[%RH]	

Note 2-1: Temperature and relative humidity range are shown as the below figure.

1. 90% RH Max ($T_a \leq 39^\circ\text{C}$)
2. Max wet-bulb temperature at 39°C or less. ($T_a \leq 39^\circ\text{C}$)
3. No condensation





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2.3 Optical Characteristics

The optical characteristics are measured on the following test condition.

Test Condition:

1. Equipment setup: Please refer to **Note 2-2**.
2. Panel Lighting time: 30 minutes
3. VDD=12.0V, Fv=60Hz, Ta=25°C

Symbol	Description		Min.	Typ.	Max.	Unit	Remark
CR	Contrast Ratio (Center of screen)		1800	3000	-	-	Note 2-4 By SR-3
θ_R	Horizontal Viewing Angle (CR=10)	Right	75	89	-	[degree]	Note 2-5 By EZ Contrasts
θ_L		Left	75	89	-		
Φ_H	Vertical Viewing Angle (CR=10)	Up	75	89	-		
Φ_L		Down	75	89	-		
TGTG	Response Time	Gray to Gray	-	20	-	[msec]	Note 2-6 By TRD-100
R _x	Color Coordinates (CIE 1931)	Red x	0.626	0.656	0.686	-	Base on C light
R _y		Red y	0.295	0.325	0.355		
G _x		Green x	0.242	0.272	0.302		
G _y		Green y	0.555	0.585	0.615		
B _x		Blue x	0.106	0.136	0.166		
B _y		Blue y	0.075	0.105	0.135		
W _x		White x	0.270	0.300	0.330		
W _y		White y	0.315	0.345	0.375		

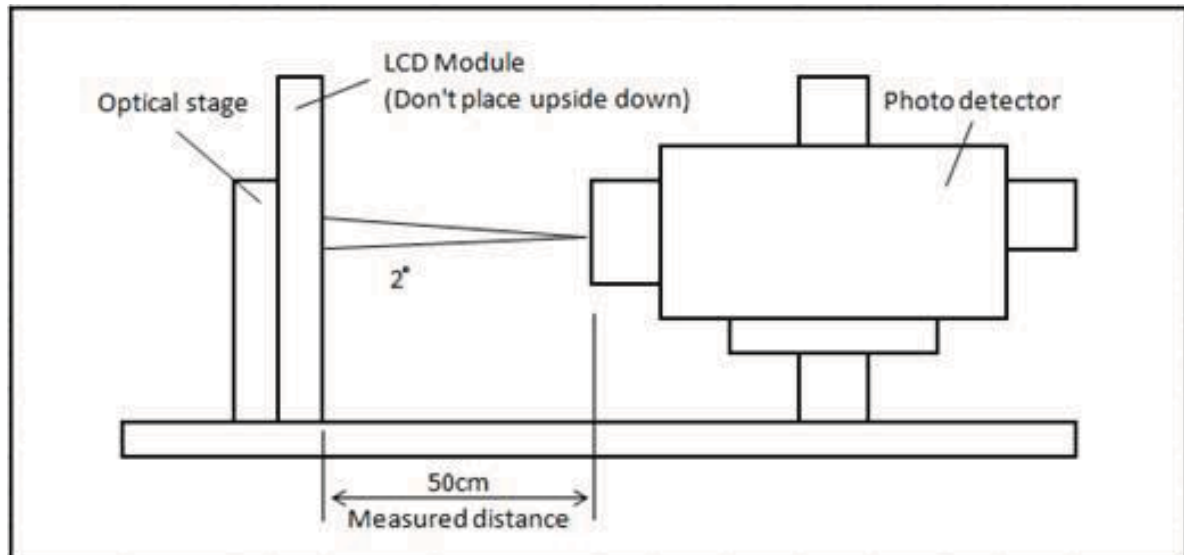


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Note 2-2: Equipment setup :

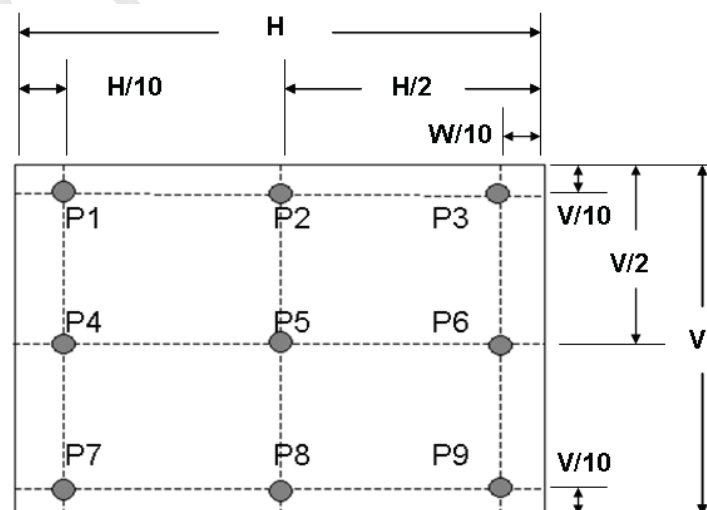


Note 2-3: Luminance Uniformity Measurement

Definition:

$$\text{Luminance Uniformity} = \frac{\text{Minimum Luminance of 9 Points (P1 ~ P9)}}{\text{Maximum Luminance of 9 Points (P1 ~ P9)}}$$

a. Test pattern: White Pattern





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Note 2-4: Contrast Ratio Measurement

Definition:

$$\text{Contrast Ratio} = \frac{\text{Luminance of White pattern}}{\text{Luminance of Black pattern}}$$

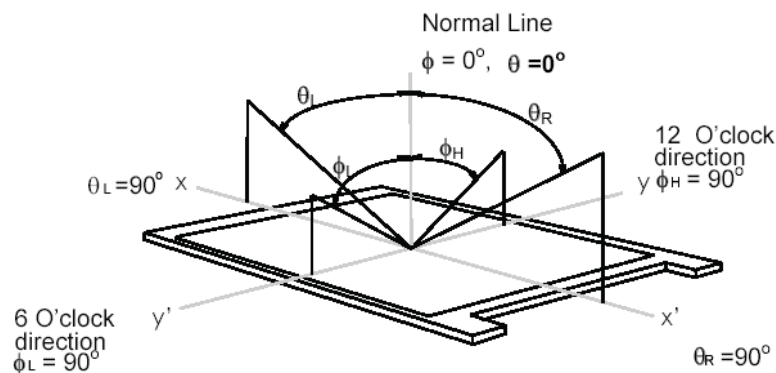
- Measured position: Center of screen (P5) & perpendicular to the screen ($\theta = \Phi = 0^\circ$)
- Base on AUO standard backlight

Note 2-5: Viewing angle measurement

Definition: The angle at which the contrast ratio is greater than 10 & 5.

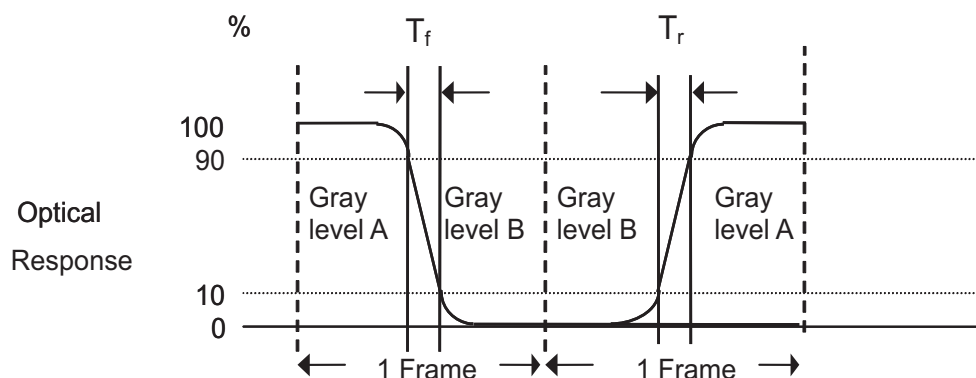
- Horizontal view angle: Divide to left & right (θ_L & θ_R)

Vertical view angle: Divide to up & down (Φ_H & Φ_L)



Note 2-6: Response time measurement

The output signals of photo detector are measured when the input signals are changed from “Gray level A” to “Gray level B” (falling time, T_f), and from “Gray level B” to “Gray level A” (rising time, T_r), respectively. The response time is interval between the 10% and 90% of optical response.





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The gray to gray response time is defined as the following table.

Gray Level to Gray Level		Target gray level				
		L0	L63	L127	L191	L255
Start gray level	L0					
	L63					
	L127					
	L191					
	L255					

■ T_{GTG_typ} is the total average time at rising time and falling time of gray to gray.



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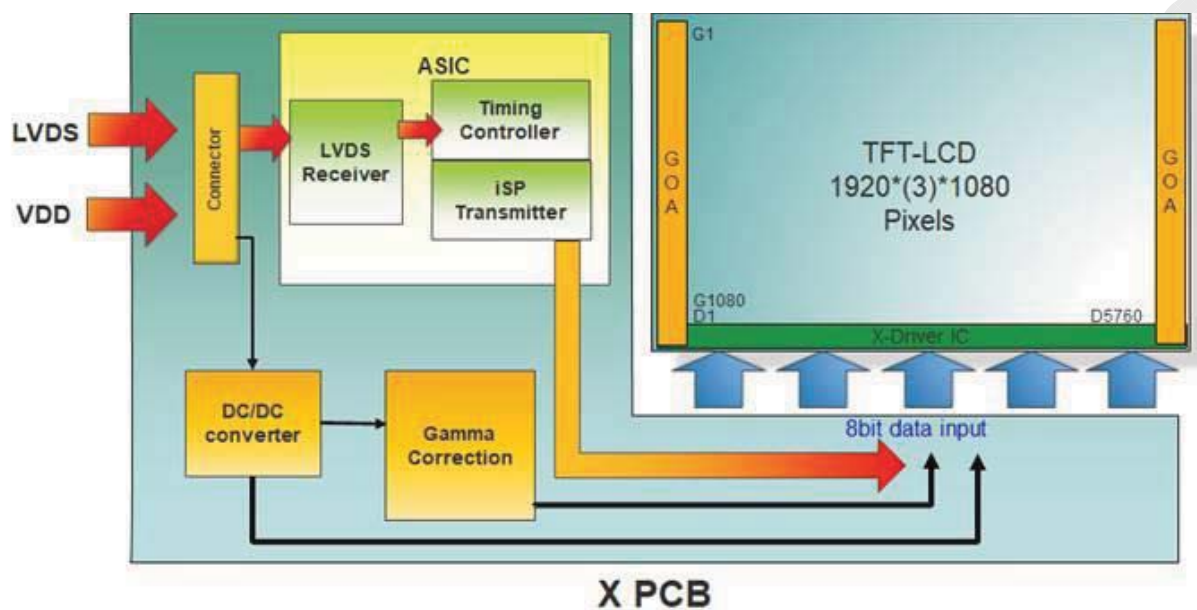
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3 TFT-LCD Module

3.1 Block Diagram

The following shows the block diagram of the 31.5 inch Color TFT-LCD Module.





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3.2 Interface Connection

3.2.1 Connector Type

TFT-LCD Connector	Manufacturer	STM	P-TWO
	Part Number	MSBKT2407P30HB	I87034-3009
Mating Connector	Manufacturer	JAE or Compatible	
	Part Number	FI-X30HL (Locked Type)	

3.2.2 Connector Pin Assignment

1	RxO0-	Negative LVDS differential data input (Odd data)	
2	RxO0+	Positive LVDS differential data input (Odd data)	
3	RxO1-	Negative LVDS differential data input (Odd data)	
4	RxO1+	Positive LVDS differential data input (Odd data)	
5	RxO2-	Negative LVDS differential data input (Odd data)	
6	RxO2+	Positive LVDS differential data input (Odd data)	
7	GND	Ground	
8	RxOCLK-	Negative LVDS differential clock input (Odd clock)	
9	RxOCLK+	Positive LVDS differential clock input (Odd clock)	
10	RxO3-	Negative LVDS differential data input (Odd data)	
11	RxO3+	Positive LVDS differential data input (Odd data)	
12	RxE0-	Negative LVDS differential data input (Even data)	
13	RxE0+	Positive LVDS differential data input (Even data)	
14	GND	Ground	
15	RxE1-	Negative LVDS differential data input (Even data)	
16	RxE1+	Positive LVDS differential data input (Even data)	
17	GND	Ground	
18	RxE2-	Negative LVDS differential data input (Even data)	
19	RxE2+	Positive LVDS differential data input (Even data)	
20	RxECLK-	Negative LVDS differential clock input (Even clock)	
21	RxECLK+	Positive LVDS differential clock input (Even clock)	
22	RxE3-	Negative LVDS differential data input (Even data)	
23	RxE3+	Positive LVDS differential data input (Even data)	
24	WP	Digital-Vcom write protection	
25	NC	No connection (for AUO test only. Do not connect)	
26	SCL	I2C-Compatible Serial-Clock Input for Vcom adjust	
27	SDA	I2C-Compatible Serial-Data Input / Output for	
28	VDD	Power Supply Input Voltage	

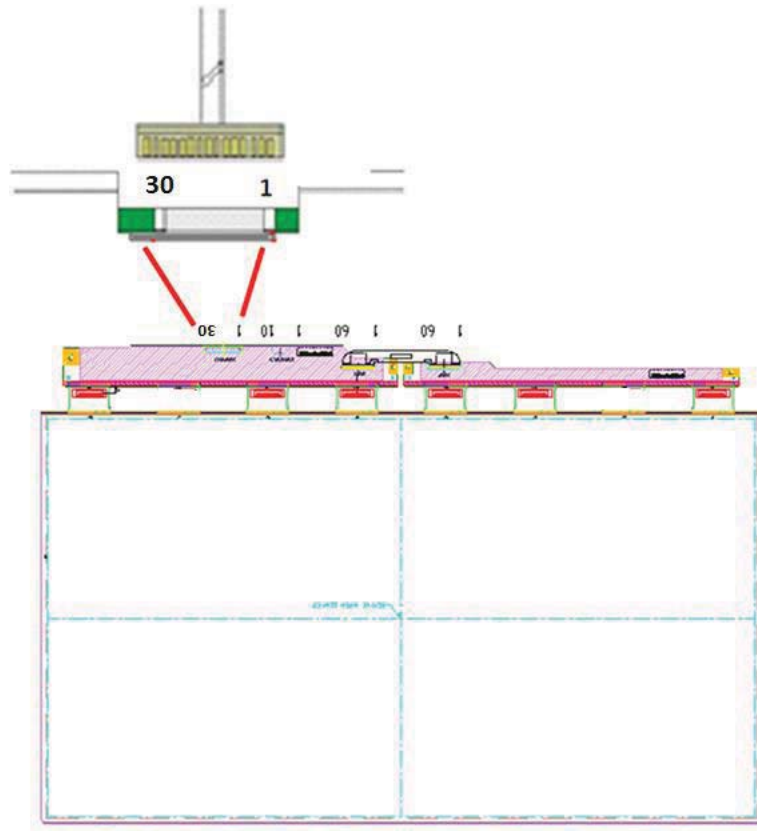


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29	VDD	Power Supply Input Voltage	
30	VDD	Power Supply Input Voltage	





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3.3 Electrical Characteristics

3.3.1 Absolute Maximum Rating

Permanent damage may occur if exceeding the following maximum rating.

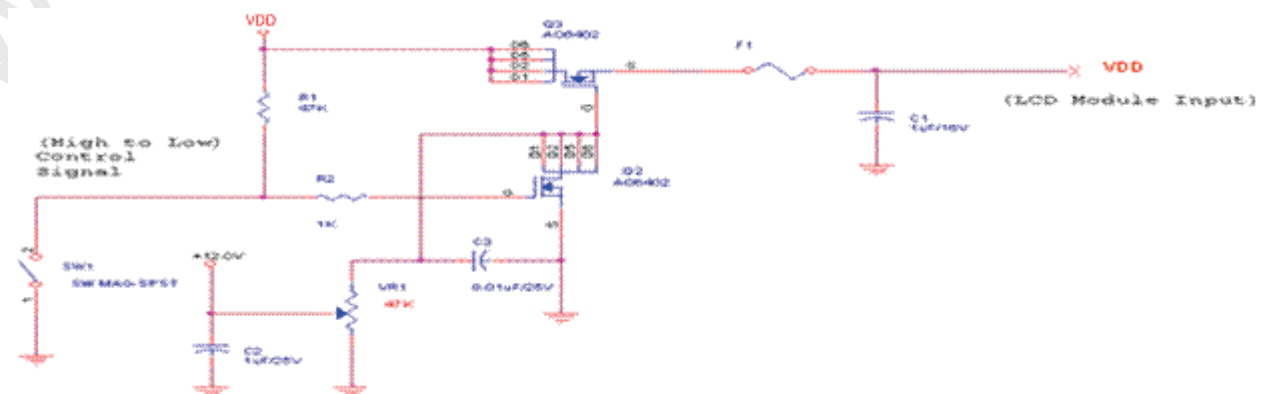
Symbol	Description	Min	Max	Unit	Remark
VDD	Power Supply Input Voltage	GND-0.3	14.0	[Volt]	Ta=25°C
SCL,SDA, WP	I2C input Voltage	GND-0.3	4.0	[Volt]	Ta=25°C

3.3.2 Recommended Operating Condition

Symbol	Description	Min	Typ	Max	Unit	Remark
VDD	Power supply Input voltage	10.8	12	13.2	[Volt]	
IDD	Power supply Input Current (RMS)	-	0.46	0.6	[A]	VDD= 12V, White Pattern, Fv=60Hz
			0.52	0.69	[A]	VDD= 12V, White Pattern, Fv=76Hz
PDD	VDD Power Consumption	-	5.52	7.2	[Watt]	VDD= 12V, White Pattern, Fv=60Hz
			6.24	8.28	[Watt]	VDD= 12V, White Pattern, Fv=76Hz
IRush	Inrush Current	-	-	3.0	[A]	Note 3-1
VDDrp	Allowable VDD Ripple Voltage	-	-	VDD*5%	[mV]	VDD= 12V, White Pattern, Fv=76Hz

Note 3-1: Inrush Current measurement:

Test circuit:

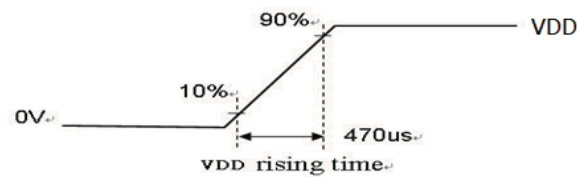




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The duration of VDD rising time: 470us.

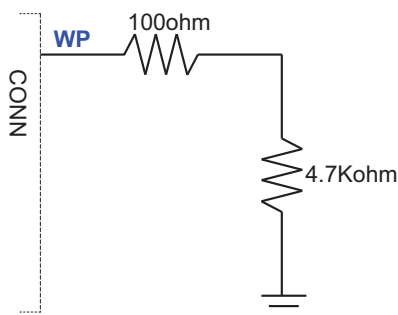
3.3.3 Input control signal threshold voltage definition

Item	Symbol	Min.	Typ.	Max.	Unit
Input High Threshold Voltage	VIH	2.7	-	3.6	V
Input Low Threshold Voltage	VIL	0	-	0.6	V

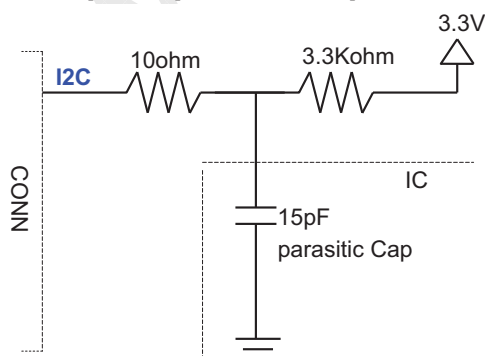
3.3.4 Write Protection mode selection

WP	Note
L or OPEN	Protection
H	Writable

3.3.5 Input equivalent impedance of WP pin



3.3.6 Input equivalent impedance of SDA/SCL pin





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3.4 Signal Characteristics

3.4.1 LCD Pixel Format

	1			2													1919			1920		
1st Line	R	G	B	R	G	B											R	G	B	R	G	B
	.	.	.	.	.	.	.										.	.	.	.	.	.
	.	.	.	.	.	.	.										.	.	.	.	.	.
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1080 Line	R	G	B	R	G	B											R	G	B	R	G	B



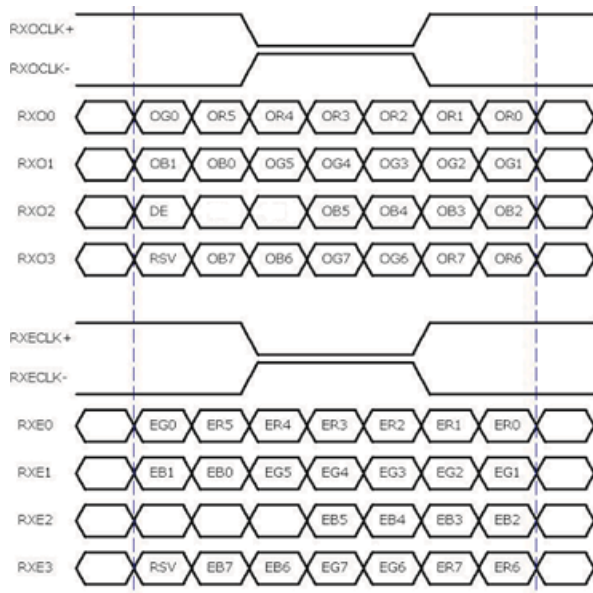
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3.4.2 LVDS Data Format

The following table is for color versus input data (8bit). The higher the gray level, the brighter the color.



8 Bit Color Bit Order			
MSB	R7	G7	B7
	R6	G6	B6
	R5	G5	B5
	R4	G4	B4
	R3	G3	B3
	R2	G2	B2
	R1	G1	B1
LSB	R0	G0	B0

Note.3-2:

- O = "Odd Pixel Data" E = "Even Pixel Data"
- Refer to 3.4.1 LCD pixel format, the 1st data is 1 (Odd Pixel Data), the 2nd data is 2 (Even Pixel Data) and the last data is 1920 (Even Pixel Data).

3.4.3 Color Versus Input Data

The following table is for color versus input data (8bit). The higher the gray level, the brighter the color.

Color	Gray Level	Color Input Data																								Remark
		RED data (MSB:R7, LSB:R0)								GREEN data (MSB:G7, LSB:G0)								BLUE data (MSB:B7, LSB:B0)								
		R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0	
Black	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
White	-	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1		
Gray 127	-	0	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	0	1	1	1	1	1	1		
Red	L0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	Black	
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:		
	L255	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
Green	L0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	Black	
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:		
	L255	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0		
Blue	L0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	Black	
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:		
	L255	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1		



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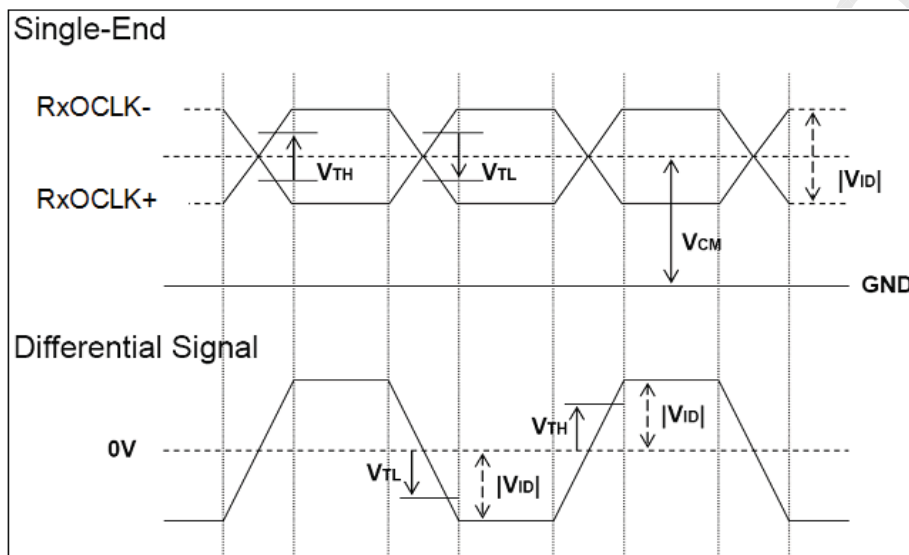
3.4.4 LVDS Specification

a. DC Characteristics:

Symbol	Description	Min	Typ	Max	Units	Condition
V_{TH}	LVDS Differential Input High Threshold	-	-	+100	[mV]	$V_{CM} = 1.2V$
V_{TL}	LVDS Differential Input Low Threshold	-100	-	-	[mV]	$V_{CM} = 1.2V$
$ V_{ID} $	LVDS Differential Input Voltage	100	-	600	[mV]	
V_{CM}	LVDS Common Mode Voltage	+1.0	+1.2	+1.5	[V]	$V_{TH}-V_{TL} = 200mV$

LVDS Signal Waveform:

Use RxOCLK- & RxOCLK+ as example.



b. AC Characteristics:

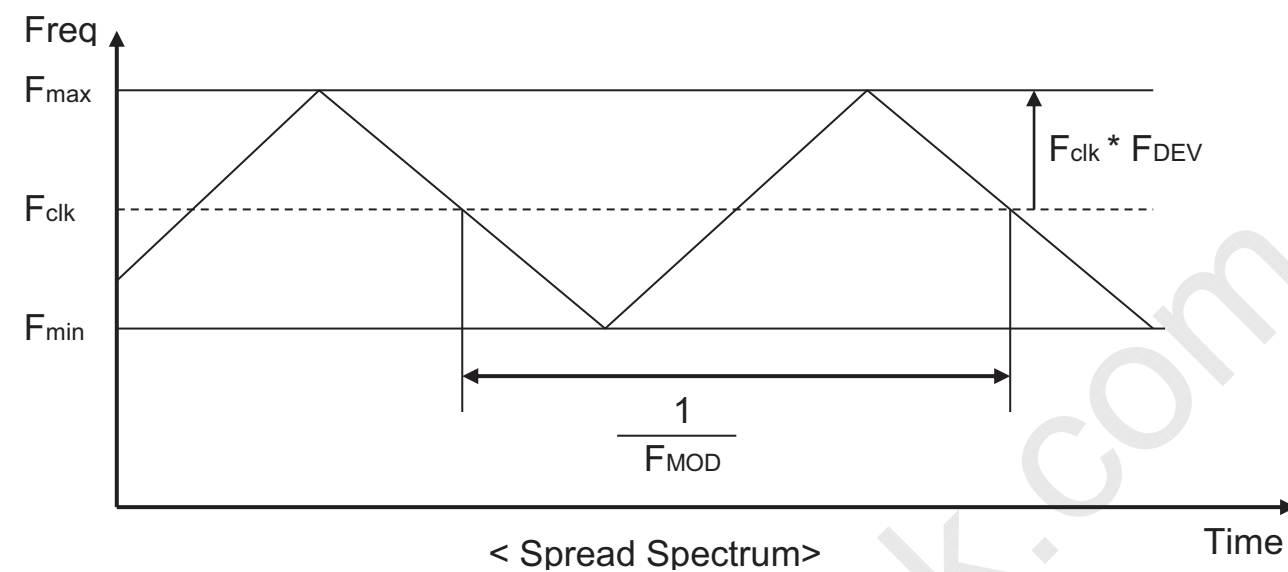
Symbol	Description	Min	Max	Unit	Remark
F_{DEV}	Maximum deviation of input clock frequency during Spread Spectrum	-	± 3	%	
F_{MOD}	Maximum modulation frequency of input clock during Spread Spectrum	-	200	KHz	



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Fclk: LVDS Clock Frequency



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3.4.5 Input Timing Specification

Symbol	Description		Min.	Typ.	Max.	Unit	Remark
Tv	Vertical Section	Period	1100	1130	1893	Th	
Tdisp (v)		Active	1080	1080	1080	Th	
Tblk (v)		Blanking	20	50	813	Th	
Fv		Frequency	48	60	76	Hz	Note 3-3
Th	Horizontal Section	Period	1034	1050	1100	Tclk	
Tdisp (h)		Active	960	960	960	Tclk	
Tblk (h)		Blanking	74	90	140	Tclk	
Fh		Frequency	52.7	68.0	91.0	KHz	Note 3-4
Tclk	LVDS Clock	Period	10.6	14.0	18.5	ns	1/Fclk
Fclk		Frequency	54.5	71.2	94.0	MHz	Note 3-5

Note 3-3:

75Hz model: Frame rate 48~76Hz / The optimal Vertical Frequency is 50~76 Hz for best picture quality

Note 3-4: The equation is listed as following. Please don't exceed the above recommended value.

$$Fh \text{ (Min.)} = Fclk \text{ (Min.)} / Th \text{ (Min.)};$$

$$Fh \text{ (Typ.)} = Fclk \text{ (Typ.)} / Th \text{ (Typ.)};$$

$$Fh \text{ (Max.)} = Fclk \text{ (Max.)} / Th \text{ (Min.)};$$

Note 3-5: The equation is listed as following. Please don't exceed the above recommended value.

$$Fclk \text{ (Min.)} = Fv \text{ (Min.)} \times Th \text{ (Min.)} \times Tv \text{ (Min.)};$$

$$Fclk \text{ (Typ.)} = Fv \text{ (Typ.)} \times Th \text{ (Typ.)} \times Tv \text{ (Typ.)};$$

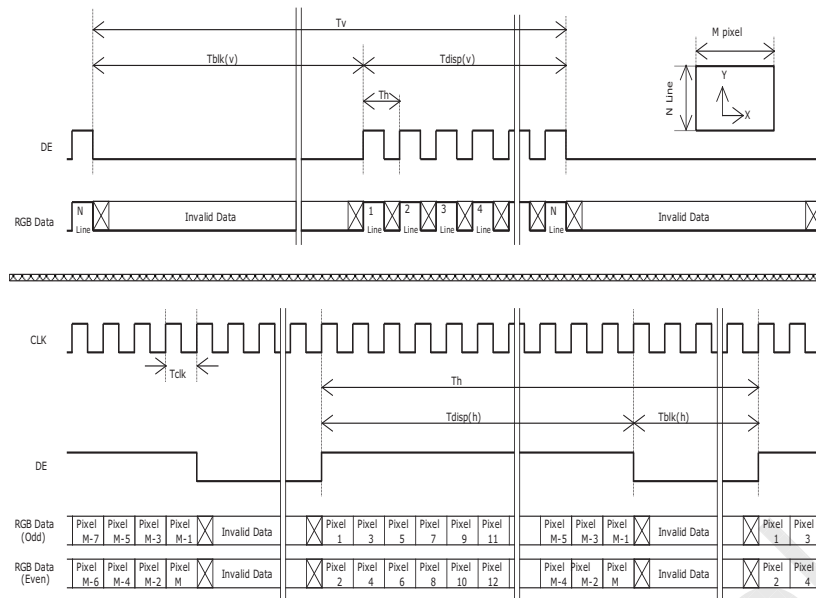


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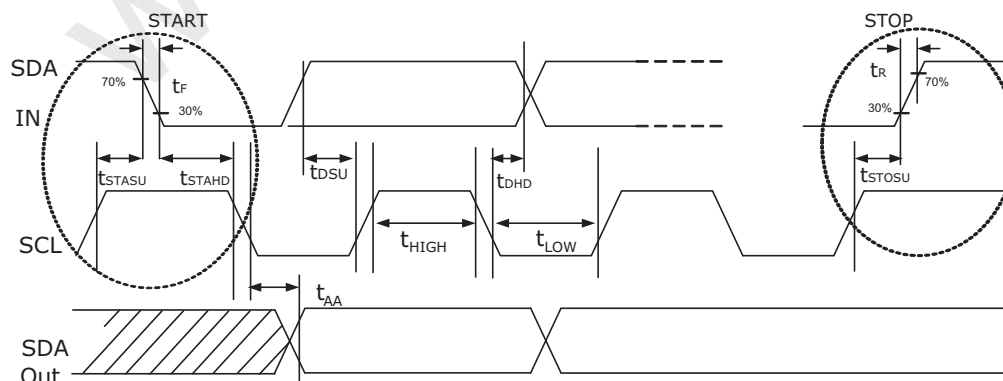
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3.4.6 Input Timing Diagram



3.4.7 I2C Electrical Characteristics (VDD=12V, VSDA/VSCL=3.3V, TA=25°C)

Parameter		Symbol	Min.	Typ.	Max	Unit
I2C	SCL clock frequency	fSCL	-	-	350	kHz
	Clock Pulse Width Low	tLOW	1.85	-	-	us
	Clock Pulse Width High	tHIGH	0.4	-	-	us
	Clock Low to Data Output Valid	tAA	1.76	-	-	us
	Start Setup Time	tSTASU	0.6	-	-	us
	Start Hold Time	tSTAHD	0.6	-	-	us
	Stop Setup Time	tSTOSU	0.6	-	-	us
	Data In Setup Time	tDSU	0.1	-	-	us
	Data In Hold Time	tDHD	0	-	-	us
	SCL/SDA Rise Time	tR	-	-	0.3	us
	SCL/SDA Fall Time	tF	-	-	0.3	us





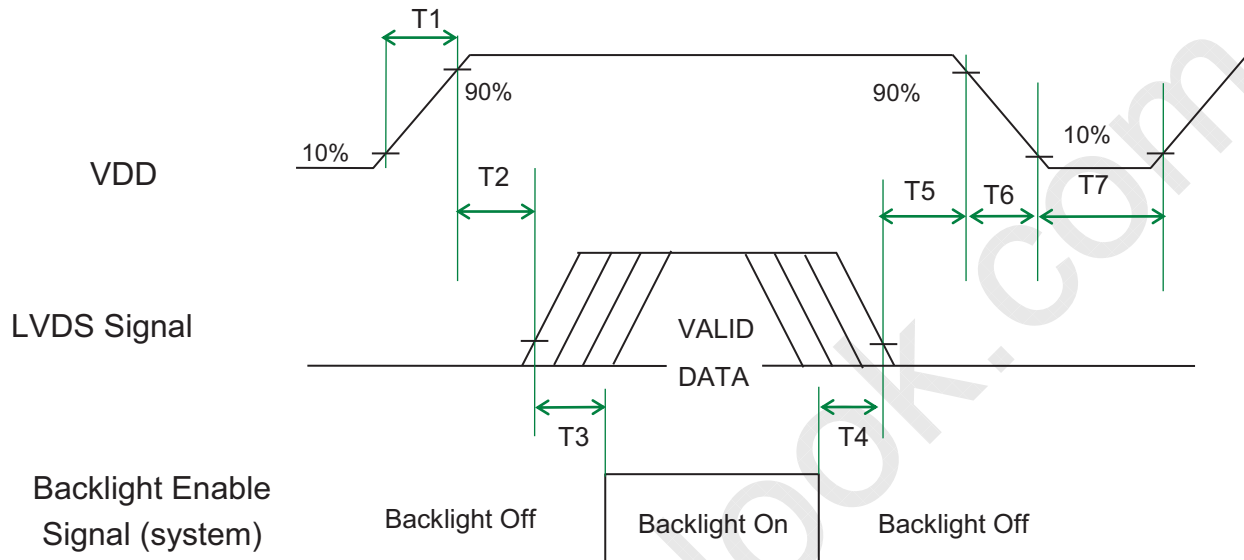
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3.5 Power ON/OFF Sequence

VDD power, LVDS signal and backlight on/off sequence are as following. LVDS signals from any system shall be Hi-Z state when VDD is off.



Power Sequence Timing

Symbol	Value			Unit	Remark
	Min.	Typ.	Max.		
T1	0.5	-	10	[ms]	
T2	0	-	50	[ms]	
T3	500	-	-	[ms]	
T4	100	-	-	[ms]	Note 3-8
T5	0	-	50	[ms]	Note 3-6 Note 3-7
T6	0	-	200	[ms]	Note 3-9
T7	1000	-	-	[ms]	

Note 3-6 : Recommend setting T5 = 0ms to avoid electronic noise when VDD is off.

Note 3-7 : During T5 period , please keep the level of input LVDS signals with Hi-Z state.

Note 3-8 : If T4 < 100ms, there will be no reliability concern, but the display may momentarily show abnormal screen.

Note 3-9: Voltage of VDD must decay smoothly after power-off.(customer system decide this value)



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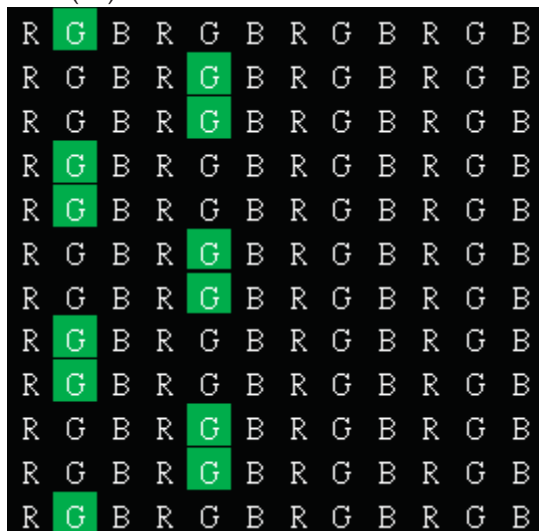
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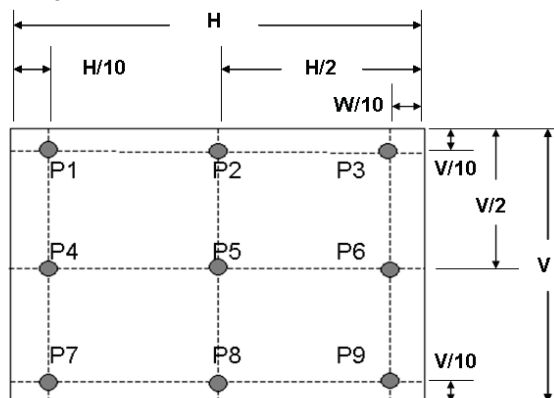
3.6 Vcom Adjustment Flow

A. Flicker Pattern

2L+1 (IV) L127



3.6.2 Vcom is optimization when minimized flicker phenomenon of location P5 (as below figure)





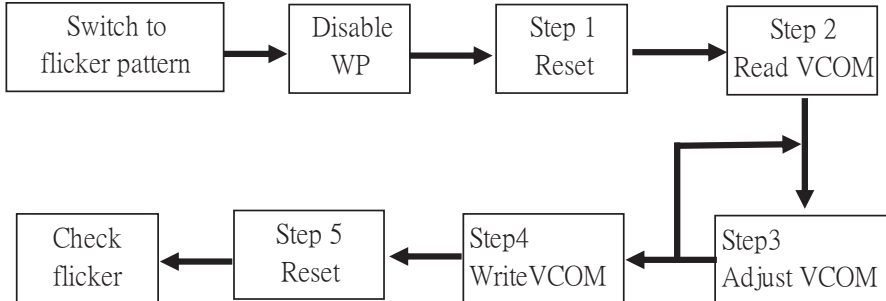
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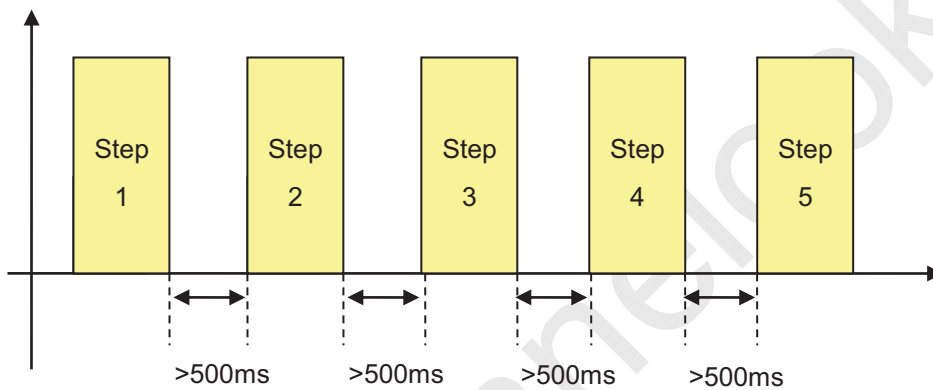
3.6.3 Tuning Step

VCOM I2C Tuning Step



3.6.4 Interval of Step to Step

VCOM I2C Tuning Step



3.6.5 I2C Protocol Define

DVCOM IC address (slave) : 1110110 (0x76)

Start	Slave Address							W	ACK	Index Address 0							ACK	Control Byte							ACK	Stop
	1	1	1	0	1	1	0	0		0	0	0	0	0	0	0		0	0	1	0	0	1	0		
0xEC								0x00								0x12										
Device Address + W								Control Address								Reset + OUT_EN										

Step2 Read Vcom Command



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Start	Slave Address							W	ACK	Index Address 0							R	ACK	Start	Slave Address							W	ACK	VCOM data							ACK	Stop
	1	1	1	0	1	1	0	0		0	0	0	0	0	1	1	1			0	1	1	0	1	X	X	X		X	X	X	NA					
	0xEC									0x01										0xED									0~127								
	Device Address + W									VCOM Address										Device Address + R									DATA								

Step3 Adjust Vcom Command

Start	Slave Address							W	ACK	Index Address 1							R	ACK	VCOM data							ACK	Stop	
	1	1	1	0	1	1	0	0		0	0	0	0	0	0	1	X		X	X	X	X	X	X	N			
	0xEC									0x01									0~127									A
	Device Address + W									VCOM Address									VCOM Value									

Step4 Write Vcom Command

Start	Slave Address							W	ACK	Index Address 0							ACK	Control Byte							ACK	Stop
	1	1	1	0	1	1	0	0		0	0	0	0	0	0	0		0	1	0	1	0				
0xEC								0x00								0x0A										
Device Address + W								Control Address								Write DAC to NVM										

Step5 Reset Command

Start	Slave Address							W	ACK	Index Address 0							ACK	Control Byte							ACK	Stop		
								R																				
	1	1	1	0	1	1	0	0		0	0	0	0	0	0	0		0	0	0	0	1	0	0			1	0
	0xEC									0x00									0x12									
	Device Address + W									Control Address								Reset + OUT EN										

4 Reliability Test

AUO reliability test items are listed as following table. (Bare Panel only)

Items	Condition	Remark
Temperature Humidity Bias (THB)	Ta= 50°C, 80%RH, 300hours	
High Temperature Operation (HTO)	Ta= 50°C, 50%RH, 300hours	
Low Temperature Operation (LTO)	Ta= 0°C, 300hours	
High Temperature Storage (HTS)	Ta= 60°C, 300hours	



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Low Temperature Storage (LTS)	Ta= -20°C, 300hours	
Thermal Shock Test (TST)	-20°C/30min, 60°C/30min, 100 cycles	Note 4-1

Note 4-1: a. A cycle of rapid temperature change consists of varying the temperature from -20°C to 60°C and back again. Power is not applied during the test.

b. After finish temperature cycling, the unit is placed in normal room ambient for at least 4 hours before power on.

Note 4-2 : Result Evaluation Criteria:

TFT-LCD panels test should take place after gradually cooling enough at room temperature

In the normal application, there should be no particular problems that may affect the display function.

5 Shipping Label

5.1 Small Shipping Label

The label is on the PCBA as shown below :



5.2 Run Card Label

The label is on the panel as shown below :

M315HVR01-x/xx		xx:xxxxxxxxxx	Remark : X	
0				SKD
	S/N xxxxxxxxxxxxxx (xxxxx)			
		Z	P	N
xxxxx	xxxxx	xxxxx		
xxxxx	xxxxx	xxxxx		
xxxxx	xxxxx	xxxxx		
xxxxx	xxxxx	xxxxx		



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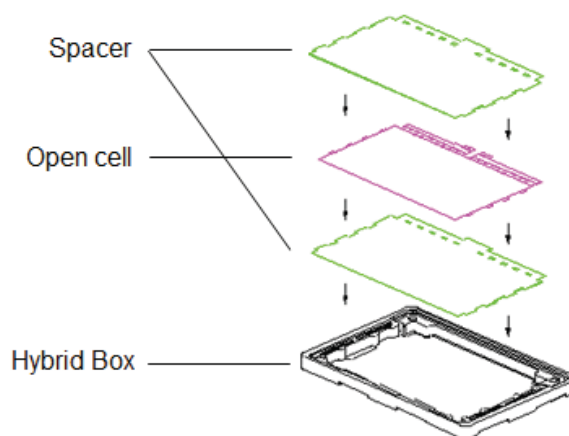


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7 Packing Specification

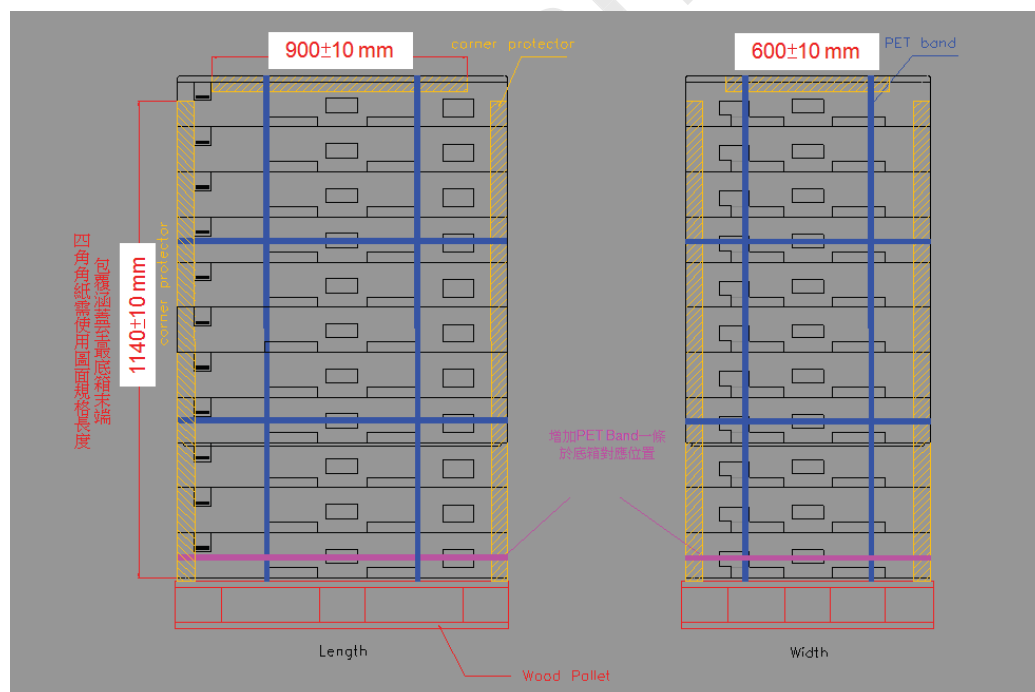
7.1 Packing Flow



- Open cell : 10(pcs/Box)
- Spacer : 11(pcs/Box)

Single pallet packing Illustration

- 1 (Box/Layer)
- 10 (Layer/Pallet)



單層pallet打棧示意圖

SingleOne pallet packaging illustration





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7.2 Pallet and Shipment information

Item	Specification			Remark
	Q'ty	Dimension	Weight(kg)	
Box	1	950.6(L)mm x 675(W)mm x 120(H)mm	1.93	without cell & spacer
Packing Box	10 pcs/Box	950.6(L)mm x 675(W)mm x 120(H)mm	10.5	with cell & cushion & spacer
Pallet	1	980(L)mm x 740(W)mm x 132(H)mm	12.0	M25 棧板
Pallet after Packing	10 boxes/pallet	980(L)mm x 740(W)mm x 1332(H)mm	117	