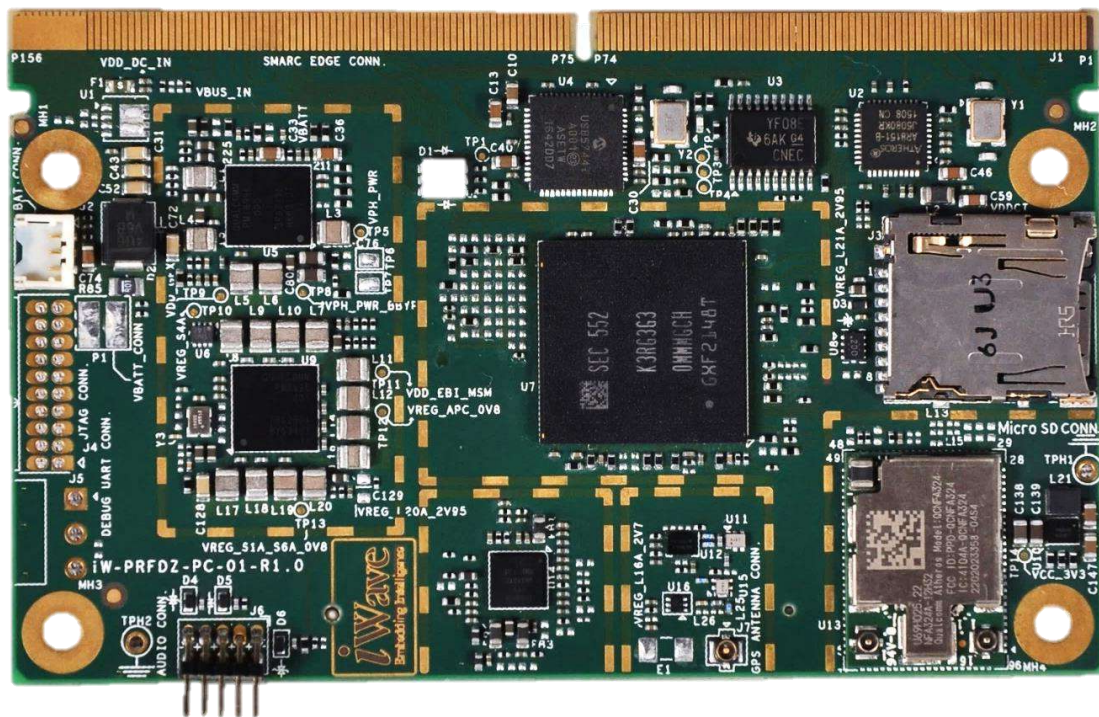


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Snapdragon 820 SMARC SOM

Hardware User Guide



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Snapdragon 820 SMARC SOM Hardware User Guide

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1. INTRODUCTION

1.1 Purpose

This document is the Hardware User Guide for the Snapdragon 820 SMARC SOM based on the Qualcomm APQ8096 Application processor. This board is fully supported by iWave Systems Technologies Pvt. Ltd. This Guide provides detailed information on the overall design and usage of the Snapdragon 820 SMARC SOM from a Hardware Systems perspective.

1.2 Snapdrgon 820 SMARC SOM Overview

The SMARC is a versatile small form factor computer Module definition targeting application that require low power, low costs, and high performance. The Module power envelope is typically under 6W although designs up to about 15W are possible.

Qualcomm Snapdragon 820 SoC based SMARC System on Module is rich with features and comes in compact 82mm x 50mm form factor. The Module PCBs have 314 edge fingers that mate with a low profile 314 pin 0.5mm pitch right angle connector. The SMARC Specification describes the functionality of all 314pins. The modular approach allows scalability, fast time to market and upgradability while still maintaining low costs, low power and small physical size.

1.3 List of Acronyms

The following acronyms will be used throughout this document.

Table 1: Acronyms & Abbreviations

Acronyms	Abbreviations
ARM	Advanced RISC Machine
BT	Bluetooth
CMOS	Complementary Metal-Oxide Semiconductor
CPU	Central Processing Unit
CSI	Camera Serial Interface
DSI	Display Serial Interface
eMMC	Enhanced Multi Media Card
GB	Giga Byte
Gbps	Gigabits per sec
GNSS	Global Navigation Satellite System
GPIO	General Purpose Input Output
GPS	Global Positioning System
I2C	Inter-Integrated Circuit
IC	Integrated Circuit
LPDDR	Low Power Double Data Rate
MHz	Mega Hertz

Acronyms	Abbreviations
MIPI	Mobile Industry Processor Interface
PCB	Printed Circuit Board
PDM	Pulse Density Modulation
PoP	Package on Package
RF	Radio Frequency
RoHS	Restriction of Hazardous Substances
RTC	Real Time Clock
SD	Secure Digital
SDRAM	Synchronous Dynamic Random Access Memory
SMARC SOM	Smart Mobility ARChitecture
SPMI	Serial power management interface
TBD	To Be Defined
UART	Universal Asynchronous Receiver/Transmitter
USF	Universal Flash Storage
USB	Universal Serial Bus
USB OTG	USB On The Go
V	Voltage
Wi-Fi	Wireless Fidelity

1.4 Terminology Description

In this document, wherever Signal Type is mentioned, below terminology is used.

Table 2: Terminology

Terminology	Description
I	Input Signal
O	Output Signal
IO	Bidirectional Input/output Signal
CMOS	Complementary Metal Oxide Semiconductor Signal
DIFF	Differential Signal
LVDS	Low Voltage Differential Signal
OD	Open Drain Signal
OC	Open Collector Signal
Power	Power Pin
PU	Pull Up
PD	Pull Down
NA	Not Applicable
NC	Not Connected

Note: Signal Type does not include internal pull-ups or pull-downs implemented by the chip vendors and only includes the pull-ups or pull-downs implemented On-SMARC SOM.

1.5 References

- APQ8096 Hardware User Manuals.
- SMARC Specification V2.0

1.6 Important Note

In this document, wherever APQ8096 CPU signal name is mentioned, it is followed as per below format for easy understanding.

- If CPU pin has multiplexing option and selected particular function, then the signal name is mentioned as **“Selected Function Name (GPIO Number)”**

Example: *BLSP8_UART_TX(GPIO_4)*

In this signal, ***BLSP8_UART_TX*** is the functionality which we are using and ***GPIO_4*** is the GPIO number.

- If CPU pin has multiplexing option and selected as GPIO function, then the signal name is mentioned as **“GPIO_Functionality Description(GPIO Number)”**

Example: *GPIO_SDC2_WP(GPIO_23)*

In this signal, ***SDC2_WP*** is the GPIO functionality which we are using and ***GPIO_23*** is the GPIO number.

- If CPU pin doesn't have multiplexing option, then the signal name is mentioned as, **“Function name”**

Example: *SPMI_CLK*

In this signal, functionality which we are using ***SPMI_CLK***

Note: The above naming is not applicable for other signals which are not connected to CPU.

2. ARCHITECTURE AND DESIGN

This section provides detailed information about the Snapdragon 820 SMARC SOM features and Hardware architecture with high level block diagram.

2.1 Snapdragon 820 SMARC SOM Block Diagram

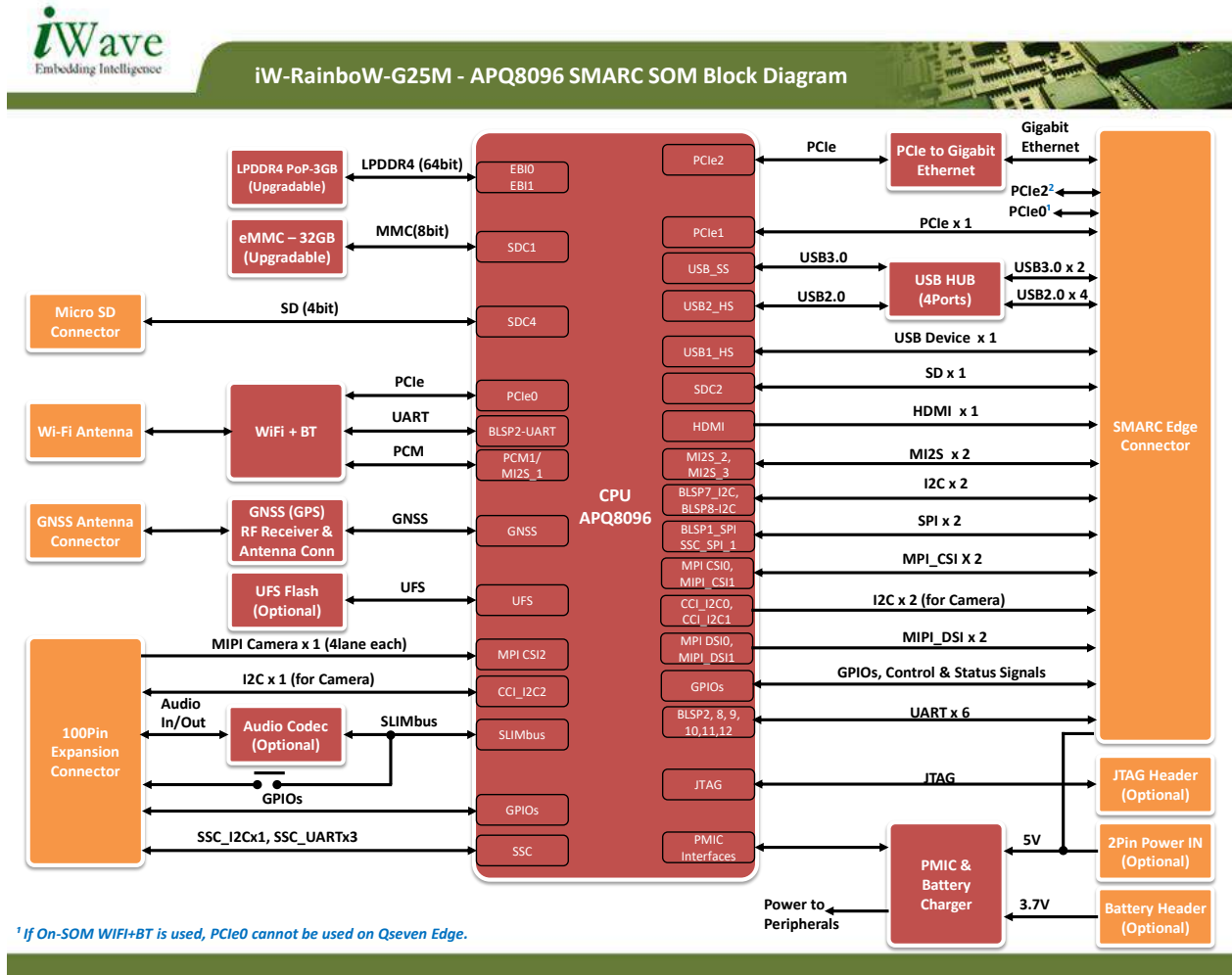


Figure 1: Snapdragon 820 SMARC SOM Block Diagram

2.2 Snapdragon 820 SMARC SOM Features

Snapdragon 820 SMARC SOM supports the following features.

CPU

- APQ8096, 64-bit Quad Kryo Snapdragon 820 CPU (without Modem)
 - Dual Kryo cores Gold cluster @ (2.15 GHz)
 - Dual Kryo cores Silver cluster @ (1.6 GHz)

Power Management

- PM8996 PMIC
- PMI8996 Battery Charger

Memory

- 3GB LPDDR4 (Expandable to 6GB)
- 32GB eMMC (Expandable to 128GB)
- Micro SD Slot

Network & Communication

- Wi-Fi and Bluetooth Module
- GPS Module
- USB3.0 Hub 1:4 Ports
- PCIe to Ethernet Bridge

On Board Switches

- VOL+ Switch
- RST/VOL- Switch

SMARC Edge Connector Interface

- MIPI CSI - 2 lanes x 1 Port
- MIPI CSI - 4 lanes x 1 Port
- Gigabit Ethernet x 1 Port
- SD (4bit) x 1 Port
- AC'97 or I2S Audio x 2 Port
- SPI x 2 Port
- USB2.0 x 2 Port
- USB3.0 x 2 Port
- USB OTG x 1 Port
- PCIe x 1 Port
- HDMI x 1 Port

- MIPI DSI - 4 lanes x 2 Port
- Debug UART x1 Ports
- Data UART (with CTS & RTS) x 2 Ports
- Data UART (without CTS & RTS) x1 Ports
- SMARC GPIOs
- Power control & Management signals

Expansion Connectors Interface

- MIPI CSI - 4 lanes x 1 Port
- SSC_UART x 3 Port
- SSC_I2C x 1 Port
- SLIMBUS x 1 Port
- Audio Code Inputs and Outputs (Optional)
- GPIO

Optional Features

- Audio Codec
- UFS (Universal Flash Storage)
- Debug UART Header
- Battery Connector
- JTAG Header

General Specification

- Power Supply : 5V,3A
- Form Factor : 82mm X 50mm (SMARC V2.0 Specification)

2.3 Qualcomm APQ8096 CPU

The Snapdragon 820 SMARC SOM is based on APQ8096 CPU with built-in 64-bit ARMv8-compliant Quad Core (Dual Kryo Gold cluster cores running @ 2.15 GHz and Dual Kryo Silver cluster cores running @ 1.6 GHz). The Kryo CPU uses Qualcomm® Symphony System Manager as an intelligent resource management tool for Snapdragon that extends control of task scheduling and power management across the entire processor.

The Hexagon 680 DSP enables the CPU to offload many tasks for more efficient processing. Featuring Qualcomm All-Ways Aware™ technology, the Hexagon 680 DSP also allows for ultra-low power “always-on” sensors and advanced low power-image processing.

The Adreno 530 in the Snapdragon 820 processor along with the Kryo CPU are capable of generating photorealistic graphics for console-quality gaming and next-generation virtual reality apps, while delivering up to 40% improvement to graphics performance and compute capabilities when compared to the Adreno 430.

Note: Please refer the latest APQ8096 Datasheet & Reference Manual for Electrical characteristics and other information related to APQ8096 CPU which may be revised from time to time.

2.4 Power Management

2.4.1 PM8996 PMIC

Snapdragon 820 SMARC SOM supports Qualcomm's PM8996 PMIC for SMARC SOM power management. The versatile design is suitable for multimode, multiband phones, and other wireless products such as data cards and PDAs. The PM8996 mixed-signal BiCMOS device is available in the 225-pin wafer-level nanoscale package (225 WLNSP) that includes ground pins for improved electrical ground, mechanical stability, and thermal continuity. The PM8996 PMIC provides all required power to APQ8096 CPU and on board peripherals. This PMIC supports up to 12 switch mode regulators, 32 linear regulators, on chip ADCs, Clock Sources, GPIOs and RTC charging.

Dedicated Serial power management interface (SPMI) used between CPU and PMIC for controlling and programming the PMIC.

2.4.2 PMI8996 Battery Charging IC

The PMI8996 supplements the PM8996 device to integrate all wireless power management requirements. PMIC is powered through PMI8996 IC, the main power is directly connected to PMI8996 for Input power management, Output power management, battery monitoring and charging.

The PMI8996 mixed-signal BiCMOS device is available in the 210-pin wafer-level nanoscale package (210 WLNSP) that includes ground pins for improved electrical ground, mechanical stability, and thermal conductivity.

2.5 Memory

2.5.1 LPDDR4 RAM

The Snapdragon 820 SMARC SOM supports 3GB LPDDR4 RAM in PoP package by default. The PoP memory provides four 16-bit channels combining to form two 32-bit channels on the CPU. The package-on-package implementation adds LPDDR4 SDRAM memory without increasing the device's footprint or PCB area. APQ8096 CPU is the first QTI device to support LPDDR4 memory. Each LPDDR4 die contains two independent channels as specified by JEDEC and supports for 6 Gb/8 Gb/12 Gb/16 Gb LPDDR4 SDRAM device.

2.5.2 eMMC Flash

The Snapdragon 820 SMARC SOM supports 32GB eMMC as default boot device and storage. This is connected to SDC1 controller of the APQ8096 CPU and operates at 1.8V (I/O supply) and 2.95V (NAND core supply) Voltage levels.

The eMMC flash (U24) memory is physically located on bottom side of the SMARC SOM. The memory size of the eMMC Flash can be expandable and the APQ8096 CPU supports eMMC version 5.1V

2.5.3 Micro SD Connector slot

The Snapdragon 820 SMARC SOM supports Micro SD slot which can be used to connect Micro SD card as Mass storage. Micro SD card connector (J3) is directly connected to the SDC4 controller of the APQ8096 CPU. The main power to Micro SD Card Connector is 2.95 Voltage. Micro SD Connector is physically located on Top side of the Snapdragon 820 SMARC SOM as shown below.

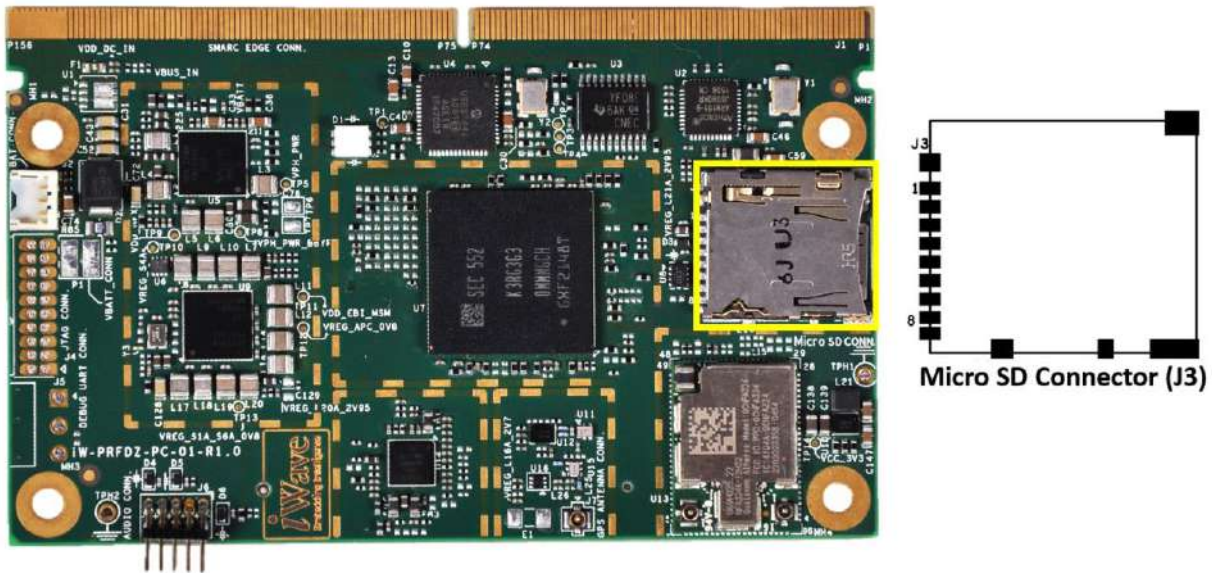


Figure 2: Micro SD Connector

Table 3: Micro SD Connector Pin Out

Pin No	Pin Name	Signal Name	Signal Type/ Termination	Description
1	DAT2	SDC4_DATA_2(GPIO_94)	IO 1.8 V CMOS	SD Interface Data Line2.
2	DAT3	SDC4_DATA_3(GPIO_92)	IO 1.8 V CMOS	SD Interface Data Line3.
3	CMD	SDC4_CMD(GPIO_91)	IO 1.8 V CMOS	SD Interface Command Line.
4	VDD	GND	O, 2.95V Power	2.95V Supply Voltage.
5	CLK	SDC4_CLK(GPIO_93)	IO 1.8 V CMOS	SD Interface Clock.
6	VSS	GND	Power	Ground.
7	DAT0	SDC4_DATA_0(GPIO_96)	IO 1.8 V CMOS	SD Interface Data Line0.
8	DAT1	SDC4_DATA_1(GPIO_95)	IO 1.8 V CMOS	SD Interface Data Line1.
9	CDB	SDC4_CD_N(GPIO_26)	I, 1.8V CMOS /1M PU	SD Interface Card Detect.
10	CDA	GND	Power	Ground.
11	M1	GND	Power	Ground.
12	M2	GND	Power	Ground.
13	M3	GND	Power	Ground.

2.6 Network & Communication

2.6.1 Wi-Fi and Bluetooth Interface

The Snapdragon 820 SMARC SOM integrated with Qualcomm Atheros QCA6174A-1 based Wi-Fi& Bluetooth module using PCIe and UART interface to supports wireless local area network (WLAN) and Bluetooth (BT) combo solution to support 2x2 MIMO with IEEE802.11a/b/g/n/ac WLAN standards and BT4.1+HS enabling seamless integration of WLAN/BT and Low Energy technology. Two antennas can be connected on the module for good signal strength, ANT1 is for WLAN/BT and ANT2 is for WLAN only. MHF-4 Micro RF Coaxl connectors are used for interfacing the RF antenna as shown below. Example of RF connector P/N: 20449-001E (MHF-4).

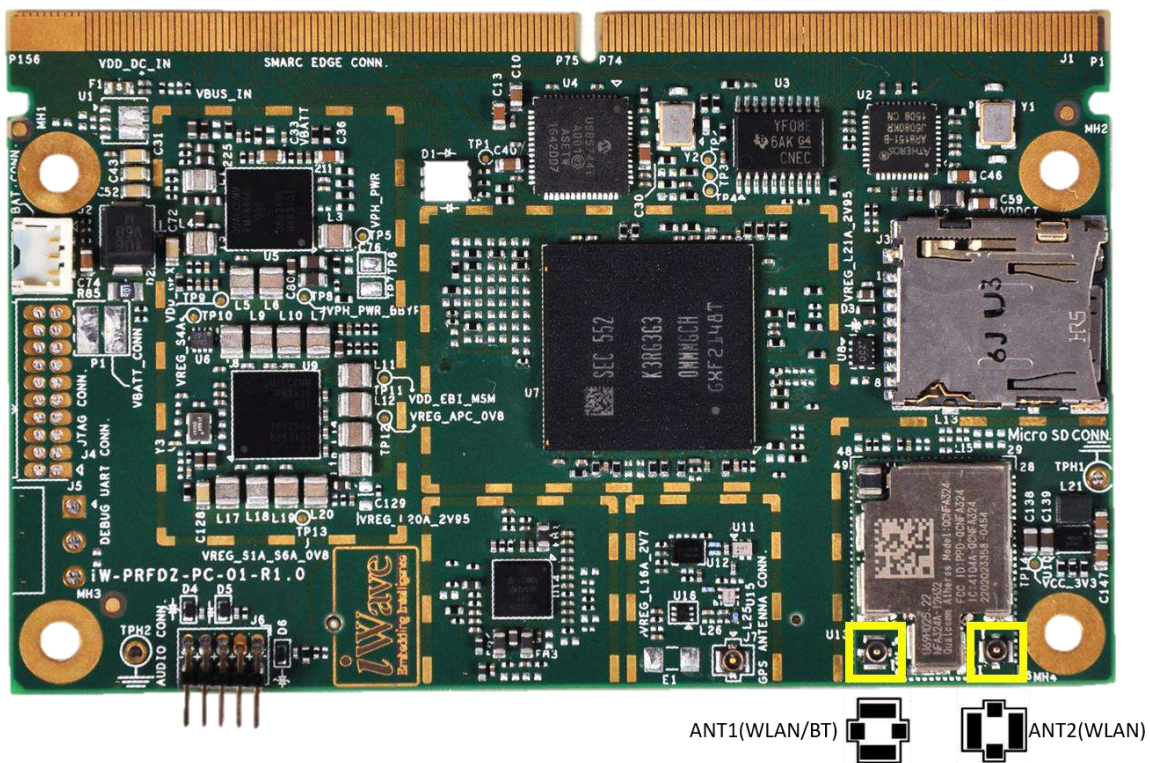


Figure 3: WLAN/BT Antenna Connector

2.6.2 GPS Interface

The Snapdragon 820 SMARC SOM supports GPS through WGR7640 chipset. The WGR7640 IC is a dedicated GNSS RF receiver and fabricated using an advanced RF CMOS process that accommodates high-frequency, high-precision analog circuits and low-power CMOS functions. Also, WGR7640 chip is dedicated for GNSS receiver input for GPS, GLONASS and COMPASS operations. RF antenna need to be connected for better GPS locking function. MHF-4 Micro R Coax connector is used for interfacing the GPS antenna (J7) as shown in below figure.

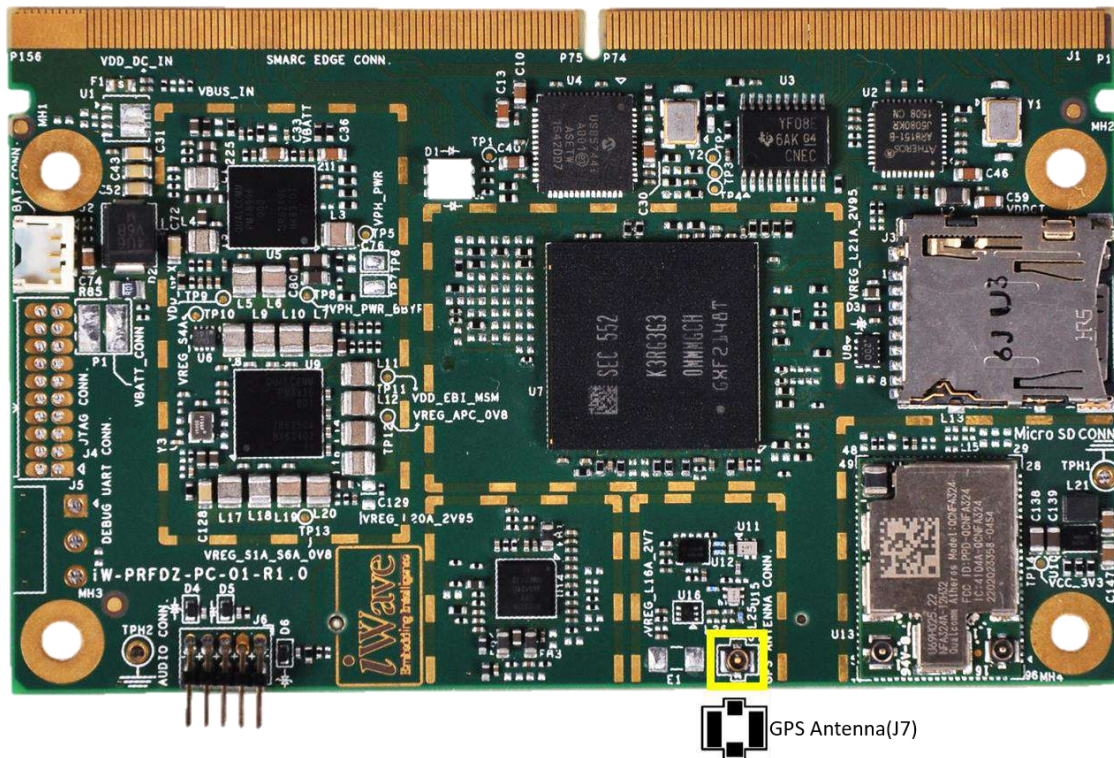


Figure 4: GPS Antenna Connector

2.7 SMARC PCB Edge Connector

SAMRC PCB edge connector has standard pin out as per SMARC Specification 2.0. The interfaces which are available at 314pin SMARC Edge connector are explained in the following sections.

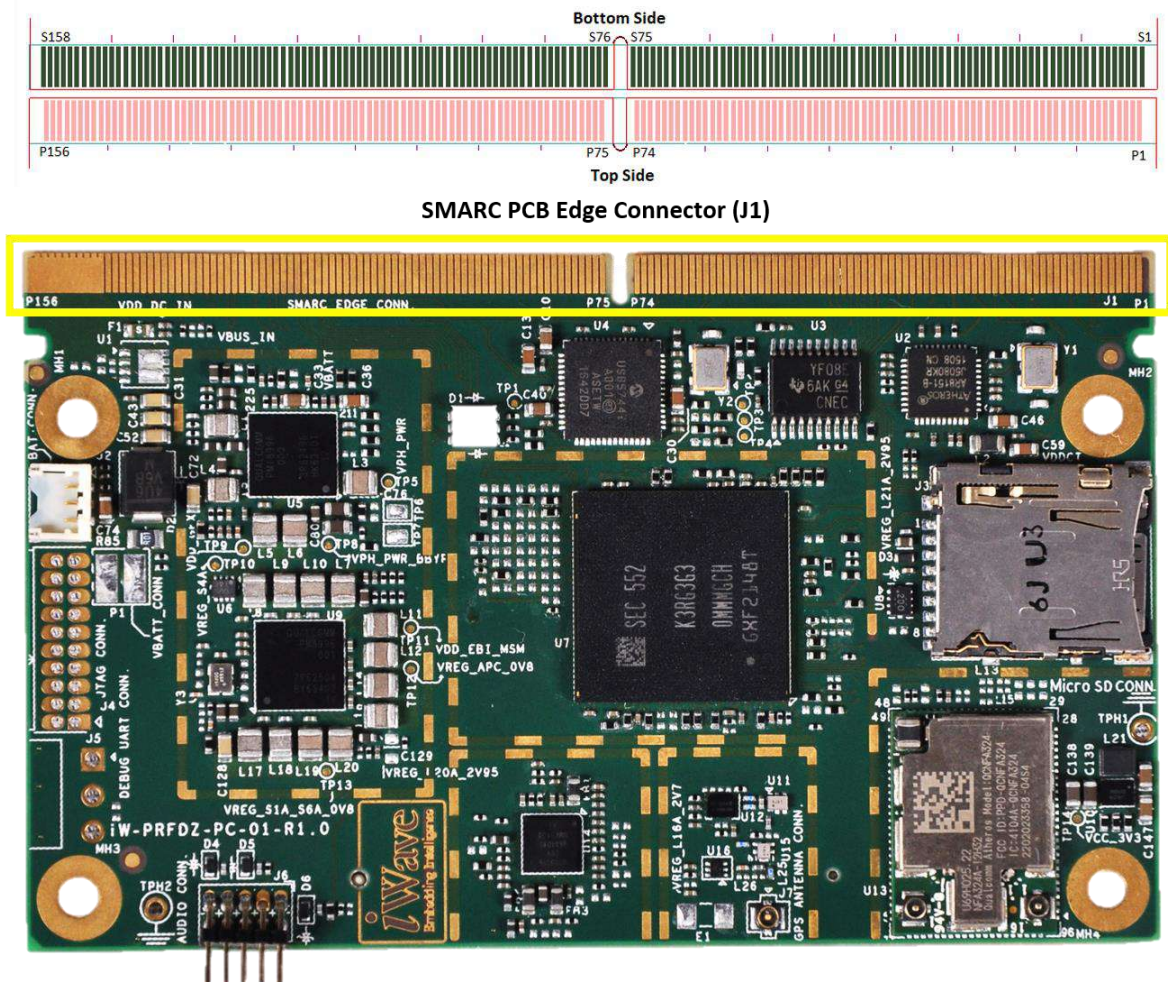


Figure 5: SMARC Edge Connector

Number of Pins -	: 314
Connector Part -	: Not Applicable (On Board PCB Edge connector)
Mating Connector -	: 91782-3140M-001 from Aces

2.7.1 Gigabit Ethernet

The Snapdragon 820 SMARC SOM supports Gigabit Ethernet using on SOM PCIe to Gigabit Ethernet Bridge “AR8151” from Atheros, Qualcomm. The AR8151-B is an ultra-high performance, ultra-low cost, and ultra-low power fully integrated 10/100/1000Mbps NIC/LOM Ethernet controller. The AR8151-B is compliant with IEEE 802.3u specification for 10/100 Mbps Ethernet and IEEE 802.3ab specification for 1000 Mbps Ethernet. The AR8151-B device combines pulse shaping, Tx/Rx PCS, echo canceller, NEXT canceller, equalizer, decoder, and timing recovery functions to deliver robust signal performance in noisy environments. The AR8151-B GbE controller supports checksum offload features for IP, TCP, and UDP, lowering CPU utilization and optimizing network performance. The Output of PCIe to Gigabit Ethernet Bridge is connected to GBE0 Port of SMARC edge connector.

For more details on SMARC Edge GBE0 pinouts, refer SAMRC Edge connector pins P19, P20, P21, P22, P23, P24, P25, P26, P27, P28, P29 & P30 on Table 6.

2.7.2 SD Interface

The Snapdragon 820 SMARC SOM supports 4bit SD interface over SMARC PCB Edge connector. which can be used to connect SD card as Mass storage or optional boot device. SDC2 controller of the APQ8096 CPU.is used to support SMARC SD interface. SDC2 supports maximum of 208 Mbit/s per line and it operates both in 3.3V and 1.8V IO level.

For more details on SMARC Edge SD pinouts, refer SAMRC Edge connector pins P33, P34, P35, P36, P37, P39, P40, P41 & P42 on Table 6.

2.7.3 Audio Interface

There are two I2S interface types supported by the APQ8096. Legacy I2S interfaces for primary and secondary microphones and speakers. Second one is multiple I2S (MI2S) interface for microphone and speaker functions, including 7.1 audio for HDMI. The Snapdragon 820 SMARC SOM supports I2S0 and I2S1 channels of SMARC Edge connector from CPU’s MI2S_2 and MI2S_3 channels respectively.

For more details on SMARC Edge SD pinouts, refer SAMRC Edge connector pins S38, S39, S40, S41, S42, S50, S51, S52 & S53 on Table 6.

2.7.4 SPI Interface

The APQ8096 supports SPI as a master only with maximum clock speed of 50MHz. The Snapdragon 820 SMARC SOM supports SPI0 and ESPI channels from the SMARC Edge connector with BLSP1_SPI and BLSP1_SPI respectively.

For more details on SMARC Edge SPI pinouts, refer SAMRC Edge connector pins P43, P44, P45, P46, P31, P54, P55, P56, P57 & P58 on Table 6.

2.7.5 USB Interface

The APQ8096 supports two USB2.0 OTG and one USB3.0 OTG. In Snapdragon 820 SMARC SOM USB1 OTG is directly connected to OTG pins of SMARC Edge connector which even can be used for debugging and flashing the CPU. USB2 and USB3 of APQ8096 CPU is connected to on SOM USB3.0 hub USB5744-I/2G from Microchip. USB Hub Feature Controller IC with 4 USB 3.1 Gen 1 / USB 2.0 downstream ports. The upstream ports are connected to SMARC Edge connector as well as Expansion connectors.

For more details on SMARC Edge USB pinouts, refer SAMRC Edge connector pins P60, P61, P62, P63, P64, P65, P66, P67, P69, P70, P71, P74, P76, S35, S36, S62, S63, S65, S66, S68, S69, S71, S72, S74 and S75 on Table 6.

Refer expansion connectors pin 8, 10, 14, 16, 20, 22, 26 & 28 other SS signals of USB Hub upstream board 3 and 4.

2.7.6 PCIe Interface

The APQ8096 supports three PCI Express Specification, Revision 2.1 channels. In Snapdragon 820 SMARC SOM PCIe0 is directly connected to PCIe to Wi-Fi Bridge and PCIe2 is directly connected PCIe to Gigabit Ethernet Bridge where as PCIe1 is directly connected to SAMRC PCIe A Port pins along with other controlling signals. PCIe0 and PCIe2 channel are also has an option to connected SMARC Edge connector provided Wi-Fi and Ethernet will not be supported.

For more details on SMARC Edge PCIe pinouts, refer SAMRC Edge connector pins P75, P80, P81, P83, P84, P86, P87, P89, P90, S76, S77, S78, S79, S81, S82, S84, S85, S87, S88, S90, S91 & S146 on Table 6.

2.7.7 HDMI Interface

APQ8096 CPU supports HDMI 2.0 audio/video out. Which includes Integrated HDMI Tx core and HDMI PHY, 1080p at 60 Hz refresh and 24-bit RGB colour, 4 K ×2 K at 60 fps + 4 K ×2 K at 30 fps HDMI, Up to eight-channel audio for 7.1 surround sound, Dolby Digital Plus, Dolby True-HD, and DTS-HD Master.

For more details on SMARC Edge HDMI pinouts, refer SAMRC Edge connector pins P92, P93, P95, P96, P98, P99, P101, P102, P104, P105 and P106 on Table 6.

2.7.8 MIPI DSI Display Interface

The APQ8096 CPU supports up to two 4-lane Display interfaces, which supported MIPI_DSI standards and MIPI Alliance Specification for Display Serial Interface D-PHY V1.2. The Snapdragon 820 SMARC SOM supports both Four lane MIPI DSI via SMARC Edge connector.

For more details on SMARC Edge DSI pinouts, refer SAMRC Edge connector S107, S108, S109, S111, S112, S114, S115, S116, S117, S118, S120, S121, S122, S125, S126, S127, S128, S129, S131, S132, S133, S134, S135, S137, S138, S139, S140 & S141 on Table 6.

2.7.9 MIPI CSI Camera

The APQ8096 CPU supports up to three 4-lane camera interfaces, which supported MIPI_CSI standards and exceptions CSI-2 v1.3, DPHY v1.2 (at 2.0 Gbps per lane) and CPHY v1.0. (three three-trio CPHY1.0 at 17 Gbps). CPHY1.0 is a new feature on the APQ8096 chipset that supports single-ended signalling with an embedded clock (three wires per trio). The Snapdragon 820 SMARC SOM supports one two lanes and one four lane MIPI CSI camera interface via SMARC Edge connector and one four lane camera over expansion connector along with the other controlling signals.

For more details on SMARC Edge CSI pinouts, refer SAMRC Edge connector pins S1, S2, S5, S6, S7, S8, S9, S11, S12, S14, S15, P3, P4, P7, P8, P10, P11, P13, P14, P16 & P17 on Table 6.

2.7.10 Data UART

SMARC V2.0 supports four UART channels where two channels SER0 & SER2 are with CTS and RTS and two channels SER1 & SER3 are without. The APQ8096 CPU's BLSP9, BLSP10 & BLSP11 are connected SER0, SER1 & SER2 channels of SMARC Edge connector respectively. Which can be used for any data communication. Whereas BLSP8 UART is used as Debug UART. Which will give the boot long and terminal access to the CPU. In Snapdragon 820 SMARC SOM BLSP8 UART is connected to SER3 UART channel of SMARC Edge connector.

For more details on SMARC Edge UART pinouts, refer SAMRC Edge connector P129, P130, P131, P132, P134, P135, P136, P137, P138, P139, P140 & P141 pins on Table 6.

2.7.11 SMARC GPIOs

SMARC V2.0 supports 12 GPIO, which can be used for any general-purpose application. But for first six GPIOs SMARC specification describe the functionality. Hence its recommend to use for same if supported.

For more details on SMARC Edge GPIO pinouts, refer SAMRC Edge connector P108, P109, P110, P111, P112, P113, P114, P115, P116, P117, P118 & P119 pins on Table 6.

2.7.12 Power control & Management signals

SMARC V2.0 specification supports System and Power & Management Signals. For more details on SMARC Edge Power & Management Signals pinouts, refer SAMRC Edge connector P123, P124, P125, P126, P127, P128, S145, S147, S150, S153, S154 & S155 pins on Table 6.

Table 4: 314-Pin PCB Edge Connector Pin Assignment

Pin No.	SMARC Edge Connector Pin Name	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
P1	SMB_ALERT_1V8#	SMB_ALERT(GPI O_14)	GPIO_14/ BE7	I, 1.8V CMOS	SM Bus Alert# (interrupt) signal
P2	GND	GND	NA	Power	Ground.
P3	CSI1_CK+	MIPI_CSI1_DCLK _P	MIPI_CSI1_DCLK_P /BE5	I, DIFF	MIPI CSI1 differential clock positive
P4	CSI1_CK-	MIPI_CSI1_DCLK _M	MIPI_CSI1_DCLK_M /BD6	I, DIFF	MIPI CSI1 differential clock negative
P5	GBE1_SDP	NC	NA	NA	NC
P6	GBE0_SDP	NC	NA	NA	NC
P7	CSI1_RX0+	MIPI_CSI1_DLN 0_P	MIPI_CSI1_DLN0_P /BD4	I, DIFF	MIPI CSI1 differential data lane 0 positive
P8	CSI1_RX0-	MIPI_CSI1_DLN 0_M	MIPI_CSI1_DLN0_ M/BC7	I, DIFF	MIPI CSI1 differential data lane 0 negative
P9	GND	GND	NA	Power	Ground.
P10	CSI1_RX1+	MIPI_CSI1_DLN 1_P	MIPI_CSI1_DLN1_P /BC5	I, DIFF	MIPI CSI1 differential data lane 1 positive
P11	CSI1_RX1-	MIPI_CSI1_DLN 1_M	MIPI_CSI1_DLN1_ M/BB6	I, DIFF	MIPI CSI1 differential data lane 1 negative
P12	GND	GND	NA	Power	Ground.
P13	CSI1_RX2+	MIPI_CSI1_DLN 2_P	MIPI_CSI1_DLN2_P /BA7	I, DIFF	MIPI CSI1 differential data lane 2 positive
P14	CSI1_RX2-	MIPI_CSI1_DLN 2_M	MIPI_CSI1_DLN2_ M/BA5	I, DIFF	MIPI CSI1 differential data lane 2 negative
P15	GND	GND	NA	Power	Ground.
P16	CSI1_RX3+	MIPI_CSI1_DLN 3_P	MIPI_CSI1_DLN3_P /AY6	I, DIFF	MIPI CSI1 differential data lane 3 positive
P17	CSI1_RX3-	MIPI_CSI1_DLN 3_M	MIPI_CSI1_DLN3_ M/AY4	I, DIFF	MIPI CSI1 differential data lane 3 negative
P18	GND	GND	NA	Power	Ground.
P19	GBE0_MDI3-	GBE0_MDI3-	NA	IO, DIFF	Gigabit Ethernet MDI differential pair 3 negative.
P20	GBE0_MDI3+	GBE0_MDI3+	NA	IO, DIFF	Gigabit Ethernet MDI differential pair 3 positive.
P21	GBE0_LINK100#	GBE0_LINK100#	NA	O, 3.3V CMOS	100Mbps Ethernet link status LED
P22	GBE0_LINK1000#	GBE0_LINK1000 #	NA	O, 3.3V CMOS	Gigabit Ethernet link status LED
P23	GBE0_MDI2-	GBE0_MDI2-	NA	IO, DIFF	Gigabit Ethernet MDI differential pair 2 negative.
P24	GBE0_MDI2+	GBE0_MDI2+	NA	IO, DIFF	Gigabit Ethernet MDI differential pair 2 positive.

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Pin No.	SMARC Edge Connector Pin Name	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
P25	GBEO_LINK_ACT#	GBEO_LINK_ACT#	NA	O, 3.3V CMOS	Gigabit Ethernet activity status
P26	GBEO_MDI1-	GBEO_MDI1-	NA	IO, DIFF	Gigabit Ethernet MDI differential pair 1 negative.
P27	GBEO_MDI1+	GBEO_MDI1+	NA	IO, DIFF	Gigabit Ethernet MDI differential pair 1 positive.
P28	GBEO_CTREF	VDDCT	NA	Power	Power for the Centre Tap of Mack Jack connector
P29	GBEO_MDIO-	GBEO_MDIO-	NA	IO, DIFF	Gigabit Ethernet MDI differential pair 0 negative.
P30	GBEO_MDIO+	GBEO_MDIO+	NA	IO, DIFF	Gigabit Ethernet MDI differential pair 0 positive.
P31	SPIO_CS1#	BLSP1_SPI_CS1_N(GPIO_90)	GPIO_90/ W3	O, 1.8V CMOS	SPIO Chip Select 1
P32	GND	GND	NA	Power	Ground.
P33	SDIO_WP	SDIO_WP	GPIO_23/ L5	I, 3.3V CMOS	SDC write Protect.
P34	SDIO_CMD	SDC2_CMD	SDC2_CMD/ AD6	IO, 1.8/3.3V CMOS	SD command.
P35	SDIO_CD#	SDIO_CD#	GPIO_38/ BJ47	I, 3.3V/ CMOS	SD Card Detect.
P36	SDIO_CLK	SDC2_CLK	SDC2_CLK/ AE5	O, 1.8/3.3V CMOS	SD Clock.
P37	SDIO_PWR_EN	SDIO_PWR_EN	GPIO_29/ BG3	O, 3.3V CMOS	SD Power enable.
P38	GND	GND	NA	Power	Ground.
P39	SDIO_D0	SDC2_DATA_0	SDC2_DATA_0/ AD8	IO, 1.8/3.3V CMOS	SD data 0.
P40	SDIO_D1	SDC2_DATA_1	SDC2_DATA_1/ AC5	IO, 1.8/3.3V CMOS	SD data 1
P41	SDIO_D2	SDC2_DATA_2	SDC2_DATA_2/ AE7	IO, 1.8/3.3V CMOS	SD data 2
P42	SDIO_D3	SDC2_DATA_3	SDC2_DATA_3/ AF6	IO, 1.8/3.3V CMOS	SD data 3
P43	SPIO_CS0#	BLSP1_SPI_CS_N(GPIO_2)	GPIO_2/ H6	O, 1.8V CMOS	SPIO Chip Select 0
P44	SPIO_CLK	BLSP1_SPI_CLK(GPIO_3)	GPIO_3/ H8	O, 1.8V CMOS	SPIO Clock
P45	SPIO_DIN	BLSP1_SPI_MISO(GPIO_1)	GPIO_1/ G7	I, 1.8V CMOS	SPIO Master IN Slave Out

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Pin No.	SMARC Edge Connector Pin Name	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
P46	SPI0_DO	BLSP1_SPI_MOS I(GPIO_0)	GPIO_0/ G5	O, 1.8V CMOS	SPI0 Master Out Slave In
P47	GND	GND	NA	Power	Ground.
P48	SATA_TX+	NC	NA	NA	NA
P49	SATA_TX-	NC	NA	NA	NA
P50	GND	GND	NA	Power	Ground.
P51	SATA_RX+	NC	NA	NA	NA
P52	SATA_RX-	NC	NA	NA	NA
P53	GND	GND	NA	Power	Ground.
P54	ESPI_CS0#	SSC_SPI_1_CS_N(SSC_8)	SSC_8/ C33	O, 1.8V CMOS	SSC_SPI_1 Chip Select 0
P55	ESPI_CS1#	SSC_SPI_1_CS1_N(SSC_0)	SSC_0/ D36	O, 1.8V CMOS	SSC_SPI_1 Chip Select 1
P56	ESPI_CK	SSC_SPI_1_CLK(SSC_9)	SSC_9/ E33	O, 1.8V CMOS	SSC_SPI_1 Clock
P57	ESPI_IO_0	SSC_SPI_1_MOS I(SSC_10)	SSC_10/ D32	IO, 1.8V CMOS	SSC_SPI_1 Master Out Slave IN
P58	ESPI_IO_1	SSC_SPI_1_MIS O(SSC_11)	SSC_11/ C35	IO, 1.8V CMOS	SSC_SPI_1 Master IN Slave Out
P59	GND	GND	NA	Power	Ground.
P60	USB0+	USB1_HS_DP	USB1_HS_DP/ AA3	IO, DIFF	USB Port0 Data Positive
P61	USB0-	USB1_HS_DM	USB1_HS_DM/ AB4	IO, DIFF	USB Port0 Data Negative
P62	USB0_EN_OC#	USB0_EN_OC#(GPIO_21)	GPIO_21/ H2	IO, 3.3V CMOS	USB Port0 Power Enable/ Over Current Indicator <i>Note: Connected via 1.8 to 3.3V level Translator</i>
P63	USB0_VBUS_DET	USB0_VBUS_DET	NA`	5V, Power	USB host power detection, when this port is used as a device.
P64	USB0_OTG_ID	USB0_OTG_ID	NA	I, 3.3V CMOS	Connected to PMI IC
P65	USB1+	USB_HUB3OUT_DP	NA	IO, DIFF	USB Port1 Data Positive <i>Note: Connected to USB Hub</i>
P66	USB1-	USB_HUB3OUT_DM	NA	IO, DIFF	USB Port1 Data Negative <i>Note: Connected to USB Hub</i>
P67	USB1_EN_OC#	USB_HUB3_OC	NA	IO, 3.3V CMOS	USB Port1 Power Enable/ Over Current Indicator <i>Note: Connected to USB Hub</i>
P68	GND	GND	NA	Power	Ground.
P69	USB2+	USB_HUB1OUT_DP	NA	IO, DIFF	USB Port2 Data Positive <i>Note: Connected to USB Hub</i>

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Pin No.	SMARC Edge Connector Pin Name	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
P70	USB2-	USB_HUB1OUT_DM	NA	IO, DIFF	USB Port2 Data Negative Note: Connected to USB Hub
P71	USB2_EN_OC#	USB_HUB1_OC	NA	IO, 3.3V CMOS	USB Port2 Power Enable/ Over Current Indicator Note: Connected to USB Hub
P72	RSVD4	NC	NA	NA	NA
P73	RSVD5	NC	NA	NA	NA
P74	USB3_EN_OC#	USB_HUB2_OC	NA	IO, 3.3V CMOS	USB Port3 Power Enable/ Over Current Indicator Note: Connected to USB Hub
P75	PCIE_A_RST#	PCIE1_RST_N(GPIO_130)	GPIO_130/ C3	O, 3.3V CMOS	PCIE_A RESET Out Note: Connected via 1.8 to 3.3V level Translator
P76	USB4_EN_OC#	USB_HUB4_OC	NA	IO, 3.3V CMOS	USB Port4 Power Enable/ Over Current Indicator Note: Connected to USB Hub
P77	RSVD6	NC	NA	NA	NA
P78	RSVD7	NC	NA	NA	NA
P79	GND	GND	NA	Power	Ground.
P80	PCIE_C_REFCK+	NC	NA	NA	NC Note: Optionally connected to PCIE0_REFCLK_P
P81	PCIE_C_REFCK-	NC	NA	NA	NC Note: Optionally connected to PCIE0_REFCLK_M
P82	GND	GND	NA	Power	Ground.
P83	PCIE_A_REFCK+	PCIE1_REFCLK_P	PCIE1_REFCLK_P/ AK4	O, Diff	PCIE1 Clock Positive
P84	PCIE_A_REFCK-	PCIE1_REFCLK_M	PCIE1_REFCLK_M/ AL3	O, Diff	PCIE1 Clock Negative
P85	GND	GND	NA	Power	Ground.
P86	PCIE_A_RX+	PCIE1_RX_P	PCIE1_RX_P/ AK2	I, Diff	PCIE1 Receive Positive
P87	PCIE_A_RX-	PCIE1_RX_M	PCIE1_RX_M/ AJ3	I, Diff	PCIE1 Receive Negative
P88	GND	GND	NA	Power	Ground.
P89	PCIE_A_TX+	PCIE1_TX_P	PCIE1_TX_P/ AH2	O, Diff/ 0.1uF AC Couple	PCIE1 Transmit Positive
P90	PCIE_A_TX-	PCIE1_TX_M	PCIE1_TX_M/ AJ1	O, Diff/ 0.1uF AC Couple	PCIE1 Transmit Negative

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Pin No.	SMARC Edge Connector Pin Name	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
P91	GND	GND	NA	Power	Ground.
P92	HDMI_D2+ / DP1_LANE0+	HDMI_TX2_P	HDMI_TX2_P/ BE23	O, Diff	HDMI Transceiver 2 Positive
P93	HDMI_D2- / DP1_LANE0-	HDMI_TX2_M	HDMI_TX2_M/ BF22	O, Diff	HDMI Transceiver 2 Negative
P94	GND	GND	NA	Power	Ground.
P95	HDMI_D1+ / DP1_LANE1+	HDMI_TX1_P	HDMI_TX1_P/ BH22	O, Diff	HDMI Transceiver 1 Positive
P96	HDMI_D1- / DP1_LANE1-	HDMI_TX1_M	HDMI_TX1_M/ BG23	O, Diff	HDMI Transceiver 1 Negative
P97	GND	GND	NA	Power	Ground.
P98	HDMI_D0+ / DP1_LANE2+	HDMI_TX0_P	HDMI_TX0_P/ BJ23	O, Diff	HDMI Transceiver 0 Positive
P99	HDMI_D0- / DP1_LANE2-	HDMI_TX0_M	HDMI_TX0_M/ BH24	O, Diff	HDMI Transceiver 0 Negative
P100	GND	GND	NA	Power	Ground.
P101	HDMI_CK+ / DP1_LANE3+	HDMI_TCLK_P	HDMI_TCLK_P/ BH20	O, Diff	HDMI Transceiver CLK Positive
P102	HDMI_CK- / DP1_LANE3-	HDMI_TCLK_M	HDMI_TCLK_M/ BG21	O, Diff	HDMI Transceiver CLK Negative
P103	GND	GND	NA	Power	Ground.
P104	HDMI_HPD / DP1_HPD	HDMI_HOT_PLUG_DET(GPIO_34)	GPIO_34/ BG45	I, 1.8V CMOS	HDMI Hot Plug Detect
P105	HDMI_CTRL_CK / DP1_AUX+	HDMI_DDC_CLK (GPIO_32)	GPIO_32/ BH44	O, 1.8V CMOS	HDMI I2C Clock
P106	HDMI_CTRL_DAT / DP1_AUX-	HDMI_DDC_DATA(GPIO_33)	GPIO_33/ BH42	IO, 1.8V CMOS	HDMI I2C DATA
P107	DP1_AUX_SEL	NC	NA	NA	NA
P108	GPIO0 / CAM0_PWR#	SMARC_GPIO_0 (GPIO_73)	GPIO_73/ E9	IO, 1.8V CMOS	SMARC General Purpose Input/output 0
P109	GPIO1 / CAM1_PWR#	SMARC_GPIO_1 (GPIO_89)	GPIO_89/ T6	IO, 1.8V CMOS	SMARC General Purpose Input/output 1
P110	GPIO2 / CAM0_RST#	SMARC_GPIO_2 (GPIO_97)	GPIO_97/ AR49	IO, 1.8V CMOS	SMARC General Purpose Input/output 2
P111	GPIO3 / CAM1_RST#	SMARC_GPIO_3 (GPIO_98)	GPIO_98/ AP48	IO, 1.8V CMOS	SMARC General Purpose Input/output 3
P112	GPIO4 / HDA_RST#	SMARC_GPIO_4 (GPIO_100)	GPIO_100/ AP46	IO, 1.8V CMOS	SMARC General Purpose Input/output 4
P113	GPIO5 / PWM_OUT	SMARC_GPIO_5 (PM_GPIO4)	NA	IO, 1.8V CMOS	SMARC General Purpose Input/output 5 <i>Note: Connected to PMIC</i>

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Pin No.	SMARC Edge Connector Pin Name	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
P114	GPIO6 / TACHIN	SMARC_GPIO_6 (GPIO_106)	GPIO_106/ B24	IO, 1.8V CMOS	SMARC General Purpose Input/output 6
P115	GPIO7	SMARC_GPIO_7 (GPIO_107)	GPIO_107/ A25	IO, 1.8V CMOS	SMARC General Purpose Input/output 7
P116	GPIO8	SMARC_GPIO_8 (GPIO_108)	GPIO_108/ C25	IO, 1.8V CMOS	SMARC General Purpose Input/output 8
P117	GPIO9	SMARC_GPIO_9 (GPIO_109)	GPIO_109/ D24	IO, 1.8V CMOS	SMARC General Purpose Input/output 9
P118	GPIO10	SMARC_GPIO_10 (GPIO_110)	GPIO_110/ E23	IO, 1.8V CMOS	SMARC General Purpose Input/output 10
P119	GPIO11	SMARC_GPIO_11 (GPIO_111)	GPIO_111/ F26	IO, 1.8V CMOS	SMARC General Purpose Input/output 11
P120	GND	GND	NA	Power	Ground.
P121	I2C_PM_CLK	NC	NA	NA	NC <i>Note: optionally connected to BLSP8_I2C_CLK</i>
P122	I2C_PM_DAT	NC	NA	NA	NC <i>Note: optionally connected to BLSP8_I2C_DAT</i>
P123	BOOT_SEL0#	BOOT_SEL0#	NA	I, 1.8V CMOS	Boot Media Select bit 0
P124	BOOT_SEL1#	BOOT_SEL1#	NA	I, 1.8V CMOS	Boot Media Select bit 1
P125	BOOT_SEL2#	BOOT_SEL2#	NA	I, 1.8V CMOS	Boot Media Select bit 2
P126	RESET_OUT#	RESOUT_N	RESOUT_N / B26	I, 1.8V CMOS	RESOUT from CPU to all other peripherals
P127	RESET_IN#	RESIN_N_BTN	NA	I, 1.8V CMOS	Hard RESET Input to SOM <i>Note: Connected to PMIC</i>
P128	POWER_BTN#	POWER_ON_BTN	NA	I, 1.8V CMOS	Power ON /OFF Input to SOM <i>Note: Connected to PMIC</i>
P129	SER0_TX	BLSP9_UART_TX (GPIO_49)	GPIO_49/ BE49	O, 1.8V CMOS	BLSP9_UART Transmitter
P130	SER0_RX	BLSP9_UART_RX (GPIO_50)	GPIO_50/ BE51	I, 1.8V CMOS	BLSP9_UART Receiver
P131	SER0_RTS#	BLSP9_UART_RFR_N (GPIO_52)	GPIO_52/ BD50	O, 1.8V CMOS	BLSP9_UART Request to Send
P132	SER0_CTS#	BLSP9_UART_CTS_N (GPIO_51)	GPIO_51/ BD52	I, 1.8V CMOS	BLSP9_UART Clear to Send
P133	GND	GND	NA	Power	Ground.
P134	SER1_TX	BLSP10_UART_TX (GPIO_8)	GPIO_8/ BF50	O, 1.8V CMOS	BLSP10_UART Transmitter
P135	SER1_RX	BLSP10_UART_RX (GPIO_9)	GPIO_9/ BG51	I, 1.8V CMOS	BLSP10_UART Receiver

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Pin No.	SMARC Edge Connector Pin Name	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
P136	SER2_TX	BLSP11_UART_TX(GPIO_58)	GPIO_58/ AJ51	O, 1.8V CMOS	BLSP11_UART Transmitter
P137	SER2_RX	BLSP11_UART_RX(GPIO_59)	GPIO_59/ AJ49	I, 1.8V CMOS	BLSP11_UART Receiver
P138	SER2_RTS#	BLSP11_UART_REQUEST_N(GPIO_61)	GPIO_61/ AH50	O, 1.8V CMOS	BLSP11_UART Request to Send
P139	SER2_CTS#	BLSP11_UART_CLEAR_N(GPIO_60)	GPIO_60/ AH48	I, 1.8V CMOS	BLSP11_UART Clear to Send
P140	SER3_TX	BLSP8_UART_TX(GPIO_4)	GPIO_4/ BA49	O, 1.8V CMOS	Debug UART Transmitter <i>Note: Optionally connected to BLSP12_UART_TX</i>
P141	SER3_RX	BLSP8_UART_RX(GPIO_5)	GPIO_5/ BB48	I, 1.8V CMOS	Debug UART Receiver. <i>Note: Optionally connected to BLSP12_UART_RX</i>
P142	GND	GND	NA	Power	Ground.
P143	CAN0_TX	NC	NA	NA	NC
P144	CAN0_RX	NC	NA	NA	NC
P145	CAN1_TX	NC	NA	NA	NC
P146	CAN1_RX	NC	NA	NA	NC
P147	VDD_IN	VDD_IN	NA	I, 5V Power	Supply Voltage
P148	VDD_IN	VDD_IN	NA	I, 5V Power	Supply Voltage
P149	VDD_IN	VDD_IN	NA	I, 5V Power	Supply Voltage
P150	VDD_IN	VDD_IN	NA	I, 5V Power	Supply Voltage
P151	VDD_IN	VDD_IN	NA	I, 5V Power	Supply Voltage
P152	VDD_IN	VDD_IN	NA	I, 5V Power	Supply Voltage
P153	VDD_IN	VDD_IN	NA	I, 5V Power	Supply Voltage
P154	VDD_IN	VDD_IN	NA	I, 5V Power	Supply Voltage
P155	VDD_IN	VDD_IN	NA	I, 5V Power	Supply Voltage
P156	VDD_IN	VDD_IN	NA	I, 5V Power	Supply Voltage
S1	CSI1_TX+ / I2C_CAM1_CK	CCI_I2C1_SCL(GPIO_20)	GPIO_20/	O, 1.8V CMOS	MIPI CSI1 I2C Clock
S2	CSI1_TX- / I2C_CAM1_DAT	CCI_I2C1_SDA(GPIO_19)	GPIO_19/	IO, 1.8V CMOS	MIPI CSI1 I2C Data
S3	GND	GND	NA	Power	Ground.
S4	RSVD1	NC	NA	NA	NA
S5	CSI0_TX- / I2C_CAM0_CK	CCI_I2C0_SCL(GPIO_18)	GPIO_18/	O, 1.8V CMOS	MIPI CSI0 I2C Clock
S6	CAM_MCK	CLK1_OUT(GPIO_13)	GPIO_13/	O, 1.8V CMOS	Master Clock for Camera
S7	CSI0_TX+ / I2C_CAM0_DAT	CCI_I2C0_SDA(GPIO_17)	GPIO_17/	IO, 1.8V CMOS	MIPI CSI0 I2C Data

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S8	CSIO_CK+	MIPI_CSIO_DCLK_P	MIPI_CSIO_DCLK_P	I, DIFF	MIPI CSIO differential Clock positive
S9	CSIO_CK-	MIPI_CSIO_DCLK_M	MIPI_CSIO_DCLK_M	I, DIFF	MIPI CSIO differential Clock negative
S10	GND	GND	NA	Power	Ground.
S11	CSIO_RX0+	MIPI_CSIO_DLN0_P	MIPI_CSIO_DLN0_P	I, DIFF	MIPI CSIO differential data lane 0 positive
S12	CSIO_RX0-	MIPI_CSIO_DLN0_M	MIPI_CSIO_DLN0_M	I, DIFF	MIPI CSIO differential data lane 0 negative
S13	GND	GND	NA	Power	Ground.
S14	CSIO_RX1+	MIPI_CSIO_DLN1_P	MIPI_CSIO_DLN1_P	I, DIFF	MIPI CSIO differential data lane 1 positive
S15	CSIO_RX1-	MIPI_CSIO_DLN1_M	MIPI_CSIO_DLN1_M	I, DIFF	MIPI CSIO differential data lane 1 negative
S16	GND	GND	NA	Power	Ground.
S17	GBE1_MDI0+	NC	NA	NA	NA
S18	GBE1_MDI0-	NC	NA	NA	NA
S19	GBE1_LINK100#	NC	NA	NA	NA
S20	GBE1_MDI1+	NC	NA	NA	NA
S21	GBE1_MDI1-	NC	NA	NA	NA
S22	GBE1_LINK1000#	NC	NA	NA	NA
S23	GBE1_MDI2+	NC	NA	NA	NA
S24	GBE1_MDI2-	NC	NA	NA	NA
S25	GND	GND	NA	Power	Ground.
S26	GBE1_MDI3+	NC	NA	NA	NA
S27	GBE1_MDI3-	NC	NA	NA	NA
S28	GBE1_CTREF	NC	NA	NA	NA
S29	PCIE_D_TX+	NC	NA	NA	NA
S30	PCIE_D_TX-	NC	NA	NA	NA
S31	GBE1_LINK_ACT#	NC	NA	NA	NA
S32	PCIE_D_RX+	NC	NA	NA	NA
S33	PCIE_D_RX-	NC	NA	NA	NA
S34	GND	GND	NA	Power	Ground.
S35	USB4+	USB_HUB4OUT_DP	NA	IO, DIFF	USB Port4 Data Positive <i>Note: Connected to USB Hub</i>
S36	USB4-	USB_HUB4OUT_DM	NA	IO, DIFF	USB Port4 Data Negative <i>Note: Connected to USB Hub</i>
S37	USB3_VBUS_DET	NC	NA	NA	NA
S38	AUDIO_MCK	MI2S_2_MCLK(GPIO_79)	GPIO_79/ E11	O, 1.8V CMOS	Master Clock for Audio codec
S39	I2S0_LRCK	MI2S_2_WS(GPIO_81)	GPIO_81/ D8	O, 1.8V CMOS	I2S Channel0 Left Right Clock

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Pin No.	SMARC Edge Connector Pin Name	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
S40	I2S0_SDOUT	MI2S_2_D1(GPI O_83)	GPIO_83/ A9	O, 1.8V CMOS	I2S Channel0 Data Output
S41	I2S0_SDIN	MI2S_2_D0(GPI O_82)	GPIO_82/ C7	I, 1.8V CMOS	I2S Channel0 Data Input
S42	I2S0_CK	MI2S_2_SCK(GP IO_80)	GPIO_80/ E5	O, 1.8V CMOS	I2S Channel0 Clock
S43	ESPI_ALERT0#	NC	NA	NA	NA
S44	ESPI_ALERT1#	NC	NA	NA	NA
S45	RSVD2	NC	NA	NA	NA
S46	RSVD3	NC	NA	NA	NA
S47	GND	GND	NA	Power	Ground.
S48	I2C_GP_CK	BLSP7_I2C_SCL(GPIO_56)	GPIO_56/ BD46	O, 1.8V CMOS	General Purpose I2C Clock
S49	I2C_GP_DAT	BLSP7_I2C_SDA(GPIO_55)	GPIO_55/ BD48	IO, 1.8V CMOS	General Purpose I2C Data
S50	HDA_SYNC / I2S2_LRCK	MI2S_3_WS(GPI O_76)	GPIO_76/ G11	O, 1.8V CMOS	I2S Channel1 Left Right Clock
S51	HDA_SDO / I2S2_SDOUT	MI2S_3_D1(GPI O_78)	GPIO_78/ F10	O, 1.8V CMOS	I2S Channel1 Data Output
S52	HDA_SDI / I2S2_SDIN	MI2S_3_D0(GPI O_77)	GPIO_77/ C13	I, 1.8V CMOS	I2S Channel1 Data Input
S53	HDA_CK / I2S2_CK	MI2S_3_SCK(GP IO_75)	GPIO_75/ G9	O, 1.8V CMOS	I2S Channel1 Clock
S54	SATA_ACT#	NC	NA	NA	NA
S55	USB5_EN_OC#	NC	NA	NA	NA
S56	ESPI_IO_2	NC	NA	NA	NA
S57	ESPI_IO_3	NC	NA	NA	NA
S58	ESPI_RESET#	NC	NA	NA	NA
S59	USB5+	NC	NA	NA	NA
S60	USB5-	NC	NA	NA	NA
S61	GND	GND	NA	Power	Ground.
S62	USB3_SSTX+	USB3_HUB2_TX P	NA	O, DIFF	USB3.0 Port3 Transmit Positive <i>Note: Connected to USB Hub</i>
S63	USB3_SSTX-	USB3_HUB2_TX M	NA	O, DIFF	USB3.0 Port3 Transmit Negative <i>Note: Connected to USB Hub</i>
S64	GND	GND	NA	Power	Ground.
S65	USB3_SSRX+	USB3_HUB2_RX P	NA	I, DIFF	USB3.0 Port3 Receive Positive <i>Note: Connected to USB Hub</i>

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Pin No.	SMARC Edge Connector Pin Name	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
S66	USB3_SSRX-	USB3_HUB2_RX M	NA	I, DIFF	USB3.0 Port3 Receive Negative <i>Note: Connected to USB Hub</i>
S67	GND	GND	NA	Power	Ground.
S68	USB3+	USB_HUB2OUT_ DP	NA	IO, DIFF	USB Port3 Data Positive <i>Note: Connected to USB Hub</i>
S69	USB3-	USB_HUB2OUT_ DM	NA	IO, DIFF	USB Port3 Data Negative <i>Note: Connected to USB Hub</i>
S70	GND	GND	NA	Power	Ground.
S71	USB2_SSTX+	USB3_HUB1_TX P	NA	O, DIFF	USB3.0 Port2 Transmit Positive <i>Note: Connected to USB Hub</i>
S72	USB2_SSTX-	USB3_HUB1_TX M	NA	O, DIFF	USB3.0 Port2 Transmit Negative <i>Note: Connected to USB Hub</i>
S73	GND	GND	NA	Power	Ground.
S74	USB2_SSRX+	USB3_HUB1_RX P	NA	I, DIFF	USB3.0 Port2 Receive Positive <i>Note: Connected to USB Hub</i>
S75	USB2_SSRX-	USB3_HUB1_RX M	NA	I, DIFF	USB3.0 Port2 Receive Negative <i>Note: Connected to USB Hub</i>
S76	PCIE_B_RST#	PCIE2_RST_N(G PIO_35)	GPIO_35/ E3	O, 3.3V CMOS	PCIe 2 RESET OUT
S77	PCIE_C_RST#	PCIE0_RST_N (GPIO_128)	GPIO_128)/ AV46	O, 3.3V CMOS	PCIe 3 RESET OUT
S78	PCIE_C_RX+	NC	NA	NA	NC <i>Note: Optionally connected to PCIE0_RX_P</i>
S79	PCIE_C_RX-	NC	NA	NA	NC <i>Note: Optionally connected to PCIE0_RX_M</i>
S80	GND	GND	NA	Power	Ground.
S81	PCIE_C_TX+	NC	NA	NA	NC <i>Note: Optionally connected to PCIE0_TX_P</i>
S82	PCIE_C_TX-	NC	NA	NA	NC <i>Note: Optionally connected to PCIE0_TX_M</i>
S83	GND	GND	NA	Power	Ground.
S84	PCIE_B_REFCK+	NC	NA	NA	NC

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Pin No.	SMARC Edge Connector Pin Name	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
					<i>Note: Optionally connected to PCIE2_REFCLK_P</i>
S85	PCIE_B_REFCK-	NC	NA	NA	NC <i>Note: Optionally connected to PCIE2_REFCLK_M</i>
S86	GND	GND	NA	Power	Ground.
S87	PCIE_B_RX+	NC	NA	NA	NC <i>Note: Optionally connected to PCIE2_RX_P</i>
S88	PCIE_B_RX-	NC	NA	NA	NC <i>Note: Optionally connected to PCIE2_RX_M</i>
S89	GND	GND	NA	Power	Ground.
S90	PCIE_B_TX+	NC	NA	NA	NC <i>Note: Optionally connected to PCIE2_TX_P</i>
S91	PCIE_B_TX-	NC	NA	NA	NC <i>Note: Optionally connected to PCIE2_TX_M</i>
S92	GND	GND	NA	Power	Ground.
S93	DPO_LANE0+	NC	NA	NA	NA
S94	DPO_LANE0-	NC	NA	NA	NA
S95	DPO_AUX_SEL	NC	NA	NA	NA
S96	DPO_LANE1+	NC	NA	NA	NA
S97	DPO_LANE1-	NC	NA	NA	NA
S98	DPO_HPDP	NC	NA	NA	NA
S99	DPO_LANE2+	NC	NA	NA	NA
S100	DPO_LANE2-	NC	NA	NA	NA
S101	GND	GND	NA	Power	Ground.
S102	DPO_LANE3+	NC	NA	NA	NA
S103	DPO_LANE3-	NC	NA	NA	NA
S104	USB3_OTG_ID	NC	NA	NA	NA
S105	DPO_AUX+	NC	NA	NA	NA
S106	DPO_AUX-	NC	NA	NA	NA
S107	LCD1_BKLT_EN	LCD1_BKLT_EN(GPIO_117)	GPIO_117/ BC49	O, 1.8V CMOS	LCD1 Backlight Enable
S108	LVDS1_CK+ / eDP1_AUX+ / DSI1_CLK+	MIPI_DSI1_CLK_ P	MIPI_DSI1_CLK_P/ BE31	O, DIFF	MIPI DSI1 differential clock positive
S109	LVDS1_CK- / eDP1_AUX- / DSI1_CLK-	MIPI_DSI1_CLK_ N	MIPI_DSI1_CLK_N/ BF32	O, DIFF	MIPI DSI1 differential clock negative

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Pin No.	SMARC Edge Connector Pin Name	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
S110	GND	GND	NA	Power	Ground.
S111	LVDS1_0+ / eDP1_TX0+ / DSI1_D0+	MIPI_DSI1_LN0 _P	MIPI_DSI1_LN0_P/ BG31	O, DIFF	MIPI DSI1 differential data lane 0 positive
S112	LVDS1_0- / eDP1_TX0- / DSI1_D0-	MIPI_DSI1_LN0 _N	MIPI_DSI1_LN0_N/ BF30	O, DIFF	MIPI DSI1 differential data lane 0 negative
S113	eDP1_HPD	NC	NA	NA	NA
S114	LVDS1_1+ / eDP1_TX1+ / DSI1_D1+	MIPI_DSI1_LN1 _P	MIPI_DSI1_LN1_P/ BJ33	O, DIFF	MIPI DSI1 differential data lane 1 positive
S115	LVDS1_1- / eDP1_TX1- / DSI1_D1-	MIPI_DSI1_LN1 _N	MIPI_DSI1_LN1_N/ BK34	O, DIFF	MIPI DSI1 differential data lane 1 negative
S116	LCD1_VDD_EN	LCD1_VDD_EN(GPIO_118)	GPIO_118/ BG41	O, 1.8V CMOS	LCD1Power Enable
S117	LVDS1_2+ / eDP1_TX2+ / DSI1_D2+	MIPI_DSI1_LN2 _P	MIPI_DSI1_LN2_P/ BE29	O, DIFF	MIPI DSI1 differential data lane 2 positive
S118	LVDS1_2- / eDP1_TX2- / DSI1_D2-	MIPI_DSI1_LN2 _N	MIPI_DSI1_LN2_N/ BD28	O, DIFF	MIPI DSI1 differential data lane 2 negative
S119	GND	GND	NA	Power	Ground.
S120	LVDS1_3+ / eDP1_TX3+ / DSI1_D3+	MIPI_DSI1_LN3 _P	MIPI_DSI1_LN3_P/ BF28	O, DIFF	MIPI DSI1 differential data lane 3 positive
S121	LVDS1_3- / eDP1_TX3- / DSI1_D3-	MIPI_DSI1_LN3 _N	MIPI_DSI1_LN3_N/ BE27	O, DIFF	MIPI DSI1 differential data lane 3 negative
S122	LCD1_BKLT_PWM	LCD1_BKLT_PW M(PM_GPIO1)	NA	O, 1.8V CMOS	LCD0 Back light Brightness control PWM <i>Note: from PMIC</i>
S123	RSVD8	NC	NA	NA	NA
S124	GND	GND	NA	Power	Ground.
S125	LVDS0_0+ / eDP0_TX0+ / DSI0_D0+	MIPI_DSI0_LN0 _P	MIPI_DSI0_LN0_P/ BK38	O, DIFF	MIPI DSI0 differential data lane 0 positive
S126	LVDS0_0- / eDP0_TX0- / DSI0_D0-	MIPI_DSI0_LN0 _N	MIPI_DSI0_LN0_N/ BJ37	O, DIFF	MIPI DSI0 differential data lane 0 negative
S127	LCD0_BKLT_EN	LCD0_BKLT_EN(GPIO_119)	GPIO_119/ AR51	O, 1.8V CMOS	LCD0 Backlight Enable

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Pin No.	SMARC Edge Connector Pin Name	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
S128	LVDS0_1+ / eDP0_TX1+ / DSIO_D1+	MIPI_DSIO_LN1_P	MIPI_DSIO_LN1_P/ BH38	O, DIFF	MIPI DSIO differential data lane 1 positive
S129	LVDS0_1- / eDP0_TX1- / DSIO_D1-	MIPI_DSIO_LN1_N	MIPI_DSIO_LN1_N/ BG37	O, DIFF	MIPI DSIO differential data lane 1 negative
S130	GND	GND	NA	Power	Ground.
S131	LVDS0_2+ / eDP0_TX2+ / DSIO_D2+	MIPI_DSIO_LN2_P	MIPI_DSIO_LN2_P/ BG35	O, DIFF	MIPI DSIO differential data lane 2 positive
S132	LVDS0_2- / eDP0_TX2- / DSIO_D2-	MIPI_DSIO_LN2_N	MIPI_DSIO_LN2_N/ BH36	O, DIFF	MIPI DSIO differential data lane 2 negative
S133	LCD0_VDD_EN	LCD0_VDD_EN(GPIO_120)	GPIO_120/ AU47	O, 1.8V CMOS	LCD0 Power Enable
S134	LVDS0_CLK+ / eDP0_AUX+ / DSIO_CLK+	MIPI_DSIO_CLK_P	MIPI_DSIO_CLK_P/ BF34	O, DIFF	MIPI DSIO differential clock positive
S135	LVDS0_CLK- / eDP0_AUX- / DSIO_CLK-	MIPI_DSIO_CLK_N	MIPI_DSIO_CLK_N/ BE33	O, DIFF	MIPI DSIO differential clock negative
S136	GND	GND	NA	Power	Ground.
S137	LVDS0_3+ / eDP0_TX3+ / DSIO_D3+	MIPI_DSIO_LN3_P	MIPI_DSIO_LN3_P/ BG33	O, DIFF	MIPI DSIO differential data lane 3 positive
S138	LVDS0_3- / eDP0_TX3- / DSIO_D3-	MIPI_DSIO_LN3_N	MIPI_DSIO_LN3_N/ BH34	O, DIFF	MIPI DSIO differential data lane 3 negative
S139	I2C_LCD_CLK	BLSP8_I2C_SCL(GPIO_7)	GPIO_7/ BB50	O, 1.8V CMOS	I2C CLK for Display and Touch
S140	I2C_LCD_DAT	BLSP8_I2C_SDA(GPIO_6)	GPIO_6/ BC51	IO, 1.8V CMOS	I2C DATA for Display and Touch
S141	LCD0_BKLT_PWM	LCD0_BKLT_PWM(PM_GPIO3)	NA	O, 1.8V CMOS	LCD0 Back Light Brightness control PWM <i>Note: from PMIC</i>
S142	RSVD9	NC	NA	NA	NA
S143	GND	GND	NA	Power	Ground.
S144	eDP0_HPD	NC	NA	NA	NA
S145	WDT_TIME_OUT#	WDT_TIME_OUT# T#	GPIO_101/ AT52	O, 1.8V CMOS	Watch DOG Time Out Interrupt

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Pin No.	SMARC Edge Connector Pin Name	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
S146	PCIE_WAKE#	PCIE_WAKE	GPIO_131/ B4	I, 3.3V CMOS	PCIe wake up interrupt to host <i>Note: Connected via 1.8 to 3.3V level Translator</i>
S147	VDD_RTC	VDD_RTC	NA	I, 3V Power	RTC backup power
S148	LID#	NC	NA	NA	NA
S149	SLEEP#	NC	NA	NA	NA
S150	VIN_PWR_BAD#	VIN_PWR_BAD#	NA	I, 5V CMOS 10K PU	Power bad indication from Carrier board. Module and Carrier power supplies shall not be enabled while this signal is held low by the Carrier.
S151	CHARGING#	NC	NA	NA	NA
S152	CHARGER_PRSENT#	NC	NA	NA	NA
S153	CARRIER_STBY#	CARRIER_STBY#	NA	O, 1.8V CMOS 10K PU	Carrier power should be enabled only after CARRIER_STBY# goes High.
S154	CARRIER_PWR_ON	CARRIER_PWR_ON	NA	O, 1.8V CMOS 10K PU	Carrier power should be enabled only after CARRIER_PWR_ON goes High
S155	FORCE_RECOV#	FORCE_RECOV#	NA	I, 1.8V CMOS 10K PU	Low on this pin allows non-protected segments of Module boot device to be rewritten / restored from an external USB Host on Module USB0. The Module USB0 operates in Client Mode when in the Force Recovery function is invoked.
S156	BATLOW#	NC	NA	NA	NA
S157	TEST#	TEST#	NA	I, 1.8V CMOS 10K PU	Module vendor specific test is not supported.
S158	GND	GND	NA	Power	Ground.

2.8 Expansion Connector

APQ8096 SMARC SOM as Expansion connector to utilise extra interfaces which is not covered under SMARC specification V2.0. edge connector. These signals are takeout from SOM via 100pin expansion connector and connector is placed on bottom side of the SOM.

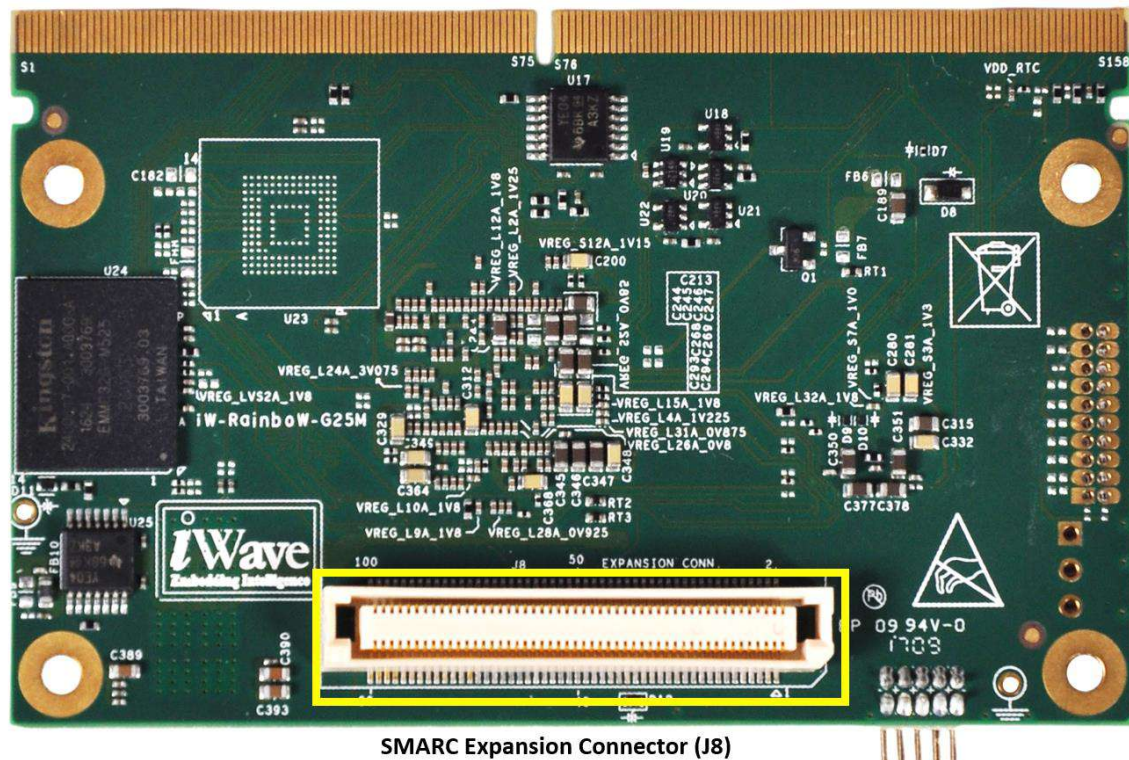


Figure 6: SMARC Expansion Connector

Number of Pins - : 100

Connector Part - : FX8C-100S-SV(91) from Hirose

Mating Connector - : FX8C-100P-SV(91) from Hirose

Table 5: Expansion Connector Pin Assignment

Pin No	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
1	VOLUME_P_BTN	NA	IO, 1.8V CMOS	GPIO from PMIC
2	VBUS_IN	NA	I, 5V Power	VBUS Power
3	HDMI_EN	NA	IO, 1.8V CMOS	GPIO from PMIC
4	VBUS_IN	NA	I, 5V Power	VBUS Power
5	GND	NA	Power	Ground.
6	GND	NA	Power	Ground.
7	LINE_OUT2_P	NA	NA	NC. <i>Note: On SOM Audio Codec is not supported by default</i>
8	USB3_HUB3_TXP	NA	I, DIFF	USB3.0 Port3 Transmit Positive <i>Note: Connected to USB Hub</i>
9	LINE_OUT2_M	NA	NA	NC. <i>Note: On SOM Audio Codec is not supported by default</i>
10	USB3_HUB3_TXM	NA	I, DIFF	USB3.0 Port3 Transmit Negative <i>Note: Connected to USB Hub</i>
11	GND	NA	Power	Ground.
12	GND	NA	Power	Ground.
13	LINE_OUT4	NA	NA	NC. <i>Note: On SOM Audio Codec is not supported by default</i>
14	USB3_HUB3_RXP	NA	I, DIFF	USB3.0 Port3 Receive Positive <i>Note: Connected to USB Hub</i>
15	LINE_OUT3	NA	NA	NC. <i>Note: On SOM Audio Codec is not supported by default</i>
16	USB3_HUB3_RXM	NA	I, DIFF	USB3.0 Port3 Receive Negative <i>Note: Connected to USB Hub</i>
17	EXP_HPH_REF	NA	NA	NC. <i>Note: On SOM Audio Codec is not supported by default</i>
18	GND	NA	Power	Ground.
19	EXP_HPH_R	NA	NA	NC. <i>Note: On SOM Audio Codec is not supported by default</i>
20	USB3_HUB4_TXP	NA	I, DIFF	USB3.0 Port3 Transmit Positive <i>Note: Connected to USB Hub</i>

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Pin No	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
21	EXP_HPH_L	NA	NA	NC. <i>Note: On SOM Audio Codec is not supported by default</i>
22	USB3_HUB4_TXM	NA	I, DIFF	USB3.0 Port3 Transmit Negative <i>Note: Connected to USB Hub</i>
23	GND	NA	Power	Ground.
24	GND	NA	Power	Ground.
25	LINE_OUT1_M	NA	NA	NC. <i>Note: On SOM Audio Codec is not supported by default</i>
26	USB3_HUB4_RXP	NA	I, DIFF	USB3.0 Port3 Receive Positive <i>Note: Connected to USB Hub</i>
27	LINE_OUT1_P	NA	NA	NC. <i>Note: On SOM Audio Codec is not supported by default</i>
28	USB3_HUB4_RXM	NA	I, DIFF	USB3.0 Port3 Receive Negative <i>Note: Connected to USB Hub</i>
29	GND	NA	Power	Ground.
30	GND	NA	Power	Ground.
31	EAROM	NA	NA	NC. <i>Note: On SOM Audio Codec is not supported by default</i>
32	AMIC1_INP	NA	NA	NC. <i>Note: On SOM Audio Codec is not supported by default</i>
33	EAROP	NA	NA	NC. <i>Note: On SOM Audio Codec is not supported by default</i>
34	AMIC1_INM	NA	NA	NC. <i>Note: On SOM Audio Codec is not supported by default</i>
35	GND	NA	Power	Ground.
36	GND	NA	Power	Ground.
37	HSDet_L	NA	NA	NC. <i>Note: On SOM Audio Codec is not supported by default</i>
38	AMIC3_INP	NA	NA	NC. <i>Note: On SOM Audio Codec is not supported by default</i>
39	GND	NA	Power	Ground.

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Pin No	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
40	AMIC3_INM	NA	NA	NC. <i>Note: On SOM Audio Codec is not supported by default</i>
41	DMIC2_DIN	NA	NA	NC. <i>Note: On SOM Audio Codec is not supported by default</i>
42	GND	NA	Power	Ground.
43	DMIC2_CLK	NA	NA	NC. <i>Note: On SOM Audio Codec is not supported by default</i>
44	HDMI_CEC(GPIO_31)	GPIO_31/ BH46	IO, 1.8V CMOS	General Purpose Input / Output
45	GND	NA	Power	Ground.
46	GPIO_127	GPIO_127/ AY48	IO, 1.8V CMOS	General Purpose Input / Output
47	DMIC1_DIN	NA	NA	NC. <i>Note: On SOM Audio Codec is not supported by default</i>
48	GPIO_149	GPIO_149/ AM47	IO, 1.8V CMOS	General Purpose Input / Output
49	DMIC1_CLK	NA	NA	NC. <i>Note: On SOM Audio Codec is not supported by default</i>
50	GPIO_148	GPIO_148/ AN47	IO, 1.8V CMOS	General Purpose Input / Output
51	GND	NA	Power	Ground.
52	GPIO_10	GPIO_10/ BH50	IO, 1.8V CMOS	General Purpose Input / Output
53	EXP_SLIMBUS_DATA0(GPIO_71)	GPIO_71/ D12	IO, 1.8V CMOS	SLIMBUS DATA0 line
54	GPIO_11	GPIO_11/ BJ51	IO, 1.8V CMOS	General Purpose Input / Output
55	EXP_SLIMBUS_DATA1(GPIO_72)	GPIO_72/ E13	IO, 1.8V CMOS	SLIMBUS DATA1 Line
56	GPIO_12	GPIO_12/ BJ45	IO, 1.8V CMOS	General Purpose Input / Output
57	EXP_SLIMBUS_CLK(GPIO_70)	GPIO_70/ D14	IO, 1.8V CMOS	SLIMBUS Clock
58	SSC_UART_2_TX (SSC_14)	SSC_14/ E39	IO, 1.8V CMOS	Sensor Core UART2 Transmitter
59	GND	NA	Power	Ground.

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Pin No	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
60	SSC_UART_1_RX(SSC_13)	SSC_13/ D38	IO, 1.8V CMOS	Sensor Core UART1 Receiver
61	MIC_BIAS3	NA	NA	NC. <i>Note: On SOM Audio Codec is not supported by default</i>
62	SSC_UART_2_RX (SSC_15)	SSC_15/ E37	IO, 1.8V CMOS	Sensor Core UART2 Receiver
63	MIC_BIAS1	NA	NA	NC. <i>Note: On SOM Audio Codec is not supported by default</i>
64	SSC_UART_1_TX (SSC_12)	SSC_12/ C39	IO, 1.8V CMOS	Sensor Core UART1 Transmitter
65	MIC_BIAS2	NA	NA	NC. <i>Note: On SOM Audio Codec is not supported by default</i>
66	SSC_UART_3_RX (SSC_7)	SSC_7/ C31	IO, 1.8V CMOS	Sensor Core UART3 Receiver
67	MIC_BIAS4	NA	NA	NC. <i>Note: On SOM Audio Codec is not supported by default</i>
68	SSC_UART_3_TX (SSC_6)	SSC_6/ E31	IO, 1.8V CMOS	Sensor Core UART3 Transmitter
69	GND	NA	Power	Ground.
70	SSC_I2C_2_SCL(SSC_5)	SSC_5/ D30	O, 1.8V CMOS	Sensor Core I2C2 clock
71	SSC_I2C_3_SCL(SSC_3)	SSC_3/ C37	O, 1.8V CMOS	Sensor Core I2C3 clock
72	SSC_I2C_2_SDA(SSC_4)	SSC_4/ B36	IO, 1.8V CMOS	Sensor Core I2C2 Data
73	SSC_I2C_3_SDA(SSC_2)	SSC_2/ B38	IO, 1.8V CMOS	Sensor Core I2C3 Data
74	BLSP6_I2C_SCL(GPIO_28)	GPIO_28/ B6	O, 1.8V CMOS	BLSP6 I2C2 Clock
75	GPIO_74	GPIO_74/ E7	IO, 1.8V CMOS	General Purpose Input / Output
76	BLSP6_I2C_SDA(GPIO_27)	GPIO_27/ C5	IO, 1.8V CMOS	BLSP6 I2C2 Data
77	GPIO_22	GPIO_22/ J3	IO, 1.8V CMOS	General Purpose Input / Output
78	GND	NA	Power	Ground.
79	GPIO_24	GPIO_24/ M6	IO, 1.8V CMOS	General Purpose Input / Output

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Pin No	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
80	MIPI_CSI0_DLN2_P	MIPI_CSI0_DLN2_P /BJ7	I, DIFF	MIPI CS0 differential data lane 2 positive
81	CLK3_OUT(GPIO_15)	GPIO_15/ BF8	O, 1.8V CMOS	General purpose Clock
82	MIPI_CSI0_DLN2_M	MIPI_CSI0_DLN2_M/ BH6	I, DIFF	MIPI CSI0 differential data lane 2 negative
83	GND	NA	Power	Ground.
84	GND	NA	Power	Ground.
85	MIPI_CSI2_DLN1_P	MIPI_CSI2_DLN1_P /BC3		MIPI CSI2 differential data lane 0 positive
86	MIPI_CSI0_DLN3_P	MIPI_CSI0_DLN3_P /BJ5	I, DIFF	MIPI CS0 differential data lane 3 positive
87	MIPI_CSI2_DLN1_M	MIPI_CSI2_DLN1_M/ BB4	I, DIFF	MIPI CSI2 differential data lane 0 negative
88	MIPI_CSI0_DLN3_M	MIPI_CSI0_DLN3_M/ BH4	I, DIFF	MIPI CSI0 differential data lane 3 negative
89	GND	NA	Power	Ground.
90	GND	NA	Power	Ground.
91	MIPI_CSI2_DLN2_P	MIPI_CSI2_DLN2_P /BB2	I, DIFF	MIPI CSI2 differential data lane 2 positive
92	MIPI_CSI2_DLN0_P	MIPI_CSI2_DLN0_P /BE1	I, DIFF	MIPI CS2 differential data lane 0 positive
93	MIPI_CSI2_DLN2_M	MIPI_CSI2_DLN2_M/ BA3	I, DIFF	MIPI CSI2 differential data lane 2 negative
94	MIPI_CSI2_DLN0_M	MIPI_CSI2_DLN0_M/ BD2	I, DIFF	MIPI CSI2 differential data lane 0 negative
95	GND	NA	Power	Ground.
96	GND	NA	Power	Ground.
97	MIPI_CSI2_DLN3_P	MIPI_CSI2_DLN3_P /BA1	I, DIFF	MIPI CSI2 differential data lane 3 positive
98	MIPI_CSI2_DCLK_P	MIPI_CSI2_DCLK_P /BF2	I, DIFF	MIPI CSI2 differential Clock positive
99	MIPI_CSI2_DLN3_M	MIPI_CSI2_DLN3_M/ AY2	I, DIFF	MIPI CSI2 differential data lane 3 negative
100	MIPI_CSI2_DCLK_M	MIPI_CSI2_DCLK_M/ BE3	I, DIFF	MIPI CSI2 differential Clock negative

2.9 Optional Features

2.9.1 JTAG Header

The Snapdragon 820 SMARC SOM supports one JTAG interface for CPU debug purpose. A customized 20-pin ARM JTAG connector (J4) is available in SOM for JTAG interface. Even though this JTAG connector pinout is fully compatible with “ARM JTAG 20” connector, the physical dimension of connector is made smaller because of space constraint.

APQ8096 CPU’s JTAG pins are 1.8V tolerant and so 1.8V reference power is provided to pin 1 of the connector to allow JTAG tool to automatically configure the logic signals for the right voltage. JTAG connector (J4) is physically located on topside of the SOM. This is the optional feature and will not be populated in default configuration.

Number of Pins - 20

Connector Part - GRPB102MWCN-RC from Sullins Connector Solutions

Mating Connector - LPPB102CFFN-RC from Sullins Connector Solutions

Table 6: JTAG Header Pin Assignment

Pin No	Signal Name	Signal Type/ Termination	Description
1	VCC_1V8	O, 1.8V Power	VTREF Voltage Reference.
2	VCC_1V8	O, 1.8V Power	Supply Voltage.
3	JTAG_TRSTB	I, 1.8V CMOS/ 10K PD	JTAG test reset signal.
4	GND	Power	Ground.
5	JTAG_TDI	I, 1.8V CMOS/ 10K PU	JTAG test data input.
6	GND	Power	Ground.
7	JTAG_TMS	I, 1.8V CMOS/ 10K PU	JTAG test mode select.
8	GND	Power	Ground.
9	JTAG_TCK	I, 1.8V CMOS/ 10K PU	JTAG test Clock.
10	GND	Power	Ground.
11	-	I, 1.8V CMOS/ 10K PD	Only pull down is provided.
12	GND	Power	Ground.
13	JTAG_TDO	O, 1.8V CMOS	JTAG test data output.
14	GND	Power	Ground.
15	JTAG_RESETB	I, 1.8V CMOS/ 10K PU	Reset input.
16	GND	Power	Ground.
17	-	I, 1.8V CMOS/ 10K PU	Only pull up is provided.

Pin No	Signal Name	Signal Type/ Termination	Description
18	GND	Power	Ground.
19	-	-	Default NC. <i>Note: Optionally this pin is connected to CPU ACK pin (AE17) through resistor and default not populated.</i>
20	GND	Power	Ground.

2.9.2 Debug UART Header

The APQ8096 CPU's BLSP8 UART is used as Debug UART. Which will give the boot long and terminal access to the CPU. In Snapdragon 820 SMARC SOM BLSP8 UART is connected to SER3 UART channel of SMARC Edge connector. But also as an option to connect to J5 connector. FTDI's UART to USB smart cable (*TTL-232R-RPI*) can be used for connecting to Host Computer for debugging.

Table 7: Debug UART Header Pin Out

Pin No	Pin Name	Signal Name	Signal Type/ Termination	Description
1	TX	BLSP8_UART_TX	O, 3.3V CMOS0	UART8 Transmit
2	RX	BLSP8_UART_RX	I, 3.3V CMOS0 10K PD	UART8 Receive
3	GND	GND	Power	Ground

2.9.3 Battery Connector

The Snapdragon 820 SMARC is default powered with SMARC Edge connector pins, but it as option to connect battery as a backup power supply source with On SOM Battery Charging controller IC. 3.7 to 4.5V battery can be connected to J2 connector. J2 is placed on to side of PCB and J2 pinout is as given below:

Number of Pins - 3

Connector Part - BM03B-ACHSS-GAN-TF(LF)(SN) from JST Sales America Inc.

Mating Connector - ACHR-03V-S from JST Sales America Inc.

Table 8: Battery Connector Pin Out

Pin No	Pin Name	Signal Name	Signal Type/ Termination	Description
1	VBATT	VBATT	I, 3.6 ~ 4.35V	Battery input pin
2	BATT_THERM	BATT_THERM	I,	Battery thermal sense pin.
	GND	GND	Power	Ground

2.9.4 Audio In/Out Jack

The Snapdragon 820 SMARC SOM has option for on SOM SLIMBUS codec “WCD9335” from Qualcomm. WCD9335 supports 6 Number analog inputs and 7 number PA outputs, 6 Number digital microphones inputs, 6 Number audio ADCs, 9 number decimators, 9 Number interpolators, 7 number DACs and 4 Number of line outputs. WCD9335 comes with Snapdragon Voice Activation power and Smart Boost (class-D/G) stereo speaker amplifier with feedback speaker protection.

Note: Contact iWave for more information.

2.9.5 UFS - Universal Flash Storage

The Snapdragon 820 SMARC SOM supports 64GB UFS as optional boot device and storage. The memory size of the UFS Flash can be expandable and the APQ8096 CPU UFS host controller is compliant with the following specifications: JEDEC specification for Universal Flash Storage (UFS)(JESD220B) –v2.0, JEDEC specification for UFS Host Controller Interface(JESD223A) –v2.0, MIPI Alliance specification for Unified Protocol(UniPro) –v1.6.00 and MIPI Alliance specification for M-PHY–v3Audio/Video Feature

The UFS(U23) memory is physically located on bottom side of the SMARC SOM Contact iWave Support team for further information.

3. TECHNICAL SPECIFICATION

This section provides detailed information about the Snapdragon 820 SMARC SOM technical specification with Electrical, Environmental and Mechanical characteristics.

3.1 Electrical Characteristics

The Module input power voltage is brought in on the ten VDD_IN pins and returned through the numerous GND pins on the connector. A Module will withstand an indefinite exposure to an applied VDD_IN that may vary over the 4.2V to 5.25V range, without damage, and it will operate over the entire VDD_IN range of 4.2V to 5.25V. Ten pins are allocated to VDD_IN. The connector pin current rating is 0.5A per pin. This works out to 5A total for the 10 pins.

Table 9: Power Input Requirement

Sl. No.	Power Rail	Min (V)	Typical (V)	Max(V)	Max Input Ripple
1	VDD_IN ¹	4.2V	5V	5.25	±50mV

¹ VDD_IN pin can be powered from either SMRAC Carrier Card or External power source.

3.1.1 Power Input Sequencing

The APQ8096 SMARC SOM's Power Input sequence requirement is explained below.

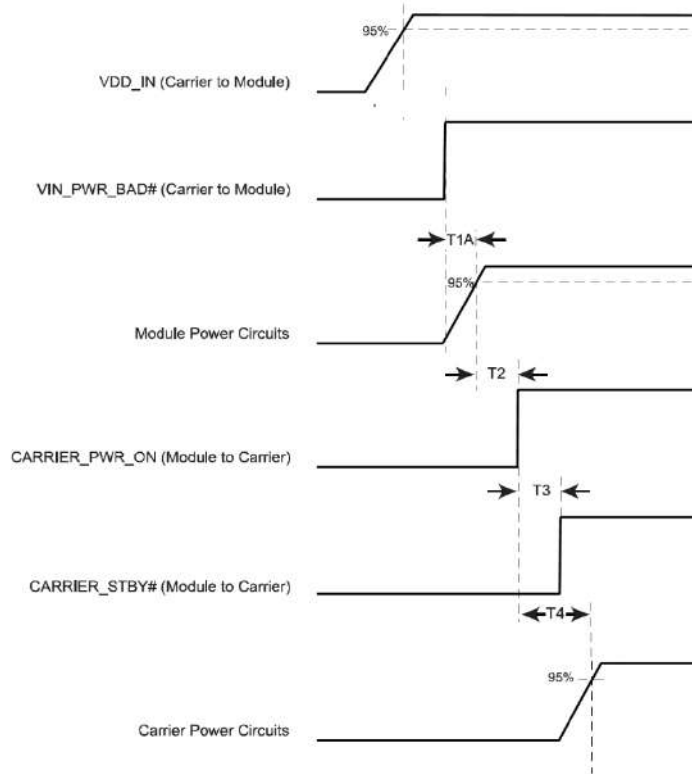


Figure 7: Power Input Sequencing

Table 10: Power Sequence Timing

Item	Description	Value
T1	VDD_IN rise time to VIN_PWR_BAD# rise time	≥ 0 ms
T1A	VIN_PWR_BAD# rise time to SOM Power rise time	≥ 0 ms
T3	SOM Power rise time to CARRIER_PWR_ON rise time	≥ 0 ms
T4	CARRIER_PWR_ON rise time to CARRIER_STBY# rise time	≥ 0 ms
T5	CARRIER_STBY# rise time to CARRIER POWER rise time	100 to 500ms

3.1.2 Power Consumption

TBD

3.2 Environmental Characteristics

3.2.1 Environmental Specification

The below table provides the Environment specification of Snapdragon 820 SMARC SOM.

Table 11: Environmental Specification

Parameters	Min	Max
Operating temperature range ¹	0°C	70°C

¹ iWave guarantees the component selection for the given operating temperature. The operating temperature at the system level will be affected by the various system components like carrier board and its components, system enclosure, air circulation in the system, system power supply etc. Based on the system design, specific heat dissipating approach might be required from system to system. It is recommended to do the necessary system level thermal simulation and find necessary thermal solution in the system before using this board in the end application.

3.2.2 RoHS Compliance

iWave's Snapdragon 820 SMARC SOM is designed by using RoHS compliant components and manufactured on lead free production process.

3.2.3 Electrostatic Discharge

iWave's Snapdragon 820 SMARC SOM is sensitive to electro static discharge and so high voltages caused by static electricity could damage some of the devices on board. It is packed with necessary protection while shipping. Do not open or use the SOM except at an electrostatic free workstation.

3.3 Mechanical Characteristics

3.3.1 Snapdragon 820 SMARC SOM Mechanical Dimensions

Snapdragon 820 SMARC SOM PCB size is 50 mm x 82mm x 1.2mm. SMARC SOM mechanical dimension is shown below.
(All dimensions are shown in mm)

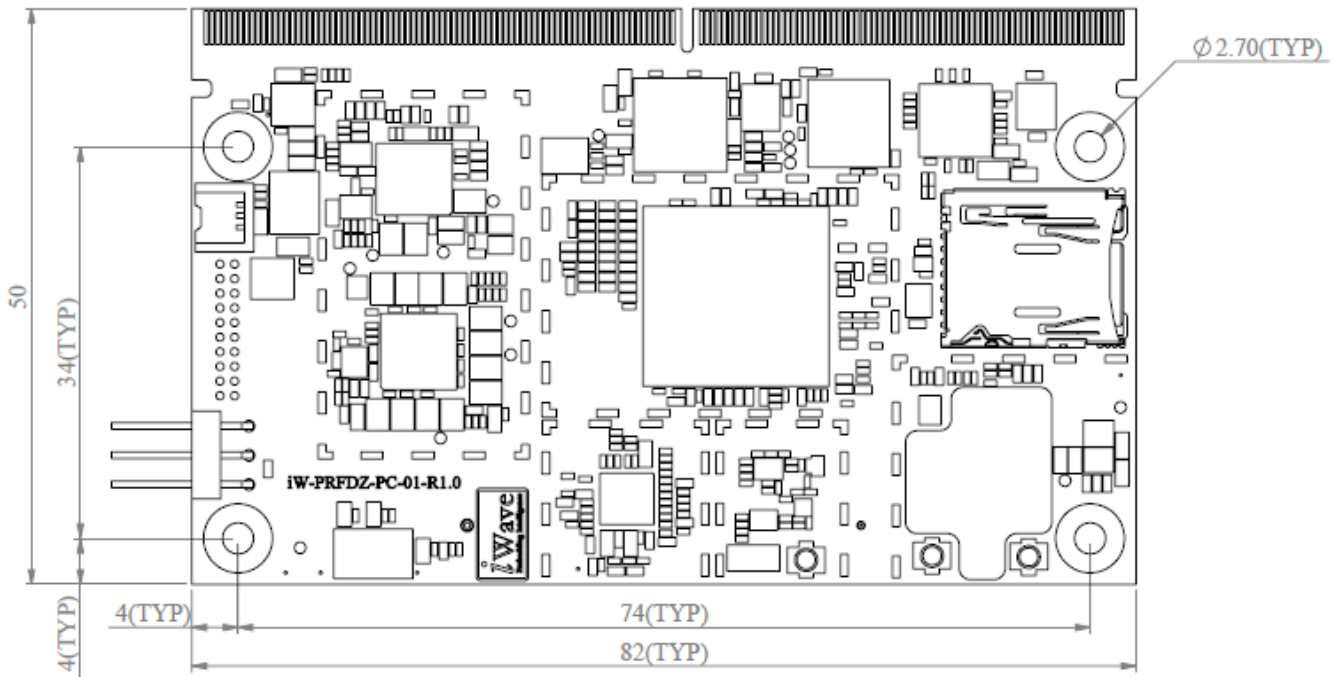


Figure 8: Mechanical dimension of Snapdragon 820 SMARC SOM Top View

Snapdragon 820 SMARC SOM PCB thickness is 1.2mm±0.15mm, top side maximum height component is Diode D3 (4mm) followed by SD slot(1.93mm) and bottom side maximum height component is expansion connector (3.95mm) followed by IC U25 (1.2mm). Please refer the below figure which gives height details of the Snapdragon 820 SMARC SOM.

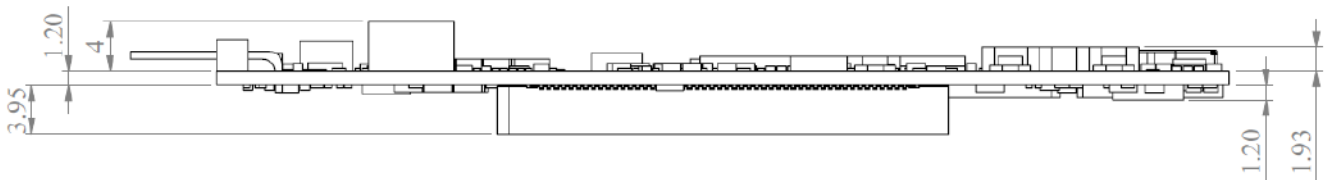


Figure 9: Mechanical dimension of Snapdragon 820 SMARC SOM- Side View

4. ORDERING INFORMATION

The below table provides the standard orderable part numbers for different Snapdragon 820 SMARC SOM variations. Please contact iWave for orderable part number of higher RAM memory size or Flash memory size SOM configurations. Also, if the desired part number is not listed in below table or if any custom configuration part number is required, please contact iWave.

Table 12: Orderable Product Part Numbers

Product Part Number	Description	Temperature
iW-G25M-SC04-4L003G-E032G-ACA	With APQ8096 CPU, 3GB LPDDR4, 32GB eMMC flash, Wi-Fi, BT, GPS with Expansion Connector - Android	0°C to 70°C

5. APPENDIX

5.1 Snapdragon 820 SMARC SOM Development Platform

iWave Systems supports iW-RainboW-G25D – Snapdragon 820 SMARC SOM Development Platform which is targeted for quick validation of Snapdragon 820 CPU based SMARC SOM and its features. Being a Nano-ITX form factor with 120mm x 120mm size, the carrier board is highly packed with all necessary interfaces & on-board connectors to validate complete SMARC supported features.

For more details on Snapdragon 820 SMARC SOM Development Platform, visit the below web link.

<http://www.iwavesystems.com/snapdragon-820-apq8096-smarc-development-kit.html>



Figure 10: Snapdragon 820 SMARC SOM Development Platform

