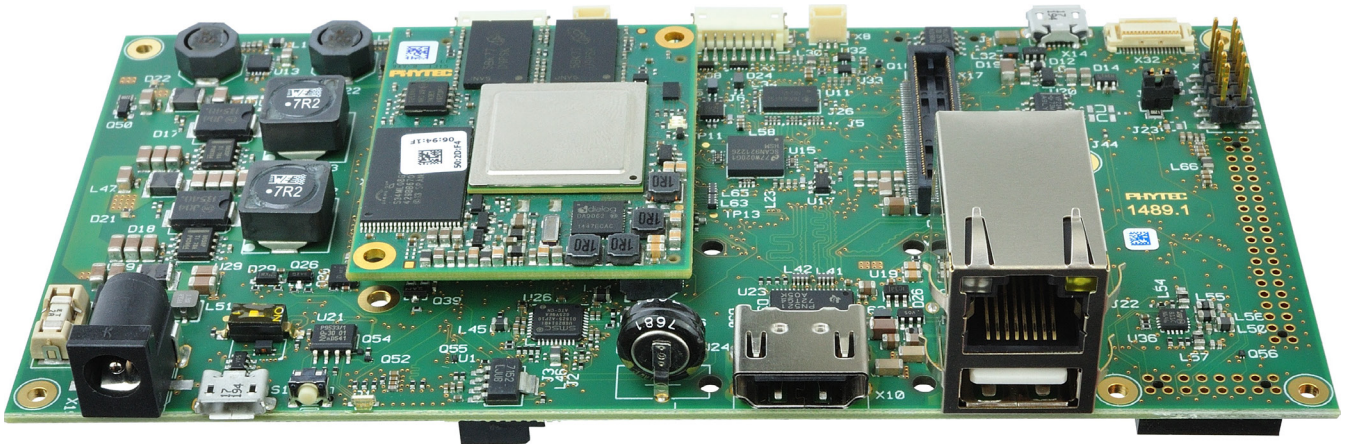
phyBOARD®-Nunki i.MX 6

Hardware Manual

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Conventions, Abbreviations and Acronyms

This hardware manual describes the PB-02013-XXX Single Board Computer (SBC), henceforth referred to as phyBOARD-Nunki i.MX 6. This manual specifies the phyBOARD-Nunki i.MX 6's design and function. Precise specifications for the NXP® Semiconductor i.MX 6 microcontrollers can be found in the NXP® Semiconductor's *i.MX 6 Data Sheet and Technical Reference Manual*.

Conventions

The conventions used in this manual are as follows:

- Signals that are preceded by an "n", "/", or "#"character (e.g.: nRD, /RD, or #RD), or that have a dash on top of the signal name (e.g.: $\overline{\text{RD}}$) are designated as active low signals. That is, their active state is when they are driven low, or are driving low.
- A "0" indicates a logic zero or low-level signal, while a "1" represents a logic one or high-level signal.
- The hex-numbers given for addresses of I^2C devices always represent the 7 MSB of the address byte. The correct value of the LSB which depends on the desired command (read (1), or write (0)) must be added to get the complete address byte. E.g. given address in this manual 0x41 => complete address byte = 0x83 to read from the device and 0x82 to write to the device.
- Tables which describe jumper settings show the default position in **bold, blue text.**
- Text in *blue italic* indicates a hyperlink within, or external to the document. Click these links to quickly jump to the applicable URL, part, chapter, table, or figure.
- Text in ***bold italic*** indicates an interaction by the user, which is defined on the screen.
- Text in `Consolas` indicates an input by the user, without a premade text or button to click on.
- Text in *italic* indicates proper names of development tools and corresponding controls (windows, tabs, commands etc.) used within the development tool, no interaction takes place.
- White Text on black background shows the result of any user interaction (command, program execution, etc.)

Types of Signals

Different types of signals are brought out at the phyCORE-Connector. *Table 1* lists the abbreviations used to specify the type of a signal.

Refer to the SOM manual for pin muxing options.

Signal Type	Description	Abbr.
Power Input	Supply voltage input	PWR_I
Power Output	Supply voltage output for external devices	PWR_O
Ref-Voltage	Reference voltage output	REF_O
Input	Digital input	I
Output	Digital output	O
Input / output	Bidirectional input/output	I/O
OD-Bidir PU	Open drain input/output with pull-up resistor	OD-BI
LVDS Output	Differential line pairs 100 Ohm LVDS level output	LVDS_O
LVDS Input	Differential line pairs 100 Ohm LVDS level input	LVDS_I
USB-Power	USB voltage	USB
USB IO	Differential line pairs 90 Ohm USB level bidirectional input/output	USB_I/O
Ethernet IO	Differential line pairs 100 Ohm Ethernet level bidirectional input/output	ETH_I/O
Analog	Analog input or output	Analog

Table 1: Signal Types used in this Manual

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Abbreviations and Acronyms

Many acronyms and abbreviations are used throughout this manual. Use *Table 2* to navigate unfamiliar terms used in this document.

Abbreviation	Definition
A/V	Audio/Video
BSP	Board Support Package (Software delivered with the Development Kit including an operating system (*Windows*, or *Linux*) pre-installed on the module and Development Tools)
CB	Carrier Board, used in reference to the phyBOARD-Nunki Development Kit Carrier Board
DFF	D flip-flop
DSC	Direct Solder Connect
EMB	External memory bus
EMI	Electromagnetic Interference
GPIO	General purpose input and output
GPO	General purpose output
J	Solder jumper, these types of jumpers require solder equipment to remove and place
JP	Solderless jumper, these types of jumpers can be removed and placed by hand with no special tools
NC	Not Connected
NM	Not Mounted
NS	Not Specified
PCB	Printed circuit board
UDI	Universal Display Interface, defined to connect custom display adapters with or without touch screen
PEB	PHYTEC Expansion Board
POR	Power-on reset
RTC	Real-time clock
SBC	Single Board Computer, used in reference to the PBA-CD-10 / phyBOARD-Nunki i.MX 6
SMT	Surface mount technology
SOM	System on Module, used in reference to the PCL-063 / phyCORE-i.MX 6 module
Sx	User button Sx (e.g. S1, S2) used in reference to the available user buttons, or DIP switches on the CB
Sx_y	Switch y of DIP switch Sx, used in reference to the DIP switch on the carrier board

Table 2: Abbreviations and Acronyms used in this Manual

Note:

- The BSP is configured according to the hardware configuration including the expansion board optionally delivered with the kit. Thus, some functions of the phyBOARD-Nunki°i.MX 6 might not be available of the corresponding pins and drivers are needed to support an expansion board. If the expansion board is removed or exchanged, the BSP must be exchanged as well.

Preface

As a member of PHYTEC's phyBOARD® product family, the phyBOARD-Nunki i.MX 6 is one of a series of PHYTEC System on Modules (SBCs) that offer off-the-shelf solutions for a huge variety of industrial applications. The new phyBOARD® product family consists of a series of extremely compact embedded control engines featuring various processing performance classes. All phyBOARDs are rated for industry, cost optimized, and offer long-term availability. The phyBOARD-Nunki i.MX 6 is one of currently six industrial-grade carrier boards which are suitable for series production and that has been realized in accordance with PHYTEC's new SBCplus concept. It is an excellent example of this concept.

SBCplus Concept

The SBCplus concept was developed to meet fine differences in customer requirements with little development effort and thus greatly reduce the time-to-market.

Core of the SBCplus concept is the SBC design library (a kind of construction set) that consists of a great number of function blocks (so-called "building blocks") which are constantly refined. The recombination of these function blocks allows PHYTEC to develop a customer specific SBC within a short time. Thus, PHYTEC is able to deliver production-ready custom Single Board Computers within a few weeks at very low costs.

The already developed SBCs, such as the phyBOARD-Nunki i.MX 6, each represent an intersection of different customer wishes. Due to this, all necessary interfaces are available on the standard versions, thus, allowing them to be integrated in a large number of applications without modification. For any specific adjustments that are needed, extension connectors are available to add a wide variety of functions.

Customized Expandability from PHYTEC

Common interface signals route to standard connector interfaces on the carrier board such as Ethernet, CAN, RS-232, and audio. Due to the easily modifiable phyBOARD design approach (see "*SBCplus concept*"), these plug-and-play interfaces can be readily adapted into customer-specific variants according to end system requirements.
Some signals from the processor populating the SOM also extend to the expansion and A/V connectors of the phyBOARD-Nunki i.MX 6. This provides customized expandability according to end user requirements. Thus, expandability is made easy by available plug-and-play expansion modules (for example Parallel Displays) from PHYTEC.

The default orientation of the expansion bus connectors is parallel and on the top side of the carrier board PCB. However, in custom configurations, the connectors can be mounted on the PCB's underside. Connectors in perpendicular orientation can also populate the top or underside of the PCB. This enables maximum flexibility for the orientation of expansion

modules on the phyBOARD-Nunki i.MX 6, as well as easily integrating the system into a variety of end application physical envelopes and form factors.

Easy Integration of Display und Touch

The phyBOARD and its expansion modules enable easy connection of parallel or LVDS based displays, as well as resistive or capacitive touch screens.

OEM Implementation

Implementing an OEM-able SBC subassembly as the "core" of your embedded design allows for increased focus on hardware peripherals and firmware without expending resources to "re-invent" microcontroller circuitry. Furthermore, much of the value of the phyBOARD® SBC lies in its layout and production test.

Software Support

Production-ready Board Support Packages (BSPs) and Design Services for PHYTEC hardware will further reduce development time and risk and allow for increased focus on the product expertise.

Ordering Information

Ordering numbers:

phyBOARD-Nunki i.MX 6 Development Kit:	**KPB-02301-xxx**
phyBOARD-Nunki i.MX 6 SBC:	**PB-02301-xxx**
phyCORE-i.MX 6 SOM:	**PCM-058**

Product Specific Information and Technical Support

In order to receive product specific information on all future changes and updates, we recommend registering at:

http://www.phytec.de/de/support/registrierung.html or
http://www.phytec.eu/europe/support/registration.html

For technical support and additional information concerning your product, please visit the download section of our web site which provides product specific information such as errata sheets, application notes, FAQs, etc.

http://www.phytec.de/produkt/single-board-computer/phyboard-nunki-download/ or
http://www.phytec.eu/europe/support/faq/faq-phyBOARD-Nunki-i.MX6.html

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Other Products and Development Support

Apart from the new phyBOARD® family, PHYTEC supports a variety of 8-/16- and 32-bit controllers in two ways:

(1) As the basis for Rapid Development Kits, which serve as a reference and evaluation platform

(2) As insert-ready, fully functional OEM modules which can be embedded directly into the user's peripheral hardware design.

Take advantage of PHYTEC products to shorten time-to-market, reduce development costs, and avoid substantial design issues and risks. With this new innovative full system solution new ideas can be brought to market in the most timely and cost-efficient manner.

For more information, go to:

http://www.phytec.de/de/leistungen/entwicklungsunterstuetzung.html or
http://www.phytec.eu/europe/oem-integration/evaluation-start-up.html

Declaration of Electro Magnetic Conformity of the PHYTEC phyBOARD-Nunki i.MX 6

PHYTEC Single Board Computers (henceforth products) are designed for installation in electrical appliances, as part of custom applications, or as dedicated Evaluation Boards (i.e.: for use as a test and prototype platform for hardware/software development) in laboratory environments.

Caution!

- PHYTEC products lacing protective enclosures are subject to damage by ESD and, therefore, must be unpacked, handled or operated in environments in which sufficient precautionary measures have been take in respect to ESD dangers. It is also necessary that only appropriately trained personnel (such as electricians, technicians and engineers) handle and/or operate these products. Moreover, PHYTEC products should not be operated without protection circuitry if connections to the product's pin header rows are longer then 3m.

PHYTEC products fulfill the norms of the European Union's Directive for Electro Magnetic Conformity only in accordance with the descriptions and rules of usage indicated in this hardware manual (particularly in respect to the pin header row connectors, power connector and serial interface to a host-PC).

Implementation of PHYTEC products into target devices, as well as user modifications and extensions of PHYTEC products, is subject to renewed establishment of conformity to, and certification of, Electro Magnetic Directives. Users should ensure conformance following any modifications to the products as well as implementation of the products into target systems.

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Product Change Management and information in this manual on parts populated on the SOM / SBC

When buying a PHYTEC SOM / SBC, you will, in addition to our HW and SW offerings, receive free obsolescence maintenance service for the HW we provide.

Our PCM (Product Change Management) developer team is continuously processing all incoming PCN's (Product Change Notifications) from vendors and distributors concerning parts which are used in our products.

Possible impacts to the functionality of our products, due to changes of functionality or obsolesce of a certain part, are constantly being evaluated in order to take the right measures in purchasing or within our HW/SW design.

Our general philosophy here is: **We never discontinue a product as long as there is demand for it.**

Therefore we have established a set of methods to fulfill our philosophy:

Avoiding strategies

- Avoid changes by evaluating longevity of parts during design in phase.
- Ensure availability of equivalent second source parts.
- Stay in close contact with part vendors to be aware of roadmap strategies.

Change management (in case of functional changes)

- Avoid impacts on product functionality by choosing equivalent replacement parts.
- Avoid impacts on product functionality by compensating changes through HW redesign or backward compatible SW maintenance.
- Provide early change notifications concerning functional relevant changes of our products.

Change management (in rare event of an obsolete and non replaceable part)

- Ensure long term availability by stocking parts through last time buy management according to product forecasts.
- Offer long term frame contract to customers.

Therefore, we refrain from providing detailed part specific information within this manual, which can be subject to continuous changes, due to part maintenance for our products.

In order to receive reliable, up to date and detailed information concerning parts used for our product, please contact our support team through the contact information given within this manual.

1 Introduction

1.1 Hardware Overview

The phyBOARD-Nunki i.MX 6 for phyCORE-i.MX 6 modules is a low-cost, feature-rich software development platform supporting the NXP® Semiconductor i.MX 6 microcontroller. Moreover, due to the numerous standard interfaces, the phyBOARD-Nunki i.MX 6 can serve as the foundation for any application. At the core of the phyBOARD-Nunki is the PCM-058/phyCORE-i.MX 6 System On Module (SOM), containing the processor, DRAM, NAND Flash, power regulation, supervision, transceivers, and other core functions required to support the i.MX 6 processor. Surrounding the SOM is the PBA-C-11/ phyBOARD-Nunki carrier board adding power input, buttons, connectors, signal breakout, and Ethernet connectivity among other peripherals.

Adding the phyCORE-i.MX 6 SOM into your own design is as simple as ordering the connectored version (PCM-058) and making use of our phyCORE Carrier Board reference schematics.

1.1.1 Features of the phyBOARD-Nunki i.MX 6

The phyBOARD-Nunki i.MX 6 supports the following features :

- Developed in accordance with PHYTEC's new SBCplus concept (*Preface*)
- PHYTEC's phyCORE-i.MX 6 SOM featuring an ARM Cortex-A9 single, dual, or quad core operating at speeds up to 1.2 GHz
- 150 mm × 75 mm form factor
- Boot from SD card or NAND Flash
- Two different power supply options (10.8 V to 26.4 V) via Barrel Connector (2.0 mm/6.3 mm) or 2 pole Molex Micro-Fit 3.0™ Right Angle Header (optional)
- One RJ45 jack for 10/100/1000 Mbps Ethernet
- One USB host interface brought out to an upright USB Standard-A connector
- One USB OTG interface available at an USB Micro-AB connector
- One Secure Digital / Multi Media Memory Card interface brought out to a Micro-SD connector (found on the bottom of the phyBOARD)
- CAN interface at 2×5 pin header 2.54 mm
- Two camera interfaces, each compatible with the PHYTEC phyCAM-P and phyCAM-S+ standard
- One MIPI CSI-2 interface (4 Lanes + Clock, +5 V, +3V3, Clock Input, I²C, additional control signals)
- Serial Debug Interface (UART2 over USB) at an USB Micro-AB connector
- Audio/Video (A/V) connectors (parallel, resistive touch screen, I2S, I²C, additional control signals)
- LVDS Display Connector (4 Lanes + Clock, USB, I²C, UART, power supply)
- Display Power Connector (VCC_IN, +5 V, +3V3, PWM, Display Enable)
- HDMI Connector

- Mini-PCIe Connector
- SATA Connector
- JTAG
- Reset-Button
- Multicolor-LED
- Expansion connector with different interfaces
- Additional gold cap buffered RTC

1.1.2 Block Diagram

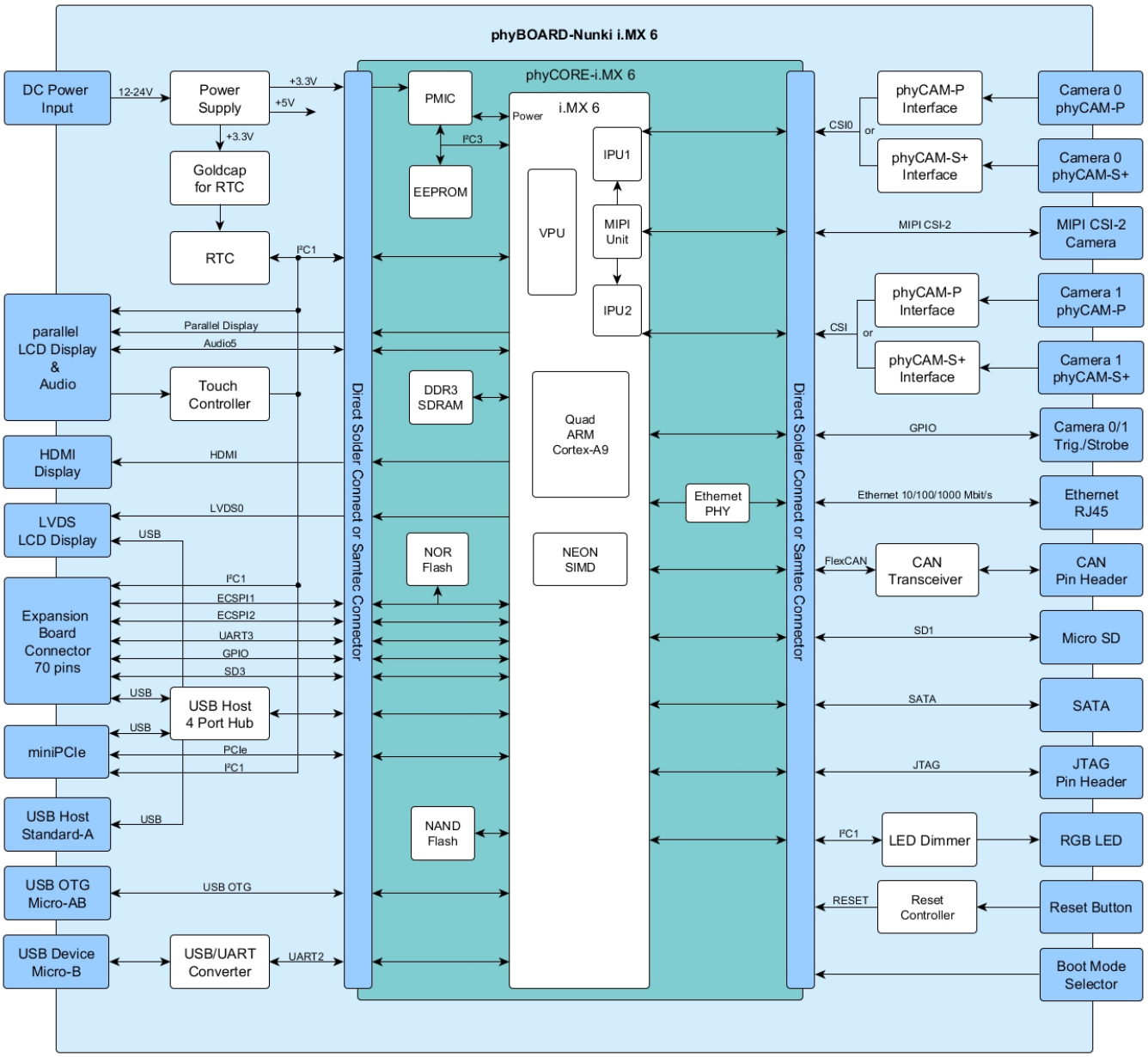


Figure 1: Block Diagram of the phyBOARD-Nunki i.MX 6

1.1.3 View of the phyBOARD-Nunki i.MX 6

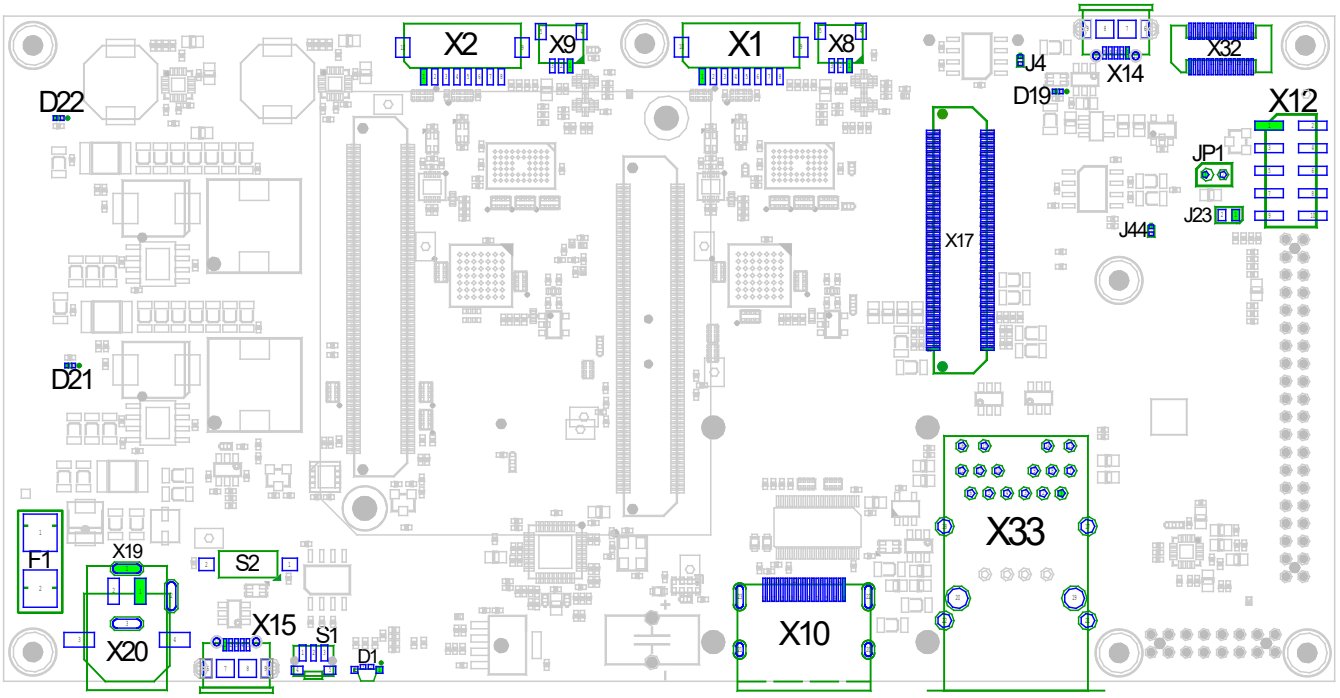


Figure 2: View of the phyBOARD-Nunki i.MX 6 (top)

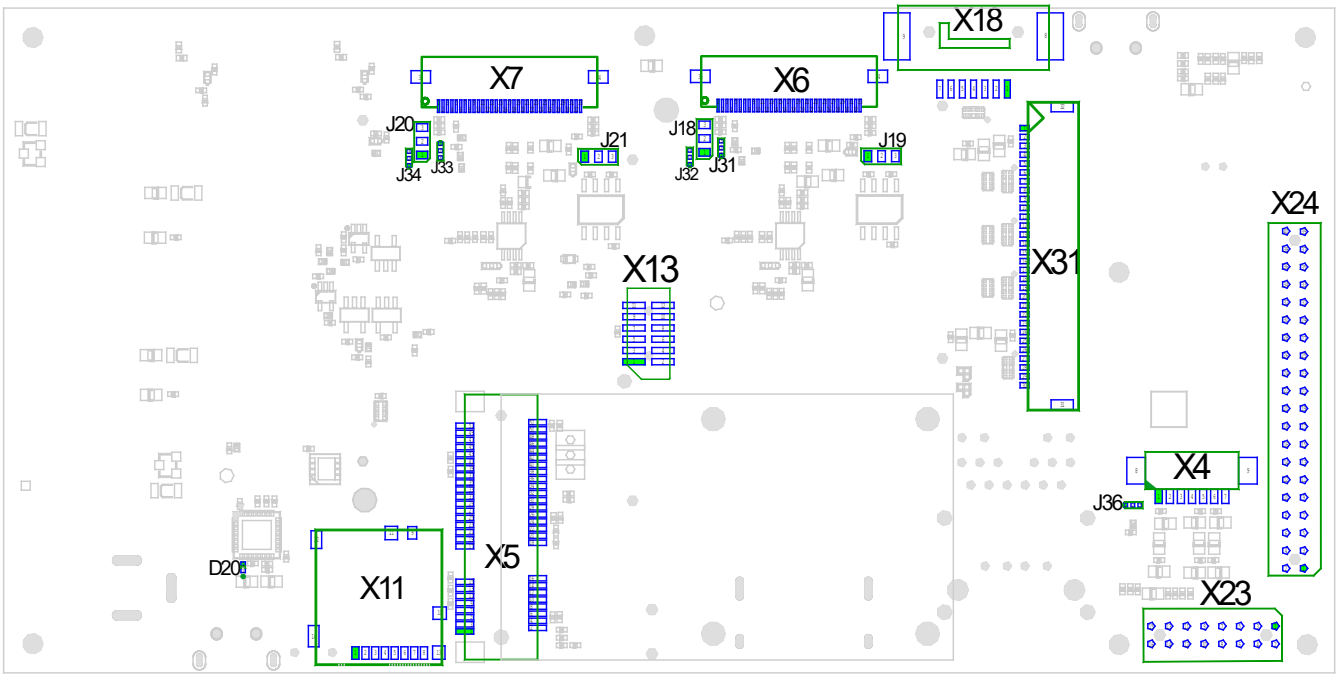


Figure 3: View of the phyBOARD-Nunki i.MX 6 (bottom)

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2 Accessing the phyBOARD-Nunki Features

PHYTEC phyBOARD-Nunki is fully equipped with all mechanical and electrical components necessary for a quick and secure start-up.

2.1 Overview of the phyBOARD-Nunki Peripherals

The phyBOARD-Nunki is depicted in *Figure 2* and *Figure 3*. It features many different interfaces and is equipped with the components listed in *Table 3* to *Table 6*. For a more detailed description of each peripheral refer to the appropriate chapter listed in the applicable table. *Figure 2* and *Figure 3* highlight the location and Pin 1 of each peripheral for easy identification.

2.1.1 Connectors and Pin Header

Table 3 lists all available connectors on the phyBOARD-Nunki. *Figure 2* and *Figure 3* highlight the location of each connector for easy identification.

Reference Designator	Description	See Section
X1	CSI0 phyCAM-S+ Connector	*2.2.4.1*
X10	HDMI Connector	*2.2.9*
X11	µSD-Card Slot	*2.2.7*
X12	CAN Connector	*2.2.6*
X13	JTAG Connector	*2.2.13*
X14	USB OTG Connector	*2.2.5.2*
X15	USB Debug Connector (UART2 to USB)	*2.2.3*
X17	Expansion Connector	*2.2.14*
X18	SATA Connector	*2.2.8*
X19	Power Connector +24 V (10,8 V – 26,4 V)	*2.2.1.1.1*
X2	CSI1 phyCAM-S+ Connector	*2.2.4.1*
X20	Power Connector +24 V (10,8 V – 26,4 V)	*2.2.1.1.2*
X23	Audio/res. Touch Connector	*2.2.11*
X24	Display Connector (Parallel Display)	*2.2.11*
X31	Universal Display Interface Connector (LVDS Display)	*2.2.10.1*
X32	MIPI CSI-2 Connector	*2.2.4.3*
X33	10/100/1000 Ethernet, USB Host Connector	*2.2.2/ 2.2.5.1*

Table 3: phyBOARD-Nunki i.MX 6 Connectors and Pin Headers

Reference Designator	Description	See Section
X4	Display Power Connector	2.2.10.2
X5	Mini PCIe Connector	2.2.12
X6	CSI0 phyCAM-P Connector	2.2.4.2
X7	CSI1 phyCAM-P Connector	2.2.4.2
X8	CSI0 phyCAM Trigger/Strobe Connector	2.2.4.4
X9	CSI1 phyCAM Trigger/Strobe Connector	2.2.4.4

Table 3: phyBOARD-Nunki i.MX 6 Connectors and Pin Headers (continued)

Caution!

- Ensure that all connections do not exceed their expressed maximum voltage or current. Maximum signal input values are indicated in the corresponding controller User's Manual/Data Sheets. As damage from improper connections varies according to use and application, it is the user's responsibility to take appropriate safety measures to ensure that the module connections are protected from overloading through connected peripherals.

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2.1.2 LEDs

The phyBOARD-Nunki i.MX 6 is populated with four LEDs to indicate the status of the USB VBUS voltages and the power supply voltage. There is also one user programmable multicolor LED

Figure 2 shows the location of the LEDs. Their functions are listed in *Table 4*.

LED	Color	Description	See Section
D1	RGB	Multicolor User-LED	*2.2.15*
D19	Green	Indicator for USB OTG voltage at connector X14	*2.2.5.2*
D20	Green	Indicator for USB Debug voltage at connector X15	*2.2.3*
D21	Green	Indicator for +3.3 V voltage for phyCORE	*2.2.1*
D22	Green	Indicator for +5 V voltage	*2.2.1*

Table 4: phyBOARD-Nunki i.MX 6 LEDs Descriptions

2.1.3 Buttons and Switches

The phyBOARD-Nunki i.MX 6 is populated with a push button to reset the phyBOARD and another DIP-Switch to select the boot source of the phyCORE i.MX 6.

Figure 2 shows the location of the button and switch. Their functions are listed in *Table 5*.

Switch	Description	See Section
S1	Reset Button	*2.2.17*
S2	Boot Source Selection	*2.2.16*

Table 5: phyBOARD-Nunki i.MX 6 Buttons Description

2.1.4 Jumpers

The phyBOARD-Nunki i.MX 6 comes pre-configured with one removable jumper (JP) and several solder jumpers (J). The jumpers allow for flexible configuration of a limited number of features for user development purposes.

Caution!

- Due to the small footprint of the solder jumpers (J), PHYTEC does not recommend manual jumper modifications. This might render the warranty invalid. Due to this, only the removable jumper is described in this section. For information on the solder jumpers, see *section 3.2* and contact our sales team if you need jumper configurations different from the default configuration.

The function of the removable jumper on the phyBOARD-Nunki i.MX 6 is shown in *Table 6*. More detailed information can be found in the appropriate section.

Figure 2 shows the location of jumper JP1.

Jumper	Description	See Section
JP1	CAN Termination Selection	*2.2.6*

Table 6: phyBOARD-Nunki i.MX 6 Jumper Description

Note:

- Detailed descriptions of the assembled connectors, jumpers and switches can be found in the following chapters.

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2.2 Functional Components on the phyBOARD-Nunki i.MX 6

This section describes the functional components of the phyBOARD-Nunki i.MX 6. Each subsection details a particular connector/interface and associated jumpers for configuring that interface.

2.2.1 Power Supply

Caution!

- Do not change modules or jumper settings while the phyBOARD is supplied with power!

2.2.1.1 Power Connectors (X19 and X20)

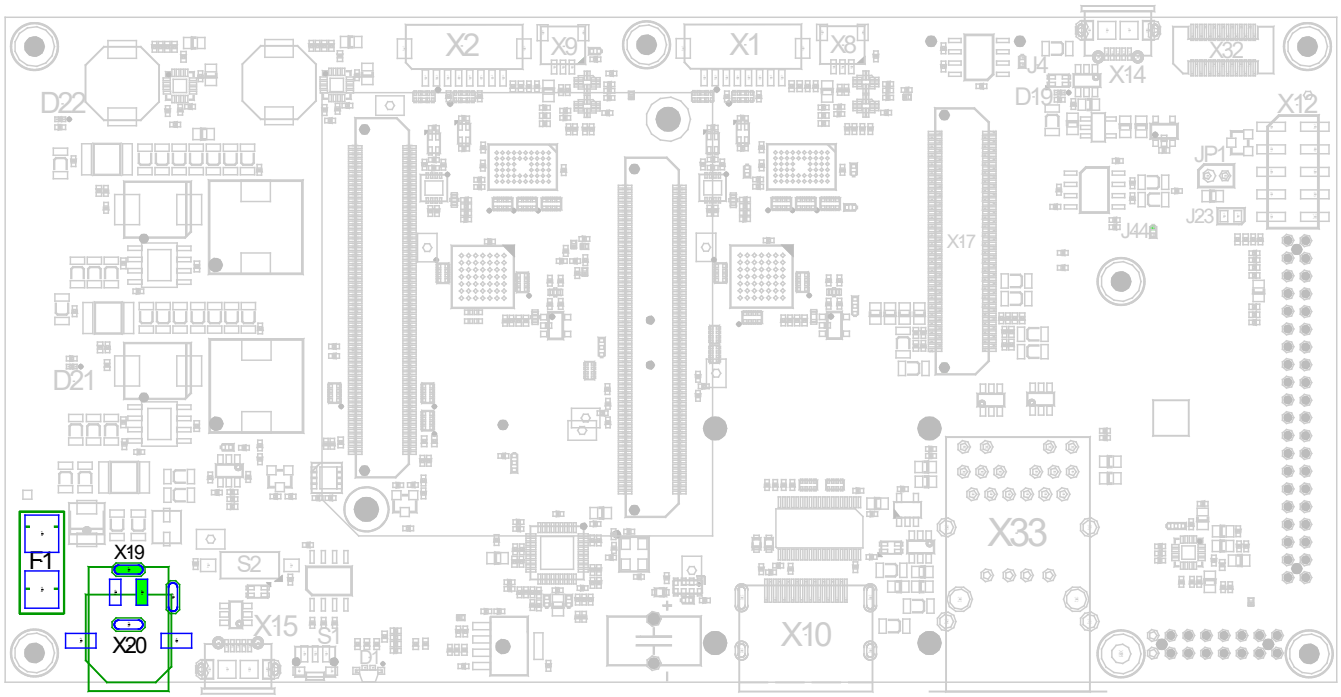


Figure 4: Power Supply Connectors(X19 and X20)

The phyBOARD-Nunki i.MX 6 is available with two different power supply connectors. Depending on your order, you will find one of the following connectors on your SBC:

1. a Barrel Connector with a diameter of 2.0 mm/6.3 mm, or
2. a 2 pole Molex Micro-Fit 3.0™ Right Angle Header (optional)

The required current load capacity for all power supply solutions depends on the specific configuration of the phyCORE mounted on the phyBOARD-Nunki i.MX 6, the particular interfaces enabled while executing software, as well as whether an optional expansion board is connected to the carrier board.

A 2 A Fuse (Fast-Acting Fuse) is used to cut off the external power supply from the phyBOARD in case of an electrical error.

2.2.1.1.1 Barrel Connector (X19)

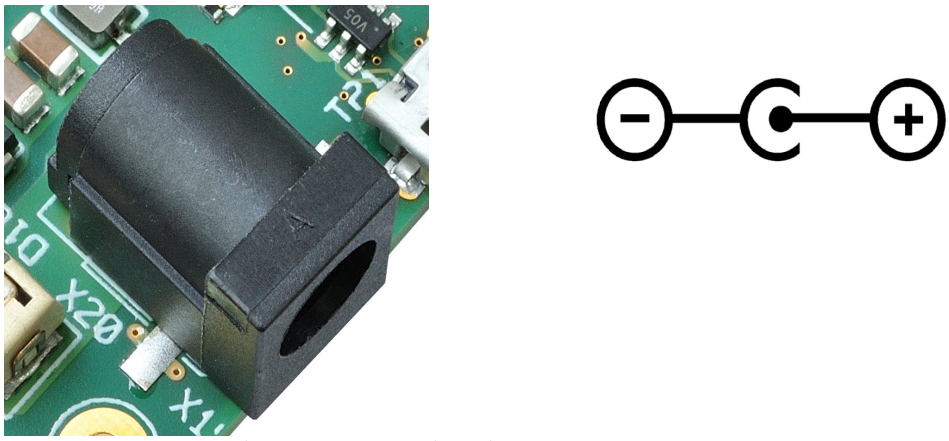


Figure 5: Barrel Connector with polarity

The permissible input voltage is +10.8 V to +26.4 V DC. The phyBOARD-Nunki i.MX 6 is designed for a nominal voltage of +24 V ± 10 %. The power supply voltage +24V_IN is routed to several plug connectors on the board as +24V_IN_FILTER. An external power supply with a minimum supply of 2 A is recommended to supply the board via the 2-pole base strip.

Pin assignment of the Barrel Connector at X19:

Pin	Signal	Description
1	+24V_IN	+24 V power supply in (+10.8 V to +26.4 V)
2/3	GND	Ground

Table 7: Pin Assignment of the Barrel Connector at X19

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2.2.1.1.2 Molex Micro-Fit 3.0™ (X20)

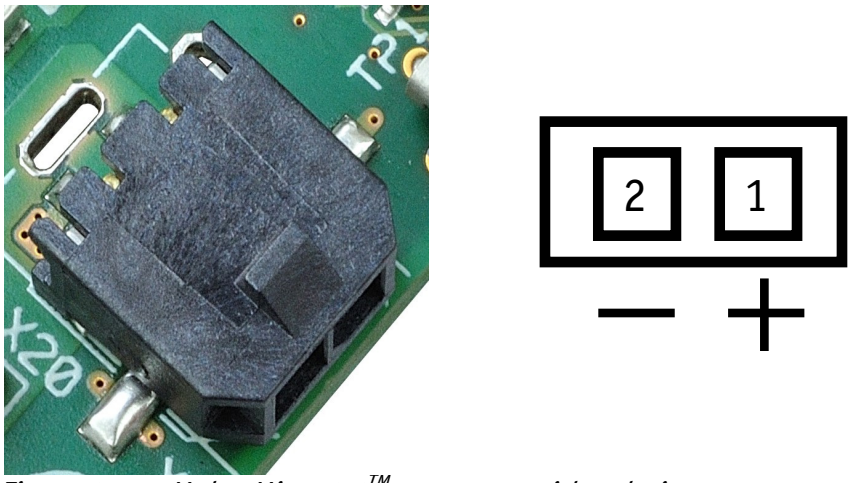


Figure 6: Molex Micro 3.0™ connector with polarity

With a Molex Micro-Fit 3.0™, the phyBOARD can be supplied using a plug connector.

Use of the 2-pole connector has the following advantages:

- Lockable plug connection
- Flexible Design
- Secure against accidental disconnection or misconnection
- Ideal for product-specific power supply solutions

Pin assignment of the 2–pole Molex Micro-Fit 3.0™ Header at X20:

Pin	Signal	Description
1	+24V_IN	+24 V power supply in (+10.8 V to +26.4 V)
2	GND	Ground

Table 8: Pin Assignment of the 2-pole Molex Micro-Fit 3.0™ Connector at X20

2.2.1.2 Power LED D21 and D22

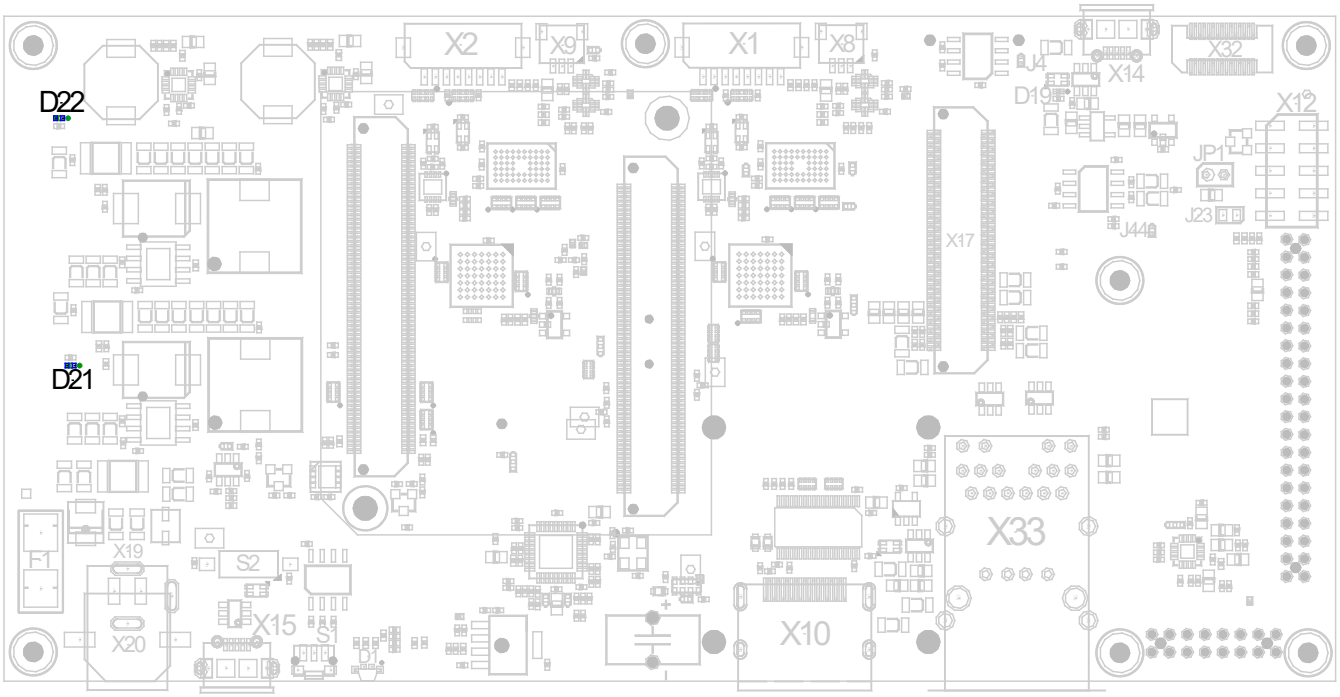


Figure 7: Power Supply LEDs D21 and D22

The green LED D21 on the middle left-hand side of the board (*Figure 7*) indicates the presence of the +3.3 V supply voltage of the phyCORE module generated from the +24V_IN input voltage.

The green LED D22 on the upper left-hand side of the board (*Figure 7*) indicates the presence of the +5 V supply voltage of the phyBOARD peripherals generated from the +24V_IN input voltage.

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2.2.2 Ethernet Connectivity (X33)

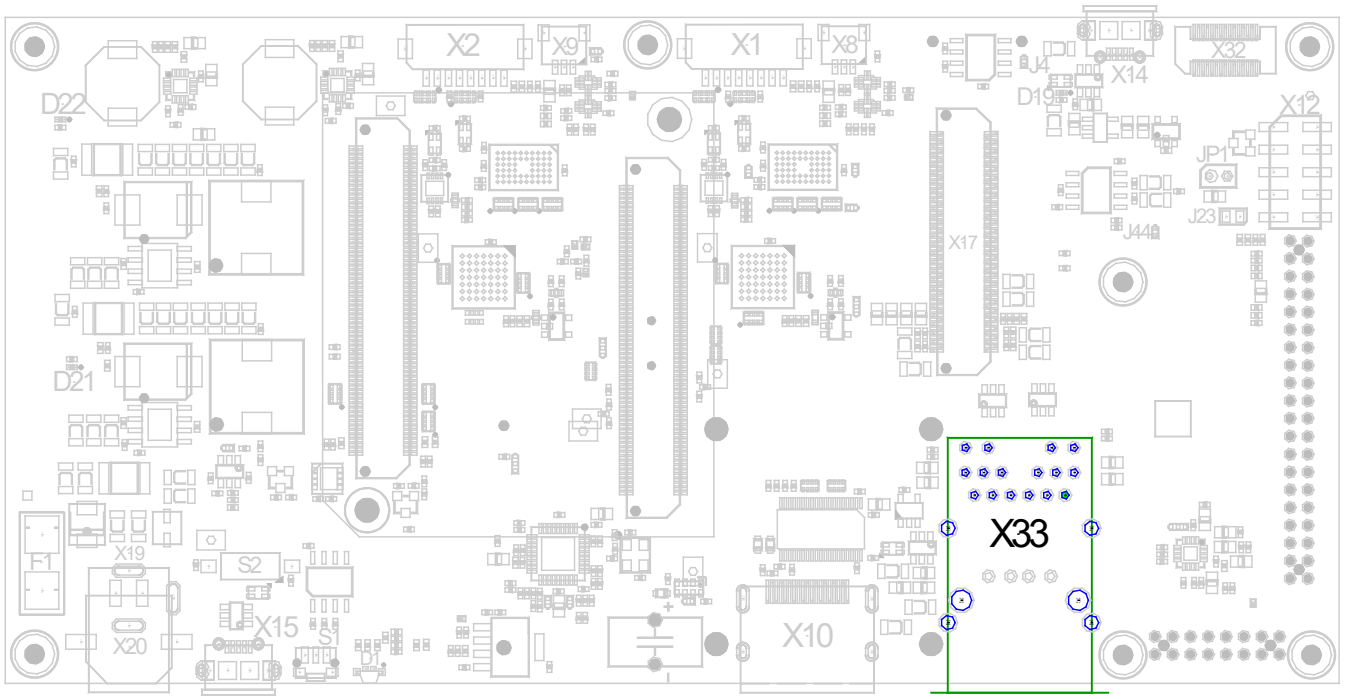


Figure 8: Ethernet Interfaces at Connector X33

The Ethernet interfaces of the phyBOARD-Nunki i.MX 6 are accessible at RJ45 connector X33. X33 is located on the lower right side of the board (see *Figure 8)*

Ethernet is directly brought out from the SOM's Ethernet interface. The Ethernet interface is configured as 10/100/1000Base-T network. The LEDs for LINK (green) and TRAFFIC (orange) are integrated into the connector. The Ethernet transceiver supports HP Auto-MDIX, eliminating the need for a direct connect LAN or a cross-over path cable. They detect the TX and RX pins of the connected device and automatically configure the PHY TX and RX pins accordingly.

2.2.2.1 MAC Address

In a computer network such as a local area network (LAN), the MAC (Media Access Control) address is a unique computer hardware number. For a connection to the Internet, a table is used to convert the assigned IP number to the hardware's MAC address.

In order to guarantee that the MAC address is unique, all addresses are managed in a central location. PHYTEC has acquired a pool of MAC addresses. The MAC address of the phyBOARD-Nunki i.MX 6 is located on the Data Matrix sticker attached to the module. This number is a 12-digit HEX value.

2.2.3 UART Connectivity (X15 and X17)

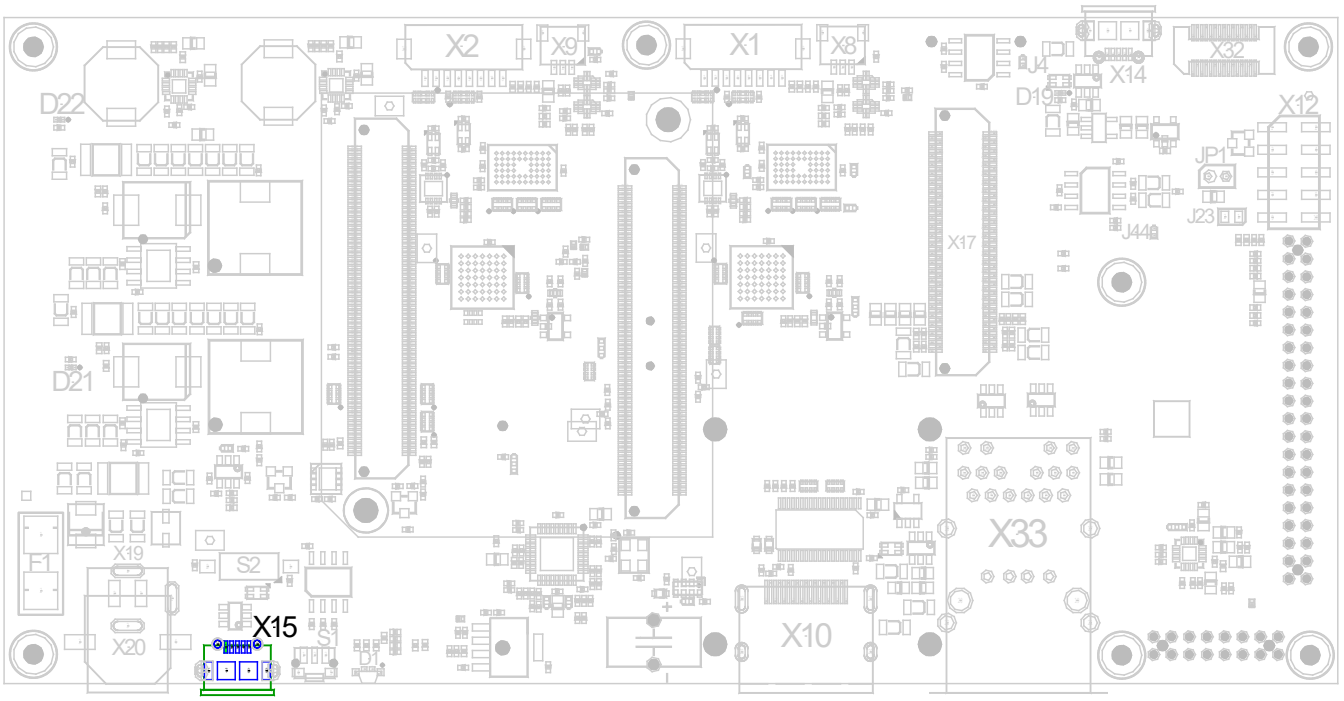


Figure 9: USB Debug Connector (X15)

The phyCORE-i.MX 6 provides up to 2 high speed universal asynchronous interfaces. The phyBOARD UART2 (the standard console) is routed to X15 (micro USB AB) via an UART USB converter. X15 is located on the top of the board next to the power converter (see *Figure 9*). The UART USB converter accesses the host PC as COM interface and can be used as such with a terminal program. The green LED D20 (*Figure 7*) indicates that the UART USB converter is powered by the Host-PC.

Suitable connection cables:

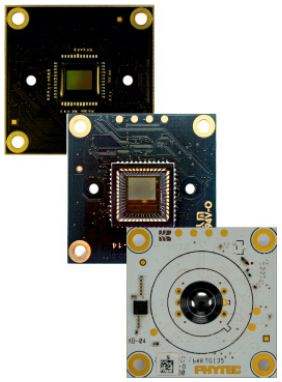
PHYTEC Item no.	Length	Remarks
WK345	1 m	USB A to micro USB B

UART3 is routed to expansion connector X17. Further information on the expansion connector can be found in *section 2.2.14* and *section 3.2.10*.

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2.2.4 Camera Connectivity (X1, X2, X6-X9)

The phyBOARD-Nunki i.MX 6 provides three types of camera interfaces (parallel, LVDS and MIPI/CSI-2).



On the target application, the camera interfaces can be used to connect:

- camera modules with phyCAM-S+ interface (*Figure 9* and *section 3.2.4.1*, circuitries "Camera_0, phyCAM-S+" and "Camera_1, phyCAM-S+")
- camera modules with phyCAM-P interface (*Figure 9* and *section 3.2.4.2*, circuitries "Camera_0, phyCAM-P" and "Camera_1, phyCAM-P)
- camera modules with MIPI/CSI-2 interface (circuitry "Camera_2, CSI-2 (MIPI)")
- Two trigger/strobe headers, e.g. for synchronized image capturing, exposure control, etc.

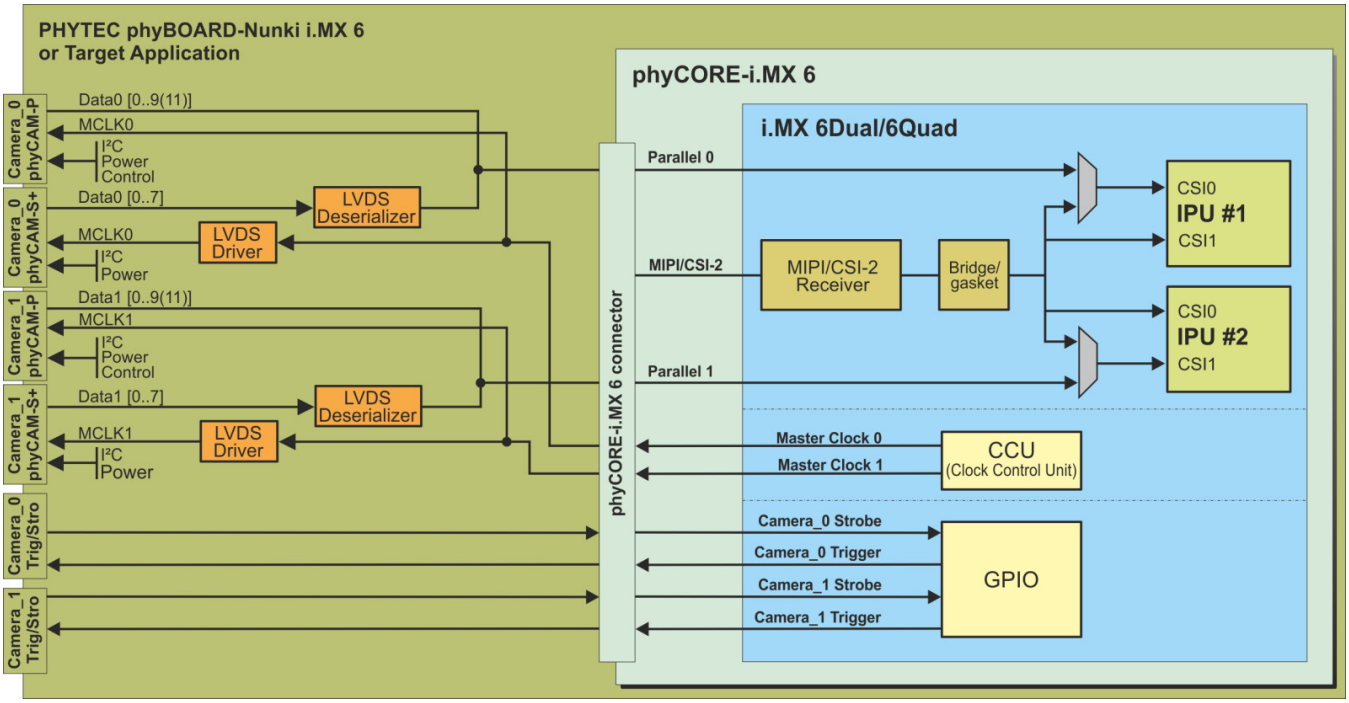


Figure 10: Overview phyBOARD-Nunki i.MX 6 phyCAM interface

The following sections give a basic overview on how to connect a camera using the different interface options. All figures show the phyBOARD-Nunki i.MX 6 equipped with the i.MX 6 dual and quad core with two parallel interfaces.

Additional information on connectable phyCAM modules can be found in the *phyCAM manual (L-748e)*.

2.2.4.1 phyCAM-S+ (LVDS) Camera Interfaces (X1, X2)

Available phyCAM-S+ cables:

PHYTEC Item no.	Length	Cable type
WK262-0.2	20 cm	wires
WK353-0.2	20 cm	CAT5
WK353-0.5	50 cm	CAT5
WK431-0.5	50 cm	USB3.0

Table 9: Available phyCAM-S+ cables

The phyCAM-S+ is particularly suitable for external camera installation. Usually, the recommended cable length is 5 m. The maximum achievable cable length, however, greatly depends on the operating parameters (e.g. power consumption, clock frequency, read-out mode) of the camera module and the overall device configuration. Under certain circumstances, longer cable lengths may be possible or shorter cable lengths may be required. Please consult with PHYTEC project engineers to determine the best configuration.

Camera_0 (connected to IPU1_CSI0) as phyCAM-S+ (X1)

The 1-channel 10-Bit LVDS random lock deserializer (U15) on the phyBOARD-Nunki i.MX 6 is connected to the i.MX 6's camera sensor interface CSI0 of IPU#1. The LVDS deserializer converts the LVDS signals received at the header X1 on the carrier board to a 10-bit wide parallel data signal and separate clock. The camera interface is compatible with the PHYTEC phyCAM-S+ camera interface standard. *Figure 7* depicts the signal path.

For pin assignment see: *section 3.2.4.1*

Camera_1[1] (connected to IPU2_CSI1) as phyCAM-S(+) (X2)

The 1-channel 10-Bit LVDS random lock deserializer (U16) on the phyBOARD-Nunki i.MX 6 is connected to the i.MX 6's camera sensor interface CSI1 of IPU#2. The LVDS deserializer converts the LVDS signals received at the header X2 on the carrier board to a 10-bit wide parallel data signal and separate clock. The camera interface is compatible with the PHYTEC phyCAM-S+ camera interface standard. *Figure 7* depicts the signal path.

For pin assignment see: *section 3.2.4.1*

1 Only i.MX 6 with Dual-, or Quad core. i.MX 6 with Solo-, or DualLite core provide only one parallel camera interface and one IPU.

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2.2.4.2 phyCAM-P (Parallel) Camera Interfaces (X6, X7)

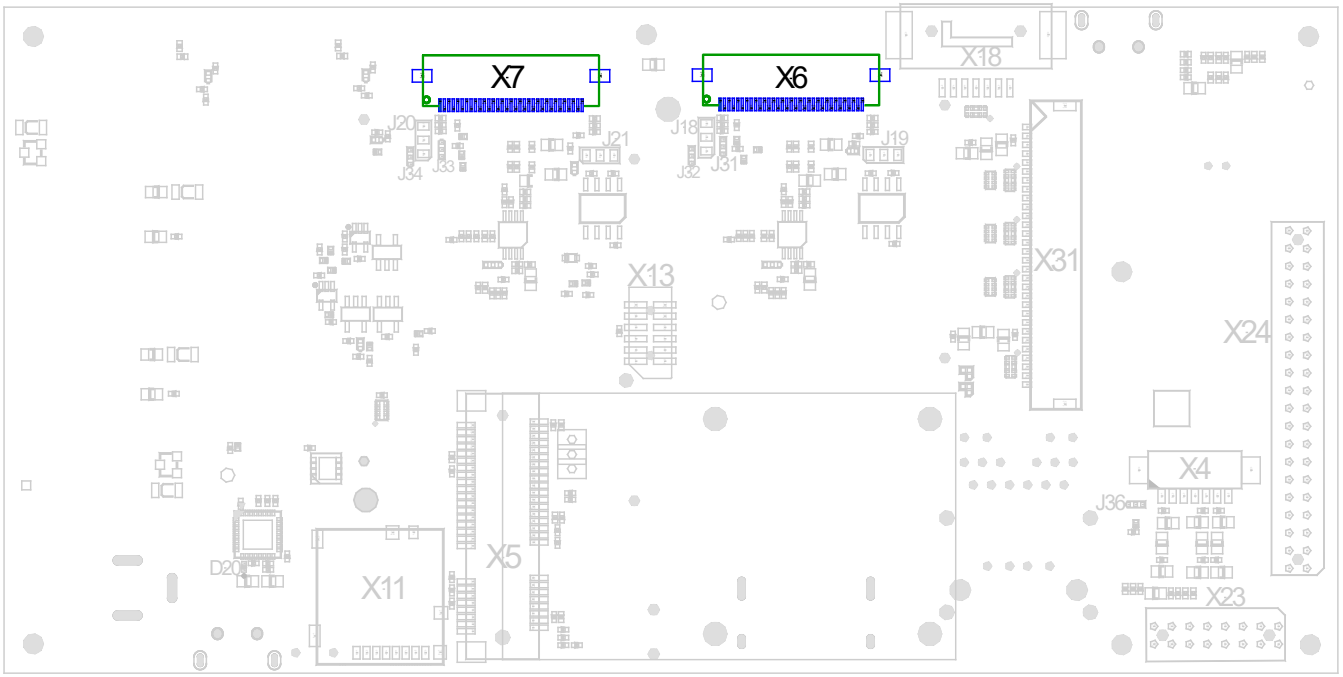


Figure 11: phyCAM P Interfaces (X6 and X7)

Available phyCAM-P cables:

PHYTEC Item no.	Length	Cable type
WF062	12 cm	FFC
WF043	20 cm	FFC
WF046	30 cm	FFC

Table 10: Available phyCAM P cables

The phyCAM-P is particularly suitable for the internal camera installation. Usually, the recommended cable length is 30 cm. The maximum achievable cable length, however, greatly depends on the operating parameters (e.g. power consumption, clock frequency, read-out mode) of the camera module and the overall device configuration. Under certain circumstances, longer cable lengths may be possible or shorter cable lengths may be required. Please consult with PHYTEC project engineers to determine the best configuration.

The voltage suppy (VCC_CAM) and the signal voltages depend on the camera module in use. The phyCAM-P Interface of the phyBOARD-Nunki i.MX 6 is designed for the greatest possible compatibility with different phyCAM-P modules to easily use such devices without hardware customization. Further information on the control signals (for example CAM-CTRLx) can be found in the *phyCAM manual (L-748e)*.

Camera_0 (connected to IPU1_CSI0) as phyCAM-P (X6)

The Parallel 0 camera interface of the i.MX 6 connects to CSI0 of IPU#1. It is brought out as a parallel interface on the phyCORE connector X3. The phyBOARD allows either camera module to connect with phyCAM-P interface at connector X6 (33-pin FPC-connector, 0.5 mm pitch). *Figure 7* depicts the signal path.

For pin assignment see: *section 3.2.4.2*

Camera_1[2] (connected to IPU2_CSI1) as phyCAM-P (X7)

The Parallel 1 camera interface of the i.MX 6 connects to CSI1 of IPU#2. It is brought out as a parallel interface on the phyCORE connector X3. The phyBOARD allows either camera module to connect with phyCAM-P interface at connector X6 (33-pin FPC-connector, 0.5 mm pitch). *Figure 7* depicts the signal path.

For pin assignment see: *section 3.2.4.2.*

Caution!

- It is not possible to simultaneously connect a phyCAM-P and a phyCAM-S+ camera to one of the interfaces (Camera_0 or Camera_1). Selection of either phyCAM-P or phyCAM-S+ as interface type can be done at run time.

Note:

- For more information on the PHYTEC camera interfaces phyCAM-P and phyCAM-S+, refer to the documentation delivered with the camera module (*phyCAM manual L-748e*).

2: Only i.MX 6 with Dual-, or Quad core. i.MX 6 with Solo-, or DualLite core provide only one parallel camera interface and one IPU.

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2.2.4.3 MIPI/CSI-2 Interface (X32)

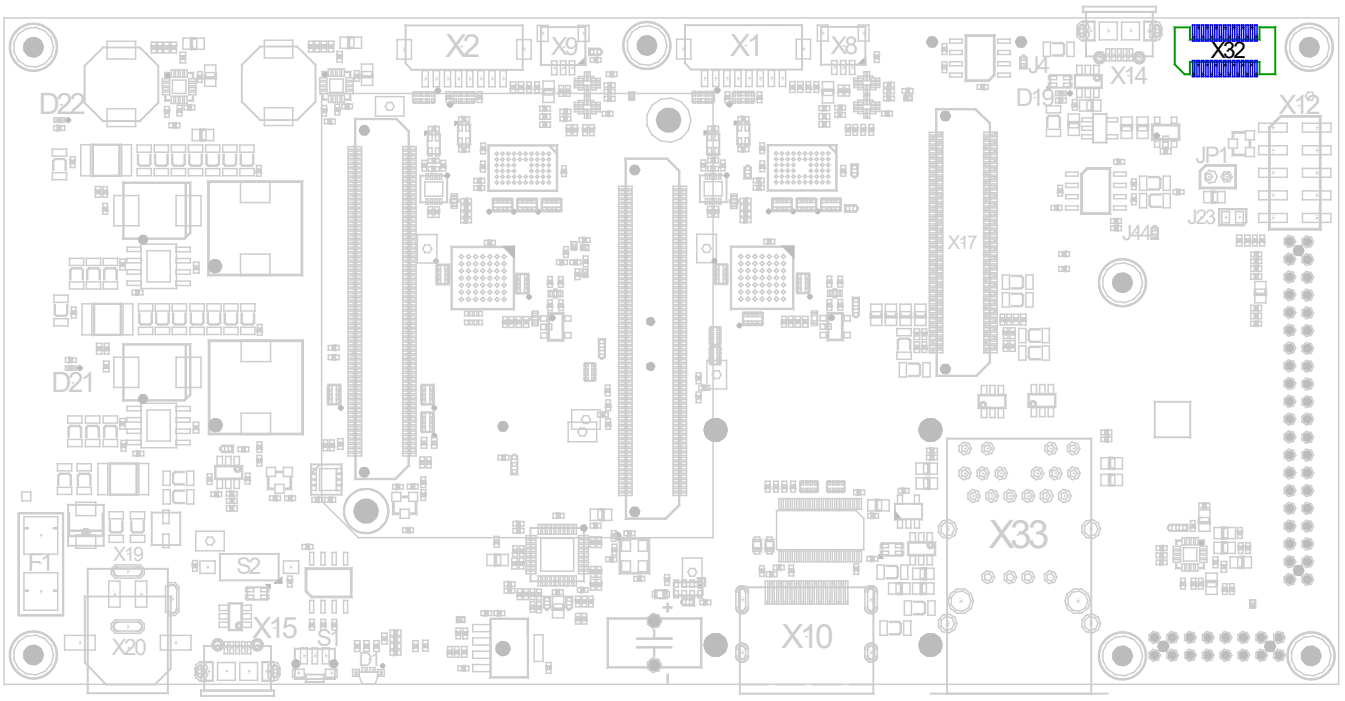


Figure 12: MIPI/CSI-2 Interface (X32)

The MIPI CSI-2 camera interface is also available at the connectors of the phyBOARD-Nunki i.MX 6. It can be used alternatively to connect camera sensors with MIPI/CSI-2 interface. The phyBOARD-Nunki i.MX 6 allows for the connection of camera modules with MIPI/CSI-2 interface (with up to 4 data lanes and one clock) at connector X32 (30-pinMolex connector, 0.5 mm pitch).

For pin assignment see: *section 3.2.4.3*

Note:

- Depending on the configuration of the CSI2IPU Bridge/Gasket and the internal multiplexer(s), Camera_0 and/or Camera_1 are not available if one or more MIPI compliant sensors are connected to the Camera_2 connector of the mapper.

2.2.4.4 Trigger-/ Strobe Connector (X8, X9)

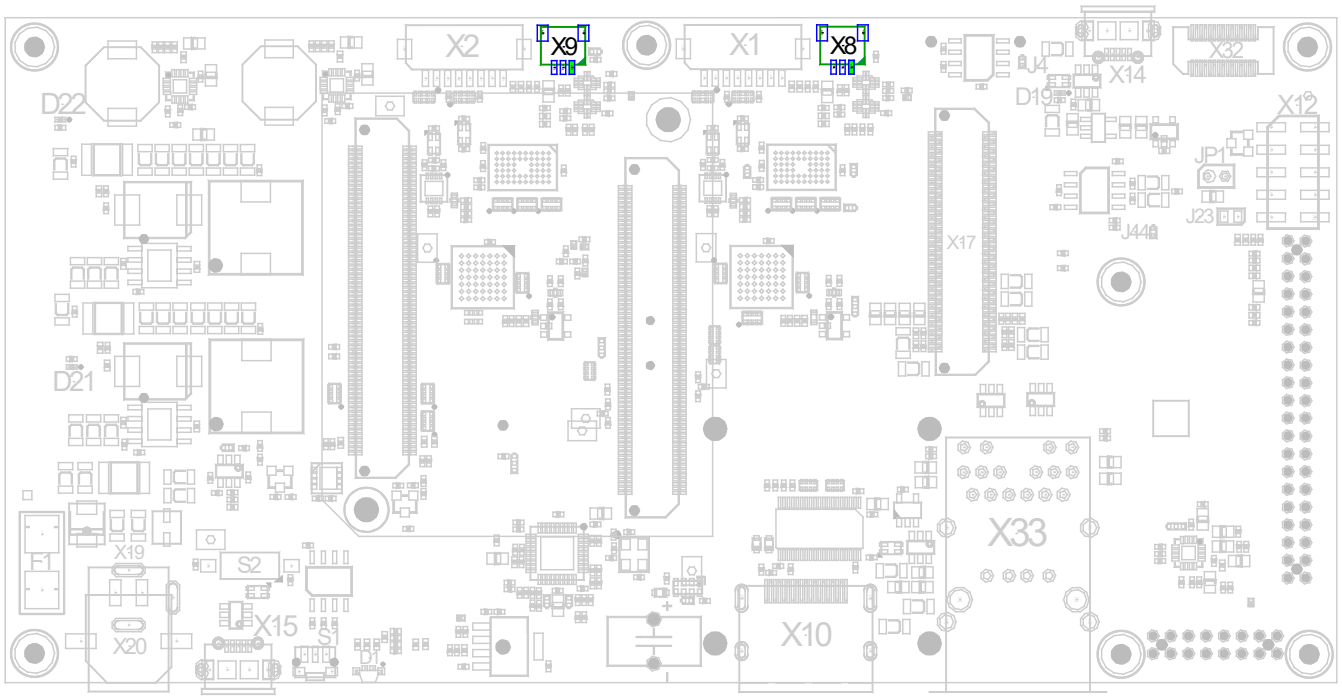


Figure 13: Trigger/Strobe Connector (X8 and X9)

Many phyCAM modules are equipped with an additional header for controlling the image capturing. This allows for various configurations. For instance, a timed image capture can be started or two camera sensors can be synchronized with each other. The specific mode of operation depends on the sensor. Please refer to the *phyCAM manual (L-748e)* for further information.

For pin assignment see: *section 3.2.4.4*

Available trigger/strobe cables:

PHYTEC Item no.	Length
WK295	25 cm
WK295-0.03	3 cm

Table 11: Available phyCAM trigger/strobe cables

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2.2.5 USB Connectivity

2.2.5.1 USB-Host Connectivity (X33)

The phyBOARD-Nunki i.MX 6 provides one USB host and one USB OTG interface. The USB OTG interface (see *Figure 6*) is described in *section 2.2.5.2*.

USB1 is accessible at connector X33 (USB Standard-A) located on the top of the phyBOARD and is configured as USB host. This interface is compliant with USB revision 2.0.

2.2.5.2 USB-OTG Connectivity (X14)

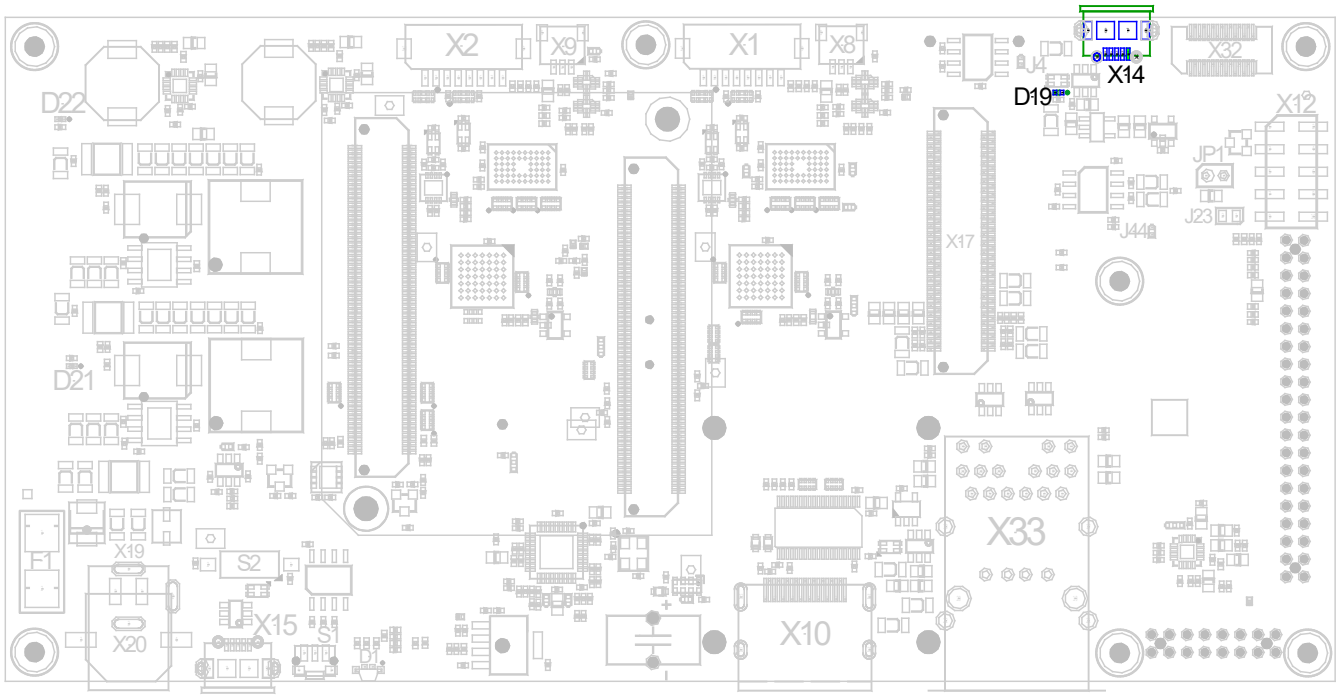


Figure 14: USB OTG (X14) with LED (D19)

The USB OTG interface is routed to X14. USB OTG devices are capable of initiating a session, controlling the connection, and exchanging host and peripheral roles between each other. This interface is compliant with USB revision 2.0.

LED D19 displays the status of USB_OTG_VBUS. If D19 is turned off, the USB OTG interface is configured as USB Device (e.g. as a serial console). In this case, the phyBOARD does not have to be powered by a Host-PC as the phyBOARD provides the needed voltage itself. If D19 is turned on, the USB OTG interface is configured as a USB Host like X33. That means the phyBOARD powers the connected USB Device.

Caution!

- If the USD OTG interface is configured as a host, do not short USB_OTG_VBUS to an external power supply. Doing so may cause damaging cross current!

2.2.6 CAN Connectivity (X12, JP1)

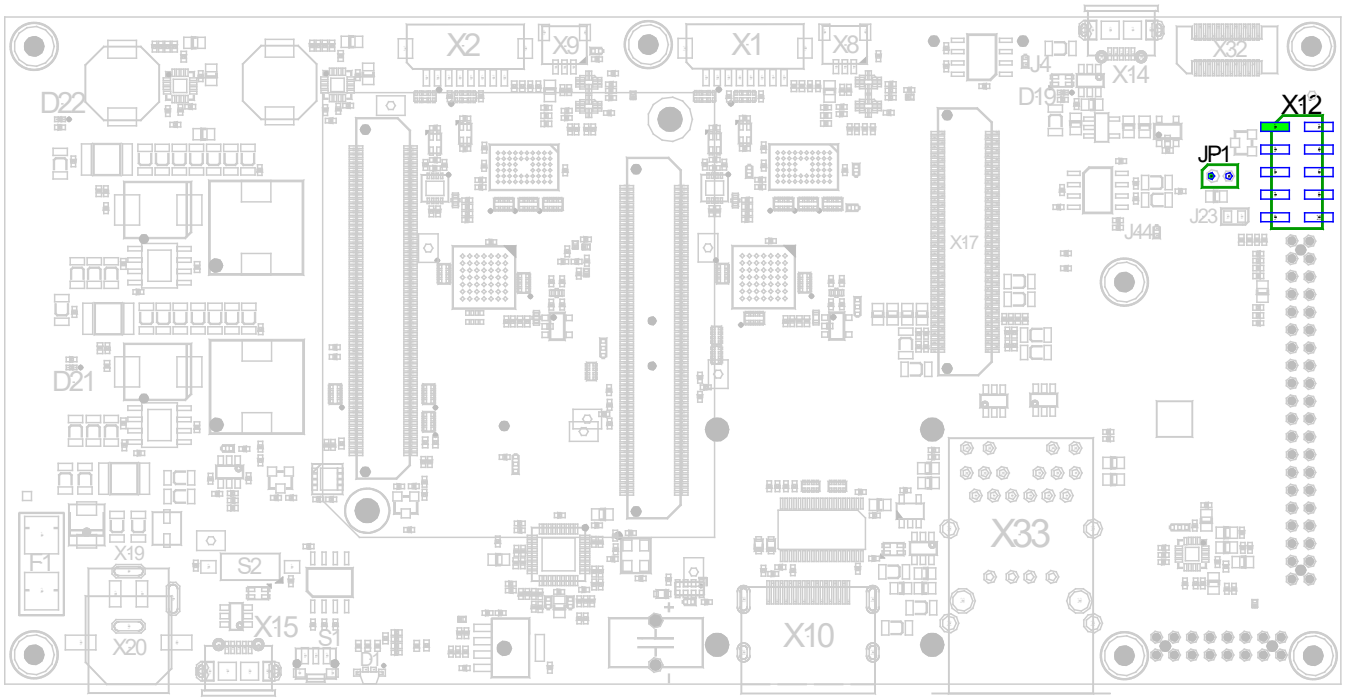


Figure 15: Connectors supporting the CAN Interface

The Controller Area Network (CAN) bus offers a low-bandwidth, prioritized message fieldbus for serial communication between microcontrollers. It efficiently supports distributed real time control with a high level of security. The Flexible Controller Area Network (FLEXCAN1) module of the iMX 6 is a full implementation of the CAN protocol specification version 2.0B. It supports standard and extended message frames and supports bitrates of up to 1 Mbit/s.

The first interface (FLEXCAN1) of the Flexible Controller Area Network is accessible at connector X12 (2×5 pin header, 2.54 mm pitch).

Jumper JP1 can be mounted to add a 120 Ohm termination resistor across the CAN data lines if needed.

Suitable connection cables

PHYTEC Item no.	Length	Remarks
WF228	12 cm	10-pole RM2.54 pin connector to 9-pole SUB-D male

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Table 12 shows the signal mapping of the CAN1 signals at connector X6.

Pin	Signal	Pin	Signal
1	NC	2	GND
3	X_CANL	4	X_CANH
5	GND	6	NC
7	NC	8	NC
9	Shield	10	NC

Table 12: Pin Assignment of CAN Connector X6

An adapter cable is included in the phyBOARD-Nunki i.MX 6 Kit to facilitate the use of the CAN interface. The following figure shows the signal mapping of the adapter.

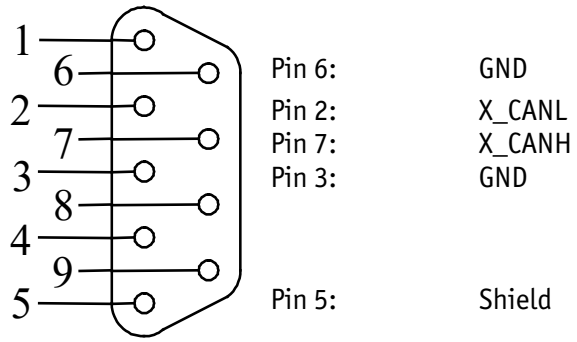


Figure 16: WF228 CAN Connector Signal Mapping

2.2.7 Secure Digital Memory Card/MultiMedia Card (X11)

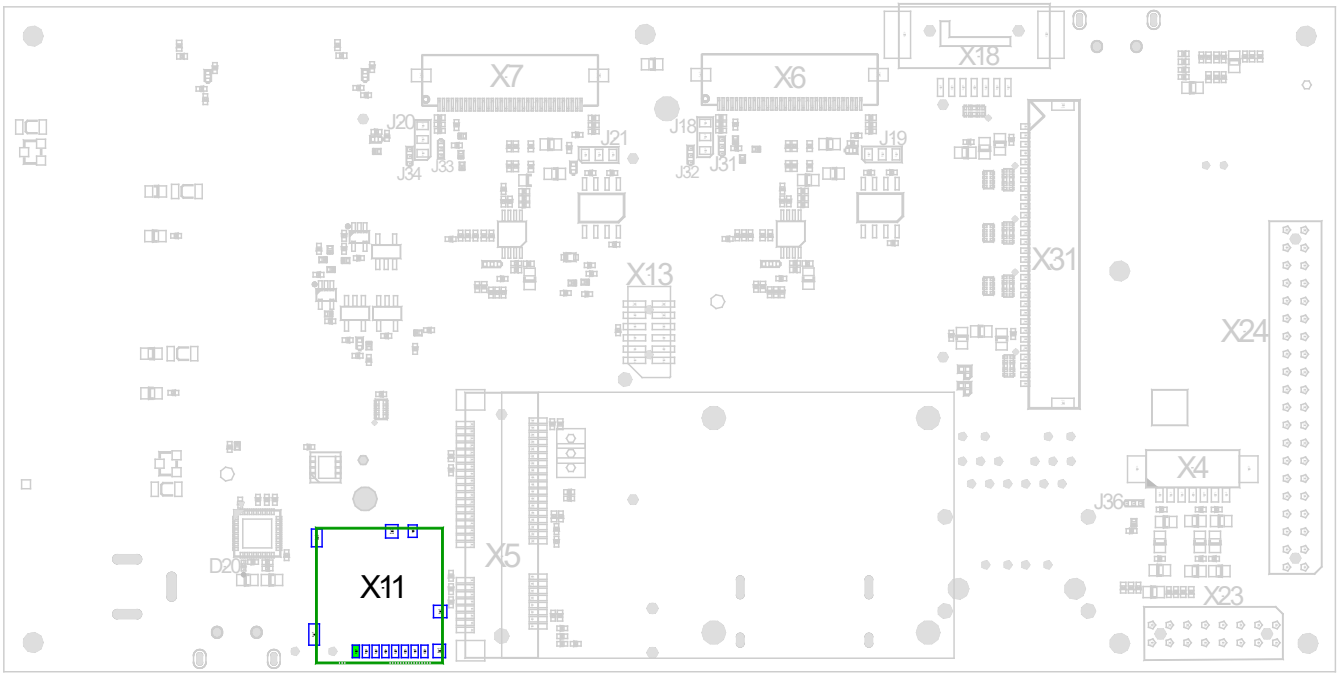


Figure 17: SD/MMC Interface at Connector X11

The phyBOARD-Nunki i.MX 6 provides a standard microSDHC card slot at X11 for connection to SD/MMC interface cards. It allows for an easy and convenient connection to peripheral devices such as SD and MMC cards. Power to the SD interface is supplied by inserting the appropriate card into the SD/MMC connector, which features card detection, a lock mechanism and a smooth extraction function by Push-in/Push-out of card.

An inserted SD card can be used as a boot source via S2. See *section 2.2.16* for a description of the boot configuration.

The SD/MMC connector complies with High Speed Bus IF and can support up to Class 10 speed rating.

Suitable micro SD memory cards:

PHYTEC Item no.	Memory	Class	Temp. range
MC057	1 GB	Class 4	-25 / +85°C
MC023	2 GB	Class 4	-40 / +85°C
MC042	4 GB	Class 4	-25 / +85°C
MC047	4 GB	Class 10	-25 / +85°C
MC051	32 GB	Class 10	-25 / +85°C

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2.2.8 SATA (X18)

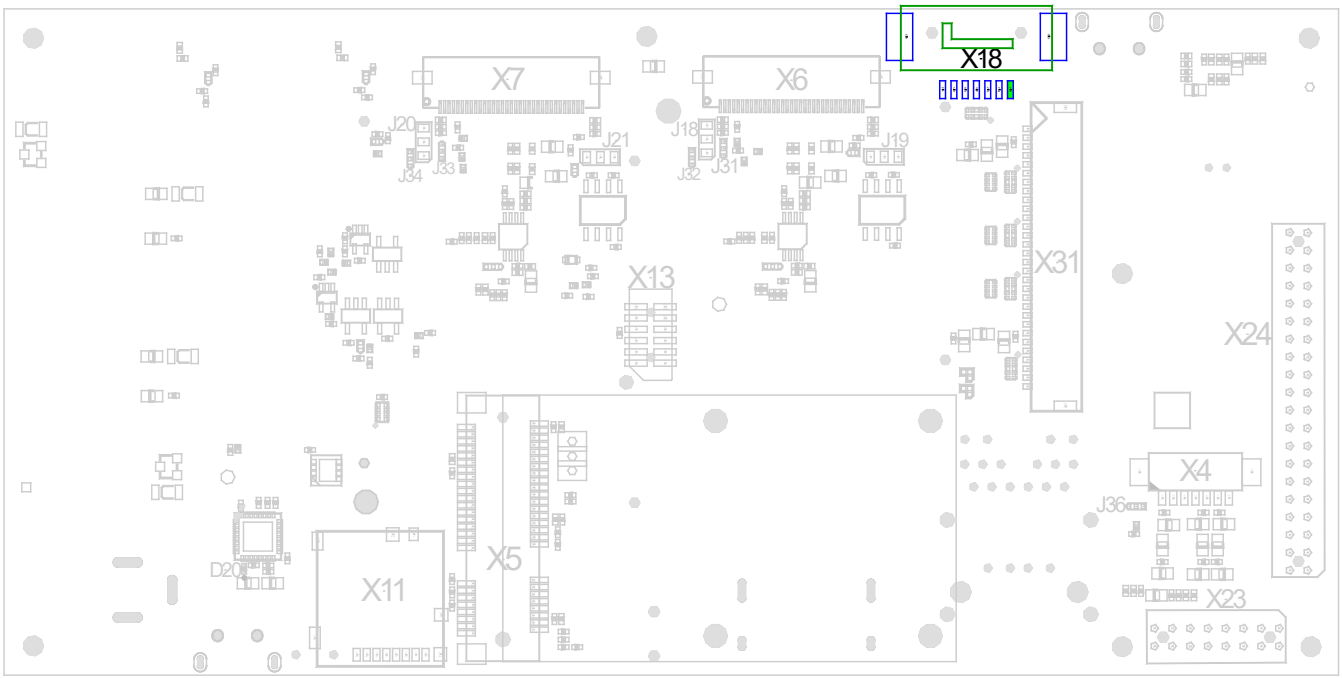


Figure 18: SATA Connector X18

The SATA II interface of the phyBOARD-Nunki i.MX 6 is a high-speed serialized ATA data link interface compliant with SATA Revision 3.0 (physical layer complies with SATA Revision 2.5). The interface includes an internal DMA engine, command layer, transport layer, link layer and the physical layer. The interface is brought out at a standard SATA connector (X18) on the phyBOARD.

2.2.9 HDMI Connectivity (X10)

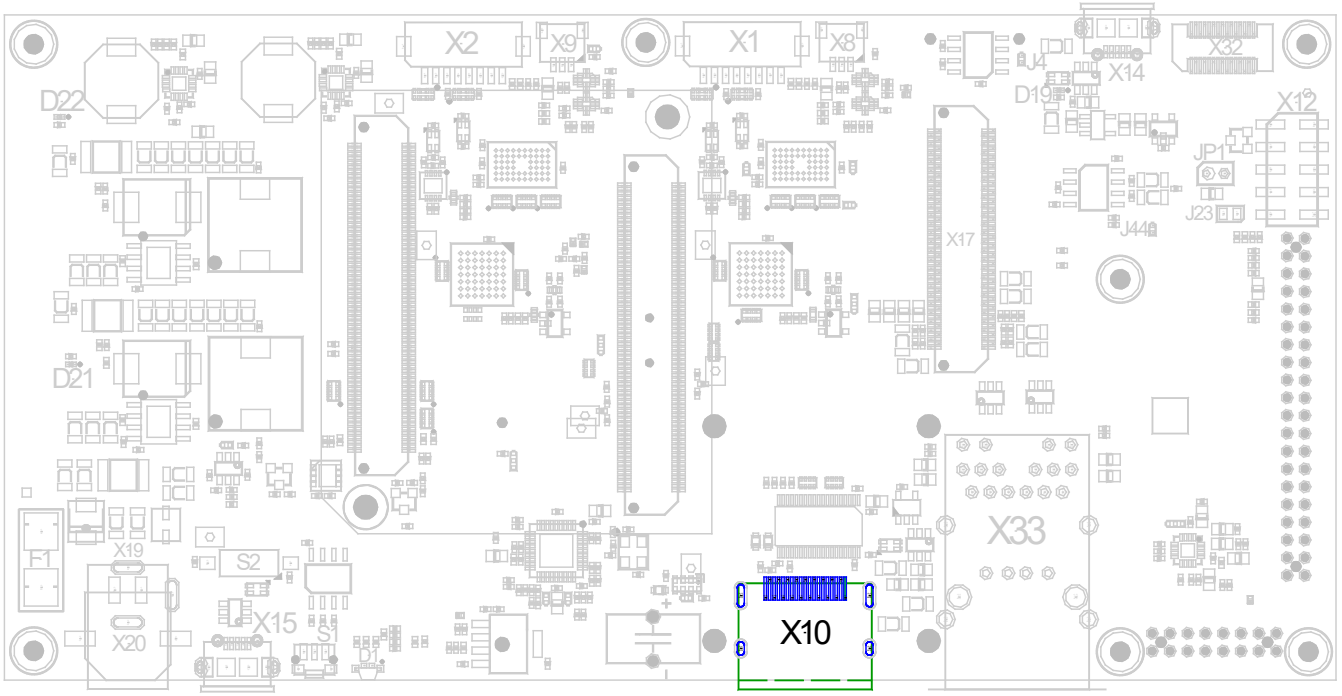


Figure 19: HDMI Interface X10

The phyBOARD-Nunki i.MX 6 provides a High-Definition Multimedia Interface (HDMI) which is compliant to HDMI 1.4a, DVI 1.0, HDCP 1.4. It supports a maximum pixel clock of up to 340 MHz for up to 720p at 100 Hz and 720i at 200 Hz, or 1080p at 60 Hz and 1080i/720i at 120 Hz HDTV display resolutions, and a graphic display resolution of up to 2048x1536 (QXGA). Audio streams reach a sampling rate of up to 192 kHz. Please refer to the *i.MX 6 Applications Processor Reference Manual* for more information.

The HDMI interface is brought out at a standard HDMI type A connector (X10) on the phyBOARD-Nunki i.MX 6 and is comprised of the following signal groups: three pairs of data signals, one pair of clock signals, an I²C bus which is exclusively for the HDMI interface, the Consumer Electronics Control (CEC) signal and the hot plug detect (HPD) signal. All signals are routed from the phyCORE-Connector to the HDMI receptacle through an HDMI Transmitter Port Protection and Interface Device. This device provides ESD protection and includes level shifting to shift the I²C interface signals and the hot plug detect signal from IO voltage (VCC3V3) to 5 V. The hot plug detect signal is pulled down to ground at the output of the protection device.

Caution!

- Ensure that all connections do not exceed their expressed maximum voltage or current. Maximum signal input values are indicated in the corresponding controller User's Manual/Data Sheets. As damage from improper connections varies according to use and application, it is the user's responsibility to take appropriate safety measures to ensure that the module connections are protected from overloading through connected peripherals.

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2.2.10 Universal Display Interface

2.2.10.1 LVDS Display Connector (X31)

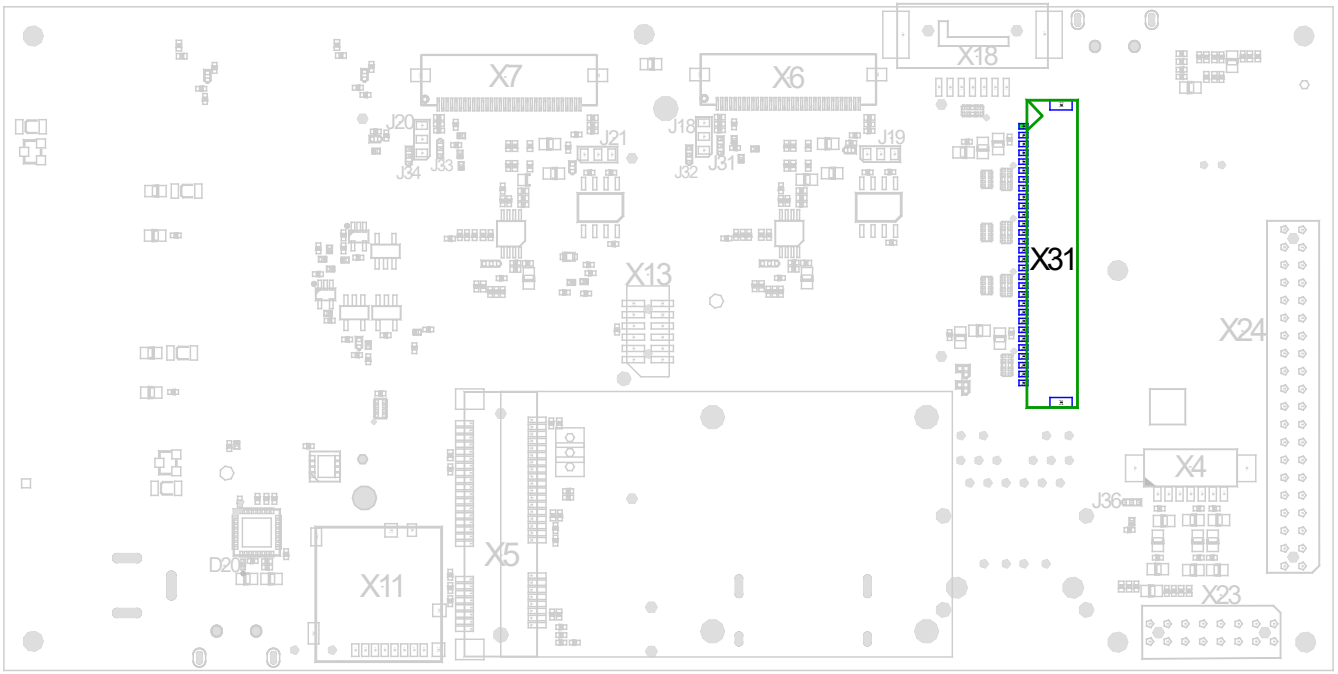


Figure 20: LVDS Display Connector X31

At present, there are a few LVDS displays on the market with some kind of standardized interface. The LVDS display connector X31 is intended to connect these displays with screen diagonals ranging from 7" to 12.1" with different resolutions.

The display connector X31 is a 30-pole receptacle with 1 mm pitch.

For more detailed information about the pin assignment and how to set up the right configuration for a custom display, refer to *section 3.2.6.1.*

2.2.10.2 Display Power Connector (X4)

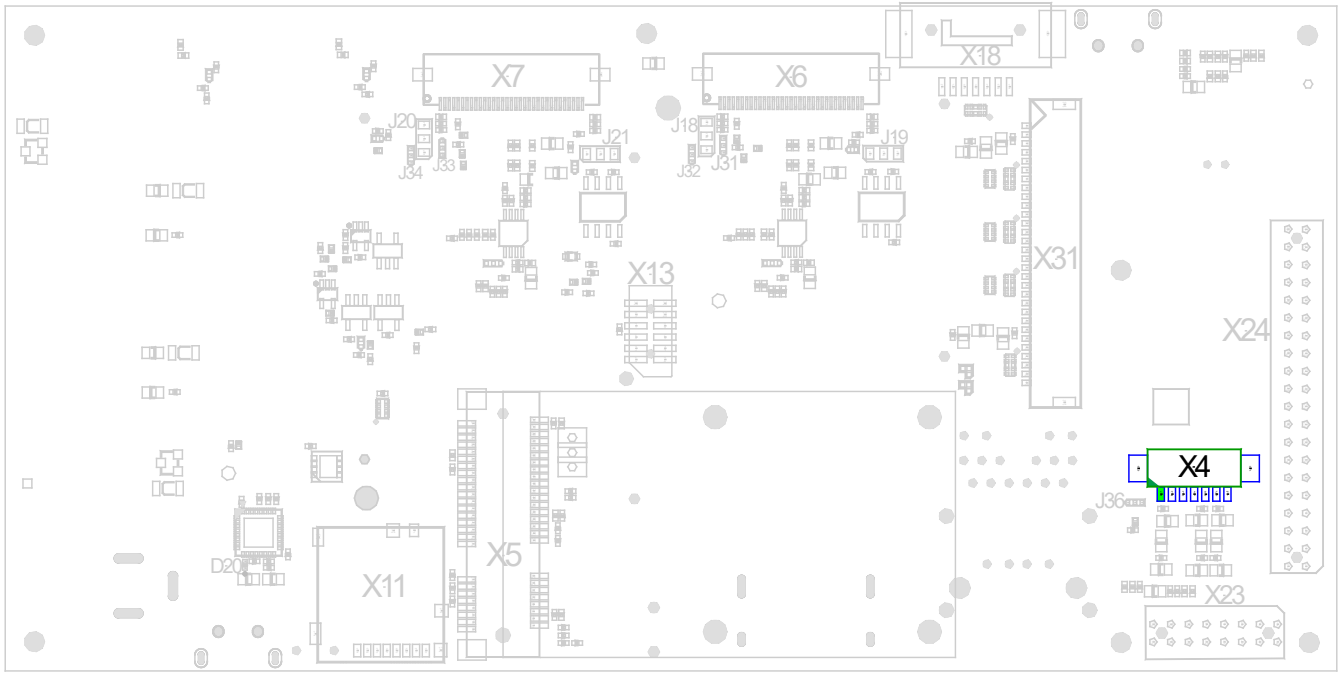


Figure 21: Backlight and Display Control Connector X4

In order to support a backlight for the LVDS display, X4 provides the supply voltages and control signals necessary.

For more detailed information about the pin assignment and how to set up the right configuration for a custom display, refer to *section 3.2.6.2.*

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2.2.11 Audio/Video connectors (X23 and X24)

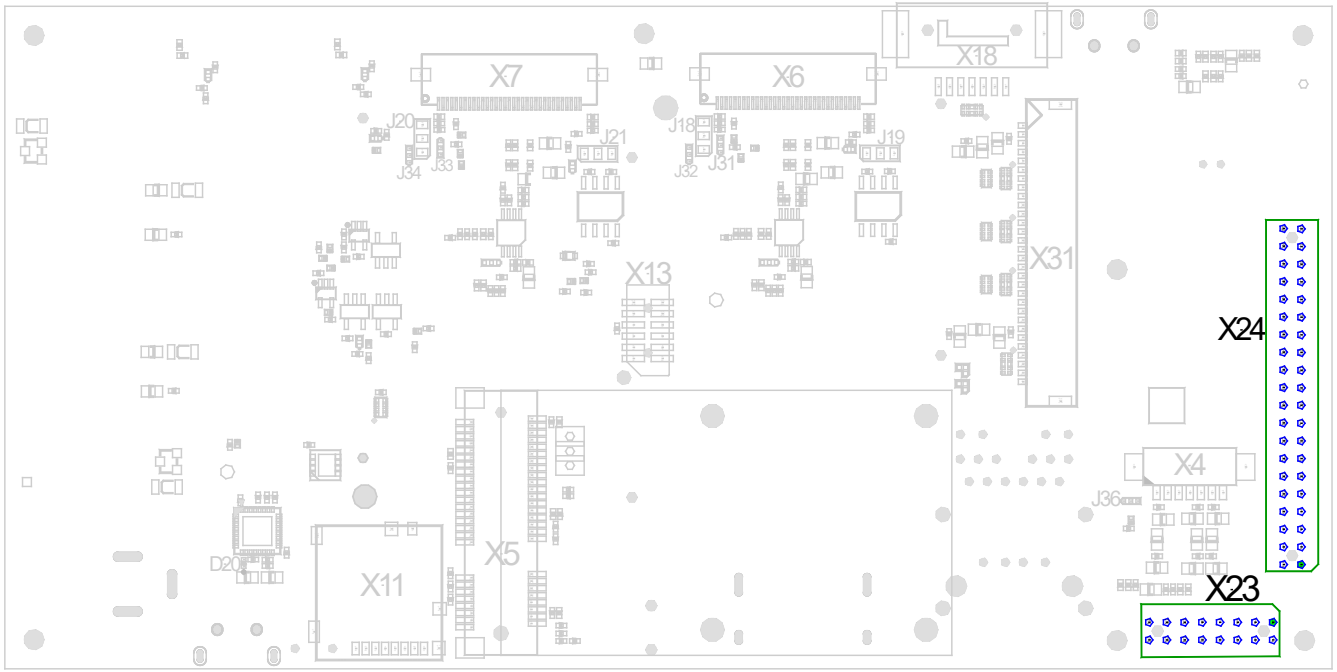


Figure 22: Audio/Visual Connectors X23, X24

The Audio/Video (A/V) connectors X23 and X24 provide an easy way to add typical A/V functions and features to the phyBOARD-Nunki i.MX 6. Standard interfaces such as parallel display, I^2S and I^2C as well as different supply voltages are available at the two A/V female dual entry connectors. One special feature of these connectors are their connectivity from the bottom or the top of the PCB.

For further information about the A/V connectors, see *chapter 3.2.7*. Information on expansion boards available for the A/V Connectors can be found in the *phyBOARD Expansion Boards Application Guide L-793*.

2.2.12 Mini PCIe (X5)

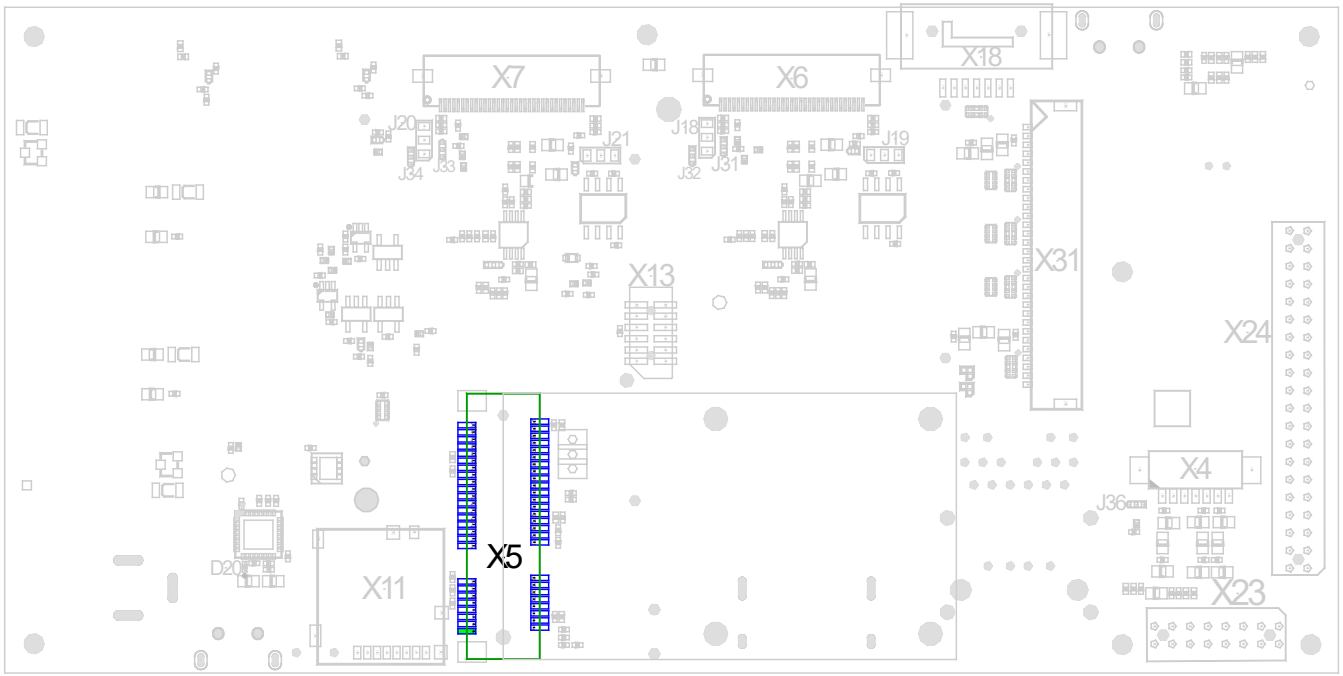


Figure 23: Mini PCIe X5

The 1-lane PCI express interface of the phyBOARD-Nunki i.MX 6 provides PCIe Gen. 2.0 functionality which supports 5 Gbit/s operations. Furthermore, the interface is fully backwards compatible with the 2.5 Gbit/s Gen. 1.1 specification. Various control signals are implemented with GPIOs. The PCIe interface is brought out at the Mini PCIe connector X5 shown in *Figure 23*. The SIM/UIM card signals of a connected PCIe module can be made available at expansion connector X17. Please refer to *section 3.2.8* for in-depth information such as pin assignment and signals used to implement special features of the Mini PCIe interface.

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2.2.13 JTAG (X13)

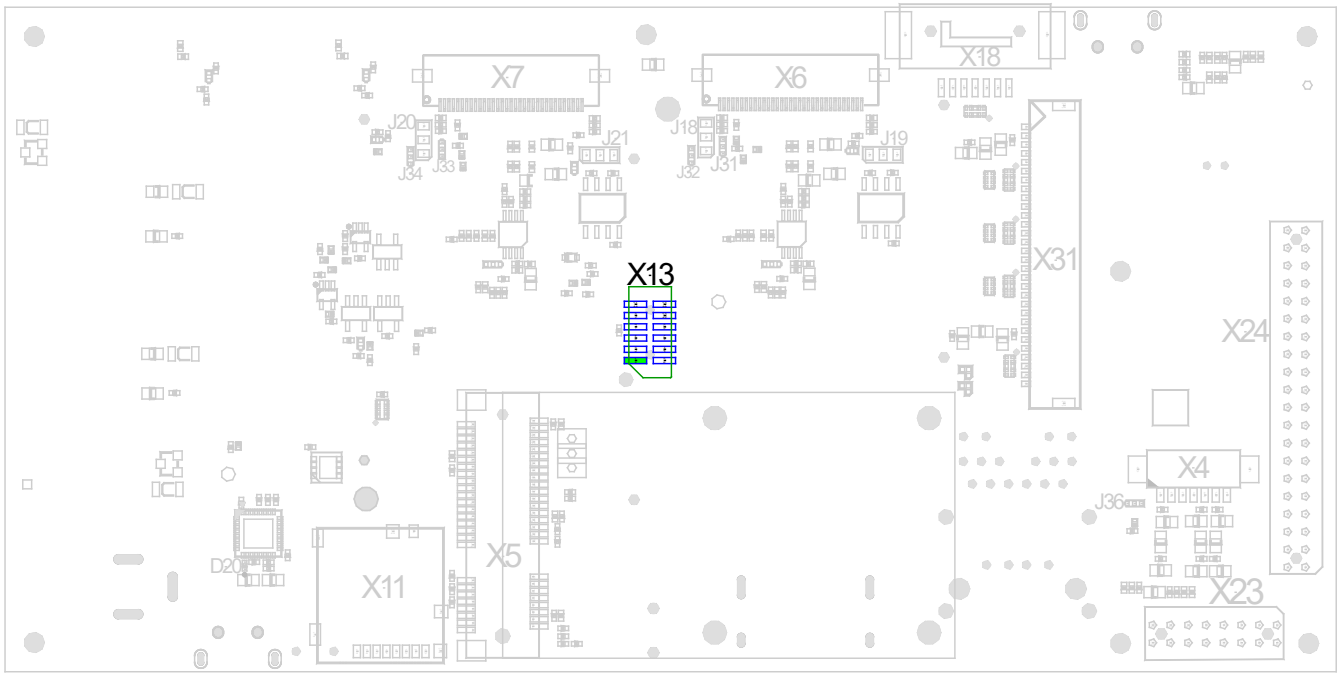


Figure 24: JTAG Interface X13

The JTAG interface of the phyCORE-i.MX 6 is accessible at connector X13 on the phyBOARD-Nunki i.MX 6. This interface is compliant with JTAG specification IEEE 1149.1 or IEEE 1149.7. No jumper settings are necessary to use the JTAG port.

For the pinout, see *chapter 3.2.9*.

2.2.14 Expansion connector (X17)

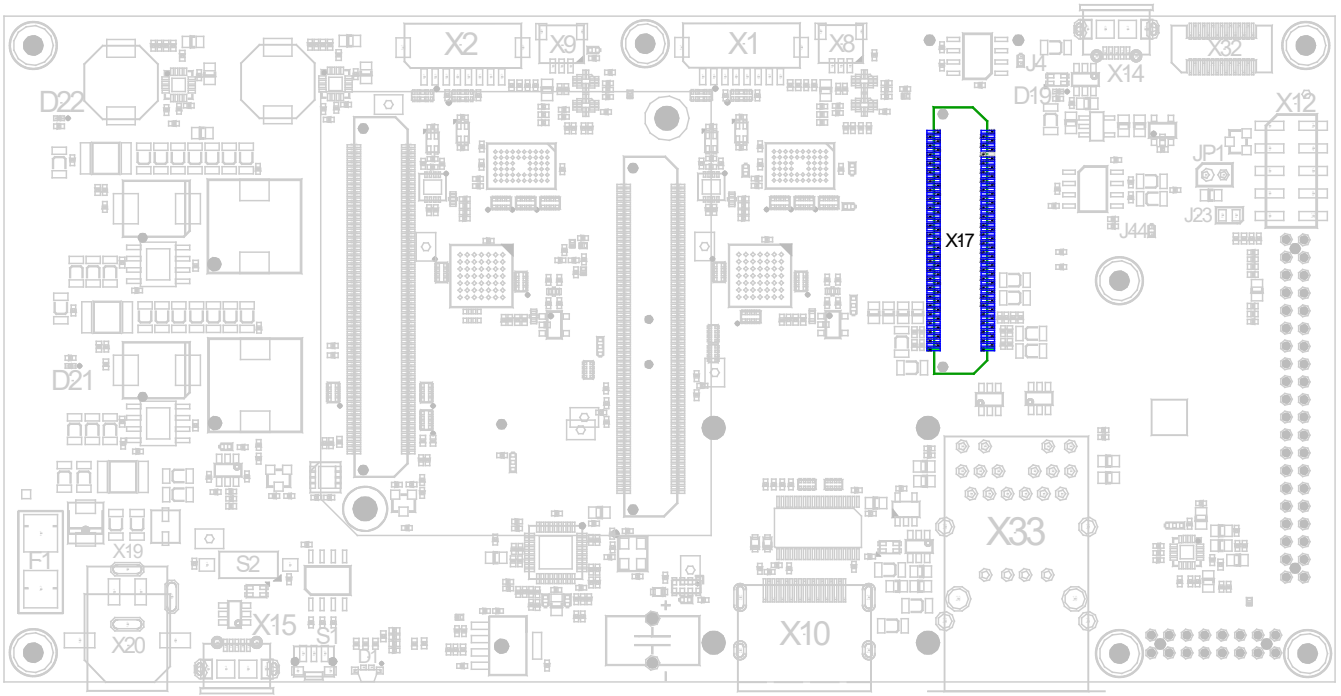


Figure 25: Expansion Connector X17

Expansion connector X16 provides an easy way to add other functions and features to the phyBOARD-Nunki i.MX 6. Standard interfaces such as USB, UART, SDIO, SPI and I^2C as well as different supply voltages and some GPIOs are available at the female expansion connector.

For further information of the expansion connector and the pinout, see *chapter 3.2.10*.

2.2.15 Multicolor (RGB) LED (D1)

The phyBOARD-Nunki i.MX 6 provides one multicolor (RGB) LED (D1) (*Figure 2*) for user applications. The colors can be controlled the LED dimmer IC at U21. The LED dimmer can be accessed via I2C1 at address 0x62 and dynamically controls the LED with PWM signals.

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2.2.16 Boot Mode (S2)

The phyBOARD-Nunki i.MX 6 has two defined boot sequences which can be selected by configuring switch S2.

Boot Mode	Description
Boot mode 0 (S2 = off)	Boot from NAND
Boot mode 1 (S2 = on)	Boot from SD/MMC 1

Table 13: Boot Mode Configuration S2

2.2.17 System Reset Button (S1)

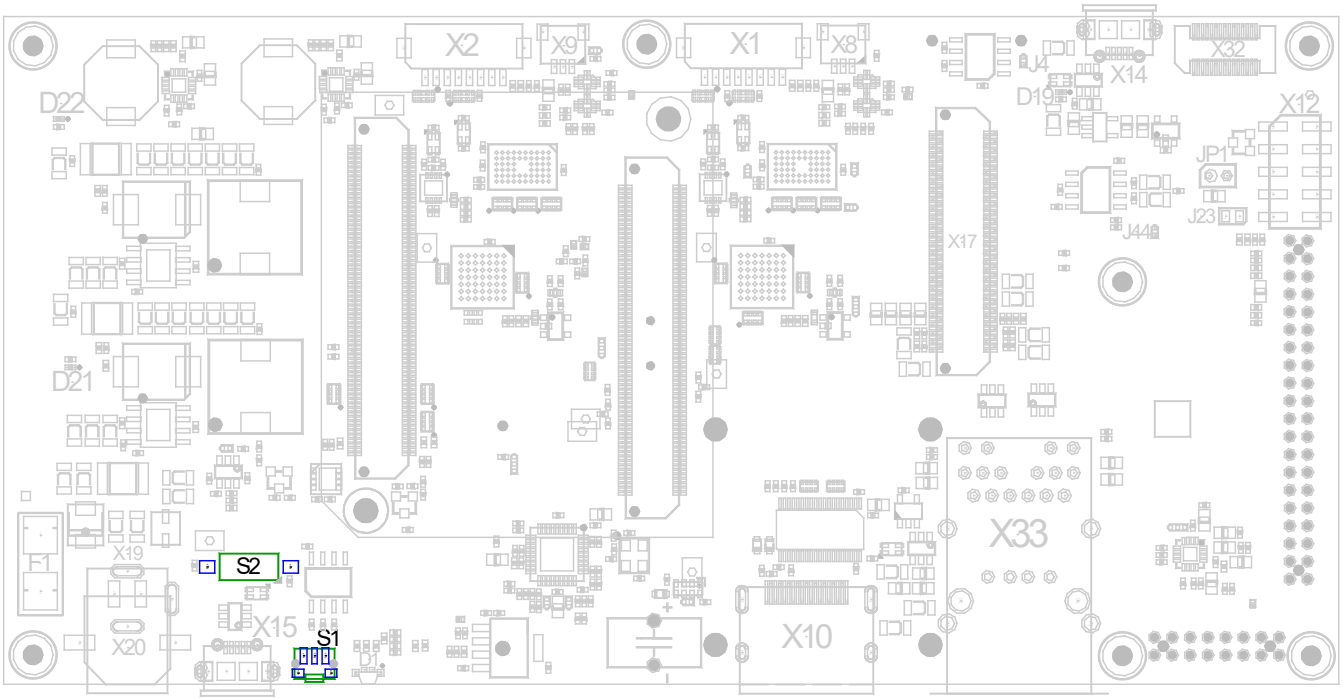


Figure 26: Boot Mode(S2) and System Reset Buttons(S1)

The phyBOARD-Nunki i.MX 6 is equipped with a system reset button at S1. Pressing this button will hold the X_nRESET pin (X3-D32) of the phyCORE SOM low, causing the module and all peripherals (power on reset) on the carrier board to be reset when the button is released.

2.2.18 RTC

The internal RTC can be used as an accurate time source (typically 20 ppm) for the applied application. As long as the phyBOARD is powered by an external power supply, the Gold-Cap capacitor will be charged. In the event of an external power failure, the Gold-Cap continues to supply the RTC with power. Gold-caps have an advantage over lithium cells in that they can be charged and discharged without additional circuitry. However, the self-discharge with the Gold-Cap capacitor (depending on the design) depends on the duration of the charging process. Typically, the Gold-Cap used on the phyBOARD can supply the RTC for > 15 days (@ 20 ° C) or > 8 days (@ 40 ° C) after a charge time of 100 hours.

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3 System Level Customizing

3.1 About this Section

This section is for advanced developers who want to design custom expansion boards or display adapters. It includes detailed information on the different interfaces and features of the phyBOARD-Nunki at a system level.

3.2 System Level Hardware Information

3.2.1 Differences in SOM Pinout

To support all features of the phyBOARD-Nunki i.MX 6, the BSP provides assigned functions different from what is described in the pinout table (*chapter 2*) of the phyCORE-i.MX 6 hardware manual to some pins of the phyCORE-i.MX 6. lists all pins with functions different from what is described in the SOM's pinout table.

Note:
- The information given in the "SIGNAL TYPE" column is from the SOM's perspective.

Pin#	Signal	Signal Type	Signal Level	Description
A25	X_EIM_DA13	I/O	3.3 V	Muxed as GPIO3_13 für X17 GPIO function
A42	X_EIM_BCLK	I	3.3 V	Muxed as nSD1_CD (µSD Card Detection)
A43	X_ECSPI2_MISO	O	3.3 V	Muxed as PCIe_nPERST for X5
A45	X_ECSPI2_SS0	I/O	3.3 V	Muxed as PCIe_COEX1 for X5
A67	X_ENET_TXER	O	3.3 V	Muxed as GPIO4_05 for X8 trigger signal
A68	X_ENET_RXD0	O	2.8 V	Muxed as GPIO1_27 for CAN enable
A69	X_ENET_RXD1	O	2.8 V	Muxed as GPIO1_26 for nEN_VCC1V5 (PCIe)
B26	X_EIM_DA14	O	3.3 V	Muxed as PCIe_nW_DISABLE for X5
B39	X_XSI1_DAT07	I/O	3.3 V	Muxed AV_INT for X23 AV connector
B40	X_XSI1_DAT06	I/O	3.3 V	Muxed PCIe_COEX2 for X5
B41	X_XSI1_DAT05	O	3.3 V	Muxed EN_SWITCH for U31
B45	X_ECSPI2_SCLK	I	3.3 V	Muxed PCIe_nCLKREQ
B46	X_ECSPI2_RDY	O	3.3 V	Muxed as GPIO5_02 for X9 trigger signal
B47	X_ECSPI2_MOSI	I	3.3 V	Muxed PCIe_nWAKE
B67	X_ENET_TXD0	I/O	2.8 V	Muxed as GPIO1_28 for X17 GPIO function

Table 14: Specifically used Pins on the phyCORE-Connector

Pin#	Signal	Signal Type	Signal Level	Description
B69	X_ENET_TXD0	O	2.8 V	Muxed as nLVDS_DISP_EN for X4
B70	X_ENET_TXD1	O	2.8 V	Muxed as nLCD_PWCTRL for X23
C16	X_SPDIF_OUT	I	3.3 V	Muxed INT_RES_TOUCH
C52	X_CSI0_DAT6	I/O	3.3 V	Muxed as GPIO5_24 for X32
C53	X_CSI0_DAT5	I/O	3.3 V	Muxed as GPIO5_23 for X32
C55	X_CSI0_DAT4	I	3.3 V	Muxed as GPIO5_22 for X9 strobe signal
D13	X_KEY_COL2	I	3.3 V	Muxed as GPIO4_10 for X8 strobe signal
D47	X_CSI0_DAT7	I/O	3.3 V	Muxed as GPIO5_25 for X32

Table 14: Specifically used Pins on the phyCORE-Connector (continued)

3.2.2 Soldering Jumpers

Numerous jumpers and resistors allow the user to configure the phyBOARD according to specific design needs.

Caution!

- Due to the small footprint of the jumpers PHYTEC does not recommend manual jumper modifications. This might also render the warranty invalid. Please contact the PHYTEC sales team if you need one of the configurations described below.

The following table lists all jumpers and resistors as well as describing their function.

Jumper / Resistor	Description	See Section
J18-J21	Jumper for phyCAM-P CTRL1 and CTRL2 see *phyCAM manual (L-748e)*	-
J31-J34	Jumper for phyCAM-S+ equalizer configuration	*3.2.4.1*
J44	TTL clock signal for X32 (MIPI CSI-2 connector)	*3.2.4.3*
J36	Voltage level for nLVDS_DISP_EN switching +3.3 V, +5 V	*3.2.6.2*
J23	Connects CAN_SHIELD with Ground	*2.2.6*
J4	Connects USB OTG ID pin with Ground	*3.2.5.1*

Table 15: Soldered Jumpers on the phyBOARD-Nunki

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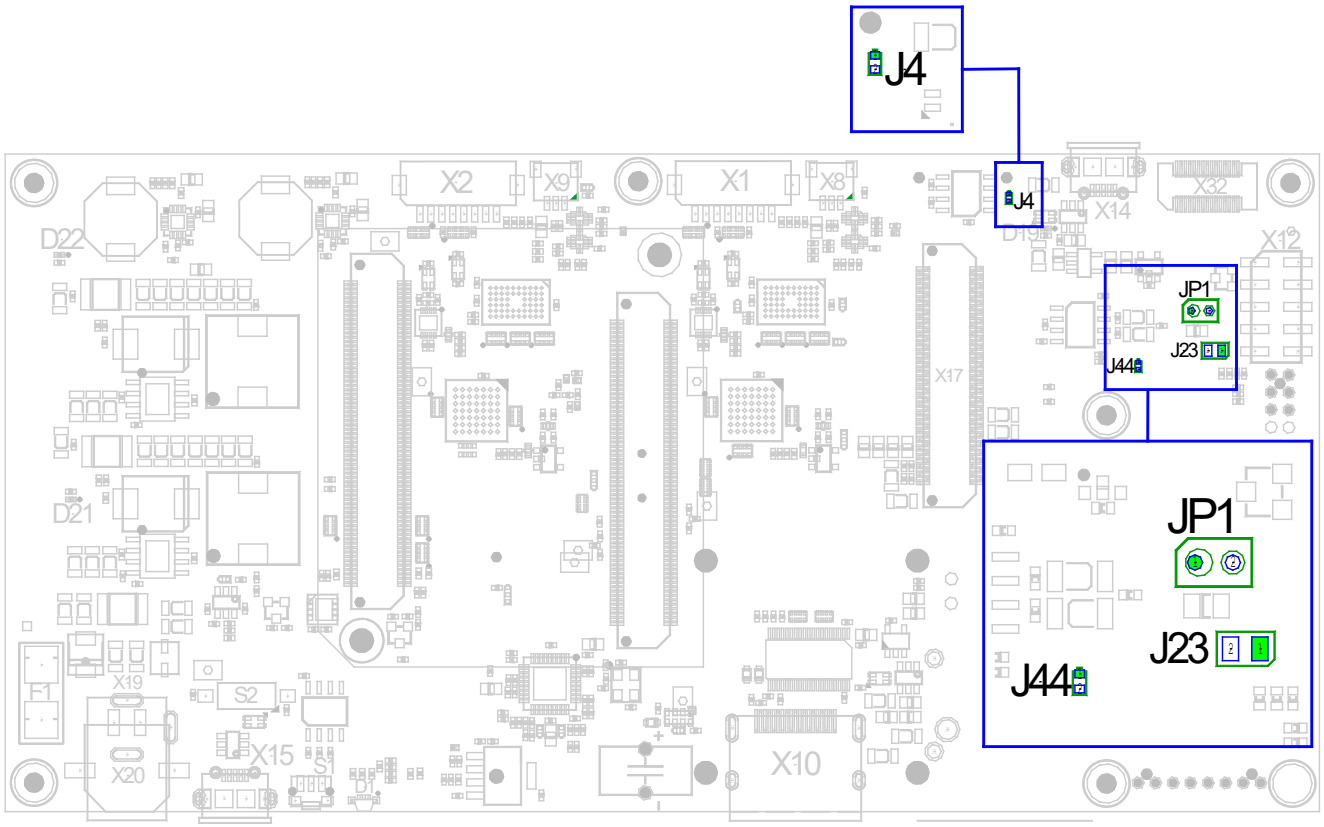


Figure 27: Jumper Positions (Top)

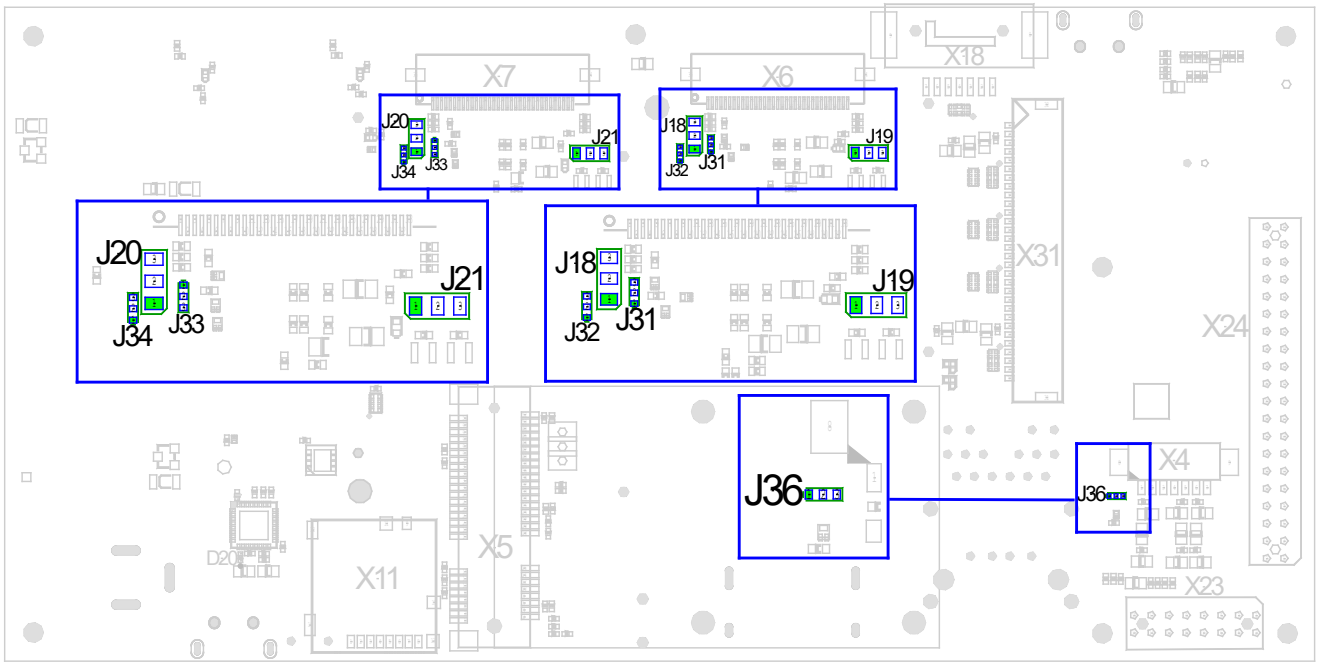


Figure 28: Jumper Positions (Bottom)

3.2.3 I²C Connectivity

The I2C1 interface of the i.MX 6 is available at different connectors on the phyBOARD-Nunki. The following table provides a list of the connectors and pins with I²C connectivity.

Connector	Location
Expansion connector X17	pin A48 (I2C1_SDA) pin A49 (I2C1_SCL)
A/V connector X23	pin 15 (I2C1_SDA) pin 16 (I2C1_SCL)
Universal Display Connector X31	pin 26 (I2C1_SDA) pin 27 (I2C1_SCL)
Mini PCIe X5	pin 32 (I2C1_SDA) pin 30 (I2C1_SCL)

Table 16: I2C1 Connectivity

To avoid any conflicts when connecting external I²C devices to the phyBOARD-Nunki, the addresses of the on-board I²C devices must be considered. *Table 17* lists the addresses already in use. Note that the table only shows the default address.

Board	Prod. No.	Device	Address used (7 MSB)
I2C3			
phyCORE-i.MX 6	PCM-058	EEPROM	0x50
		PMIC	0xB0, 0xB1
I2C1			
phyBOARD-Nunki	PBA-C-11	Touch controller	0x44
		Multi color LED	0x62
		RTC	0x68
		phyCAM	0x45, 0x48, 0x4A, 0x4C, 0x4E, 0x5A, 0x5C, 0x5D, 0x5E
Screen AV adapter	PEB-AV-02	GPIO Expander	0x41

Table 17: I²C Addresses in Use

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3.2.4 Camera Connectivity

On the phyBOARD-Nunki i.MX 6, both parallel camera interfaces (CSI0 and CSI1) can be used simultaneously. Each CSI interface is upgraded with a complete phyCAM-S+ and phyCAM-P interface. Switching between phyCAM-S+ and phyCAM-P can be done in processor runtime using GPIOs.

Control Signals				CSI Interface	
EIM_DA9 (nCAMERA0 _PWRDN)	EIM_DA8 (CAMERA1 _PWRDN)	CSI0_DATA_EN (CAMERA0_EN)	EIM_DA10 (CAMERA1_EN)	Camera0	Camera1
1	0	0	0	Off	Off
1	0	0	1	Off	Off
1	0	1	0	Off	Off
1	0	1	1	Off	Off
0	1	0	0	phyCAM-P	phyCAM-P
0	1	0	1	phyCAM-P	phyCAM-S+
0	1	1	0	phyCAM-S+	phyCAM-P
0	1	1	1	phyCAM-S+	phyCAM-S+

Table 18: phyCAM control signals

Note:

- nCAMERA0_PWRDN and CAMERA1_PWRDN are not used in the default configuration. This means setting nCAMERA0_PWRDN or CAMERA1_PWRDN in the i.MX 6 has no effect on the hardware.

Caution!

- Do not connect a phyCAM-S+ and phyCAM-P camera module to one CSI simultaneously.

3.2.4.1 phyCAM-S+ (LVDS) Camera Interfaces (X1, X2)

The table below shows the pinout of connector X1 and X2:

Pin #	Signal Name	Signal Type	Signal Level	Description
1	CAMx_DATA_IN+	LVDS_I	-	LVDS Data+
2	CAMx_DATA_IN-	LVDS_I	-	LVDS Data-
3	CAMx_CLOCK_OUT-	LVDS_O	-	LVDS Clock-
4	CAM_S_I2C_SDA	OD-BI	3.3 V	I^2C Data Signal
5	CAM_S_I2C_SCL	OD-BI	3.3 V	I^2C Clock Signal
6	CAMx_CLOCK_OUT+	LVDS_O	-	LVDS Clock+
7	VCC_CAMx_S	PWR_O	3.3 V	Power supply
8	GND	-	0 V	Ground
Pads	GND	-	0 V	Ground

Table 19: PHYTEC phyCAM-S+ Camera Connector X1 and X2

For fitted cables, see *Table 9*

phyCAM-S+ equalizer configuration
Both phyCAM-S+ interfaces have an equalizer to compensate cable-depended losses.

EQ1 (J32 / J34)	EQ0 (J31 / J33)	Equalization Level
2+3	**2+3**	Off
2+3	1+2	Low
1+2	**2+3**	Medium
1+2	1+2	High

Table 20: phyCAM-S+ equalizer configuration

3.2.4.2 phyCAM-P (Parallel) Camera Interfaces (X6, X7)

The supply voltage (VCC_CAM) and the signal voltages depend on the camera module in use. The phyCAM-P interface of the phyBOARD-Nunki i.MX 6 is designed for the greatest possible compatibility with the different phyCAM-P modules in order to use such devices without hardware customization. Further information on the control signals, e.g. CAM_CTRLx can be found in the *phyCAM manual (L-748e)*

Cable specification: 33-pole FFC/FPC, 0.5 mm pitch, 0.3 mm thick, contact position bottom. For fitted cables, see *Table 10*.

Table 21 shows the pinout of connector X6 and X7.

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Pin #	Signal Name	Signal Type	Signal Level	Description
1	VCC_CAMx_P	PWR_O	NS	Power Supply
2	CAMx_OE	O	VCC_CAMx_P	Output Enable
3	CAMx_VSET	Analog	-	Power Supply Voltage Set
4	CAMx_CTRL2	I/O	VCC_CAMx_P	Control Signal 2
5	CAMx_MCLK	O	VCC_CAMx_P	Camera Master Clock
6	GND	-	0 V	Ground
7	CAMx_PCLK	I	VCC_CAMx_P	Camera Pixel Clock
8	GND	-	0 V	Ground
9	CAMx_DD0	I	VCC_CAMx_P	Camera Data 0
10	CAMx_DD1	I	VCC_CAMx_P	Camera Data 1
11	GND	-	0 V	Ground
12	CAMx_DD2	I	VCC_CAMx_P	Camera Data 2
13	CAMx_DD3	I	VCC_CAMx_P	Camera Data 3
14	GND	-	0 V	Ground
15	CAMx_DD4	I	VCC_CAMx_P	Camera Data 4
16	CAMx_DD5	I	VCC_CAMx_P	Camera Data 5
17	GND	-	0 V	Ground
18	CAMx_DD6	I	VCC_CAMx_P	Camera Data 6
19	CAMx_DD7	I	VCC_CAMx_P	Camera Data 7
20	GND	-	0 V	Ground
21	CAMx_DD8	I	VCC_CAMx_P	Camera Data 8
22	CAMx_DD9	I	VCC_CAMx_P	Camera Data 9
23	GND	-	0 V	Ground
24	CAMx_LV	I	VCC_CAMx_P	Camera HSYNC Signal
25	CAMx_FV	I	VCC_CAMx_P	Camera VSYNC Signal
26	GND	-	0 V	Ground
27	CAMx_CTRL1	I/O	VCC_CAMx_P	Control Signal 1
28	CAMx_I2C_SCL	OD-BI	VCC_CAMx_P	I^2C Clock Signal
29	CAMx_I2C_SDA	OD-BI	VCC_CAMx_P	I^2C Data Signal
30	GND	-	0 V	Ground
31	nCAM_RST	O	VCC_CAMx_P	Reset
32	VCC_CAMx_P	PWR_O	NS	Power Supply
33	VCC_CAMx_P	PWR_O	NS	Power Supply
Pads	GND	-	0 V	Ground

Table 21: PHYTEC phyCAM-P Connector X6 and X7

3.2.4.3 MIPI/CSI-2 Camera Interface (X32)

Table 22 shows the pinout of connector X32:

Pin #	Signal Name	Signal Type	Signal Level	Description
1	VCC_MIPI3V3	PWR_O	3.3 V	Power Supply
2	GND	-	0 V	Ground
3	VCC_MIPI3V3	PWR_O	3.3 V	Power Supply
4	CSI_D3M	LVDS_I	-	Data3-
5	VCC_MIPI5V	PWR_O	5 V	Power Supply
6	CSI_D3P	LVDS_I	-	Data3+
7	VCC_MIPI5V	PWR_O	5 V	Power Supply
8	GND	-	0 V	Ground
9	GND	-	0 V	Ground
10	CSI_D1M	LVDS_I	-	Data1-
11	CCM_CLKO1	O	3.3 V	Clock (need to mount J44)
12	CSI_D1P	LVDS_I	-	Data1+
13	X_nRESET	I/O	3.3 V	Global Reset
14	GND	-	0 V	Ground
15	I2C_S_SDA	OD-BI	3.3 V	I^2C Data Signal
16	CSI_CLK0M	LVDS_I	-	Clock-
17	I2C_S_SCL	OD-BI	3.3 V	I^2C Clock Signal
18	CSI_CLK0P	LVDS_I	-	Clock+
19	GND	-	0 V	Ground
20	GND	-	0 V	Ground
21	GPIO5_23	I/O	3.3 V	GPIO
22	CSI_D0M	LVDS_I	-	Data0-
23	GPIO5_24	I/O	3.3 V	GPIO
24	CSI_D0P	LVDS_I	-	Data0+
25	GPIO5_25	I/O	3.3 V	GPIO
26	GND	-	0 V	Ground
27	GND	-	0 V	Ground
28	CSI_D2M	LVDS_I	-	Data2-
29	GND	-	0 V	Ground
30	CSI_D2P	LVDS_I	-	Data2+

Table 22: MIPI/CSI-2 Camera Connector X32

Compatible PCB-2-PCB connectors:
Molex 53748-0308

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3.2.4.4 Trigger/Strobe Connector (X8, X9)

Table 23 shows the pinout of connector X8 and X9:

Pin #	Signal Name	Signal Type	Signal Level	Description
1	CAMx_TRIGGER	O	VCC_CAMx_P/S	Trigger Output
2	GND	-	0 V	Ground
3	CAMx_STROBE	I	VCC_CAMx_P/S	Strobe Input

Table 23: PHYTEC Trigger/Strobe Connector X8 and X9

3.2.5 USB-OTG Connectivity

3.2.5.1 Configuring the OTG Operating Mode (J4)

Jumper J4 configures the OTG operating mode with the X_USB_OTG_ID signal. By default, this resistor is not mounted, which leaves the ID pin floating. This configures the OTG interface as device, or according to the configuration of the connected USB device. Mounting a 10 kΩ resistor connects the OTG1_ID pin to GND, forcing the OTG interface into host mode.

3.2.6 Universal Display Interface

3.2.6.1 LVDS Display Connector (X31)

Table 24 shows the pinout of connector X31.

Pin #	Signal Name	Signal Type	Signal Level	Description
1	3V3_UDI1	PWR_O	3.3 V	Display Power Supply
2	3V3_UDI1	PWR_O	3.3 V	Display Power Supply
3	GND	-	0 V	Ground
4	GND	-	0 V	Ground
5	LVDS0_TX0-	LVDS_O		LVDS Data0-
6	LVDS0_TX0+	LVDS_O		LVDS Data0+
7	GND	-	0 V	Ground
8	LVDS0_TX1-	LVDS_O		LVDS Data1-
9	LVDS0_TX1+	LVDS_O		LVDS Data1+
10	GND	-	0 V	Ground
11	LVDS0_TX2-	LVDS_O		LVDS Data2-
12	LVDS0_TX2+	LVDS_O		LVDS Data2+

Table 24: Universal Display Interface Connector X31

Pin #	Signal Name	Signal Type	Signal Level	Description	
13	GND	-	0 V	Ground	
14	LVDS0_TX3-	LVDS_O		LVDS Data3-	
15	LVDS0_TX3+	LVDS_O		LVDS Data3+	
16	GND	-	0 V	Ground	
17	LVDS0_CLK-	LVDS_O		LVDS Clock-	
18	LVDS0_CLK+	LVDS_O		LVDS Clock-	
19	GND	-	0 V	Ground	
20	USB_HUB_DM4	USB_I/O		USB HUB Port 4 D-	
21	USB_HUB_DP4	USB_I/O		USB HUB Port 4 D+	
22	GND	-	0 V	Ground	
23	5V_UDI1	PWR_O	5 V	Display Power Supply	
24	5V_UDI1	PWR_O	5 V	Display Power Supply	
25	GND	-	0 V	Ground	
26	I2C1_SDA	OD-BI	3.3 V	I²C1 Data	
27	I2C1_CLK	OB-BI	3.3 V	I²C1 Clock	
28	GND	-	0 V	Ground	
29	UART3_RX_DATA	I	3.3 V	UART3 In	J50 (2+3)
		O	3.3 V	CTRL0 (10k PU)	J50 (1+2)
30	UART3_TX_DATA	UART3_TX_DATA	O	3.3 V	UART3 Out
			O	3.3 V	CTRL1 (10k PU)
Pads	GND	-	0 V	Ground	

Table 24: Universal Display Interface Connector X31 (continued)

Compatible connector housings:
Hirose DF19-30S-1C

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3.2.6.2 Display Power Connector (X4)

Table 25 shows the pinout of connector X4.

Pin #	Signal Name	Signal Type	Signal Level	Description	
1	+24V_IN_FILTER	PWR_O	NS[3]	Backlight Power Supply	
2	GND	-	0 V	Ground	
3	PWM1	O	3.3 V	Pulse width modulation	
4	nLVDS_DISP_EN	O	3.3 V	Display Enable (10k PU)	**J36 (2+3)**
			5 V	Display Enable (10k PU)	J36 (1+2)
5	5V_UDI2	PWR_O	5 V	Display Power Supply	
6	3V3_UDI2	PWR_O	3.3 V	Display Power Supply	
7	GND	-	0 V	Ground	
Pads	GND	-	0 V	Ground	

Table 25: Universal Display Interface Connector X4

Compatible connector housings:
Molex 51021-0700

3: +24V_FILTER is the external supply voltage from X19 or X20 secured against transients (26.4 V). Because of this, the voltage level depends on the connected power supply and is not specified here.

3.2.7 Audio/Video connectors (X23 and X24)

Audio/Video (A/V) connectors X23 and X24 provide an easy way to add typical A/V functions and features to the phyBOARD-Nunki i.MX 6. Standard interfaces such as parallel display, I^2S and I^2C as well as different supply voltages are available at the two A/V female dual entry connectors. One special feature of these connectors is their connectivity from the bottom or the top. The pinout of the A/V connectors is shown in *Table 26* and *Table 27*.

The A/V connector is intended for use with phyBOARD Expansion Boards[4], and to add specific audio/video connectivity with custom expansion boards.

A/V connector X24 makes all signals for display connectivity available, while X23 provides signals for audio and touch screen connectivity, as well as an I^2C bus and additional control signals.

Pin #	Signal Name	Signal Type	Signal Level	Description
1	LCD_DATA16	O	3.3 V	LCD Data16
2	GND	-	0 V	Ground
3	LCD_DATA18	O	3.3 V	LCD Data16
4	LCD_DATA17	O	3.3 V	LCD Data17
5	GND	-	0 V	Ground
6	LCD_DATA19	O	3.3 V	LCD Data19
7	LCD_DATA21	O	3.3 V	LCD Data21
8	LCD_DATA20	O	3.3 V	LCD Data20
9	LCD_DATA23	O	3.3 V	LCD Data23
10	LCD_DATA22	O	3.3 V	LCD Data22
11	LCD_DATA08	O	3.3 V	LCD Data22
12	GND	-	0 V	Ground
13	LCD_DATA10	O	3.3 V	LCD Data10
14	LCD_DATA09	O	3.3 V	LCD Data09
15	GND	-	0 V	Ground
16	LCD_DATA11	O	3.3 V	LCD Data11
17	LCD_DATA13	O	3.3 V	LCD Data13
18	LCD_DATA12	O	3.3 V	LCD Data12
19	LCD_DATA15	O	3.3 V	LCD Data15
20	LCD_DATA14	O	3.3 V	LCD Data14

Table 26: PHYTEC A/V Connector X24

4: Please find additional information on phyBOARD Expansion Boards in *phyBOARD Expansion Boards Application Guide L-793*.

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Pin #	Signal Name	Signal Type	Signal Level	Description
21	LCD_DATA00	O	3.3 V	LCD Data09
22	GND	-	0 V	Ground
23	LCD_DATA02	O	3.3 V	LCD Data09
24	LCD_DATA01	O	3.3 V	LCD Data09
25	GND	-	0 V	Ground
26	LCD_DATA03	O	3.3 V	LCD Data09
27	LCD_DATA05	O	3.3 V	LCD Data09
28	LCD_DATA04	O	3.3 V	LCD Data09
29	LCD_DATA07	O	3.3 V	LCD Data09
30	LCD_DATA06	O	3.3 V	LCD Data09
31	LCD_CLK	O	3.3 V	LCD Clock
32	GND	-	0 V	Ground
33	LCD_HSYNC	O	3.3 V	LCD Horizontal Sync
34	LCD_ENABLE	O	3.3 V	LCD Output Enable
35	GND	-	0 V	Ground
36	LCD_VSYNC	O	3.3 V	LCD Vertical Sync
37	PWM1	O	3.3 V	Pulse width modulation
38	GND	-	0 V	Ground
39	+5V	PWR_O	5 V	Display Power Supply
40	+24V_FILTER	PWR_O	NS[5]	Backlight power supply

Table 26: PHYTEC A/V Connector X24 (continued)

Caution!

- To avoid accidental change of the boot configuration, please consider that the LCD data signals shown in *Table 26* are boot configuration pins which must not be driven by any device on the baseboard during reset. Please refer to 6.2 "Boot Drive Selection and Configuration" in the *phyCORE-i.MX 6 hardware manual or to the i.MX 6 Reference Manual* for more information about the boot configuration.

Pin #	Signal Name	Signal Type	Signal Level	Description
1	X_AUD5_TXFS	O	3.3 V	AUD5 transmit frame sync
2	X_AUD5_TXC	O	3.3 V	AUD5 transmit bit clock
3	X_AUD5_TXD	O	3.3 V	AUD5 transmit data
4	X_AUD5_RXD	I	3.3 V	AUD5 receive data

Table 27: PHYTEC A/V connector X23

5: +24V_FILTER is the external supply voltage from X19 or X20 secured against transients (26.4 V). Because of this, the voltage level depends on the connected power supply and is not specified here.

Pin #	Signal Name	Signal Type	Signal Level	Description	
5	LCD_PWCTRL	O	3.3 V	LCD power control	
6	AV_INT	I/O	3.3 V	A/V interrupt	
7	X_nRESET	I/O	3.3 V	Global Reset	(J15 1+2)
	X_LCD_RESET	O	3.3 V	Reset LCD	(J15 2+3)
8	GND	-	0 V	Ground	
9	TS_X-	Analog	1.8 V	Touch X-	
10	TS_X+	Analog	1.8 V	Touch X+	
11	TS_Y-	Analog	1.8 V	Touch Y-	
12	TS_Y+	Analog	1.8 V	Touch Y+	
13	GND	-	0 V	Ground	
14	+3V3	PWR_O	3.3 V	Display Power Supply	
15	I2C1_SDA	OD-BI	3.3 V	I2C1 data	
16	I2C1_SCL	OD-Bi	3.3 V	I2C1 clock	

Table 27: PHYTEC A/V connector X23 (continued)

Jumper J15 connects either signal X_LCD_RESET or signal X_nRESET_OUT to pin 7 of X15. *Table 28* shows the available configurations.

J15	Description
1+2	X_nRESET
2+3	**X_LCD_RESET**

Table 28: A/V Jumper Configuration J15

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3.2.8 Mini PCIe (X5)

Table 29 shows a complete overview of the Mini PCI Express connector pin assignment.

Pin #	Signal name	Signal Type	Signal Level	Description
1	X_ECSPI2_MOSI/PCIe_nWAKE	I	3.3 V	PCIe nWAKE
2	+3V3	PWR_O	3.3 V	3.3 V power supply
3	X_ECSPI2_SS0/PCIe_COEX1	I/O	3.3 V	Coexistence pins for wireless solutions
4	GND	-	0 V	Ground
5	X_CSI1_DATA06/PCIe_COEX2	I/O	3.3 V	Coexistence pins for wireless solutions
6	+1V5	PWR_O	1.5 V	1.5 V power supply[6]
7	X_ECSPI2_SCLK/PCIe_nCLKREQ	I	3.3 V	Clock request support
8	X_SIM_VCC	PWR_I	-	UIM_PWR[7]
9	GND	-	0 V	Ground
10	X_SIM_IO	I/O	-	UIM_DATA[7]
11	X_PCIe0_CLK-	LVDS_O	-	PCIe0 reference clock -
12	X_SIM_CLK	O	-	UIM_CLK[7]
13	X_PCIe0_CLK+	LVDS_O	-	PCIe0 reference clock +
14	X_SIM_RST	O	-	UIM_RESET[7]
15	GND	-	0 V	Ground
16	X_SIM_VPP	PWR_I	-	UIM_VPP[7]
17	RSVD3	-	-	Not connected
18	GND	-	0 V	Ground
19	RSVD4	-	-	Not connected
20	X_EIM_DA14/PCIe_nW_DISABLE	O	3.3 V	nWireless disable signal
21	GND	-	-	Ground
22	X_ECSPI2_MISO/PCIe_nPERST or X_nRESET (J13 1+2)	O	3.3 V	Functional card reset by GPIO or X_nRESET
23	X_PCIe_RXN	LVDS_I	-	PCIe receive -

Table 29: Mini PCI Express Connector X5

6 : The 1.5 V voltage can be switched OFF with signal ENET_TX_EN.
7 : User Identity Module (UIM) signals.

Pin #	Signal name	Signal Type	Signal Level	Description
24	+3V3	PWR_O	3.3 V	3.3 V power supply
25	X_PCIe_RXP	LVDS_I	-	PCIe receive +
26	GND	-	0 V	Ground
31	X_PCIe_TXN	LVDS_O	-	PCIe transmit -
32	X_I2C1_SDA	OD-BI	3.3 V	I2C1 data
33	X_PCIe_TXP	LVDS_O	-	PCIe transmit +
34	GND	-	0 V	Ground
35	GND	-	0 V	Ground
36	USB_HUB_DM3	USB_I/O	-	USB host data -[8,9]
37	GND	-	0 V	Ground
38	USB_HUB_DP3	USB_I/O	-	USB host data +[9]
39	+3V3	PWR_O	3.3 V	3.3 V power supply
40	GND	-	0 V	Ground
41	+3V3	PWR_O	3.3 V	3.3 V power supply
42	TP2	O	NS	Test point for nLED_WWAN
43	GND	-	0 V	Ground
44	TP3	O	NS	Test point for nLED_WLAN
45	RSVD9	-	-	Not connected
46	TP4	O	NS	Test point for nLED_WPAN
47	RSVD10	-	-	Not connected
48	+1V5	PWR_O	1.5 V	1.5 V power supply[6]
49	RSVD11	-	-	Not connected
50	GND	-	0 V	Ground
51	RSVD12	-	-	Not connected
52	+3V3	PWR_O	3.3 V	3.3 V power supply
Pads	GND	-	0 V	Ground

Table 29: Mini PCI Express Connector X5 (continued)

8 : J9 and J10 need to be set to 2+3 to route the USB2 host interface to the Mini PCI Express connector (section 2.2.11)
9 : Caution! There is no protective circuit for the USB interfaces brought out at the Mini PCI Express controller (X5).

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3.2.9 JTAG (X13)

The phyCORE-i.MX 6 is equipped with a JTAG interface for downloading program code into the external flash, internal controller RAM or for debugging programs currently executing. The JTAG interface is accessible at connector X13 (2×6 pin header, 1.27 mm pitch).

Table 30 shows the location of the JTAG pins on Connector X13.

Pin #	Signal	Signal Type	Signal Level	Description
1	+3V3_CORE	PWR_O	3.3 V	phyCORE Power Supply
2	X_JTAG_TMS	I	3.3 V	JTAG TMS
3	GND	-	0 V	Ground
4	X_JTAG_TCK	I	3.3 V	JTAG clock input
5	GND	-	0 V	Ground
6	X_JTAG_TDO	O	3.3 V	JTAG TDO
7	JTAG_RTCK	O	3.3 V	Do Not Use
8	X_JTAG_TDI	I	3.3 V	JTAG TDI
9	GND	-	0 V	Ground
10	X_nRESET	I	3.3 V	Global Reset
11	+3V3_CORE	PWR_O	3.3 V	phyCORE Power Supply
12	X_JTAG_TRSTB	I	3.3 V	JTAG reset input (low active)

Table 30: JTAG Interface Signal at X13

3.2.10 Expansion Connector (X17)

Expansion connector X17 provides an easy way to add other functions and features to the phyBOARD-Nunki. Standard interfaces such as USB, UART, SDIO, SPI and I^2C as well as different supply voltages and some GPIOs are available at the expansion female connector.

The expansion connector is intended to add specific functions with custom expansion boards.

Some signals can be multiplexed to perform different functions. Refer to the phyCORE hardware manual and the chip vendor documentation(NXP iMX6) for multiplexing information.

Table 31 and *Table 32* shows the pinout of the expansion connector.

Pin #	Signal Name	Signal Type	Signal Level	Description
A1	+3V3	PWR_O	3.3 V	Peripherals supply voltage
A2	+3V3	PWR_O	3.3 V	Peripherals supply voltage
A3	GND	-	0 V	Ground
A4	GND	-	0 V	Ground
A5	+3V3	PWR_O	3.3 V	Peripherals supply voltage
A6	+3V3	PWR_O	3.3 V	Peripherals supply voltage
A7	+3V3_CORE	PWR_O	3.3 V	phyCORE supply voltage
A8	+3V3_CORE	PWR_O	3.3 V	phyCORE supply voltage
A9	GND	-	0 V	Ground
A10	GND	-	0 V	Ground
A11	VCC_RESERVED	PWR_O	-	Reserved
A12	VCC_RESERVED	PWR_O	-	Reserved
A13	GND	-	0 V	Ground
A14	GND	-	0 V	Ground
A15	PWRGOOD_3V3	O	3.3 V	phyCORE power-good signal
A16	+3V3_LOGIC	REF_O	3.3 V	phyCORE IO reference voltage
A17	X_nRESET	I/O	3.3 V	Global reset signal
A18	GND	-	0 V	Ground
A19	USB_HUB_PRTPW2	I	3.3 V	Control signal current limiting IO switch on
A20	USB_HUB_nOSC2	O	3.3 V	Control signal Overcurrentdetection
A21	GND	-	0 V	Ground
A22	USB_HUB_DM2	USB_I/O	-	USB HUB Port 2 D-
A23	USB_HUB_DP2	USB_I/O	-	USB HUB Prot 2 D+
A24	GND	-	0 V	Ground
A25	X_SD3_CMD	I/O	3.3 V	SDIO3 Command
A26	GND	-	0 V	Ground
A27	X_SD3_CLK	I/O	3.3 V	SDIO3 Clock
A28	GND	-	0 V	Ground
A29	X_SD3_DATA0	I/O	3.3 V	SDIO3 Data0
A30	X_SD3_DATA1	I/O	3.3 V	SDIO3 Data1
A31	GND	-	0 V	Ground
A32	X_SD3_DATA2	I/O	3.3 V	SDIO3 Data2

Table 31: PHYTEC Expansion Connector X17 Row A

Pin #	Signal Name	Signal Type	Signal Level	Description
A33	X_SD3_DATA3	I/O	3.3 V	SDIO3 Data3
A34	GND	-	0 V	Ground
A35	X_SD3_DATA4	I/O	3.3 V	SDIO3 Data4
A36	X_SD3_DATA5	I/O	3.3 V	SDIO3 Data5
A37	GND	-	0 V	Ground
A38	X_SD3_DATA6	I/O	3.3 V	SDIO3 Data6
A39	X_SD3_DATA7	I/O	3.3 V	SDIO3 Data7
A40	GND	-	0 V	Ground
A41	X_UART3_RTS_B	I/O	3.3 V	UART3 Ready to Send
A42	X_UART3_CTS_B	I/O	3.3 V	UART3 Clear to Send
A43	GND	-	0 V	Ground
A44	X_UART3_TX_DATA	O	3.3 V	UART3 Tx Data
A45	GND	-	0 V	Ground
A46	X_UART3_RX_DATA	I	3.3 V	UART3 Rx Data
A47	GND	-	0 V	Ground
A48	I2C1_SDA	OD-BI	3.3 V	I²C1 SDA
A49	I2C1_SCL	OD-BI	3.3 V	I²C1 SCL
A50	GND	-	0 V	Ground

Table 31: PHYTEC Expansion Connector X17 Row A (continued)

Pin #	Signal Name	Signal Type	Signal Level	Description
B1	+5V	PWR_O	5 V	Peripherals supply voltage
B2	+5V	PWR_O	5 V	Peripherals supply voltage
B3	GND	-	0 V	Ground
B4	GND	-	0 V	Ground
B5	+5V	PWR_O	5 V	Peripherals supply voltage
B6	+5V	PWR_O	5 V	Peripherals supply voltage
B7	+24V_IN_FILTER	PWR_O	NS	External supply voltage
B8	+24V_IN_FILTER	PWR_O	NS	External supply voltage
B9	GND	-	0 V	Ground
B10	GND	-	0 V	Ground

Table 32: PHYTEC Expansion Connector X17 Row B

Pin #	Signal Name	Signal Type	Signal Level	Description
B11	X_PWR1_OUT	O	3.3 V	PWM signal
B12	GND	-	0 V	Ground
B13	X_SIM_VCC	PWR_I	-	Mini PCIe SIM VCC (X5)
B14	X_SIM_VPP	PWR_I	-	Mini PCIe SIM VPP (X5)
B15	GND	-	0 V	Ground
B16	X_SIM_RST	I	-	Mini PCIe SIM RST (X5)
B17	X_SIM_IO	I/O	-	Mini PCIe SIM IO (X5)
B18	GND	-	0 V	Ground
B19	X_SIM_CLK	I	-	Mini PCIe SIM CLK (X5)
B20	GND	-	0 V	Ground
B21	GPIO1_30	I/O	2.8 V	GPIO
B22	GND	-	0 V	Ground
B23	GPIO1_29	I/O	2.8 V	GPIO
B24	GPIO1_28	I/O	2.8 V	GPIO
B25	GND	-	0 V	Ground
B26	GPIO1_27	I/O	2.8 V	GPIO
B27	GPIO1_26	I/O	2.8 V	GPIO
B28	GND	-	0 V	Ground
B29	GPIO4_9	I/O	3.3 V	GPIO
B30	GND	-	0 V	Ground
B31	GPIO4_6	I/O	3.3 V	GPIO
B32	GND	-	0 V	Ground
B33	GPIO4_7	I/O	3.3 V	GPIO
B34	GND	-	0 V	Ground
B35	GPIO4_8	I/O	3.3 V	GPIO
B36	GND	-	0 V	Ground
B37	GND	-	0 V	Ground
B38	X_ECSPI2_SS1	O	3.3 V	SPI2 Chip Select1
B29	X_ECSPI2_SS0	O	3.3 V	SPI2 Chip Select0
B40	X_ECSPI2_SCLK	O	3.3 V	SPI2 Clock
B41	GND	-	0 V	Ground
B42	X_ECSPI2_MOSI	O	3.3 V	SPI2 MOSI
B43	X_ECSPI2_MISO	I	3.3 V	SPI2 MISO

Table 32: PHYTEC Expansion Connector X17 Row B (continued)

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Pin #	Signal Name	Signal Type	Signal Level	Description
B44	GND	-	0 V	Ground
B45	X_ECSPI1_SS0	I/O	3.3 V	SPI1 Chip Select0
B46	X_ECSPI1_SCLK	O	3.3 V	SPI1 Clock
B47	GND	PWR	0 V	Ground
B48	X_ECSPI1_MOSI	O	3.3 V	SPI1 MOSI
B49	X_ECSPI1_MISO	I	3.3 V	SPI1 MISO
B50	GND	-	0 V	Ground

Table 32: PHYTEC Expansion Connector X17 Row B (continued)

Compatible PCB-2-PCB connectors:
Samtec BSH-050-01-L-D-A-TR

4 Revision History

Date	Version #	Changes in this manual
09.05.2018	Manual L-852e_1	First edition. Describes the phyCORE-i.MX 6 SOM (PCB 1429.5) with phyBOARD-Nunki-Carrier Board (PCB 1489.0)

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