ARM®-based 32-bit Cortex®-M4F MCU with 256 to 4032 KB Flash, sLib, 2 QSPI, SDRAM, DVP, 18 timers, 3 ADCs, 23 communication interfaces (2 OTGFS and Ethernet)

Features

- **Core: ARM® 32-bit Cortex®-M4F CPU with FPU**
  - 288 MHz maximum frequency, with a memory protection unit (MPU), single-cycle multiplication and hardware division
  - Floating point unit (FPU)
  - DSP instructions
- **Memories**
  - 256 to 4032 Kbytes of internal Flash memory
  - sLib: configurable part of main Flash set as a library area with code executable but secured, non-readable
  - Default 384 Kbytes of SRAM, configurable up to maximum 512 Kbytes
  - External memory controller (XMC) with 16-bit data bus. Supports CF card, SRAM, PSRAM, NOR, NAND, and SDRAM memories
  - Up to 2 x QSPI interfaces for external SPI Flash or SPI RAM extension, and memory mapping mode
- **XMC as LCD parallel interface, compatible with 8080/6800 modes**
- **Power control (PWC)**
  - 2.6 V ~ 3.6 V power supply
  - Power on reset (POR), low voltage reset (LVR), and power voltage monitoring (PVM)
  - Low power: Sleep, Deepsleep, and Standby modes
  - V_{BAT} supply for LEXT, ERTC and 20 x 32-bit battery powered registers (BPR)
- **Clock and reset management (CRM)**
  - 4 to 25 MHz crystal oscillator (HEXT)
  - 48 MHz internal factory-trimmed clock (HICK), accuracy ±1 % at T_A = 25 °C and ±2.5 % at T_A = -40 to +105 °C, with automatic clock calibration (ACC)
  - PLL flexible multiplication and division factor
  - 32 kHz crystal (LEXT)
  - Low speed internal clock (LICK)
- **Analog**
  - 3 x 12-bit 5.33 MSPS A/D converters, up to 24 input channels, 12/10/8/6-bit configurable resolution, hardware over-sampling up to equivalent 16-bit resolution
  - Temperature sensor (V_{TS}), internal reference voltage (V_{INTRV}), V_{BAT} battery voltage monitor (V_{BAT}/4)
  - 2 x 12-bit D/A converters
- **DMA**
  - 2 x general-purpose DMAs and 1 x EDMA
  - 22 channels in all
- **Up to 116 fast GPIO interfaces**
  - All mappable to 16 external interrupts (EXINT)
  - Almost 5V-tolerant
- **Up to 18 timers (TMR)**
  - Up to 3 x 16-bit 7-channel advanced timer, including three pairs of complementary channels for PWM output, with dead-time generator and emergency brake
  - Up to 8 x 16-bit + 2 x 32-bit timers, each with 4 IC/OC/PWM or pulse counter
  - 2 x watchdog timers (general WDT and windowed WWDT)
  - SysTick timer: a 24-bit downcounter
- **ERTC: enhanced RTC with auto-wakeup, alarm, subsecond precision, hardware calendar and calibration feature**
- **Up to 23 communication interfaces**
  - Up to 3 x I^2C interfaces (SMBus/PMBus)
  - Up to 4 x USARTs/4 x UARTs (ISO7816, LIN, IrDA capability, modern control and RS485 drive enable), support TX/RX swap
  - Up to 4 x SPIs (50 Mbit/s), all with I^2S interface multiplexed, I^2S2/I^2S3 support full-duplex
  - Up to 2 x CAN interfaces (2.0B Active)
  - Up to 2 x OTG FS controller, supporting crystal-less in device mode
  - Up to 2 x SDIO interfaces
  - Infrared transmitter (IRTMR)
  - 10/100M Ethernet MAC (EMAC), with dedicated DMA and 4 KB of buffer, IEEE 1588 hardware support, MII/RMII available (for AT32F437 only)
- **8~14-bit digital video parallel (DVP) interface**
- **CRC calculation unit**
- **96-bit unique ID (UID)**
- **Debug mode**
  - Serial wire debug (SWD) and JTAG interfaces
- **Operating temperatures: -40 to +105 °C**

- **Packages**
  - LQFP144 20 x 20 mm
  - LQFP100 14 x 14 mm
  - BGA100 7 x 7 mm
  - LQFP64 10 x 10 mm
  - LQFP48 7 x 7 mm
  - QFN48 6 x 6 mm

Table 1. AT32F435 device summary

Internal Flash	Part number
4032 Kbytes	AT32F435ZMT7, AT32F435VMT7, AT32F435VMH7, AT32F435RMT7, AT32F435CMT7, AT32F435CMU7
1024 Kbytes	AT32F435ZGT7, AT32F435VGT7, AT32F435VGH7, AT32F435RGT7, AT32F435CGT7, AT32F435CGU7
448 Kbytes	AT32F435ZDT7, AT32F435VDT7, AT32F435VDH7, AT32F435RDT7, AT32F435CDT7, AT32F435CDU7
256 Kbytes	AT32F435ZCT7, AT32F435VCT7, AT32F435VCH7, AT32F435RCT7, AT32F435CCT7, AT32F435CCU7

Table 2. AT32F437 device summary

Internal Flash	Part number
4032 Kbytes	AT32F437ZMT7, AT32F437VMT7, AT32F437VMH7, AT32F437RMT7
1024 Kbytes	AT32F437ZGT7, AT32F437VGT7, AT32F437VGH7, AT32F437RGT7
448 Kbytes	AT32F437ZDT7, AT32F437VDT7, AT32F437VDH7, AT32F437RDT7
256 Kbytes	AT32F437ZCT7, AT32F437VCT7, AT32F437VCH7, AT32F437RCT7

Contents

1 Description 13

2 Functionality overview 18

2.1 ARM®Cortex®-M4F 18

2.2 Memory 19

2.2.1 Internal Flash memory 19

2.2.2 Memory protection unit (MPU) 19

2.2.3 SRAM 19

2.2.4 External memory controller (XMC) 19

2.2.5 Quad serial peripheral interface (QSPI) 19

2.3 Interrupts 20

2.3.1 Nested vectored interrupt controller (NVIC) 20

2.3.2 External interrupts (EXINT) 20

2.4 Power control (PWC) 20

2.4.1 Power supply schemes 20

2.4.2 Reset and power voltage monitoring (POR / LVR / PVM) 20

2.4.3 Voltage regulator (LDO) 20

2.4.4 Low-power modes 21

2.5 Boot modes 21

2.6 Clocks 22

2.7 General-purpose inputs / outputs (GPIO) 22

2.8 Direct Memory Access Controller (DMA) 23

2.9 Timers (TMR) 23

2.9.1 Advanced timers (TMR1, TMR8 and TMR20) 24

2.9.2 General-purpose timers (TMR2~5 and TMR9~14) 24

2.9.3 Basic timers (TMR6 and TMR7) 25

2.9.4 SysTick timer 25

2.10 Watchdog (WDT) 25

2.11 Window watchdog (WWDT) 25

2.12 Enhanced real-time clock (ERTC) and battery powered registers (BPR) 25

2.13 Communication interfaces 26

2.13.1 Serial peripheral interface (SPI) 26

2.13.2 Inter-integrated sound interface (I^2S) 26
2.13.3 Universal synchronous / asynchronous receiver transmitters (USART) 26
2.13.4 Inter-integrated-circuit interface (I^2C) 27
2.13.5 Secure digital input / output interface (SDIO) 27
2.13.6 Controller area network (CAN) 27
2.13.7 Universal serial bus On-The-Go full-speed (OTGFS) 28
2.13.8 Infrared transmitter (IRTMR) 28
2.13.9 Ethernet MAC interface (EMAC) 29
2.14 Digital video parallel interface (DVP) 29
2.15 Cyclic redundancy check (CRC) calculation unit 29
2.16 Analog-to-digital converter (ADC) 30
2.16.1 Temperature sensor (V_{TS}) 30
2.16.2 Internal reference voltage (V_{INTRV}) 30
2.16.3 V_{BAT} monitor ($V_{BAT}/4$) 30
2.17 Digital-to-analog converter (DAC) 31
2.18 Serial wire (SWD) / JTAG debug port 31

3 Pin functional definitions 32

4 Memory mapping 48

5 Electrical characteristics 49

5.1 Test conditions 49
5.1.1 Minimum and maximum values 49
5.1.2 Typical values 49
5.1.3 Typical curves 49
5.1.4 Power supply scheme 49
5.2 Absolute maximum values 50
5.2.1 Ratings 50
5.2.2 Electrical sensitivity 51
5.3 Specification 52
5.3.1 General operating conditions 52
5.3.2 Operating conditions at power-up / power-down 52
5.3.3 Embedded reset and power control block characteristics 53
5.3.4 Memory characteristics 54

5.3.5 Supply current characteristics 55
5.3.6 External clock source characteristics 65
5.3.7 Internal clock source characteristics 69
5.3.8 PLL characteristics 70
5.3.9 Wakeup time from low-power mode 70
5.3.10 EMC characteristics 70
5.3.11 GPIO port characteristics 71
5.3.12 NRST pin characteristics 73
5.3.13 XMC (SDRAM included) characteristics 73
5.3.14 TMR characteristics 92
5.3.15 SPI characteristics 92
5.3.16 I^2S characteristics 94
5.3.17 QSPI characteristics 96
5.3.18 I^2C characteristics 96
5.3.19 SDIO characteristics 97
5.3.20 OTGFS characteristics 98
5.3.21 EMAC characteristics 99
5.3.22 DVP characteristics 101
5.3.23 12-bit ADC characteristics 102
5.3.24 Internal reference voltage (V_{INTRV}) characteristics 105
5.3.25 Temperature sensor (V_{TS}) characteristics 106
5.3.26 V_{BAT} voltage monitor characteristics 107
5.3.27 12-bit DAC characteristics 108

6 Package information 109

6.1 LQFP144 109
6.2 LQFP100 111
6.3 BGA100 113
6.4 LQFP64 115
6.5 LQFP48 117
6.6 QFN48 119
6.7 Device marking 120
6.8 Thermal characteristics 121

7 Part numbering 122

8 Document revision history 123

List of tables

Table 1. AT32F435 device summary 2
Table 2. AT32F437 device summary 2
Table 3. AT32F435 features and peripheral counts 14
Table 4. AT32F437 features and peripheral counts 16
Table 5. Bootloader supporting part numbers and pin configurations 22
Table 6. Timer feature comparison 23
Table 7. USART/UART feature comparison 27
Table 8. AT32F435/437 series pin and solder ball definitions 37
Table 9. XMC pin definition 45
Table 10. Voltage characteristics 50
Table 11. Current characteristics 50
Table 12. Temperature characteristics 50
Table 13. ESD values 51
Table 14. Latch-up values 51
Table 15. General operating conditions 52
Table 16. Operating conditions at power-up/power-down 52
Table 17. Embedded reset and power management block characteristics 53
Table 18. Internal Flash memory characteristics (1) 54
Table 19. Internal Flash memory endurance and data retention (1) 54
Table 20. Typical current consumption in Run mode 56
Table 21. Typical current consumption in Sleep mode 57
Table 22. Maximum current consumption in Run mode 58
Table 23. Maximum current consumption in Sleep mode 59
Table 24. Typical and maximum current consumptions in Deepsleep and Standby modes(1) 60
Table 25. Typical and maximum current consumptions on V_{BAT}(1) 62
Table 26. Peripheral current consumption 63
Table 27. HEXT 4 ~ 25 MHz crystal characteristics (1)(2) 65
Table 28. HEXT external source characteristics 66
Table 29. LEXT 32.768 kHz crystal characteristics (1)(2) 67
Table 30. LEXT external source characteristics 68
Table 31. HICK clock characteristics 69
Table 32. LICK clock characteristics 69
Table 33. PLL characteristics 70
Table 34. Low-power mode wakeup time 70

Table 35. EMS characteristics 70
Table 36. GPIO static characteristics 71
Table 37. Output voltage characteristics 72
Table 38. Input AC characteristics 72
Table 39. NRST pin characteristics 73
Table 40. Asynchronous non-multiplexed SRAM/PSRAM/NOR read timings 74
Table 41. Asynchronous non-multiplexed SRAM/PSRAM/NOR write timings 75
Table 42. Asynchronous multiplexed PSRAM/NOR read timings 76
Table 43. Asynchronous multiplexed PSRAM/NOR write timings 77
Table 44. Synchronous non-multiplexed PSRAM/NOR read timings 78
Table 45. Synchronous non-multiplexed PSRAM write timings 80
Table 46. Synchronous multiplexed PSRAM/NOR read timings 81
Table 47. Synchronous multiplexed PSRAM write timings 82
Table 48. NAND Flash read and write timings 83
Table 49. PC card /CF read and write timings 86
Table 50. SDRAM read timings 90
Table 51. SDRAM write timings 91
Table 52. TMR characteristics 92
Table 53. SPI characteristics(1) 92
Table 54. I^2S characteristics(1) 94
Table 55. QSPI characteristics(1) 96
Table 56. SD/MMC characteristics(1) 97
Table 57. OTGFS startup time 98
Table 58. OTGFS DC electrical characteristics (1)(2) 98
Table 59. OTGFS electrical characteristics (1) 98
Table 60. EMAC DC electrical characteristics(1) 99
Table 61. Dynamic characteristics: EMAC signals for SMI(1) 99
Table 62. Dynamic characteristics: EMAC signals for RMII(1) 99
Table 63. Dynamic characteristics: EMAC signals for MII(1) 100
Table 64. ADC characteristics 102
Table 65. R_{AIN} max for f_{ADC} = 80 MHz 103
Table 66. ADC accuracy (1)(2) 103
Table 67. Internal reference voltage characteristics 105
Table 68. Temperature sensor characteristics 106
Table 69. V_{BAT} voltage monitor characteristics 107

Table 70. DAC characteristics 108
Table 71. LQFP144 – 20 x 20 mm 144 pin low-profile quad flat package mechanical data 110
Table 72. LQFP100 – 14 x 14 mm 100 pin low-profile quad flat package mechanical data 112
Table 73. BGA100 – 7 x 7 mm 100 solder balls array package mechanical data 114
Table 74. LQFP64 – 10 x 10 mm 64 pin low-profile quad flat package mechanical data 116
Table 75. LQFP48 – 7 x 7 mm 48 pin low-profile quad flat package mechanical data 118
Table 76. QFN48 – 6 x 6 mm 48 pin quad flat no-leads package mechanical data 120
Table 77. Package thermal characteristics 121
Table 78. AT32F435/437 series part numbering 122
Table 79. Document revision history 123

List of figures

Figure 1. AT32F435/437 block diagram 18
Figure 2. AT32F435/437 LQFP144 pinout 32
Figure 3. AT32F435/437 LQFP100 pinout 33
Figure 4. AT32F435/437 BGA100 solder ball array 34
Figure 5. AT32F435/437 LQFP64 pinout 35
Figure 6. AT32F435 LQFP48 pinout 36
Figure 7. AT32F435 QFN48 pinout 36
Figure 8. Memory mapping (AT32F435/437xM) 48
Figure 9. Power supply scheme 49
Figure 10. Power on reset and low voltage reset waveform 54
Figure 11. Typical current consumption in Deepsleep mode with regulator in run mode and output 1.2 V vs. temperature at different V_{DD} 60
Figure 12. Typical current consumption in Deepsleep mode with regulator in low-power mode and output 1.1 V vs. temperature at different V_{DD} 61
Figure 13. Typical current consumption in Standby mode vs. temperature at different V_{DD} (AT32F435/437xD) 61
Figure 14. Typical current consumption in Standby mode vs. temperature at different V_{DD} (others) 62
Figure 15. Typical current consumption on V_{BAT} with LEXT and ERTC ON vs. temperature at different V_{BAT} 62
Figure 16. HEXT typical application with an 8 MHz crystal 65
Figure 17. HEXT external source AC timing diagram 66
Figure 18. LEXT typical application with a 32.768 kHz crystal 67
Figure 19. LEXT external source AC timing diagram 68
Figure 20. HICK clock frequency accuracy vs. temperature 69
Figure 21. Recommended NRST pin protection 73
Figure 22. Asynchronous non-multiplexed SRAM/PSRAM/NOR read waveforms 74
Figure 23. Asynchronous non-multiplexed SRAM/PSRAM/NOR write waveforms 75
Figure 24. Asynchronous multiplexed PSRAM/NOR read waveforms 76
Figure 25. Asynchronous multiplexed PSRAM/NOR write waveforms 77
Figure 26. Synchronous non-multiplexed PSRAM/NOR read waveforms 79
Figure 27. Synchronous non-multiplexed PSRAM write waveforms 80
Figure 28. Synchronous multiplexed PSRAM/NOR read waveforms 81
Figure 29. Synchronous multiplexed PSRAM write waveforms 82
Figure 30. NAND controller read waveforms 84

Figure 31. NAND controller write waveforms 84
Figure 32. NAND controller common memory read waveforms 84
Figure 33. NAND controller for common memory write waveforms 85
Figure 34. PC card/CF controller waveforms for common memory read access 87
Figure 35. PC card/CF controller waveforms for common memory write access 87
Figure 36. PC card/CF controller waveforms for attribute memory read access 88
Figure 37. PC card/CF controller waveforms for attribute memory write access 88
Figure 38. PC card /CF controller waveforms for I/O space read access 89
Figure 39. PC card/CF controller waveforms for I/O space write access 89
Figure 40. SDRAM read waveforms 90
Figure 41. SDRAM write waveforms 91
Figure 42. SPI timing diagram – slave mode and CPHA = 0 93
Figure 43. SPI timing diagram – slave mode and CPHA = 1 93
Figure 44. SPI timing diagram – master mode 93
Figure 45. I^2S slave timing diagram (Philips protocol) 94
Figure 46. I^2S master timing diagram (Philips protocol) 95
Figure 47. QSPI timing diagram 96
Figure 48. SDIO high-speed mode 97
Figure 49. SD default mode 97
Figure 50. OTGFS timings: definition of data signal rise and fall time 98
Figure 51. EMAC SMI timing diagram 99
Figure 52. EMAC RMII timing diagram 100
Figure 53. EMAC MII timing diagram 100
Figure 54. DVP timing diagram 101
Figure 55. ADC accuracy characteristics 104
Figure 56. Typical connection diagram using the ADC 104
Figure 57. Power supply and reference decoupling (V_{REF+} connected to V_{DDA}) 105
Figure 58. Power supply and reference decoupling (V_{REF+} not connected to V_{DDA}) 105
Figure 59. Ideal curve of V_{TS} vs. temperature 106
Figure 60. LQFP144 – 20 x 20 mm 144 pin low-profile quad flat package outline 109
Figure 61. LQFP100 – 14 x 14 mm 100 pin low-profile quad flat package outline 111
Figure 62. BGA100 – 7 x 7 mm 100 solder balls array package outline 113
Figure 63. LQFP64 – 10 x 10 mm 64 pin low-profile quad flat package outline 115
Figure 64. LQFP48 – 7 x 7 mm 48 pin low-profile quad flat package outline 117
Figure 65. QFN48 – 6 x 6 mm 48 pin quad flat no-leads package outline 119

Figure 66. Marking example 120

1 Description

The AT32F435/437 is based on the high-performance ARM® Cortex®-M4F 32-bit RISC core running up to 288 MHz. The Cortex®-M4F core features a Floating point unit (FPU) single precision which supports all ARM single-precision data processing instructions and data type. It also implements a full set of DSP instructions and a memory protection unit (MPU) which enhances application security.

The AT32F435/437 incorporates high-speed embedded memories (up to 4032 Kbytes of internal Flash memory and configurable maximum 512 Kbytes of SRAM), enhanced GPIOs and peripherals connected to two APB buses. Any block of the embedded Flash memory can be protected by the “sLib”, functioning as a security area with code-executable only. In addition, the AT32F435/437 includes high-level memory extension: one external memory controller (XMC) (SDRAM interfaced included) and two quad-SPI interface (QSPI).

The AT32F435/437 offers three 12-bit ADCs, two 12-bit DACs, 13 general-purpose 16-bit timers (three PWM advanced timers for motor control included), two general-purpose 32-bit timers, and one low-power ERTC. It supports standard and advanced communication interfaces: up to three I^2Cs, four SPIs (all multiplexed as I^2Ss), two SDIOs, four USARTs plus four UARTs, one infrared transmitter, two OTGFS interfaces, two CANs, one digital video parallel (DVP) interface, and an Ethernet MAC (EMAC) interface.

The AT32F435/437 operates in the -40 to +105 °C temperature range, from a 2.6 to 3.6 V power supply. A comprehensive set of power-saving mode meets the requirements of low-power application.

The AT32F435/437 offers devices in different package types. Depending on the different packages, the pin-to-pin is compatible among devices, and also the software and functionality. Only different sets of peripherals are included.

Table 3. AT32F435 features and peripheral counts

Part number		AT32F435xxU7				AT32F435xxT7								AT32F435xxH7				AT32F435xxT7							
		CC	CD	CG	CM	CC	CD	CG	CM	RC	RD	RG	RM	VC	VD	VG	VM	VC	VD	VG	VM	ZC	ZD	ZG	ZM
Frequency (MHz)		288																							
Int. Flash(1)(2)	ZW (Kbytes)	256	256	256	256	256	256	256	256	256	256	256	256	256	256	256	256	256	256	256	256	256	256	256	256
	NZW (Kbytes)	0	192	768	3776	0	192	768	3776	0	192	768	3776	0	192	768	3776	0	192	768	3776	0	192	768	3776
	Total (Kbytes)	256	448	1024	4032	256	448	1024	4032	256	448	1024	4032	256	448	1024	4032	256	448	1024	4032	256	448	1024	4032
SRAM(2) (Kbytes)		384 by default, configurable maximum 512																							
XMC		-				-				1(3)				1(4)(5)				1(4)(5)				1			
SDRAM		-				-				-				1(4)				1(4)				1			
QSPI		2				2				2				2				2				2			
Timers	Advanced	3				3				3				3				3				3			
	32-bit general-purpose	2				2				2				2				2				2			
	16-bit general-purpose	8				8				8				8				8				8			
	Basic	2				2				2				2				2				2			
	SysTick	1				1				1				1				1				1			
	WDT	1				1				1				1				1				1			
	WWDT	1				1				1				1				1				1			
	ERTC	1				1				1				1				1				1			
Communication interfaces	I^2C	3				3				3				3				3				3			
	SPI(6)	4				4				4				4				4				4			
	I^2S(6)	4 (2 full-duplex)				4 (2 full-duplex)				4 (2 full-duplex)				4 (2 full-duplex)				4 (2 full-duplex)				4 (2 full-duplex)			
	USART + UART	3 + 4(7)				3 + 4(7)				4 + 4				4 + 4				4 + 4				4 + 4			
	SDIO	1(8)				1(8)				2				2				2				2			
	OTGFS	2				2				2				2				2				2			
	CAN	2				2				2				2				2				2			
	IRTMR	1				1				1				1				1				1			
Analog	12-bit ADC numbers/channels	3																							
		10				10				16				16				16				24			
	12-bti DAC numbers	2																							
DVP(9)		1				1				1				1				1				1			
GPIO		39				39				53				84				84				116			
Operating temperature		-40 °C to +105 °C																							
Packages		QFN48 6 x 6 mm				LQFP48 7 x 7 mm				LQFP64 10 x 10 mm				BGA100 7 x 7 mm				LQFP100 14 x 14 mm				LQFP144 20 x 20 mm			

(1) ZW = = zero wait-state, up to SYSCLK 288 MHz
NZW = non-zero wait-state
(2) The internal Flash and SRAM sizes are configurable with User System Data, configurable in every 64-KByte step.
Take the AT32F435xC as an example, the Flash/SRAM can be configured into three options below:
- ZW: 256 Kbytes, NZW: 0 Kbyte, SRAM: 384 Kbytes (default setting before shipping form the factory)
- ZW: 192 Kbytes, NZW: 64 Kbytes, SRAM: 448 Kbytes
- ZW: 128 Kbytes, NZW: 128 Kbytes, SRAM: 512 Kbytes
Take the AT32F435xD as an example, the Flash/SRAM can be configured into six options below:
- ZW: 448 Kbytes, NZW: 0 Kbyte, SRAM: 192 Kbytes
……
- ZW: 256 Kbytes, NZW: 192 Kbytes, SRAM: 384 Kbytes (default setting before shipping form the factory)
……
- ZW: 128 Kbytes, NZW: 320 Kbytes, SRAM: 512 Kbytes
Take the AT32F435xG as an example, the Flash/SRAM can be configured into seven options below:
- ZW: 512 Kbytes, NZW: 512 Kbytes, SRAM: 128 Kbytes
……
- ZW: 256 Kbytes, NZW: 768 Kbytes, SRAM: 384 Kbytes (default setting before shipping form the factory)
……
- ZW: 128 Kbytes, NZW: 896 Kbytes, SRAM: 512 Kbytes
Take the AT32F435xM as an example, the Flash/SRAM can be configured into seven options below:
- ZW: 512 Kbytes, NZW: 3520 Kbytes, SRAM: 128 Kbytes
……
- ZW: 256 Kbytes, NZW: 3776 Kbytes, SRAM: 384 Kbytes (default setting before shipping form the factory)
……
- ZW: 128 Kbytes, NZW: 3904 Kbytes, SRAM: 512 Kbytes
(3) For LQFP64 package, XMC only supports the LCD panel with 8-bit mode.
(4) For the LQFP100 and BGA100 packages, XMC supports to directly connect a multiplexed NOR/PSRAM memory, a 16- or 8-bit NAND Flash memory, and the SDRAM. The interrupt line cannot be used since Port G is not available in this package.
(5) For the LQFP100 and BGA100 packages, XMC supports a non-multiplexed NOR/PSRAM memory via the external latch circuit. Please refer to the application note AN0068.
(6) Half-duplex I^2S shares the same pin with SPI.
(7) For LQFP48 and QFN48 packages, UART8 is not available and USART6 is used as UART for no CK pinout.
(8) For LQFP48 and QFN48 packages, either SDIO1 or SDIO2 can be used. The SDIO2 only supports maximum 4-bit (D0~D3) mode.
(9) Only LQFP144 package supports maximum 14-bit mode; LQPF48 and QFN48 packages support only 8-bit mode; LQFP100, BGA100 and LQFP64 packages support maximum 12-bit mode.

Table 4. AT32F437 features and peripheral counts

Part number		AT32F437xxT7				AT32F437xxH7				AT32F437xxT7							
		RC	RD	RG	RM	VC	VD	VG	VM	VC	VD	VG	VM	ZC	ZD	ZG	ZM
Frequency (MHz)		288															
Int. Flash[1][2]	ZW (Kbytes)	256	256	256	256	256	256	256	256	256	256	256	256	256	256	256	256
	NZW (Kbytes)	0	192	768	3776	0	192	768	3776	0	192	768	3776	0	192	768	3776
	Total (Kbytes)	256	448	1024	4032	256	448	1024	4032	256	448	1024	4032	256	448	1024	4032
SRAM[2] (Kbytes)		384 by default, configurable maximum 512															
XMC		1[3]				1[4][5]				1[4][5]				1			
SDRAM		-				1[4]				1[4]				1			
QSPI		2				2				2				2			
Timers	Advanced	3				3				3				3			
	32-bit general-purpose	2				2				2				2			
	16-bit general-purpose	8				8				8				8			
	Basic	2				2				2				2			
	SysTick	1				1				1				1			
	WDT	1				1				1				1			
	WWDT	1				1				1				1			
	ERTC	1				1				1				1			
Communication interfaces	I^2C	3				3				3				3			
	SPI[6]	4				4				4				4			
	I^2S[6]	4 (2 full-duplex)				4 (2 full-duplex)				4 (2 full-duplex)				4 (2 full-duplex)			
	USART + UART	4 + 4				4 + 4				4 + 4				4 + 4			
	SDIO	2				2				2				2			
	OTGFS	2				2				2				2			
	CAN	2				2				2				2			
	Ethernet MAC	1				1				1				1			
	IRTMR	1				1				1				1			
Analog	12-bit ADC numbers/channels	3															
		16				16				16				24			
	12-bit DAC numbers	2															
DVP[7]		1				1				1				1			
GPIO		53				84				84				116			
Operating temperature		-40 °C to +105 °C															
Packages		LQFP64 10 x 10 mm				BGA100 7 x 7 mm				LQFP100 14 x 14 mm				LQFP144 20 x 20 mm			

(1) ZW = zero wait-state, up to SYSCLK 288 MHz
NZW = non-zero wait-state

(2) The internal Flash and SRAM sizes are configurable with User System Data, configurable in every 64-KByte step.
Take the AT32F437xC as an example, the Flash/SRAM can be configured into three options below:
- ZW: 256 Kbytes, NZW: 0 Kbyte, SRAM: 384 Kbytes (default setting before shipping form the factory)
- ZW: 192 Kbytes, NZW: 64 Kbytes, SRAM: 448 Kbytes
- ZW: 128 Kbytes, NZW: 128 Kbytes, SRAM: 512 Kbytes

Take the AT32F437xD as an example, the Flash/SRAM can be configured into six options below:
- ZW: 448 Kbytes, NZW: 0 Kbyte, SRAM: 192 Kbytes
……
- ZW: 256 Kbytes, NZW: 192 Kbytes, SRAM: 384 Kbytes (default setting before shipping form the factory)
……
- ZW: 128 Kbytes, NZW: 320 Kbytes, SRAM: 512 Kbytes

Take the AT32F437xG as an example, the Flash/SRAM can be configured into seven options below:
- ZW: 512 Kbytes, NZW: 512 Kbytes, SRAM: 128 Kbytes
……
- ZW: 256 Kbytes, NZW: 768 Kbytes, SRAM: 384 Kbytes (default setting before shipping form the factory)
……
- ZW: 128 Kbytes, NZW: 896 Kbytes, SRAM: 512 Kbytes

Take the AT32F437xM as an example, the Flash/SRAM can be configured into seven options below:
- ZW: 512 Kbytes, NZW: 3520 Kbytes, SRAM: 128 Kbytes
……
- ZW: 256 Kbytes, NZW: 3776 Kbytes, SRAM: 384 Kbytes (default setting before shipping form the factory)
……
- ZW: 128 Kbytes, NZW: 3904 Kbytes, SRAM: 512 Kbytes

(3) For LQFP64 package, XMC only supports the LCD panel with 8-bit mode.

(4) For the LQFP100 and BGA100 packages, XMC supports to directly connect a multiplexed NOR/PSRAM memory, a 16- or 8-bit NAND Flash memory, and the SDRAM. The interrupt line cannot be used since Port G is not available in this package.

(5) For the LQFP100 and BGA100 packages, XMC supports a non-multiplexed NOR/PSRAM memory via the external latch circuit. Please refer to the application note AN0068.

(6) Half-duplex I^2S shares the same pin with SPI.

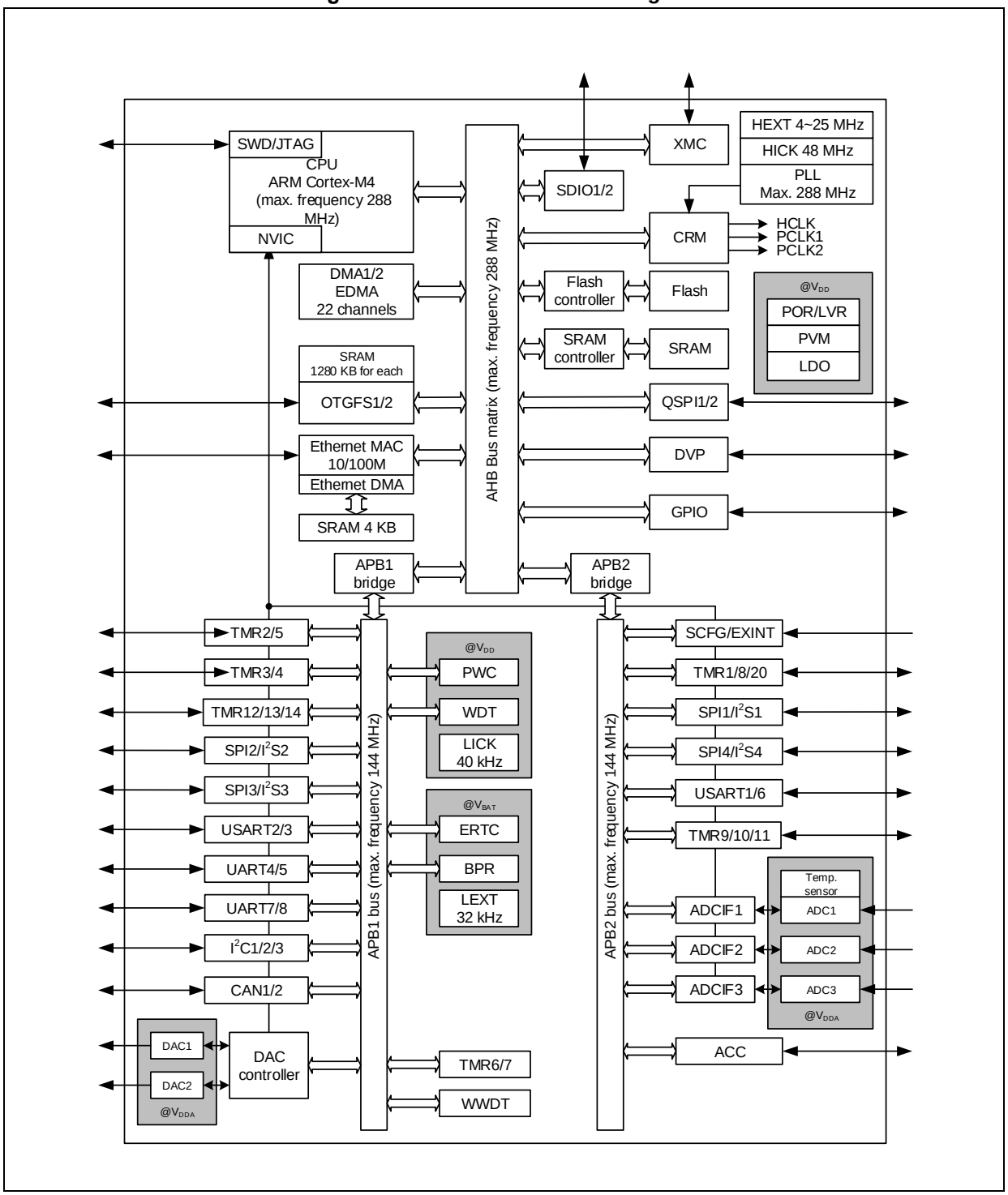
(7) Only LQFP144 package supports maximum 14-bit mode; LQFP100, BGA100 and LQFP64 packages support maximum 12-bit mode.

2 Functionality overview

2.1 ARM®Cortex®-M4F

The ARM Cortex®-M4F processor is the latest generation of ARM processors for embedded systems. It is a 32-bit RISC processor features exceptional code efficiency, outstanding computational power and advanced response to interrupts. The processor supports a set of DSP instructions which enable efficient signal processing and complex algorithm execution. Its single precision FPU (floating point unit) speeds up floating point calculation while avoiding saturation. *Figure 1* shows the general block diagram of the AT32F435/437.

Figure 1. AT32F435/437 block diagram



2.2 Memory

2.2.1 Internal Flash memory

Up to 4032 Kbytes of embedded Flash is available for storing programs and data. User can configure any part of the embedded Flash memory protected by the sLib, functioning as a security area with code-executable only but non-readable. “sLib” is a mechanism that protects the intelligence of solution venders and facilitates the second-level development by customers. After the register bit NZW_BST is enabled, the overall NZW area code execution performance can be improved, but the maximum clock frequency of AHB is lower than that when it is disabled. Please refer to *Table 15* when using it.

There is another 18-KByte boot memory in which the bootloader is stored.

A User System Data block is included, which is used as configuration of the hardware behaviors such as read/erase/write protection and watchdog self-enable. User System Data allows to set erase/write and read protection individually, with the latter supporting low-level and high-level protection.

2.2.2 Memory protection unit (MPU)

The memory protection unit (MPU) is used to manage the CPU accesses to memory to prevent one task to accidentally corrupt the memory or resources used by any other active task. This memory area consists of up to 8 protected areas that can in turn be divided up into 8 subareas. The protection area sizes are between 32 bytes and the whole 4 gigabytes of addressable memory. The MPU is especially suited to the applications where some critical or certified code has to be protected against the misbehavior of other tasks. It is usually managed by an RTOS (real-time operating system).

2.2.3 SRAM

384 Kbytes of on-chip SRAM by default and configurable maximum 512 Kbytes, accessed (read/write) at CPU clock speed with 0 wait state.

2.2.4 External memory controller (XMC)

The XMC is embedded in the AT32F435/437. It has four Chip Select outputs supporting the following modes: CF card, SRAM, PSRAM, NOR flash, NAND flash, and SDRAM.

Main features:

- 8-bit or 16-bit data bus width
- Read buffer for SDRAM controller
- Write buffer

The XMC can be configured to interface with most graphic LCD controllers. It supports the Intel 8080 and Motorola 6800 modes.

2.2.5 Quad serial peripheral interface (QSPI)

The AT32F435/437 series embed two quad serial peripheral interfaces (QSPI). This is a dedicated communication interface which connects single, dual, or quad data lines of SPI flash memory or SPI RAM. It can work in indirect mode (fully accessed by control registers), status polling mode, or

memory mapping mode with up to 256 Mbytes mapping of the external SPI flash or RAM. QSPI can be accessed by bytes, half-words, or words, supporting execution-in-place (XIP) operation and fully programmable command and frame format.

2.3 Interrupts

2.3.1 Nested vectored interrupt controller (NVIC)

The AT32F435/437 series embed a nested vectored interrupt controller that is able to manage 16 priority levels and handle maskable interrupt channels plus the 16 interrupt lines of the Cortex®-M4F with FPU. This hardware block provides flexible interrupt management features with minimal interrupt latency.

2.3.2 External interrupts (EXINT)

The external interrupt (EXINT), which is connected directly with NVIC, consists of 22 edge detector lines used to generate interrupt requests. Each line can be independently configured to select the trigger event (rising edge, falling edge, both) and can be masked independently. A pending register maintains the status of the interrupt requests. The external interrupt lines connect up to 16 GPIOs.

2.4 Power control (PWC)

2.4.1 Power supply schemes

- V_{DD} = 2.6 ~ 3.6 V: power supply for GPIOs and the internal block such as regulator (LDO), provided externally via V_{DD} pins.
- V_{DDA} = 2.6 ~ 3.6 V: power supply for ADC and DAC. V_{DDA} and V_{SSA} must be the same voltage potential as V_{DD} and V_{SS}, respectively.
- V_{BAT} = 1.62 ~ 3.6 V: V_{BAT} pin can supply V_{BAT} domain from the external battery or super capacity, or from V_{DD} without the external battery or super capacity. V_{BAT} (through power switch) supplies for ERTC, external crystal 32 kHz (LEXT), and battery powered registers (BPR) when V_{DD} is not present.

2.4.2 Reset and power voltage monitoring (POR / LVR / PVM)

The device has an integrated power-on reset (POR)/low voltage reset (PDR) circuitry. It is always active, and allows proper operation starting from/down to 2.6 V. The device remains in reset mode when V_{DD} goes below a specified threshold (V_{LVR}) without the need for an external reset circuit.

The device embeds a power voltage monitor (PVM) that monitors the V_{DD} power supply and compares it to the V_{PVM} threshold. An interrupt can be generated when V_{DD} drops below the V_{PVM} threshold and/or when V_{DD} rises above the V_{PVM} threshold. The PVM is enabled by software.

2.4.3 Voltage regulator (LDO)

The LDO has three operating modes: normal, low-power, and power down.

- Normal mode is used in Run/Sleep mode and in the Deepsleep mode;
- Low-power mode can be used in the Deepsleep mode;
- Power down mode is used in Standby mode: The regulator output is in high impedance and the kernel circuitry is powered down but the contents of the registers and SRAM are lost.

This LDO operates always in its normal mode after chip reset.

The LDO has the ability to adjust its output voltage. Besides 1.2V by default, it supports 1.3/1.1V adjusted by software so as to enable flexibility between performance and power consumption. Note that different LDO voltages have limitation about the maximum frequency of the AHB clock. Please check *Table 15*, and follow steps specified in the AT32F435/437 reference manual to switch LDO voltage and set the system clock.

2.4.4 Low-power modes

The AT32F435/437 series support three low-power modes:

- **Sleep mode**

  In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.

- **Deepsleep mode**

  Deepsleep mode achieves the low power consumption while retaining the content of SRAM and registers. All clocks in the LDO power domain are stopped, disabling the PLL, the HICK clock, and the HEXT crystal. The voltage regulator can also be put in normal or low-power mode, with output voltage being adjustable.

  The device can be woken up from Deepsleep mode by any of the EXINT line. The EXINT line source can be one of the 16 external lines, the PVM output, an ERTC alarm/wakeup/tamper/time stamp event, and the OTGFS or the Ethernet MAC wakeup.

- **Standby mode**

  The Standby mode is used to acquire the lowest power consumption. The internal voltage regulator is switched off so that the entire LDO power domain is powered off. The PLL, HICK clock and HEXT crystal are also switched off. After entering Standby mode, SRAM and register contents are lost except for the ERTC register, registers in the BPR domain, and Standby circuitry.

  The device exits Standby mode when an external reset (NRST pin), a WDT reset, a rising edge on the WKUPx pin, or an ERTC alarm/wakeup/tamper/time stamp occurs.

Note: The ERTC and the corresponding clock sources are not stopped by entering Deepsleep or Standby mode. WDT depends on the User System Data setting.

2.5 Boot modes

At startup, boot pins are used to select one of three boot options:

- Boot from internal Flash memory. For the AT32F435/437xG/xM, user has an option to boot from any of two memory banks. By default, boot from Flash memory bank 1 is selected. User can choose to boot from Flash memory bank 2 by setting a bit in the User System Data area.
- Boot from boot memory.
- Boot from embedded SRAM.

The bootloader is stored in boot memory. It is used to reprogram the Flash memory through USART1, USART2, USART3, OTGFS1, or OTGFS2 (OTGFS1 and OTGFS2 support crystal-less). *Table 5* provides the supporting interfaces of the Bootloader regarding AT32F435/437 part numbers and pin configurations.

Table 5. Bootloader supporting part numbers and pin configurations

Interface	Part number	Pin
USART1	All part numbers	PA9: USART1_TX PA10: USART1_RX
USART2	AT32F435Zxxx, AT32F435Vxxx AT32F437Zxxx, AT32F437Vxxx	PD5: USART2_TX PD6: USART2_RX
	Other part numbers	PA2: USART2_TX PA3: USART2_RX
USART3	AT32F435Zxxx, AT32F435Vxxx, AT32F435Rxxx AT32F437Zxxx, AT32F437Vxxx, AT32F437Rxxx	PC10: USART3_TX PC11: USART3_RX or PB10: USART3_TX(1) PB11: USART3_RX(1)
	Other part numbers	PB10: USART3_TX PB11: USART3_RX
OTGFS1	All part numbers	PA11: OTGFS1_D- PA12: OTGFS1_D+
OTGFS2	All part numbers	PB14: OTGFS2_D- PB15: OTGFS2_D+

(1) Silicon version B.

2.6 Clocks

The internal 48 MHz clock (HICK) through a divided-by-6 divider (8 MHz) is selected as the default CPU clock after any reset. An external 4 to 25 MHz clock (HEXT) can be selected, in which case it is monitored for failure. If a failure is detected, HEXT will be switched off and the system automatically switches back to the internal HICK. A software interrupt is generated. Similarly, the system takes the same action once HEXT fails when it is used as the source of PLL.

Several prescalers are used for the configuration of the AHB and the APB (APB1 and APB2) frequency. The maximum frequency of the AHB domain is 288 MHz. The maximum allowed frequency of the APB domain is 144 MHz.

The AT32F435/437 series embed an automatic clock calibration (ACC) block, which calibrates the internal 48 MHz HICK clock, assuring the most precise accuracy of the HICK in the full range of the operating temperatures.

2.7 General-purpose inputs / outputs (GPIO)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain with or without pull-up or pull-down), as input (floating with or without pull-up or pull-down), or as multiple function. Most of the GPIO pins are shared with digital or analog multiple functions. All GPIOs are high current-capable.

The GPIO configuration can be locked, if needed, in order to avoid false writing to the GPIO registers by following a specific sequence.

2.8 Direct Memory Access Controller (DMA)

AT32F435/437 series have two general-purpose DMAs (DMA1 and DMA2) plus one enhanced EDMA, 22 channels in total. They are able to manage memory-to-memory, peripheral-to-memory, and memory-to-peripheral transfers. They also have dedicated buffers for APB/AHB peripherals and support burst transmission, which provides the maximum bandwidth for peripherals.

DMA/EDMA controllers support circular buffer management, removing the need for special code intervention when the controller reaches the end of the buffer. Besides, EDMA controller has double buffers, which allows the automatic use and switch between two memory buffers without the need for special code intervention.

Each channel is connected to dedicated hardware DMA/EDMA requests, with support for software trigger on each channel. Configuration is made by software and transfer sizes between source and destination are independent.

The DMA/EDMA can be used with the main peripherals: SPI and I^2S, I^2C, USART, advanced/ general-purpose/ basic timers TMRx, DAC, SDIO, ADC, DVP and QSPI.

2.9 Timers (TMR)

The AT32F435/437 devices include up to 3 advanced timers, up to 10 general-purpose timers, 2 basic timers and a SysTick timer.

The table below compares the features of the advanced, general-purpose, and basic timers.

Table 6. Timer feature comparison

Type	Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/compare channels	Complementary outputs
Advanced	TMR1 TMR8 TMR20	16-bit	Up, down, up/down	Any integer between 1 and 65536	Yes	4	3
General-purpose	TMR2 TMR5	16-bit or 32-bit	Up, down, up/down	Any integer between 1 and 65536	Yes	4	No
	TMR3 TMR4	16-bit	Up, down, up/down	Any integer between 1 and 65536	Yes	4	No
	TMR9 TMR12	16-bit	Up	Any integer between 1 and 65536	No	2	No
	TMR10 TMR11 TMR13 TMR14	16-bit	Up	Any integer between 1 and 65536	No	1	No
Basic	TMR6 TMR7	16-bit	Up	Any integer between 1 and 65536	Yes	No	No

2.9.1 Advanced timers (TMR1, TMR8 and TMR20)

The three advanced timers (TMR1, TMR8, and TMR20) can each be seen a three-phase PWM multiplexed on 6 channels. They have complementary PWM outputs with programmable inserted dead-times. Each of these timers can also be seen as a complete general-purpose timer. The 4 independent channels can be used for:

- Input capture
- Output compare
- PWM generation (edge or center-aligned modes)
- One-cycle mode output

If configured as a standard 16-bit timer, it has the same features as the TMRx timer. If configured as the 16-bit PWM generator, it has full modulation capability (0 to 100%).

In debug mode, the advanced timer counter can be frozen and the PWM outputs disabled to turn off any power switch driven by these outputs.

Many features are shared with those of the general-purpose TMR which have the same architecture. The advanced timer can therefore work together with the TMR timers via the link feature for synchronization or event chaining.

2.9.2 General-purpose timers (TMR2~5 and TMR9~14)

There are 10 synchronizable general-purpose timers embedded in the AT32F435/437 series.

- **TMR2, TMR3, TMR4 and TMR5**

  The AT32F435/437 series have 4 full-featured general-purpose timers: TMR2, TMR3, TMR4 and TMR5. The TMR2 and TMR5 timers are based on a 32-bit auto-reload upcounter/downcounter and a 16-bit prescaler. The TMR3 and TMR4 timers are based on a 16- bit auto-reload upcounter/downcounter and a 16-bit prescaler. They can offer four independent channels on the largest packages. Each channel can be used for input capture/output compare, PWM or one-cycle mode outputs.

  These general-purpose timers can work together, or with the other general-purpose timers and the advanced timers via the link feature for synchronization or event chaining. In debug mode, their counter can be frozen. Any of these general-purpose timers can be used to generate PWM outputs. Each timer has individual DMA request.

  These timers are capable of handling incremental quadrature encoder signals and the digital outputs coming from 1 to 3 hall-effect sensors.

- **TMR9 and TMR12**

  TMR9 and TMR12 are based on a 16-bit auto-reload upcounter, a 16-bit prescaler, and two independent channels for input capture/output compare, PWM, or one-cycle mode output. They can be synchronized with the TMR2, TMR3, TMR4, and TMR5 full-featured general-purpose timers. They can also be used as simple time bases.

- **TMR10, TMR11, TMR13 and TMR14**

These timers are based on a 16-bit auto-reload upcounter, a 16-bit prescaler, and one independent channels for input capture/output compare, PWM, or one-cycle mode output. They can be synchronized with the TMR2, TMR3, TMR4 and TMR5 full-featured general-purpose timers. They can also be used as simple time bases.

2.9.3 Basic timers (TMR6 and TMR7)

These two timers are mainly used for DAC trigger generation. Each of them can also be used as a generic 16-bit time base.

2.9.4 SysTick timer

This timer is dedicated to real-time operating systems, but could also be used as a standard down counter. Its features include:

- A 24-bit down counter
- Auto reload capability
- Maskable system interrupt generation when the counter reaches 0
- Programmable clock source (HCLK or HCLK/8)

2.10 Watchdog (WDT)

The watchdog consists of a 12-bit downcounter and 8-bit prescaler. It is clocked by an independent internal LICK clock. As it operates independently from the main clock, it can operate in Deepsleep and Standby modes. It can be used either as a watchdog to reset the device when an error occurs, or as a free running timer for application timeout management. It is self-enabling or not configurable through the User System Data. The counter can be frozen in debug mode.

2.11 Window watchdog (WWDT)

The window watchdog embeds a 7-bit downcounter that can be set as free running. It can be used as a watchdog to reset the device when an error occurs. It is clocked by the main clock. It has an early warning interrupt capability and the counter can be frozen in debug mode.

2.12 Enhanced real-time clock (ERTC) and battery powered registers (BPR)

The battery powered domain includes:

- Enhanced real-time clock (ERTC)
- Twenty 32-bit battery powered registers

The enhanced real-time clock (ERTC) is an independent BCD timer/counter. It supports the following features:

- Calendar with second, minute, hour (12 or 24 format), week day, date, month, year, in BCD (binary-coded decimal) format.
- The sub-seconds value is also available in binary format.
- Automatic correction for 28, 29 (leap year), 30, and 31 days of the month.
- Programmable alarms and periodic wakeup from Deepsleep or Standby mode

- To compensate quartz crystal inaccuracy, ERTC can be calibrated via a 512 Hz external output

Two alarm registers are used to generate an alarm at a specific time whereas the calendar fields can be independently masked for alarm comparison. To generate a periodic interrupt, a 16-bit programmable binary auto-reload downcounter with programmable resolution is available and allows automatic wakeup and periodic alarms from every 120 μs to every 36 hours. Other 32-bit registers also feature programmable sub-second, second, minute, hour, week day and date.

The prescaler is used as a time base clock. It is by default configured to generate a time base of 1 second from a clock at 32.768 kHz.

The battery powered registers (BPR) are 32-bit registers used to store 80 bytes of user application data. Battery powered registers are not reset by a system or power reset, or when the device is woken up from the Standby mode

ERTC and BPR are powered through a power switch. When V_{DD} exists, the switch selects V_{DD} as power supply, or V_{BAT} is used as supply source.

2.13 Communication interfaces

2.13.1 Serial peripheral interface (SPI)

There are up to four 50 Mbits/s SPIs able to communicate in slave and master modes in full-duplex and simplex communication modes. The prescaler generates several master mode frequencies and the frame is configurable to 8 bits or 16 bits. The hardware CRC generation/verification supports basic SD card/MMC/SDHC modes. All SPIs can be served by the DMA controller.

The SPI interface can be configured to operate in TI mode for communications in master and slave modes.

2.13.2 Inter-integrated sound interface (I^2S)

Four standard I^2S interfaces (multiplexed with SPI) are available, which can be operated in master or slave mode in half-duplex mode. These interfaces can be configured to operate with 16/24/32 bit resolution, as input or output channels. Audio sampling frequencies ranges from 8 kHz up to 192 kHz. When I^2S is configured in master mode, the master clock can be output to the external 256 times sampling frequency. All I^2Ss can use the DMA controller.

2.13.3 Universal synchronous / asynchronous receiver transmitters (USART)

The AT32F435/437 series embed four universal synchronous/asynchronous receiver transmitters (USART1, USART2, USART3, and USART6) and four universal asynchronous receiver transmitters (UART4, UART5, UART7, and UART8).

These eight interfaces provide asynchronous communication, IrDA SIR ENDEC support, multiprocessor communication mode, single-wire half-duplex communication mode, and have LIN Master/Slave capability. USART1, USART2, USART3, and USART6 provide hardware management of the CTS and RTS signals. They also provide Smart Card mode (ISO 7816 compliant) and SPI-like communication capability. All interfaces can be served by the DMA controller. The USART interfaces can be up to 9 Mbit/s.

Table 7. USART/UART feature comparison

USART/UART feature	USART1	USART2	USART3	UART4	UART5	USART6	UART7	UART8
Hardware flow control for modem	Yes	Yes	Yes	-	-	Yes	-	-
Continuous communication using DMA	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Multiprocessor communication	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Synchronous mode	Yes	Yes	Yes	-	-	Yes	-	-
Smartcard mode	Yes	Yes	Yes	-	-	Yes	-	-
Single-wire half-duplex communication	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
IrDA SIR ENDEC block	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
LIN mode	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
TX/RX swap	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
RS-485 driver enable	Yes	Yes	Yes	-	-	Yes	-	-

2.13.4 Inter-integrated-circuit interface (I^2C)

Up to three I^2C bus interfaces can operate in multi-master and slave modes. They support standard mode (max. 100 kHz), fast mode (max. 400 kHz), and fast mode plus (max. 1 MHz). Several GPIOs provide ultra-high sink current 20 mA.

They support 7/10-bit addressing mode and 7-bit dual addressing mode (as slave). A hardware CRC generation/verification is included.

They can be served by DMA and they support SMBus 2.0/PMBus.

2.13.5 Secure digital input / output interface (SDIO)

Two SD/SDIO/MMC host interfaces are available, supporting MultiMediaCard System Specification Version 4.2 in three different data bus modes: 1-bit (default), 4-bit and 8-bit. The interface allows data transfer at up to 48 MHz in 8-bit mode, and is compliant with SD Memory Card Specifications Version 2.0.

The two different data bus modes supported in the SDIO Card Specification Version 2.are: 1-bit (default) and 4-bit.

The current version supports only one SD/SDIO/MMC4.2 card at any one time and a series of MMC4.1 or previous.

Apart from SD/SDIO/MMC/eMMC, this interface is fully compliant with the CE-ATA digital protocol Rev1.1.

2.13.6 Controller area network (CAN)

Two CANs are compliant with specifications 2.0A and B (active) with a bit rate up to 1 Mbit/s. It can receive and transmit standard frames with 11-bit identifiers as well as extended frames with 29-bit identifiers. Each CAN has three transmit mailboxes, two receive FIFOs with 3 stages, and 28 scalable filter banks. Each also has dedicated 368 Bytes of SRAM, which is not shared with the other CAN or any other peripherals.

To guarantee CAN transmission quality, the CAN 2.0 protocol states that its clock source must come from the HEXT-based PLL clock.

2.13.7 Universal serial bus On-The-Go full-speed (OTGFS)

The AT32F435/437 series embed two OTG full-speed (12 Mb/s) modules that consists of PHY and can be set as a device/host. The OTGFS has software-configurable endpoint setting and supports suspend/resume. The OTGFS module requires a dedicated 48 MHz clock. When the OTGFS acts as a host, its clock source should be PLL clocked by HEXT; in device mode, tis clock source can be selected as 48 MHz HICK.

Each OTGFS has the major features such as:

- 1280 Kbytes of buffer used exclusively by the endpoints (not shared with the other OTGFS or any other peripherals)
- 8 IN + 8 OUT endpoints (endpoint 0 included, device mode)
- 16 channels (host mode)
- SOF output and OE output
- In accordance with the USB 2.0 Specification, the supported transfer speeds are:
  - In Host mode: full-speed and low speed
  - In Device mode: full-speed

2.13.8 Infrared transmitter (IRTMR)

The AT32F435/437 device provides an infrared transmitter solution. The solution is based on the internal connection between TMR10, USART1, or USART2 with TMR11. TMR11 is used to provide the carrier frequency, and TMR10, USART1, or USART2 provides the main signal to be sent. The infrared output signal is available on PB9 or PA13.

To generate infrared remote control signals, TMR10 channel 1 and TMR11 channel 1 must be correctly configured to generate the correct waveform. All standard IR pulse modulation modes can be obtained by programming two timer output compare channels.

2.13.9 Ethernet MAC interface (EMAC)

This peripheral is available only on AT32F437.

The AT32F437 devices provide an IEEE-802.3-2002-compliant media access controller (MAC) for Ethernet LAN communications through an industry-standard media-independent interface (MII) or a reduced media-independent interface (RMII). The AT32F437 requires an external physical interface device (PHY) to connect to the physical LAN bus (twisted-pair, fiber, etc.). The PHY is connected to the AT32F437 EMAC port using as many as 17 signals (MII) or 9 signals (RMII).

The EMAC has the following features:

- Supports 10 M and 100 Mbit/s rates
- Dedicated DMA controller enabling high-speed transfers between the dedicated buffer and the descriptors
- Supports tagged MAC frame (VLAN support)
- Half-duplex (CSMA/CD) and full-duplex operation
- MAC control sublayer (control frames) support
- 32-bit CRC generation and removal
- Several address filtering modes for physical and multicast address (multicast and group addresses)
- 32-bit status code for each transmitted or received frame
- Internal buffer for transmitted and received frames. The transmit buffer and the receive buffer are both 2 Kbytes, that is, 4 Kbytes in total
- Supports hardware PTP (precision time protocol) in line with IEEE 1588 with the timestamp comparator connected to the TMR2 trigger input
- Interrupt trigger when system time becomes greater than the target time

2.14 Digital video parallel interface (DVP)

AT32F435/437 series embed a digital video parallel interface (DVP), which connects to a digital camera module and receives video data via an 8- to 14-bit parallel interface. The DVP supports a data rate up to 54 MB/s. It has the following features:

- Configurable polarity of the input pixel clock and synchronous signals
- 8-, 10-, 12- or 14-bit communication data width
- Support 8-bit raster-scan mono or Bayer format, YCbCr 4:2:2 raster-scan, RGB 565 raster-scan, or compressed data (such as JPEG)
- Continuous mode or snapshot (one frame) mode
- Automatic image cropping
- Mono-image binarization

2.15 Cyclic redundancy check (CRC) calculation unit

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code from a 32-bit data word using a fixed generator polynomial. Among other applications, CRC-based techniques are used to verify data transmission or storage integrity.

2.16 Analog-to-digital converter (ADC)

Three 12-bit analog-to-digital converters (ADC) are embedded into AT32F435/437 devices and feature as follows:

- Configurable 12-bit, 10-bit, 8-bit, 6-bit resolution with auto calibration.
- 5.33 MSPS maximum conversion rate in 12-bit resolution, the reduction of resolution shortens the conversion period.
- Share up to 24 external channels, including 6 fast channels.
- Three internal dedicated channels: internal temperature sensor (V_{TS}), internal reference voltage (V_{INTRV}), and V_{BAT} monitor ($V_{BAT}/4$).
- Individual sampling time setting for each channel.
- 2 to 256 times over-sampling, equivalent maximum 16-bit resolution.
- Conversion can be triggered by:
  - Software.
  - Hardware (internal or GPIO input events) with polarity configurability.
- Converting modes:
  - Single mode or sequential mode.
  - In sequential mode, each trigger performs conversions on a selected group of channels.
  - Repeated mode converts selected channels continuously.
  - Partition mode.
- Simultaneous or shift sample and hold under one- or two-slave mode.
- A voltage monitor feature allows very precise monitoring of the converted voltage of one, some or all selected channels. An interrupt is generated when the converted voltage is outside the programmed thresholds.
- All ADCs can be served by the DMA controller.

2.16.1 Temperature sensor (V_{TS})

The temperature sensor generates a voltage V_{TS} that varies linearly with temperature. The temperature sensor is internally connected to the ADC1_IN16 input channel which is used to convert the sensor output voltage into a digital value.

The offset of this line varies from chip to chip due to process variation. The internal temperature sensor is more suited to applications that detect temperature variations instead of absolute temperatures. If accurate temperature readings are needed, an external temperature sensor part should be used.

2.16.2 Internal reference voltage (V_{INTRV})

The internal reference voltage (V_{INTRV}) provides a stable voltage source for ADC. The V_{INTRV} is internally connected to the ADC1_IN17 input channel.

2.16.3 V_{BAT} monitor ($V_{BAT}/4$)

This embedded hardware uses internal ADC1_IN18 channel to measure V_{BAT} voltage. As the V_{BAT} voltage may be higher than V_{REF+} or V_{DDA} to be outside the ADC input range, the V_{BAT} is internally connected to a divided-by-4 bridge. The converted value is 1/4 of the V_{BAT} voltage.

2.17 Digital-to-analog converter (DAC)

The two 12-bit buffered DACs can be used to convert two digital signals into two analog voltage signal outputs.

This DAC has the following features:

- Two DAC converters: one for each output channel
- 8-bit or 12-bit monotonic output
- Left- or right-aligned data in 12-bit mode
- Synchronized update capability
- Noise-wave generation
- Triangular-wave generation
- Dual DAC channel independent or simultaneous conversions
- DMA capability for each DAC channel
- External triggers for conversion
- Input voltage reference V_{REF+}

Several DAC trigger inputs are used in the AT32F435/437. DAC outputs are triggered through the timer update outputs that are also connected to different DMA channels.

2.18 Serial wire (SWD) / JTAG debug port

The ARM SWJ-DP Interface is embedded, and it is a combined serial wire and JTAG and debug port that enables either a serial wire debug or a JTAG probe to be connected to the target for programming and debug operation. The JTAG TMS and TCK pins are shared respectively with SWDIO and SWCLK.

3 Pin functional definitions

Figure 2. AT32F435/437 LQFP144 pinout

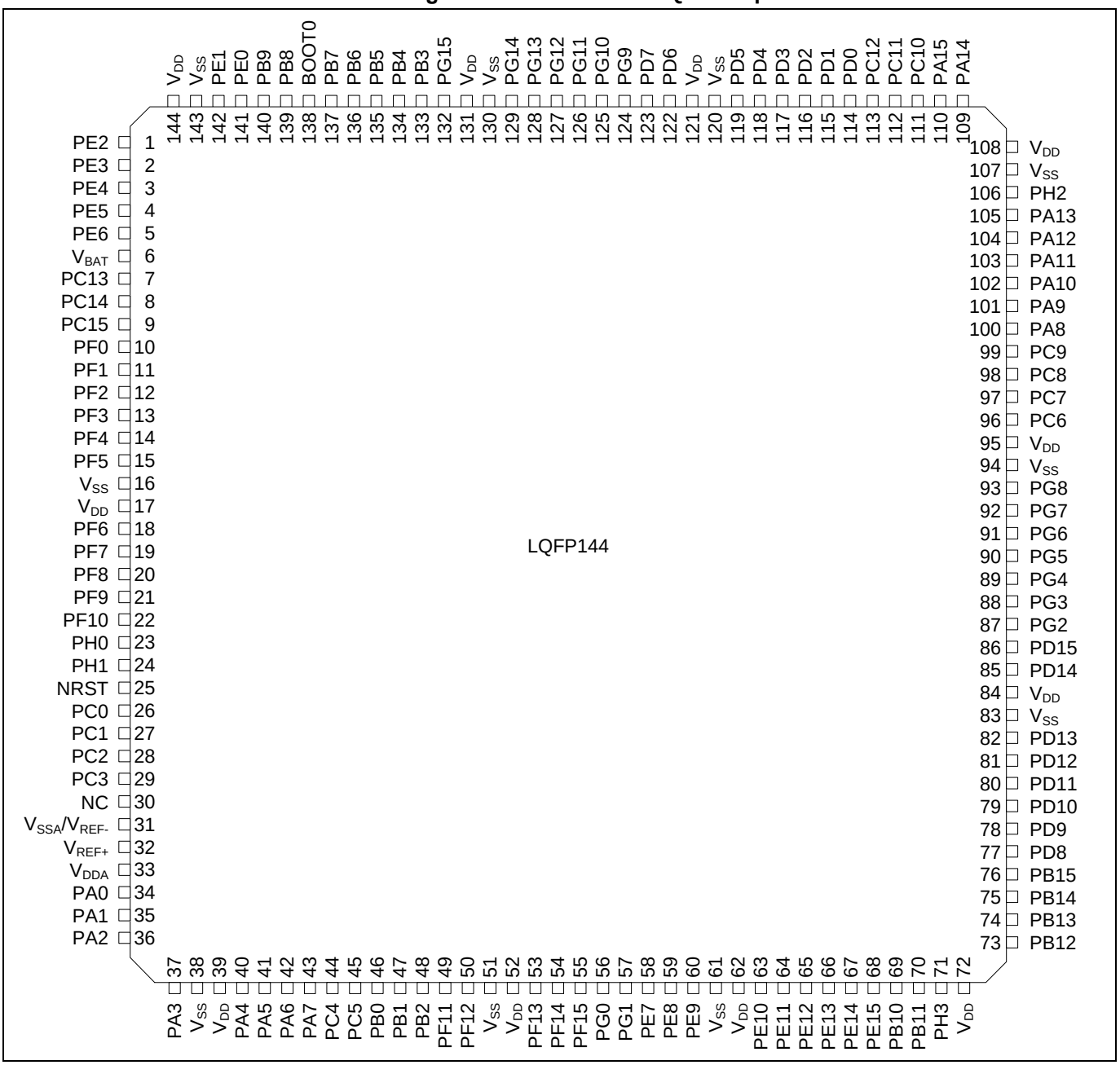


Figure 3. AT32F435/437 LQFP100 pinout

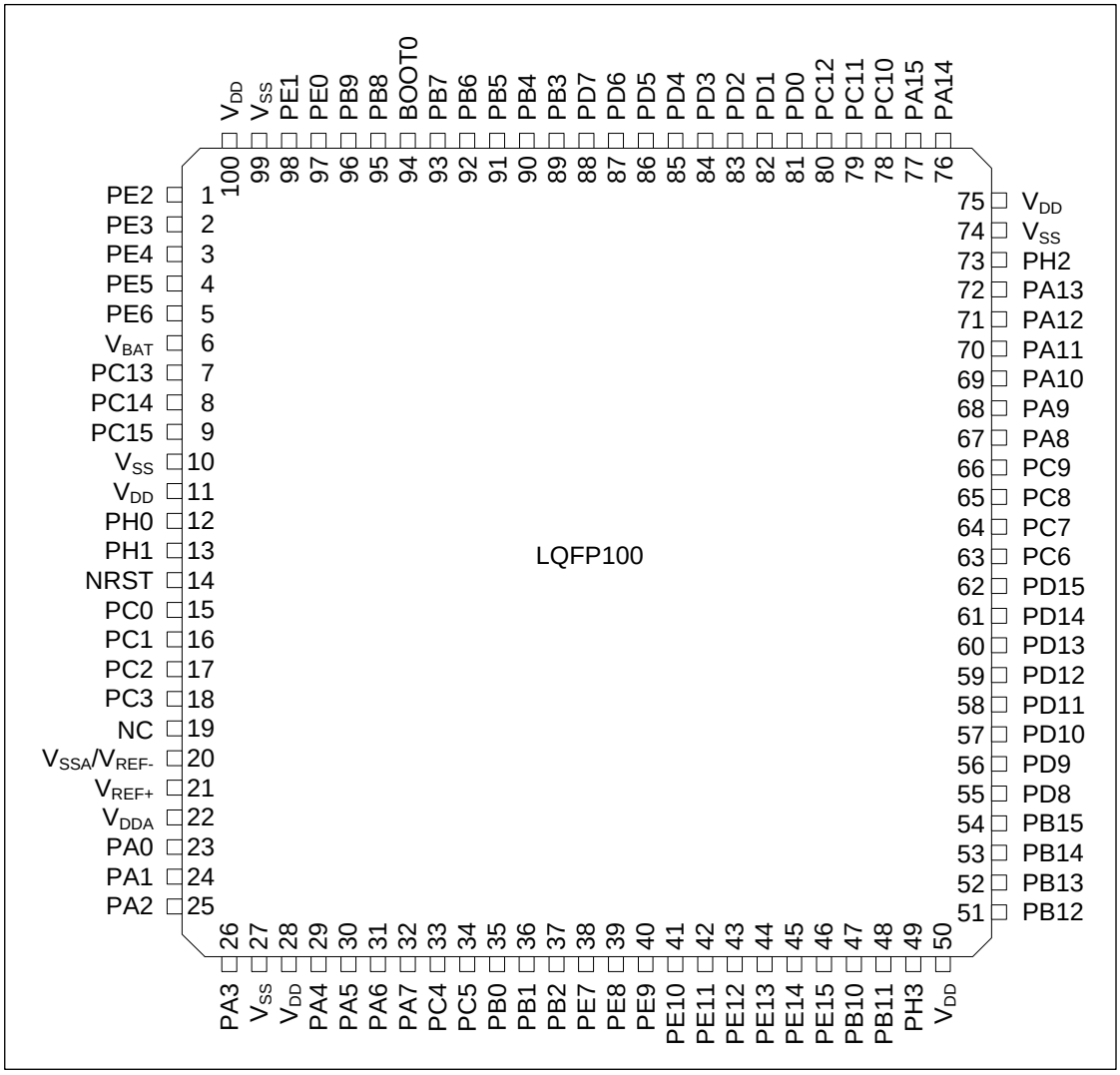


Figure 4. AT32F435/437 BGA100 solder ball array

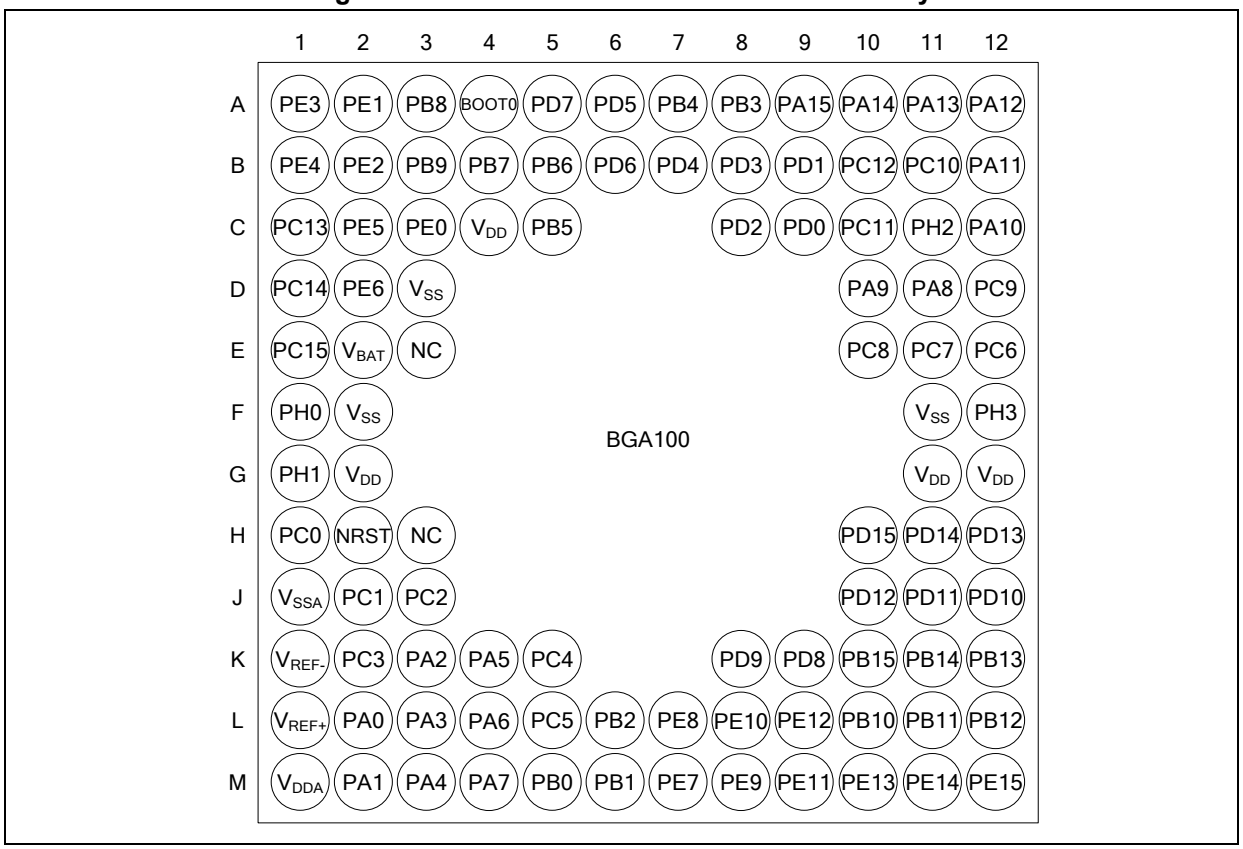


Figure 5. AT32F435/437 LQFP64 pinout

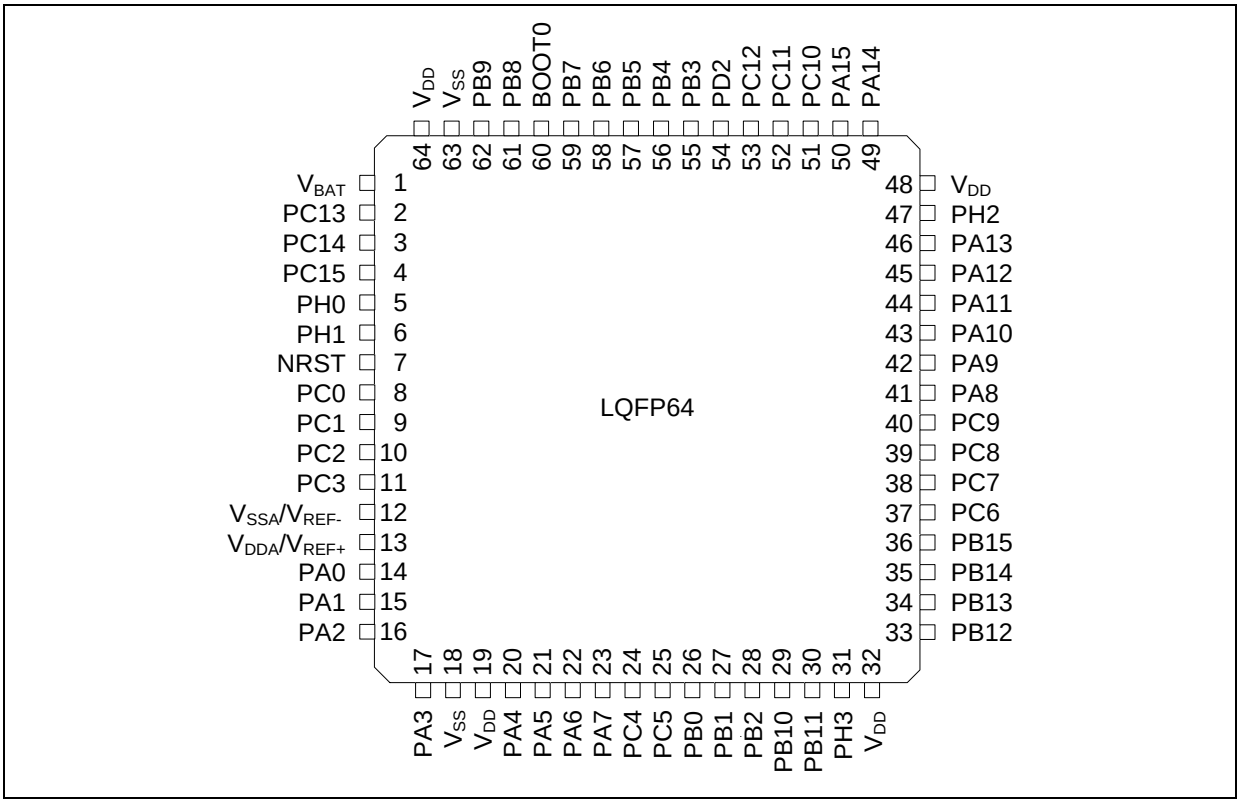


Figure 6. AT32F435 LQFP48 pinout

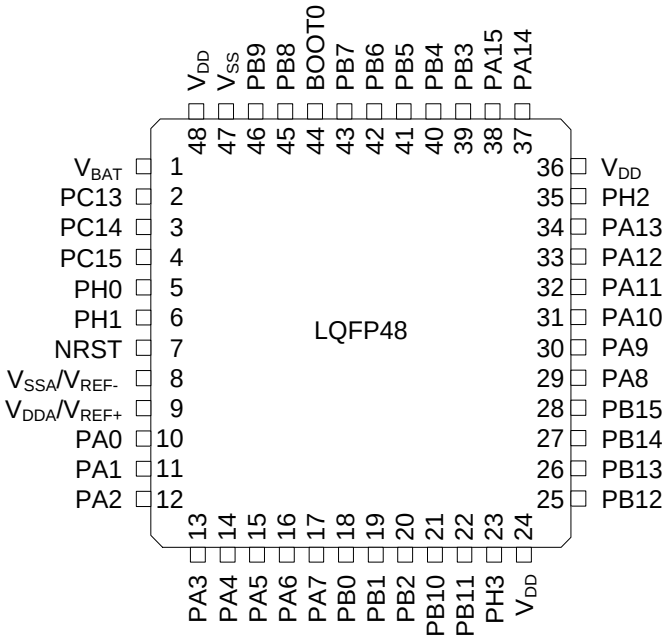
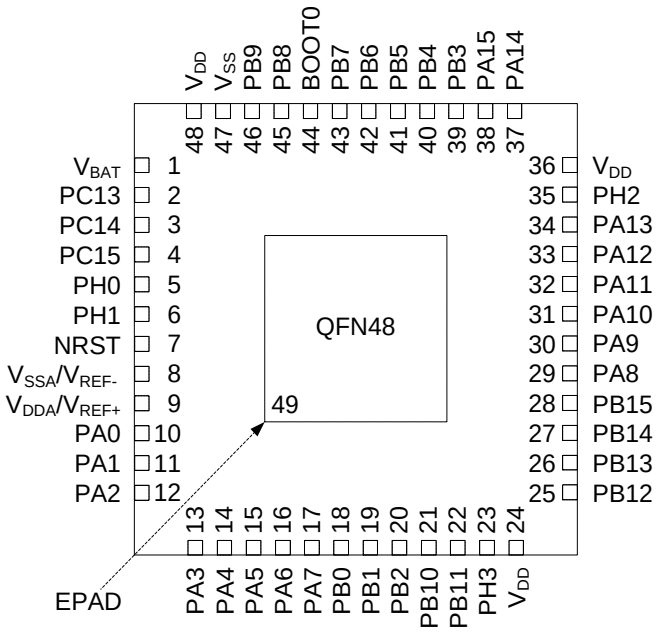


Figure 7. AT32F435 QFN48 pinout



The table below is the pin definition of the AT32F435/437. "-" represents there is no such pinout on the related packages. Unless descriptions in () under pin name, the function during reset and after reset is the same as the actual pin name. Unless notes presented, all GPIOs are set as input floating during reset and after reset. Pin multi-functions are selected through GPIOx_MUXx registers and the additional functions are directly selected and enabled via registers of peripherals.

Table 8. AT32F435/437 series pin and solder ball definitions

Pin number or solder ball coordinate					Pin name (function after reset)	Pin type[1]	GPIO structure[2]	IOMUX functions[3]	Additional function
LQFP48 / QFN48	LQFP64	BGA100	LQFP100	LQFP144					
-	-	B2	1	1	PE2	I/O	FT	TMR3_EXT / SPI4_SCK / I2S4_CK / TMR20_CH1 / QSPI1_IO2 / XMC_SDNCAS / EMAC_MII_TXD3 / XMC_A23	-
-	-	A1	2	2	PE3	I/O	FT	TMR3_CH1 / TMR20_CH2 / XMC_A19 / DVP_D9	-
-	-	B1	3	3	PE4	I/O	FT	CLKOUT1 / TMR3_CH2 / SPI4_CS / I2S4_WS / TMR20_CH1C / XMC_A20 / DVP_D4	-
-	-	C2	4	4	PE5	I/O	FT	TMR3_CH3 / TMR9_CH1 / SPI4_MISO / TMR20_CH2C / XMC_A21 / DVP_D6	-
-	-	D2	5	5	PE6	I/O	FT	TMR3_CH4 / TMR9_CH2 / SPI4_MOSI / I2S4_SD / TMR20_CH3C / XMC_SDNRAS / XMC_A22 / DVP_D7	-
1	1	E2	6	6	V_{BAT}	S	-	Battery power supply	
2	2	C1	7	7	PC13[4][5]	I/O	FT	-	ERTC_AF1 / WKUP2
3	3	D1	8	8	PC14 / LEXT_IN (PC14)[4][5]	I/O	TC	-	LEXT_IN
4	4	E1	9	9	PC15 / LEXT_OUT (PC15)[4][5]	I/O	TC	-	LEXT_OUT
-	-	-	-	10	PF0	I/O	FT	I2C2_SDA / XMC_A0	-
-	-	-	-	11	PF1	I/O	FT	I2C2_SCL / XMC_A1	-
-	-	-	-	12	PF2	I/O	FT	TMR20_CH3 / I2C2_SMBA / XMC_A2	-
-	-	-	-	13	PF3	I/O	FTa	TMR20_CH4 / XMC_A3	ADC3_IN9
-	-	-	-	14	PF4	I/O	FTa	TMR20_CH1C / XMC_A4	ADC3_IN14
-	-	-	-	15	PF5	I/O	FTa	TMR20_CH2C / XMC_A5	ADC3_IN15
-	-	F2	10	16	V_{SS}	S	-	Digital ground	
-	-	G2	11	17	V_{DD}	S	-	Digital power supply	
-	-	-	-	18	PF6	I/O	FTa	TMR10_CH1 / TMR20_CH4 / UART7_RX / QSPI1_IO3 / XMC_NIORD	ADC3_IN4
-	-	-	-	19	PF7	I/O	FTa	TMR11_CH1 / TMR20_BRK / UART7_TX / QSPI1_IO2 / XMC_NREG	ADC3_IN5
-	-	-	-	20	PF8	I/O	FTa	TMR13_CH1 / QSPI1_IO0 / XMC_NIOWR	ADC3_IN6
-	-	-	-	21	PF9	I/O	FTa	TMR14_CH1 / TMR20_BRK / QSPI1_IO1 / XMC_CD	ADC3_IN7
-	-	-	-	22	PF10	I/O	FTa	TMR1_EXT / TMR5_CH4 / QSPI1_SCK / XMC_INTR / DVP_D11	ADC3_IN8

Pin number or solder ball coordinate					Pin name (function after reset)	Pin type[1]	GPIO structure[2]	IOMUX functions[3]	Additional function
LQFP48 / QFN48	LQFP64	BGA100	LQFP100	LQFP144					
5	5	F1	12	23	PH0 / HEXT_IN (PH0)	I/O	TC	I2C1_SDA	HEXT_IN
6	6	G1	13	24	PH1 / HEXT_OUT (PH1)	I/O	TC	I2C1_SCL	HEXT_OUT
7	7	H2	14	25	NRST	I/O	R	Device reset input / internal reset output (active low)	
-	8	H1	15	26	PC0	I/O	FTa	I2C3_SCL / UART7_TX / SDIO2_D0 / XMC_SDNWE	ADC123_IN10[6]
-	9	J2	16	27	PC1	I/O	FTa	I2C3_SDA / SPI3_MOSI / I2S3_SD / SPI2_MOSI / I2S2_SD / UART7_RX SDIO2_D1 / EMAC_MDC	ADC123_IN11[6]
-	10	J3	17	28	PC2	I/O	FTa	TMR20_CH2 / SPI2_MISO / I2S2_SDEXT / UART8_TX / SDIO2_D2 / EMAC_MII_TXD2 / XMC_SDCS0 / XMC_NWE	ADC123_IN12[6]
-	11	K2	18	29	PC3	I/O	FTa	SPI2_MOSI / I2S2_SD / UART8_RX / QSPI2_IO1 / SDIO2_D3 / EMAC_MII_TX_CLK / XMC_SDCKE0 / XMC_A0	ADC123_IN13[6]
-	-	-	19	30	Not connected				
-	-	J1	-	-	V_{SSA}	S	-	Analog ground	
-	-	K1	-	-	V_{REF-}	S	-	Negative reference voltage	
8	12	-	20	31	V_{SSA} / V_{REF-}	S	-	Analog ground / negative reference voltage	
-	-	L1	21	32	V_{REF+}	S	-	Positive reference voltage	
-	-	M1	22	33	V_{DDA}	S	-	Analog power supply	
9	13	-	-	-	V_{DDA} / V_{REF+}	S	-	Analog power supply / positive reference voltage	
10	14	L2	23	34	PA0	I/O	FTa	TMR2_CH1 / TMR2_EXT / TMR5_CH1 / TMR8_EXT / I2C2_SCL / USART2_CTS / UART4_TX / EMAC_MII_CRS	ADC123_IN0[6] / ERTC_AF2 / WKUP1
11	15	M2	24	35	PA1	I/O	FTa	TMR2_CH2 / TMR5_CH2 / I2C2_SDA / SPI4_MOSI / I2S4_SD / USART2_RTS_DE / UART4_RX / QSPI1_IO3 / EMAC_MII_RX_CLK / EMAC_RMII_REF_CLK	ADC123_IN1[6]
12	16	K3	25	36	PA2	I/O	FTa	TMR2_CH3 / TMR5_CH3 / TMR9_CH1 / USART2_TX / SDIO2_CK / EMAC_MDIO / XMC_D4	ADC123_IN2
13	17	L3	26	37	PA3	I/O	FTa	TMR2_CH4 / TMR5_CH4 / TMR9_CH2 / I2S2_MCK / USART2_RX / QSPI2_IO3 / SDIO2_CMD / EMAC_MII_COL / XMC_D5	ADC123_IN3
-	18	-	27	38	V_{SS}	S	-	Digital ground	
-	19	-	28	39	V_{DD}	S	-	Digital power supply	
-	-	E3	-	-	Not connected				
-	-	H3	-	-	Not connected				

Pin number or solder ball coordinate					Pin name (function after reset)	Pin type[1]	GPIO structure[2]	IOMUX functions[3]	Additional function
LQFP48 / QFN48	LQFP64	BGA100	LQFP100	LQFP144					
14	20	M3	29	40	PA4	I/O	FTa	SPI1_CS / I2S1_WS / SPI3_CS / I2S3_WS / USART2_CK / USART6_TX / SDIO2_D4 / SDIO2_D0 / OTGFS2_SOF / DVP_HSYNC / XMC_D6	ADC12_IN4 / DAC1_OUT
15	21	K4	30	41	PA5	I/O	FTa	TMR2_CH1 / TMR2_EXT / TMR8_CH1C / SPI1_SCK / I2S1_CK / USART6_RX / QSPI2_IO2 / SDIO2_D5 / SDIO2_D1 / XMC_D7	ADC12_IN5 / DAC2_OUT
16	22	L4	31	42	PA6	I/O	FTa	TMR1_BRK / TMR3_CH1 / TMR8_BRK / SPI1_MISO / I2S2_MCK / USART3_CTS / TMR13_CH1 / QSPI1_IO0 / SDIO2_D2 / SDIO1_CMD / DVP_PCLK / SDIO2_D6	ADC12_IN6
17	23	M4	32	43	PA7	I/O	FTa	TMR1_CH1C / TMR3_CH2 / TMR8_CH1C / SPI1_MOSI / I2S1_SD / TMR14_CH1 / QSPI1_IO1 / EMAC_MII_RX_DV / EMAC_RMII_CRS_DV / XMC_SDNWE / SDIO2_D3 / SDIO2_D7	ADC12_IN7
-	24	K5	33	44	PC4	I/O	FTa	TMR9_CH1 / I2S1_MCK / USART3_TX / QSPI1_IO2 / EMAC_MII_RXD0 / EMAC_RMII_RXD0 / XMC_SDCS0 / SDIO2_CK / XMC_NE4	ADC12_IN14
-	25	L5	34	45	PC5	I/O	FTa	TMR9_CH2 / I2C1_SMBA / USART3_RX / QSPI1_IO3 / EMAC_MII_RXD1 / EMAC_RMII_RXD1 / XMC_SDCKE0 / SDIO2_CMD / XMC_NOE	ADC12_IN15
18	26	M5	35	46	PB0	I/O	FTa	TMR1_CH2C / TMR3_CH3 / TMR8_CH2C / I2S1_MCK / USART2_RX / SPI3_MOSI / I2S3_SD / USART3_CK / QSPI2_IO0 / QSPI1_IO0 / EMAC_MII_RXD2 / SDIO1_D1	ADC12_IN8
19	27	M6	36	47	PB1	I/O	FTa	TMR1_CH3C / TMR3_CH4 / TMR8_CH3C / SPI2_SCK / I2S2_CK / USART3_RTS_DE / QSPI1_SCK / QSPI2_SCK / EMAC_MII_RXD3 / SDIO1_D2	ADC12_IN9
20	28	L6	37	48	PB2 / BOOT1 (PB2)	I/O	FT	TMR2_CH4 / TMR20_CH1 / I2C3_SMBA / SPI3_MOSI / I2S3_SD / QSPI1_SCK / SDIO1_CK	-
-	-	-	-	49	PF11	I/O	FT	TMR20_EXT / TMR8_EXT / XMC_SDNRAS / DVP_D12	-
-	-	-	-	50	PF12	I/O	FT	TMR20_CH1 / TMR8_BRK / XMC_A6	-
-	-	-	-	51	V_{SS}	S	-	Digital ground	
-	-	-	-	52	V_{DD}	S	-	Digital power supply	
-	-	-	-	53	PF13	I/O	FT	TMR20_CH2 / I2C3_SMBA / XMC_A7	-
-	-	-	-	54	PF14	I/O	FTf	TMR20_CH3 / I2C3_SCL / XMC_A8	-
-	-	-	-	55	PF15	I/O	FTf	TMR20_CH4 / I2C3_SDA / XMC_A9	-

Pin number or solder ball coordinate					Pin name (function after reset)	Pin type(1)	GPIO structure(2)	IOMUX functions(3)	Additional function
LQFP48 / QFN48	LQFP64	BGA100	LQFP100	LQFP144					
-	-	-	-	56	PG0	I/O	FT	TMR20_CH1C / SPI1_MISO / CAN1_RX / XMC_A10	-
-	-	-	-	57	PG1	I/O	FT	TMR20_CH2C / SPI1_MOSI / I2S1_SD / CAN1_TX / XMC_A11	-
-	-	M7	38	58	PE7	I/O	FT	TMR1_EXT / UART7_RX / QSPI2_IO0 / XMC_D4	-
-	-	L7	39	59	PE8	I/O	FT	TMR1_CH1C / UART4_TX / UART7_TX / QSPI2_IO1 / XMC_D5	-
-	-	M8	40	60	PE9	I/O	FT	TMR1_CH1 / UART4_RX / QSPI2_IO2 / XMC_D6	-
-	-	-	-	61	V_{SS}	S	-	Digital ground	
-	-	-	-	62	V_{DD}	S	-	Digital power supply	
-	-	L8	41	63	PE10	I/O	FT	TMR1_CH2C / UART5_TX / QSPI2_IO3 / XMC_D7	-
-	-	M9	42	64	PE11	I/O	FT	TMR1_CH2 / SPI4_CS / I2S4_WS / UART5_RX / XMC_D8	-
-	-	L9	43	65	PE12	I/O	FT	TMR1_CH3C / SPI1_CS / I2S1_WS / SPI4_SCK / I2S4_CK / XMC_D9	-
-	-	M10	44	66	PE13	I/O	FT	TMR1_CH3 / SPI1_SCK / I2S1_CK / SPI4_MISO / XMC_D10	-
-	-	M11	45	67	PE14	I/O	FT	TMR1_CH4 / SPI1_MISO / SPI4_MOSI / I2S4_SD / XMC_D11	-
-	-	M12	46	68	PE15	I/O	FT	TMR1_BRK / SPI1_MOSI / I2S1_SD / XMC_D12	-
21	29	L10	47	69	PB10	I/O	FTf	TMR2_CH3 / I2C2_SCL / SPI2_SCK / I2S2_CK / I2S3_MCK / USART3_TX / QSPI1_CS / QSPI1_IO1 / EMAC_MII_RX_ER / SDIO1_D7 / XMC_NOE	-
22	30	L11	48	70	PB11	I/O	FT	TMR2_CH4 / TMR5_CH4 / I2C2_SDA / USART3_RX / QSPI1_IO0 / EMAC_MII_TX_EN / EMAC_RMII_TX_EN	-
23	31	F12	49	71	PH3	I/O	FT	TMR5_CH2 / I2C2_SDA / UART4_TX / QSPI1_IO1	-
24	32	G12	50	72	V_{DD}	S	-	Digital power supply	
25	33	L12	51	73	PB12	I/O	FT	TMR1_BRK / TMR5_CH1 / I2C2_SMBA / SPI2_CS / I2S2_WS / SPI4_CS / I2S4_WS / SPI3_SCK / I2S3_CK / USART3_CK / CAN2_RX / EMAC_MII_TXD0 / EMAC_RMII_TXD0 / OTGFS2_ID / XMC_D13	-
26	34	K12	52	74	PB13	I/O	FT	TMR1_CH1C / I2C3_SMBA / SPI2_SCK / I2S2_CK / SPI4_SCK / I2S4_CK / I2C3_SCL / USART3_CTS / CAN2_TX / EMAC_MII_TXD1 / EMAC_RMII_TXD1 / OTGFS2_VBUS	-

Pin number or solder ball coordinate					Pin name (function after reset)	Pin type(1)	GPIO structure(2)	IOMUX functions(3)	Additional function
LQFP48 / QFN48	LQFP64	BGA100	LQFP100	LQFP144					
27	35	K11	53	75	PB14	I/O	TC	TMR1_CH2C / TMR8_CH2C / I2C3_SDA / SPI2_MISO / I2S2_SDEXT / USART3_RTS_DE / TMR12_CH1 / OTGFS2_D- / SDIO1_D6 / XMC_D0	-
28	36	K10	54	76	PB15	I/O	TC	ERTC_REFIN / TMR1_CH3C / TMR8_CH3C / I2C3_SCL / SPI2_MOSI / I2S2_SD / TMR12_CH2 / OTGFS2_D+ / SDIO1_CK	-
-	-	K9	55	77	PD8	I/O	FT	USART3_TX / EMAC_MII_RX_DV / EMAC_RMII_CRS_DV / XMC_D13	-
-	-	K8	56	78	PD9	I/O	FT	USART3_RX / EMAC_MII_RXD0 / MAC_RMII_RXD0 / XMC_D14	-
-	-	J12	57	79	PD10	I/O	FT	USART3_CK / EMAC_MII_RXD1 / EMAC_RMII_RXD1 / XMC_D15	-
-	-	J11	58	80	PD11	I/O	FT	I2C2_SMBA / USART3_CTS / QSPI1 _IO0 / XMC_A14 / XMC_SDBA0 / EMAC_MII_RXD2 / XMC_A16_CLE	-
-	-	J10	59	81	PD12	I/O	FTf	TMR4_CH1/ I2C2_SCL / USART3_RTS_DE / QSPI1 _IO1 / XMC_A15 / XMC_SDBA1 / EMAC_MII_RXD3 / XMC_A17_ALE	-
-	-	H12	60	82	PD13	I/O	FTf	TMR4_CH2/ I2C2_SDA / UART8_TX / QSPI1_IO3 / XMC_SDCLK / XMC_A18	-
-	-	-	-	83	V_{SS}	S	-	Digital ground	
-	-	-	-	84	V_{DD}	S	-	Digital power supply	
-	-	H11	61	85	PD14	I/O	FTf	TMR4_CH3 / I2C3_SCL / UART8_RX / XMC_D0	-
-	-	H10	62	86	PD15	I/O	FTf	TMR4_CH4 / I2C3_SDA / XMC_D1	-
-	-	-	-	87	PG2	I/O	FT	TMR20_CH3C / XMC_A12	-
-	-	-	-	88	PG3	I/O	FT	TMR20_BRK / XMC_A13	-
-	-	-	-	89	PG4	I/O	FT	XMC_A14 / XMC_SDBA0	-
-	-	-	-	90	PG5	I/O	FT	TMR20_EXT / XMC_A15 / XMC_SDBA1	-
-	-	-	-	91	PG6	I/O	FT	QSPI1_CS / XMC_INT2 / DVP_D12	-
-	-	-	-	92	PG7	I/O	FT	USART6_CK / XMC_INT3 / DVP_D13	-
-	-	-	-	93	PG8	I/O	FT	QSPI2_CS / USART6_RTS_DE / EMAC_PPS_OUT / XMC_SDCLK	-
-	-	-	-	94	V_{SS}	S	-	Digital ground	
-	-	-	-	95	V_{DD}	S	-	Digital power supply	
-	37	E12	63	96	PC6	I/O	FT	TMR3_CH1 / TMR8_CH1 / I2C1_SCL / I2S2_MCK / USART6_TX / XMC_A0 / SDIO1_D6 / DVP_D0 / XMC_D1	-
-	38	E11	64	97	PC7	I/O	FT	TMR3_CH2 / TMR8_CH2 / I2C1_SDA / SPI2_SCK / I2S2_CK / I2S3_MCK / USART6_RX / XMC_A1 / SDIO1_D7 / DVP_D1	-

Pin number or solder ball coordinate					Pin name (function after reset)	Pin type[1]	GPIO structure[2]	IOMUX functions[3]	Additional function
LQFP48 / QFN48	LQFP64	BGA100	LQFP100	LQFP144					
-	39	E10	65	98	PC8	I/O	FT	TMR3_CH3 / TMR8_CH3 / I2S4_MCK / TMR20_CH3 / UART8_TX / USART6_CK / QSPI1_IO2 / XMC_A2 / SDIO1_D0 / DVP_D2	-
-	40	D12	66	99	PC9	I/O	FT	CLKOUT2 / TMR3_CH4 / TMR8_CH4 / I2C3_SDA / UART8_RX / QSPI1_IO0 / XMC_A3 / OTGFS2_OE / SDIO1_D1 / DVP_D3	-
29	41	D11	67	100	PA8	I/O	FT	CLKOUT1 / TMR1_CH1 / I2C3_SCL / USART1_CK / USART2_TX / OTGFS1_SOF / SDIO1_D1 / XMC_A4	-
30	42	D10	68	101	PA9	I/O	FT	TMR1_CH2 / I2C3_SMBA / SPI2_SCK / I2S2_CK / USART1_TX / I2C1_SCL / OTGFS1_VBUS / SDIO1_D2 / DVP_D0	-
31	43	C12	69	102	PA10	I/O	FT	TMR1_CH3 / SPI2_MOSI / I2S2_SD / I2S4_MCK / USART1_RX / I2C1_SDA / OTGFS1_ID / DVP_D1	-
32	44	B12	70	103	PA11	I/O	TC	TMR1_CH4 / I2C2_SCL / SPI2_CS / I2S2_WS / SPI4_MISO / USART1_CTS / USART6_TX / CAN1_RX / OTGFS1_D- / DVP_D2	-
33	45	A12	71	104	PA12	I/O	TC	TMR1_EXT / I2C2_SDA / SPI2_MISO / USART1_RTS_DE / USART6_RX / CAN1_TX / OTGFS1_D+ / DVP_D3	-
34	46	A11	72	105	PA13 (JTMS / SWDIO)	I/O	FT	JTMS / SWDIO / IR_OUT / SPI3_MISO / OTGFS1_OE	-
35	47	C11	73	106	PH2	I/O	FT	TMR5_CH1/ I2C2_SCL / UART4_RX / QSPI1_IO0	-
-	-	F11	74	107	V_{SS}	S	-	Digital ground	
36	48	G11	75	108	V_{DD}	S	-	Digital power supply	
37	49	A10	76	109	PA14 (JTCK / SWCLK)	I/O	FT	JTCK / SWCLK / SPI3_MOSI / I2S3_SD / USART2_TX	-
38	50	A9	77	110	PA15 (JTDI)	I/O	FT	JTDI / TMR2_CH1 / TMR2_EXT / SPI1_CS / I2S1_WS / SPI3_CS / I2S3_WS / USART1_TX / USART2_RX / QSPI2 _IO1 / QSPI1_IO2 / XMC_NE2 / XMC_NCE3	-
-	51	B11	78	111	PC10	I/O	FT	TMR5_CH2 / SPI3_SCK / I2S3_CK / USART3_TX / UART4_TX / QSPI1 _IO1 / SDIO1_D2 / DVP_D8	-
-	52	C10	79	112	PC11	I/O	FT	TMR5_CH3 / I2S3_SDEXT / SPI3_MISO / USART3_RX / UART4_RX / QSPI1_CS / SDIO1_D3 / DVP_D4 / XMC_D2	-
-	53	B10	80	113	PC12	I/O	FT	TMR11_CH1 / I2C2_SDA / SPI3_MOSI / I2S3_SD / USART3_CK / UART5_TX / SDIO1_CK / DVP_D9 / XMC_D3	-

Pin number or solder ball coordinate					Pin name (function after reset)	Pin type(1)	GPIO structure(2)	IOMUX functions(3)	Additional function
LQFP48 / QFN48	LQFP64	BGA100	LQFP100	LQFP144					
-	-	C9	81	114	PD0	I/O	FT	SPI4_MISO/ SPI3_MOSI / I2S3_SD / SPI2_CS / I2S2_WS / CAN1_RX / XMC_A5 / XMC_D2	-
-	-	B9	82	115	PD1	I/O	FT	SPI2_SCK / I2S2_CK / SPI2_CS / I2S2_WS / CAN1_TX / XMC_A6 / XMC_D3	-
-	54	C8	83	116	PD2	I/O	FT	TMR3_EXT / USART3_RTS_DE / UART5_RX / XMC_A7 / SDIO1_CMD / DVP_D11 / XMC_NWE	-
-	-	B8	84	117	PD3	I/O	FT	SPI2_SCK / I2S2_CK / SPI2_MISO / USART2_CTS / QSPI1_SCK / XMC_A8 / XMC_CLK / DVP_D5	-
-	-	B7	85	118	PD4	I/O	FT	SPI2_MOSI / I2S2_SD / USART2_RTS_DE / XMC_A9 / XMC_NOE	-
-	-	A6	86	119	PD5	I/O	FT	USART2_TX / XMC_A10 / XMC_NWE	-
-	-	-	-	120	V_{SS}	S	-	Digital ground	
-	-	-	-	121	V_{DD}	S	-	Digital power supply	
-	-	B6	87	122	PD6	I/O	FT	SPI3_MOSI / I2S3_SD / USART2_RX / XMC_A11 / XMC_NWAIT / DVP_D10	-
-	-	A5	88	123	PD7	I/O	FT	USART2_CK / XMC_A12 / XMC_NE1 / XMC_NCE2	-
-	-	-	-	124	PG9	I/O	FT	USART6_RX / QSPI1_IO2 / XMC_NE2 / XMC_NCE3 / DVP_VSYNC	-
-	-	-	-	125	PG10	I/O	FT	QSPI2_IO2 / XMC_NE3 / XMC_NCE4_1 / DVP_D2	-
-	-	-	-	126	PG11	I/O	FT	QSPI2_IO3 / SPI4_SCK / I2S4_CK / CAN2_RX / EMAC_MII_TX_EN / EMAC_RMII_TX_EN / XMC_NCE4_2 / DVP_D3	-
-	-	-	-	127	PG12	I/O	FT	QSPI2_IO1 / SPI4_MISO / USART6_RTS_DE / CAN2_TX / XMC_NE4	-
-	-	-	-	128	PG13	I/O	FT	QSPI2_SCK / SPI4_MOSI / I2S4_SD / USART6_CTS / EMAC_MII_TXD0 / EMAC_RMII_TXD0 / XMC_A24	-
-	-	-	-	129	PG14	I/O	FT	QSPI2_IO0 / SPI4_CS / I2S4_WS / USART6_TX / QSPI1_IO3 / EMAC_MII_TXD1 / EMAC_RMII_TXD1 / XMC_A25	-
-	-	-	-	130	V_{SS}	S	-	Digital ground	
-	-	-	-	131	V_{DD}	S	-	Digital power supply	
-	-	-	-	132	PG15	I/O	FT	USART6_CTS / XMC_SDNCAS / DVP_D13	-
39	55	A8	89	133	PB3 (JTDO)	I/O	FTf	JTDO / TMR2_CH2 / I2C2_SDA / SPI1_SCK / I2S1_CK / SPI3_SCK / I2S3_CK / USART1_RX / UART7_RX / QSPI1_IO3 / DVP_D4 / SWO	-

Pin number or solder ball coordinate					Pin name (function after reset)	Pin type(1)	GPIO structure(2)	IOMUX functions(3)	Additional function
LQFP48 / QFN48	LQFP64	BGA100	LQFP100	LQFP144					
40	56	A7	90	134	PB4 (NJTRST)	I/O	FT	JNTRST / TMR3_CH1 / I2C3_SDA / SPI1_MISO / SPI3_MISO / I2S3_SDEXT / UART7_TX / SDIO1_D0 / DVP_D5	-
41	57	C5	91	135	PB5	I/O	FT	TMR3_CH2/ I2C1_SMBA / SPI1_MOSI / I2S1_SD / SPI3_MOSI / I2S3_SD / USART1_CK / UART5_RX / CAN2_RX / EMAC_PPS_OUT / XMC_SDCKE1 / DVP_D10 / SDIO1_D3	-
42	58	B5	92	136	PB6	I/O	FT	TMR4_CH1/ I2C1_SCL / I2S1_MCK / SPI4_CS / I2S4_WS / USART1_TX / UART5_TX / CAN2_TX / QSPI1_CS / XMC_SDCS1 / DVP_D5 / SDIO1_D0	-
43	59	B4	93	137	PB7	I/O	FT	TMR4_CH2 / TMR8_BRK / I2C1_SDA / SPI4_SCK / I2S4_CK / USART1_RX / QSPI2_IO1 / XMC_NADV / DVP_VSYNC / SDIO1_D0	-
44	60	A4	94	138	BOOT0	I	B	-	-
45	61	A3	95	139	PB8	I/O	FT	TMR2_CH1 / TMR2_EXT / TMR4_CH3 / TMR10_CH1 / I2C1_SCL / SPI4_MISO / UART5_RX / CAN1_RX / QSPI2_CS / EMAC_MII_TXD3 / SDIO1_D4 / DVP_D6	-
46	62	B3	96	140	PB9	I/O	FTf	IR_OUT / TMR2_CH2 / TMR4_CH4 / TMR11_CH1 / I2C1_SDA / SPI2_CS/I2S2_WS / SPI4_MOSI / I2S4_SD / I2C2_SDA / UART5_TX / CAN1_TX / QSPI1_CS / SDIO1_D5 / DVP_D7	-
-	-	C3	97	141	PE0	I/O	FT	TMR4_EXT / TMR20_EXT / UART8_RX / XMC_LB / XMC_SDDQML / DVP_D2	-
-	-	A2	98	142	PE1	I/O	FT	TMR1_CH2C / TMR20_CH4 / UART8_TX / XMC_UB / XMC_SDDQMH / DVP_D3	-
47	63	D3	99	143	V_{SS}	S	-	Digital ground	
48	64	C4	100	144	V_{DD}	S	-	Digital power supply	
-/49	-	-	-	-	EPAD	S	-	Digital ground	

(1) I = input, O = output, S = supply

(2) TC = standard 3.3 V GPIO, FT = general 5 V-tolerant GPIO, FTa = 5 V-tolerant GPIO with analog functionalities, FTf = 5 V-tolerant GPIO with 20 mA sink current capability, R = bidirectional reset pin with embedded weak pull-up resistor, B = dedicated BOOT0 pin with embedded weak pull-down resistor. Among them, FTa pin has 5 V-tolerant characteristics when configured as input floating, input pull-up, or input pull-down mode. However, it cannot be 5 V-tolerant when configured as analog mode. Meanwhile, its input level should not higher than V_{DD} + 0.3 V.

(3) Function availability depends on the chosen device. Every GPIO can function as EVENTOUT.

(4) PC13, PC14, and PC15 are supplied through the power switch. Since the switch only drives a limited amount of current (3 mA), the use of these three GPIOs as output mode is limited not to be used as a current source (e.g. to drive an LED).

(5) Main function after the first battery powered domain power-up. Later on, it depends on the contents of the battery powered registers even after reset (because these registers are not reset by the main reset). For details on how to manage these GPIOs, refer to the battery powered domain and register description sections in the AT32F435/437 reference manual.

(6) PA0, PA1, PC0, PC1, PC2, and PC3 are ADC fast channels; others are slow channels.

Table 9. XMC pin definition

Pin name	XMC						LQFP100/BGA100	LQFP64
	CF card	SRAM/PSRAM/NOR	Multiplexed PSRAM/NOR	NAND 16-bit	SDRAM(1)			
PF0	A0	A0	-	-	-	A0	-	-
PF1	A1	A1	-	-	-	A1	-	-
PF2	A2	A2	-	-	-	A2	-	-
PF3	A3	A3	-	-	-	A3	-	-
PF4	A4	A4	-	-	-	A4	-	-
PF5	A5	A5	-	-	-	A5	-	-
PF12	A6	A6	-	-	-	A6	-	-
PF13	A7	A7	-	-	-	A7	-	-
PF14	A8	A8	-	-	-	A8	-	-
PF15	A9	A9	-	-	-	A9	-	-
PG0	A10	A10	-	-	-	A10	-	-
PG1	-	A11	-	-	-	A11	-	-
PG2	-	A12	-	-	-	A12	-	-
PG3	-	A13	-	-	-		-	-
PG4	-	A14	-	-	-	SDBA0	-	-
PG5	-	A15	-	-	-	SDBA1	-	-
PD11	-	A14 / A16	A16	- / CLE	SDBA0	-	Yes	-
PD12	-	A15 / A17	A17	- / ALE	SDBA1	-	Yes	-
PD13	-	A18	A18	-	SDCLK	-	Yes	-
PE3	-	A19	A19	-	-		Yes	-
PE4	-	A20	A20	-	-		Yes	-
PE5	-	A21	A21	-	-		Yes	-
PE6	-	A22	A22	-	SDNRAS		Yes	-
PE2	-	A23	A23	-	SDNCAS		Yes	-
PG13	-	A24	A24	-	-		-	-
PG14	-	A25	A25	-	-		-	-
PC3	-	A0	-	-	SDCKE0		Yes	Yes
PC6	A0 / D1	A0 / D1	- / AD1	- / D1	A0	-	Yes	Yes
PC7	A1	A1	-	-	A1	-	Yes	Yes
PC8	A2	A2	-	-	A2	-	Yes	Yes
PC9	A3	A3	-	-	A3	-	Yes	Yes
PA8	A4	A4	-	-	A4	-	Yes	Yes
PD0	A5 / D2	A5 / D2	- / AD2	- / D2	A5	D2	Yes	-
PD1	A6 / D3	A6 / D3	- / AD3	- / D3	A6	D3	Yes	-
PD2	A7 / NWE	A7 / NWE	NWE	NWE	A7	-	Yes	Yes

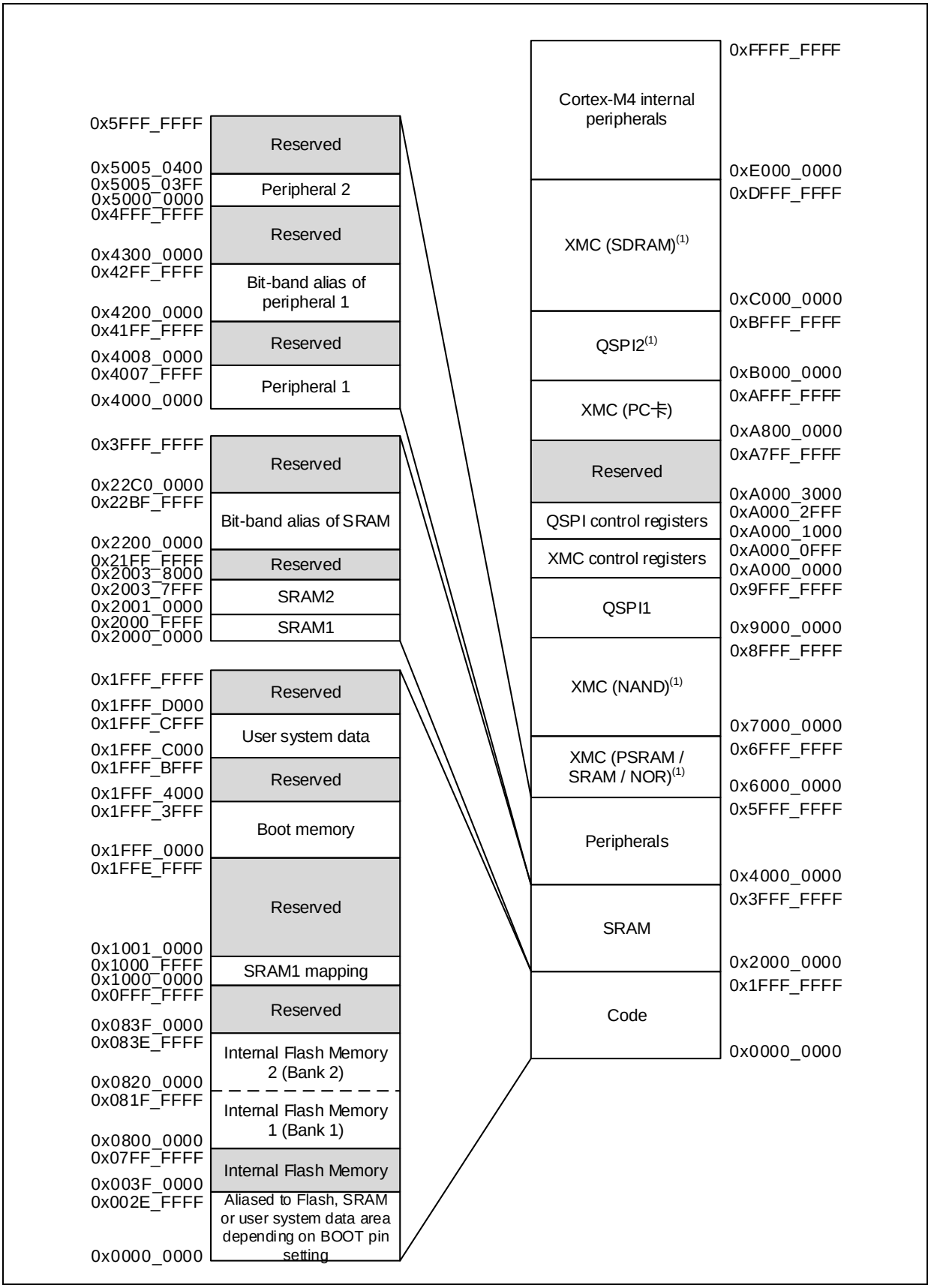
Pin name	XMC						LQFP100/BGA100	LQFP64
	CF card	SRAM/PSRAM/NOR	Multiplexed PSRAM/NOR	NAND 16-bit	SDRAM(1)			
PD3	A8 / -	A8 / CLK	- / CLK	-	A8	-	Yes	-
PD4	A9 / NOE	A9 / NOE	- / NOE	- / NOE	A9	-	Yes	-
PD5	A10 / NWE	A10 / NWE	- / NWE	- / NWE	A10	-	Yes	-
PD6	- / NWAIT	A11 / NWAIT	- / NWAIT	- / NWAIT	A11	-	Yes	-
PD7	-	A12 / NE1	- / NE1	- / NCE2	A12	-	Yes	-
PD14	D0	D0	AD0	D0	D0		Yes	-
PD15	D1	D1	AD1	D1	D1		Yes	-
PE7	D4	D4	AD4	D4	D4		Yes	-
PE8	D5	D5	AD5	D5	D5		Yes	-
PE9	D6	D6	AD6	D6	D6		Yes	-
PE10	D7	D7	AD7	D7	D7		Yes	-
PE11	D8	D8	AD8	D8	D8		Yes	-
PE12	D9	D9	AD9	D9	D9		Yes	-
PE13	D10	D10	AD10	D10	D10		Yes	-
PE14	D11	D11	AD11	D11	D11		Yes	-
PE15	D12	D12	AD12	D12	D12		Yes	-
PD8	D13	D13	AD13	D13	D13		Yes	-
PD9	D14	D14	AD14	D14	D14		Yes	-
PD10	D15	D15	AD15	D15	D15		Yes	-
PB14	D0	D0	AD0	D0	-		Yes	Yes
PC6	D1	D1	AD1	D1	-		Yes	Yes
PC11	D2	D2	AD2	D2	D2	-	Yes	Yes
PC12	D3	D3	AD3	D3	D3	-	Yes	Yes
PA2	D4	D4	AD4	D4	-		Yes	Yes
PA3	D5	D5	AD5	D5	-		Yes	Yes
PA4	D6	D6	AD6	D6	-		Yes	Yes
PA5	D7	D7	AD7	D7	-		Yes	Yes
PB12	D13	D13	AD13	D13	-		Yes	Yes
PD7	-	NE1	NE1	NCE2	-		Yes	-
PG9	-	NE2	NE2	NCE3	-		-	-
PA15	-	NE2	NE2	NCE3	-		Yes	Yes
PG10	NCE4_1	NE3	NE3	-	-		-	-
PG11	NCE4_2	-	-	-	-		-	-
PG12	-	NE4	NE4	-	-		-	-
PC4	-	NE4	NE4	-	SDCS0		Yes	Yes
PB7	-	-	NADV	-	-		Yes	Yes
PB10	NOE	NOE	NOE	NOE	-		Yes	Yes
PC5	NOE	NOE	NOE	NOE	SDCKE0		Yes	Yes

Pin name	XMC					LQFP100/BGA100	LQFP64
	CF card	SRAM/PSRAM/NOR	Multiplexed PSRAM/NOR	NAND 16-bit	SDRAM(1)		
PC2	NWE	NWE	NWE	NWE	SDCS0	Yes	Yes
PF6	NIORD	-	-	-	-	-	-
PF7	NREG	-	-	-	-	-	-
PF8	NIOWR	-	-	-	-	-	-
PF9	CD	-	-	-	-	-	-
PF10	INTR	-	-	-	-	-	-
PG6	-	-	-	INT2	-	-	-
PG7	-	-	-	INT3	-	-	-
PE0	-	LB	LB	-	SDDQML	Yes	-
PE1	-	UB	UB	-	SDDQMH	Yes	-
PG8	-	-	-	-	- SDCLK	-	-
PC0	-	-	-	-	SDNWE	Yes	-
PF11	-	-	-	-	SDNRAS	-	-
PG15	-	-	-	-	SDNCAS	-	-
PA7	-	-	-	-	SDNWE	Yes	Yes
PB5	-	-	-	-	SDCKE1	Yes	-
PB6	-	-	-	-	SDCS1	Yes	-

(1) The address, block address, data and clock lines of SDRAM are suggested to use these two set of pin combinations. Once mixed, it can still work normally but with a limited performance.

4 Memory mapping

Figure 8. Memory mapping (AT32F435/437xM)



(1) The logic addresses of several blocks can be swapped through software configuration. Code can be executed from 0x6000_0000 through 0x9FFF_FFFF. Please refer to the reference manual of AT32F435/437 series.

5 Electrical characteristics

5.1 Test conditions

5.1.1 Minimum and maximum values

The minimum and maximum values are guaranteed in the worst conditions. Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. The minimum and maximum values represent the mean value plus or minus three times the standard deviation (mean ± 3σ).

5.1.2 Typical values

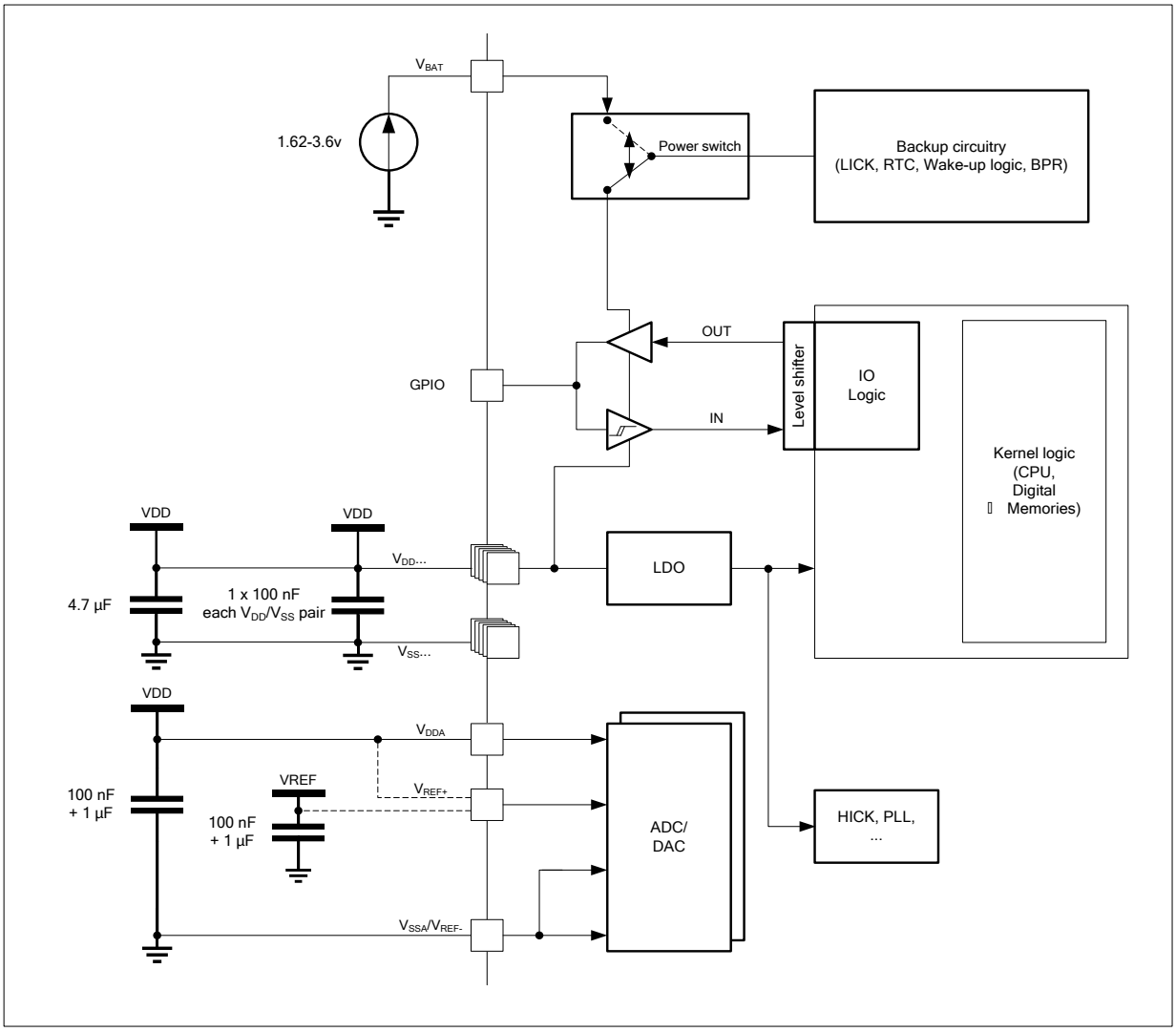
Typical data are based on T_A = 25 °C, V_{DD} = 3.3 V.

5.1.3 Typical curves

All typical curves are provided only as design guidelines and are not tested.

5.1.4 Power supply scheme

Figure 9. Power supply scheme



5.2 Absolute maximum values

5.2.1 Ratings

If stresses were out of the absolute maximum ratings listed in *Table 10*,*Table 11* and *Table 12*, it may cause permanent damage to the device. These are the maximum stress ratings only that the device could bear, but the functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for an extended period of time may affect device reliability.

Table 10. Voltage characteristics

Symbol	Description	Min	Max	Unit
V_{DDx}-V_{SS}	External main supply voltage	-0.3	4.0	V
V_{BAT}-V_{SS}	Battery power voltage	-0.3	4..0	
V_{IN}	Input voltage on FT and FTf GPIO	V_{SS}-0.3	6.0	
	Input voltage on FTa GPIO (set as input floating, input pull-up, or input pull-down mode)			
	Input voltage on TC GPIO	V_{SS}-0.3	4.0	
	Input voltage on FTa GPIO (set as analog mode)			
$\|\Delta V_{DDx}\|$	Variations between different V_{DD} power pins	-	50	mV
$\|V_{SSx}$-$V_{SS}\|$	Variations between all the different ground pins	-	50	

Table 11. Current characteristics

Symbol	Description	Max	Unit
I_{VDD}	Total current into V_{DD} power lines (source)	250	mA
I_{VSS}	Total current out of V_{SS} ground lines (sink)	250	
I_{IO}	Output current sunk by any GPIO and control pin	25	
	Output current source by any GPIOs and control pin	-25	

Table 12. Temperature characteristics

Symbol	Description	Value	Unit
T_{STG}	Storage temperature range	-60 ~ +150	°C
T_J	Maximum junction temperature	125	

5.2.2 Electrical sensitivity

Based on three different tests (HBM, CDM, and LU) using specific measurement methods, the device is stressed in order to determine its performance in terms of electrical sensitivity.

Electrostatic discharge (ESD)

Electrostatic discharges are applied to the pins of each sample according to each pin combination. This test conforms to the JS-001-2017/JS-002-2018 standard.

Table 13. ESD values

Symbol	Parameter	Conditions	Class	Min	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A = +25 °C, conforming to JS-001-2017	3A	±4000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)	T_A = +25 °C, conforming to JS-002-2018	III	±1000	

Static latch-up

Tests compliant with EIA/JESD78E IC latch-up standard are required to assess the latch-up performance:

- A supply overvoltage is applied to each power supply pin;
- A current injection is applied to each input, output and configurable GPIO pin.

Table 14. Latch-up values

Symbol	Parameter	Conditions	Level/Class
LU	Static latch-up	T_A = +105 °C, conforming to EIA/JESD78E	II / A (±200 mA)

5.3 Specification

5.3.1 General operating conditions

Table 15. General operating conditions

Symbol	Parameter	Conditions		Min	Max	Unit
f_{HCLK}	Internal AHB clock frequency	NZW_BST disabled	LDO 1.3 V	0	288	MHz
			LDO 1.2 V	0	240	
			LDO 1.1 V	0	144	
		NZW_BST enabled	LDO 1.3 V	0	192	
			LDO 1.2 V	0	160	
			LDO 1.1 V	0	108	
$f_{PCLK1/2}$	Internal APB1/2 clock frequency	LDO 1.3 V		0	144	MHz
		LDO 1.2 V		0	120	
		LDO 1.1 V		0	72	
V_{DD}	Digital operating voltage	LDO 1.3 V		3.0	3.6	V
		LDO 1.2/1.1 V		2.6	3.6	
V_{DDA}	Analog operating voltage	Must be the same potential as V_{DD}		V_{DD}		V
V_{BAT}	Battery power voltage	-		1.62	3.6	V
P_D	Power dissipation: T_A = 105 °C	LQFP144		-	402	mW
		LQFP100		-	316	
		BGA100		-	385	
		LQFP64		-	310	
		LQFP48		-	320	
		QFN48		-	500	
T_A	Ambient temperature	-		-40	105	°C

5.3.2 Operating conditions at power-up / power-down

Table 16. Operating conditions at power-up/power-down

Symbol	Parameter	Conditions	Min	Max	Unit
t_{VDD}	V_{DD} rise time rate	-	0	∞	ms/V
	V_{DD} fall time rate		20	∞	μs/V

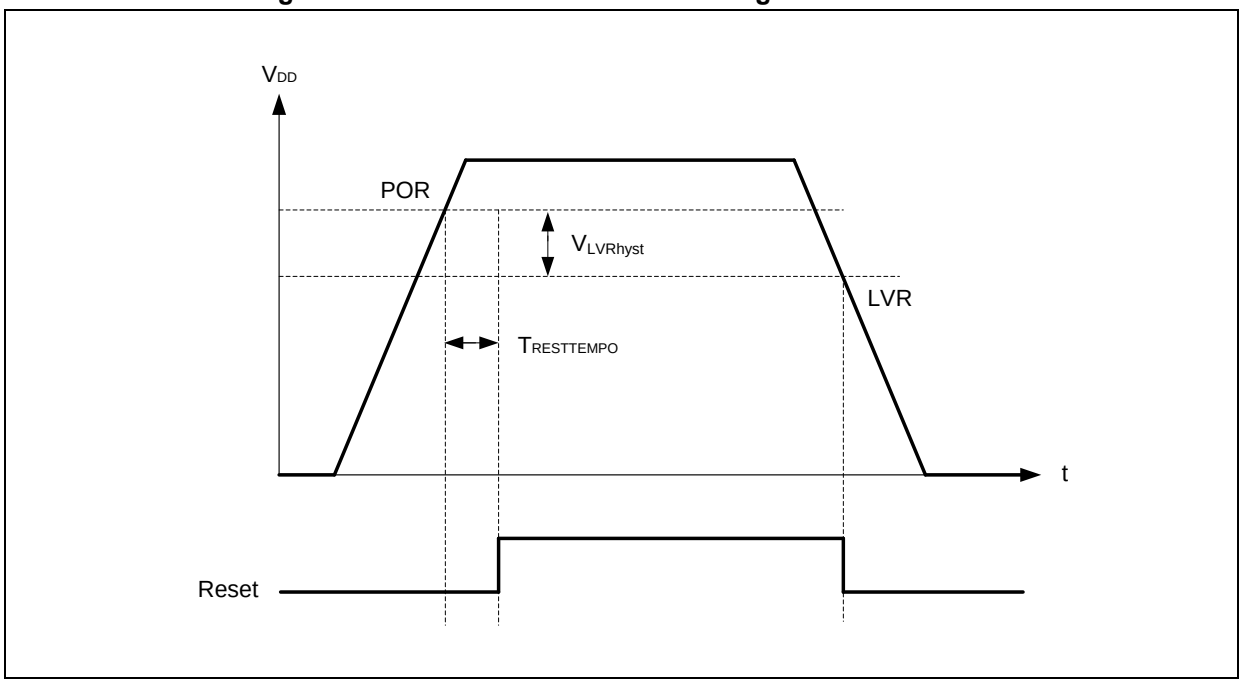
5.3.3 Embedded reset and power control block characteristics

Table 17. Embedded reset and power management block characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{PVM}	Power voltage monitoring level selection	PVMSEL[2:0] = 001 (rising edge)(1)	2.19	2.28	2.37	V
		PVMSEL[2:0] = 001 (falling edge)(1)	2.09	2.18	2.27	V
		PVMSEL[2:0] = 010 (rising edge)(2)	2.28	2.38	2.48	V
		PVMSEL[2:0] = 010 (falling edge)(2)	2.18	2.28	2.38	V
		PVMSEL[2:0] = 011 (rising edge)(2)	2.38	2.48	2.58	V
		PVMSEL[2:0] = 011 (falling edge)(2)	2.28	2.38	2.48	V
		PVMSEL[2:0] = 100 (rising edge)(2)	2.47	2.58	2.69	V
		PVMSEL[2:0] = 100 (falling edge)(2)	2.37	2.48	2.59	V
		PVMSEL[2:0] = 101 (rising edge)(2)	2.57	2.68	2.79	V
		PVMSEL[2:0] = 101 (falling edge)(2)	2.47	2.58	2.69	V
		PVMSEL[2:0] = 110 (rising edge)(2)	2.66	2.78	2.9	V
		PVMSEL[2:0] = 110 (falling edge)(2)	2.56	2.68	2.8	V
		PVMSEL[2:0] = 111 (rising edge)	2.76	2.88	3	V
		PVMSEL[2:0] = 111 (falling edge)	2.66	2.78	2.9	V
V_{HYS_P}(2)	PVM hysteresis	-	-	100	-	mV
V_{POR}(2)	Power on reset threshold	-	2.02	2.2	2.45	V
V_{LVR}(2)	Low voltage reset threshold	-	1.84(3)	2.07	2.3	V
$V_{LVRhyst}$(2)	LVR hysteresis	-	-	130	-	mV
$T_{RESTTEMPO}$(2)	Reset temporization: CPU starts execution after V_{DD} keeps higher than V_{POR} for $T_{RSTTEMPO}$	ZW = 128 Kbytes	-	10	-	ms
		ZW = 256 Kbytes	-	15	-	
		ZW = 512 Kbytes	-	25	-	

(1) PVMSEL[2:0] = 001 may be not available for its voltage detector level may be lower than V_{POR}.
(2) Guaranteed by characterization results, not tested in production.
(3) The product behavior is guaranteed by design down to the minimum V_{LVR} value.

Figure 10. Power on reset and low voltage reset waveform



5.3.4 Memory characteristics

Table 18. Internal Flash memory characteristics (1)

Symbol	Parameter	Conditions	Typ	Max	Unit
T_{PROG}	Programming time	AT32F435/437xD	30	80	μs
		Others	50	200	
t_{SE}	Sector erase time	AT32F435/437xC	50	500	ms
		AT32F435/437xD	50	240	
		AT32F435/437xG	50	500	
		AT32F435/437xM	45	400	
t_{BLE}	Block erase time	AT32F435/437xC	250	2300	ms
		AT32F435/437xD	300	1200	
		AT32F435/437xG	200	2300	
		AT32F435/437xM	225	2000	
t_{BKE}	Bank erase time	AT32F435/437xC	2.5	5	s
		AT32F435/437xD	3	10	
		AT32F435/437xG	1.6	20	
		AT32F435/437xM	7.2	64	

(1) Guaranteed by design, not tested in production.

Table 19. Internal Flash memory endurance and data retention (1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
N_{END}	Endurance	T_A = -40 ~ 105 °C	100	-	-	kcycles
t_{RET}	Data retention	T_A = 105 °C	10	-	-	years

(1) Guaranteed by design, not tested in production.

5.3.5 Supply current characteristics

The current consumption is subjected to several parameters and factors such as the operating voltage, ambient temperature, GPIO pin loading, device software configuration, operating frequencies, GPIO pin switching rate, and executed binary code. The current consumption is obtained by characterization results, not tested in production.

Typical and maximum current consumption

The MCU is placed under the following conditions:

- All GPIO pins are in analog mode.
- Prefetch in ON. (Reminder: This bit must be set before clock setting and bus prescaling)
- When the peripherals are enabled:
  - f_{HCLK} > 72 MHz, f_{PCLK1} = f_{HCLK}/2, f_{PCLK2} = f_{HCLK}/2, f_{ADCCLK} = f_{PCLK2}/2
  - f_{HCLK} ≤ 72 MHz, f_{PCLK1} = f_{HCLK}, f_{PCLK2} = f_{HCLK}, f_{ADCCLK} = f_{PCLK2}/2
- Code executes in ZW area.
- Unless otherwise specified, the typical values are measured with V_{DD} = 3.3 V and T_A = 25 °C condition and the maximum values are measured with V_{DD} = 3.6 V.

Table 20. Typical current consumption in Run mode

Symbol	Parameter	Conditions	f_{HCLK}	LDO voltage	Typ			Unit
					All peripherals enabled (AT32F437)	All peripherals enabled (AT32F435)	All peripherals disabled	
I_{DD}	Supply current in Run mode	High speed external crystal (HEXT) (1)(2)	288 MHz	1.3	247.1	237.7	63.1	mA
			264 MHz	1.3	227.5	218.7	58.2	
			240 MHz	1.2	189.1	181.8	48.6	
			216 MHz	1.2	170.9	164.4	44.1	
			192 MHz	1.2	152.6	146.6	39.6	
			168 MHz	1.2	134.2	129.1	35.1	
			144 MHz	1.1	104.9	100.8	27.5	
			120 MHz	1.1	88.3	84.9	23.8	
			108 MHz	1.1	79.8	76.8	21.7	
			72 MHz	1.1	58.7	56.6	15.8	
			48 MHz	1.1	40.4	39.0	11.9	
			36 MHz	1.1	31.0	29.9	9.68	
			24 MHz	1.1	21.9	21.2	7.79	
			16 MHz	1.1	15.6	15.1	6.23	
			8 MHz	1.1	8.85	8.63	4.41	
			4 MHz	1.1	5.99	5.86	3.77	
			2 MHz	1.1	4.57	4.49	3.45	
			1 MHz	1.1	3.86	3.80	3.29	
		High speed internal clock (HICK) (2)	288 MHz	1.3	246.2	236.8	62.8	mA
			264 MHz	1.3	226.4	217.8	57.9	
			240 MHz	1.2	188.3	181.1	48.3	
			216 MHz	1.2	170.2	164.0	43.8	
			192 MHz	1.2	152.0	146.2	39.3	
			168 MHz	1.2	133.8	128.8	34.8	
			144 MHz	1.1	104.5	100.4	27.2	
			120 MHz	1.1	88.0	84.6	23.5	
			108 MHz	1.1	79.4	76.3	21.4	
			72 MHz	1.1	58.4	56.3	15.5	
			48 MHz	1.1	40.0	38.7	11.5	
			36 MHz	1.1	30.7	29.6	9.34	
			24 MHz	1.1	21.6	20.9	7.45	
			16 MHz	1.1	15.3	14.8	5.89	
			8 MHz	1.1	8.51	8.29	4.07	
			4 MHz	1.1	5.63	5.52	3.42	
			2 MHz	1.1	4.21	4.14	3.11	
			1 MHz	1.1	3.50	3.45	2.95	

(1) External clock is 8 MHz.
(2) PLL is ON when f_{HCLK} > 8 MHz.

Table 21. Typical current consumption in Sleep mode

Symbol	Parameter	Conditions	f_{HCLK}	LDO voltage	Typ			Unit
					All peripherals enabled (AT32F437)	All peripherals enabled (AT32F435)	All peripherals disabled	
I_{DD}	Supply current in Sleep mode	High speed external crystal (HEXT) (1)(2)	288 MHz	1.3	225.0	215.4	39.2	mA
			264 MHz	1.3	205.7	198.4	36.3	
			240 MHz	1.2	172.1	164.8	30.3	
			216 MHz	1.2	155.5	149.0	27.6	
			192 MHz	1.2	138.9	132.9	24.9	
			168 MHz	1.2	122.1	117.0	22.3	
			144 MHz	1.1	95.4	91.3	17.4	
			120 MHz	1.1	80.4	77.0	15.4	
			108 MHz	1.1	72.7	69.6	14.2	
			72 MHz	1.1	53.9	51.8	10.8	
			48 MHz	1.1	37.2	35.8	8.51	
			36 MHz	1.1	28.6	27.5	7.17	
			24 MHz	1.1	20.3	19.6	6.12	
			16 MHz	1.1	14.5	14.1	5.13	
			8 MHz	1.1	8.3	8.12	3.88	
			4 MHz	1.1	5.75	5.63	3.52	
			2 MHz	1.1	4.45	4.38	3.33	
			1 MHz	1.1	3.81	3.76	3.24	
		High speed internal clock (HICK) (2)	288 MHz	1.3	224.3	214.6	38.8	mA
			264 MHz	1.3	205.9	197.7	36.0	
			240 MHz	1.2	171.3	164.0	29.9	
			216 MHz	1.2	154.9	148.6	27.3	
			192 MHz	1.2	138.4	132.5	24.6	
			168 MHz	1.2	121.7	116.7	22.0	
			144 MHz	1.1	95.0	91.0	17.1	
			120 MHz	1.1	80.1	76.7	15.1	
			108 MHz	1.1	72.2	69.2	13.9	
			72 MHz	1.1	53.6	51.5	10.4	
			48 MHz	1.1	36.8	35.4	8.18	
			36 MHz	1.1	28.2	27.2	6.83	
			24 MHz	1.1	20.0	19.3	5.79	
			16 MHz	1.1	14.2	13.8	4.80	
			8 MHz	1.1	8.00	7.78	3.54	
			4 MHz	1.1	5.40	5.29	3.17	
			2 MHz	1.1	4.11	4.04	2.99	
			1 MHz	1.1	3.47	3.42	2.90	

(1) External clock is 8 MHz.
(2) PLL is ON when f_{HCLK} > 8 MHz.

Table 22. Maximum current consumption in Run mode

Symbol	Parameter	Conditions	f_{HCLK}	LDO voltage	Max		Unit
					T_A = 85 °C	T_A = 105 °C	
I_{DD}	Supply current in Run mode	High speed external crystal (HEXT) (1), all peripherals enabled (AT32F437)	288 MHz	1.3	277.1(2)	299.3(2)	mA
			240 MHz	1.2	212.1	230.3	
			192 MHz	1.2	174.9	192.8	
			144 MHz	1.1	121.6	136.0	
			120 MHz	1.1	104.9	119.2	
			108 MHz	1.1	96.3	110.5	
			72 MHz	1.1	74.9	89.0	
			48 MHz	1.1	56.8	71.0	
			36 MHz	1.1	47.2	61.4	
			24 MHz	1.1	38.1	52.2	
			16 MHz	1.1	31.8	45.7	
			8 MHz	1.1	24.9	38.6	
		High speed external crystal (HEXT) (1), all peripherals enabled (AT32F435)	288 MHz	1.3	265.6(2)	290.0(2)	mA
			240 MHz	1.2	204.8	223.0	
			192 MHz	1.2	168.9	187.0	
			144 MHz	1.1	117.5	132.0	
			120 MHz	1.1	101.5	115.9	
			108 MHz	1.1	93.3	107.5	
			72 MHz	1.1	72.9	87.1	
			48 MHz	1.1	55.4	69.7	
			36 MHz	1.1	46.2	60.4	
			24 MHz	1.1	37.5	51.6	
			16 MHz	1.1	31.4	45.2	
			8 MHz	1.1	24.7	38.3	
		High speed external crystal (HEXT) (1), all peripherals disabled	288 MHz	1.3	88.4	109.7	mA
			240 MHz	1.2	68.8	86.1	
			192 MHz	1.2	59.9	76.9	
			144 MHz	1.1	43.5	57.4	
			120 MHz	1.1	39.7	53.7	
			108 MHz	1.1	37.7	51.5	
			72 MHz	1.1	31.8	45.6	
			48 MHz	1.1	27.8	41.7	
			36 MHz	1.1	25.6	39.3	
			24 MHz	1.1	23.7	37.4	
			16 MHz	1.1	22.1	35.7	
			8 MHz	1.1	20.3	33.8	

(1) External clock is 8 MHz. PLL is ON when f_{HCLK} > 8 MHz.
(2) Exceed the total value; for reference only.

Table 23. Maximum current consumption in Sleep mode

Symbol	Parameter	Conditions	f_{HCLK}	LDO voltage	Max		Unit
					T_A = 85 °C	T_A = 105 °C	
I_{DD}	Supply current in Sleep mode	High speed external crystal (HEXT)(1), all peripherals enabled (AT32F437)	288 MHz	1.3	252.7(2)	274.3(2)	mA
			240 MHz	1.2	192.5	211.7	
			192 MHz	1.2	159.1	177.8	
			144 MHz	1.1	110.9	125.6	
			120 MHz	1.1	95.9	110.5	
			108 MHz	1.1	88.1	102.7	
			72 MHz	1.1	69.4	83.9	
			48 MHz	1.1	52.7	67.0	
			36 MHz	1.1	44.2	58.4	
			24 MHz	1.1	36.0	50.2	
			16 MHz	1.1	30.2	44.3	
			8 MHz	1.1	23.9	37.9	
		High speed external crystal (HEXT)(1), all peripherals enabled (AT32F435)	288 MHz	1.3	243.0	265.2(2)	mA
			240 MHz	1.2	185.2	204.0	
			192 MHz	1.2	153.0	171.6	
			144 MHz	1.1	106.8	121.7	
			120 MHz	1.1	92.4	107.1	
			108 MHz	1.1	85.1	99.6	
			72 MHz	1.1	67.3	81.8	
			48 MHz	1.1	51.4	65.7	
			36 MHz	1.1	43.1	57.4	
			24 MHz	1.1	35.2	49.4	
			16 MHz	1.1	29.7	43.8	
			8 MHz	1.1	23.7	37.7	
		High speed external crystal (HEXT)(1), all peripherals disabled	288 MHz	1.3	64.8	84.9	mA
			240 MHz	1.2	50.5	67.3	
			192 MHz	1.2	45.1	61.8	
			144 MHz	1.1	33.8	47.2	
			120 MHz	1.1	32.0	45.2	
			108 MHz	1.1	30.1	43.9	
			72 MHz	1.1	26.7	40.4	
			48 MHz	1.1	24.9	38.0	
			36 MHz	1.1	23.7	36.6	
			24 MHz	1.1	22.7	35.6	
			16 MHz	1.1	20.9	34.6	
			8 MHz	1.1	19.6	33.3	

(1) External clock is 8 MHz. PLL is ON when f_{HCLK} > 8 MHz.
(2) Exceed the total value; for reference only.

Table 24. Typical and maximum current consumptions in Deepsleep and Standby modes(1)

Symbol	Parameter	Conditions		Typ		Max			Unit
				V_{DD} = 2.6 V	V_{DD} = 3.3 V	T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	
I_{DD}	Supply current in Deepsleep mode	LDO in normal mode, 1.2 V output, HICK and HEXT OFF, WDT disabled		2.21	2.22	See (2)	23.2	40.6	mA
		LDO in low-power mode,1.1 V output, HICK and HEXT OFF, WDT disabled		1.52	1.53		18.2	30.7	
	Supply current in Standby mode	LEXT and ERTC OFF	AT32F435/437xD	13.0	15.8	18.9	24.1	30.3	μA
			Others	9.2	10.9	12.5	17.1	23.2	
		LEXT and ERTC ON	AT32F435/437xD	14.5	18.8	21.0	26.4	32.7	
			Others	10.6	13.5	14.6	19.3	25.9	

(1) Guaranteed by characterization results, not tested in production.
(2) This value may be several times the typical value due to process variations.

Figure 11. Typical current consumption in Deepsleep mode with regulator in run mode and output 1.2 V vs. temperature at different V_{DD}

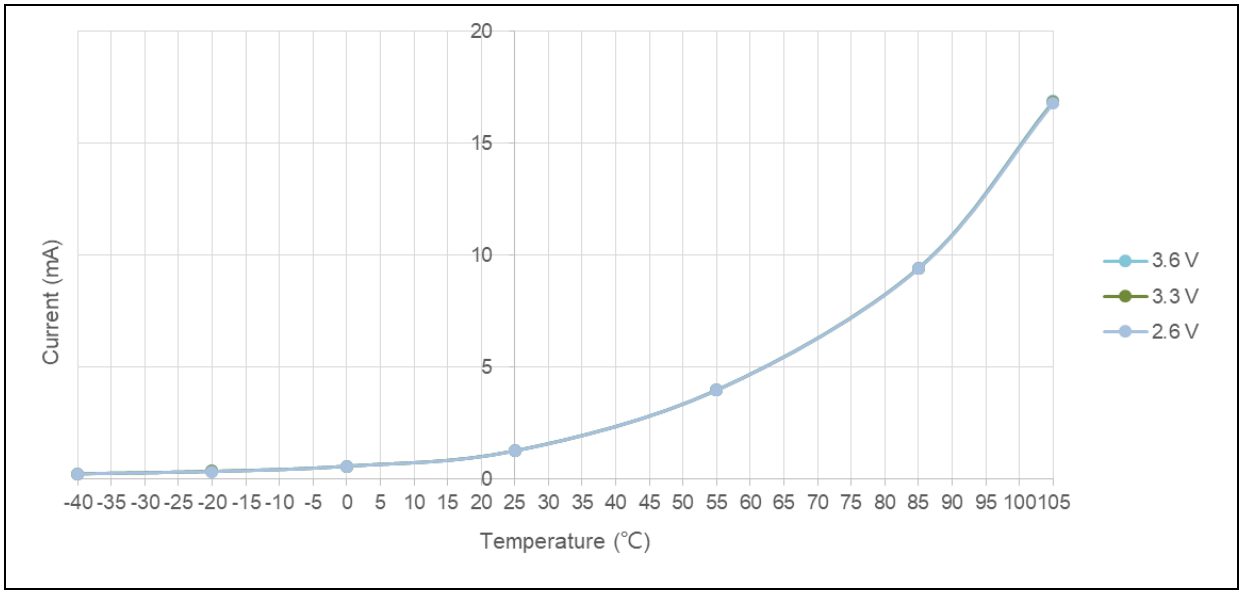


Figure 12. Typical current consumption in Deepsleep mode with regulator in low-power mode and output 1.1 V vs. temperature at different V_{DD}

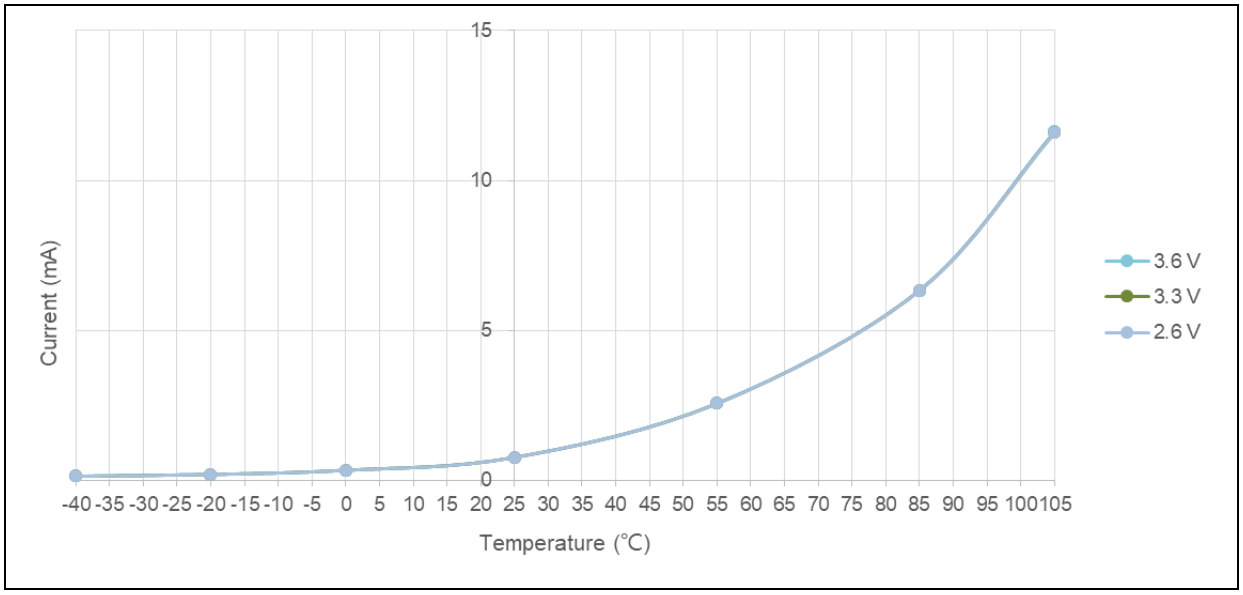


Figure 13. Typical current consumption in Standby mode vs. temperature at different V_{DD} (AT32F435/437xD)

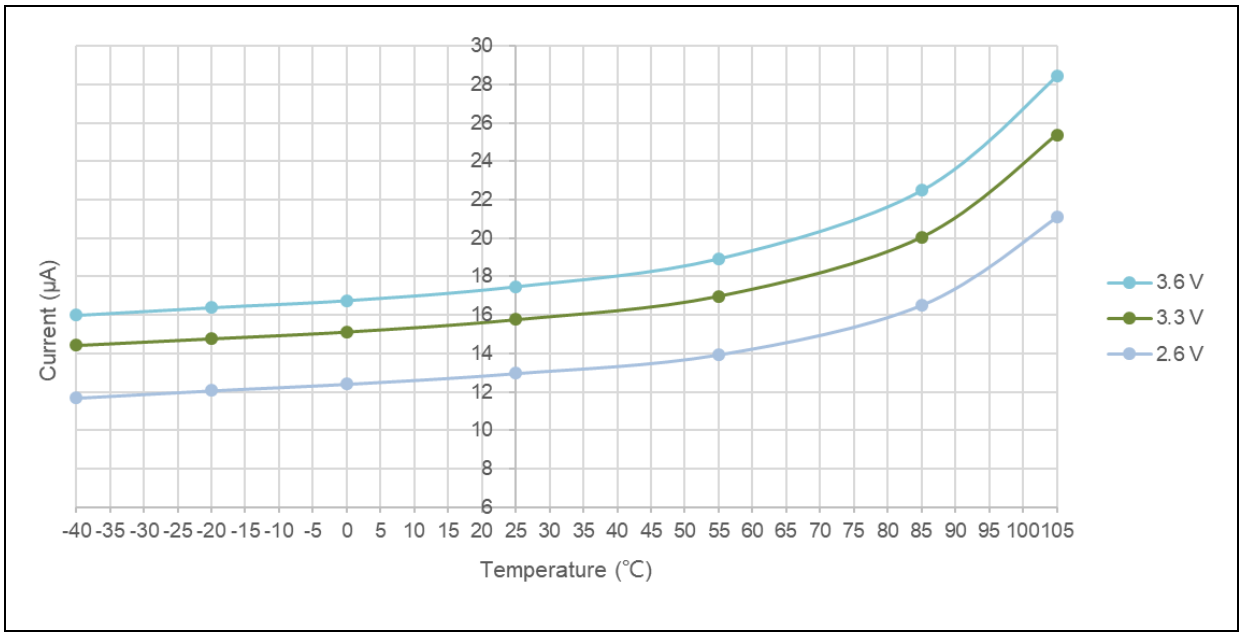


Figure 14. Typical current consumption in Standby mode vs. temperature at different V_{DD} (others)

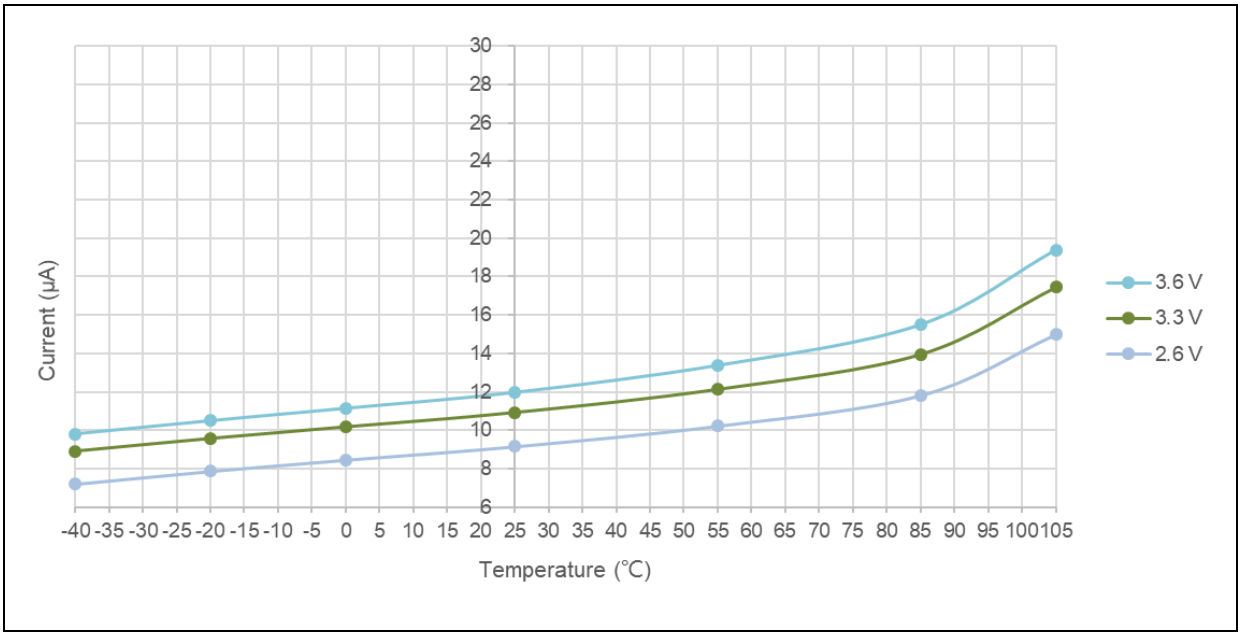
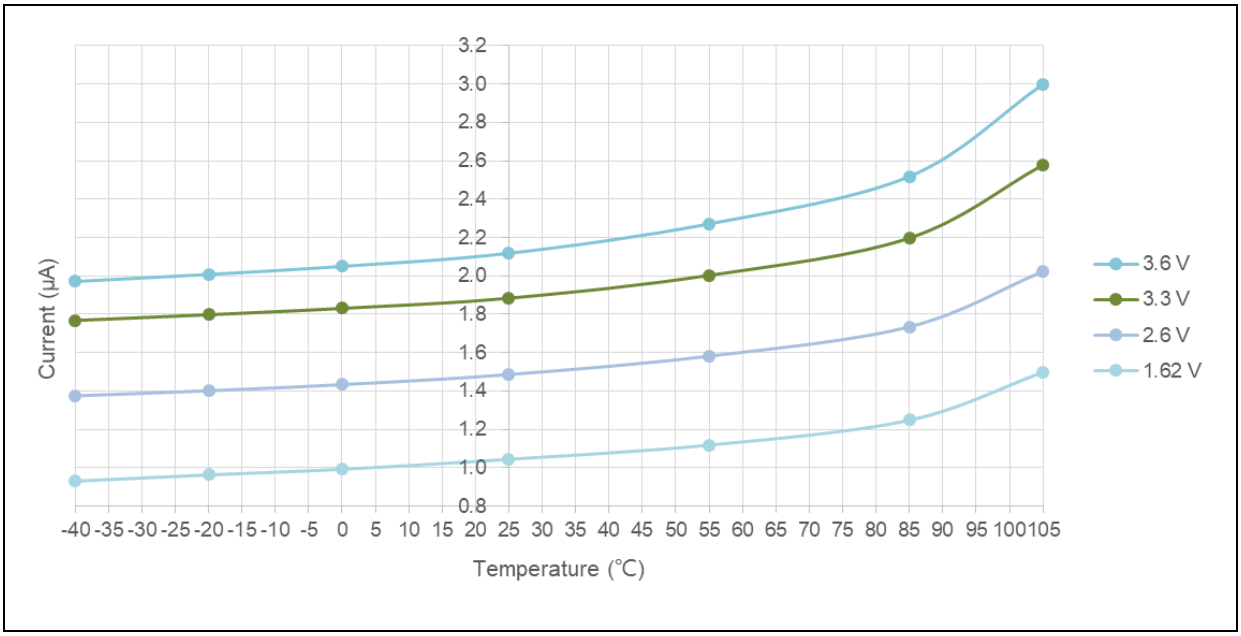


Table 25. Typical and maximum current consumptions on V_{BAT}(1)

Symbol	Parameter	Conditions	Typ			Max			Unit
			V_{BAT} = 1.62 V	V_{BAT} = 2.6 V	V_{BAT} = 3.3 V	T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	
I_{DD_VBAT}	Supply current of V_{BAT}	LEXT and ERTC ON, $V_{DD} < V_{LVR}$	1.04	1.49	1.89	2.29	2.70	3.23	μA

(1) Guaranteed by characterization results, not tested in production.

Figure 15. Typical current consumption on V_{BAT} with LEXT and ERTC ON vs. temperature at different V_{BAT}



On-chip peripheral current consumption

The MCU is placed under the following conditions:

- All GPIO pins are in analog mode.
- The given value is calculated by measuring the current consumption difference between “all peripherals clocked OFF” and “only one peripheral clocked ON”.

Table 26. Peripheral current consumption

Peripheral		Typ			Unit
		LDO = 1.3 V	LDO = 1.2 V	LDO = 1.1 V	
AHB	DMA1	14.67	13.39	12.21	μA/MHz
	DMA2	14.85	13.56	12.36	
	EDMA	68.04	62.02	56.48	
	GPIOA	2.68	2.46	2.24	
	GPIOB	2.66	2.44	2.21	
	GPIOC	2.65	2.42	2.22	
	GPIOD	2.58	2.38	2.17	
	GPIOE	2.67	2.46	2.23	
	GPIOF	2.58	2.37	2.16	
	GPIOG	2.64	2.42	2.20	
	GPIOH	2.59	2.39	2.18	
	XMC	43.05	39.29	35.81	
	QSPI1	49.85	45.54	41.53	
	QSPI2	50.05	45.66	41.59	
	CRC	1.74	1.60	1.46	
	SDIO1	20.30	18.51	16.86	
	SDIO2	20.56	18.76	17.12	
	OTGFS1	58.65	53.58	48.87	
	OTGFS2	59.09	53.96	49.17	
	DVP	8.12	7.42	6.76	
	EMAC EMAC_TX EMAC_RX EMAC_PTP	32.68	29.84	27.21	
APB1	TMR2	12.43	11.33	10.32	
	TMR3	9.11	8.30	7.57	
	TMR4	9.29	8.47	7.71	
	TMR5	12.17	11.12	10.13	
	TMR6	1.71	1.58	1.44	
	TMR7	1.59	1.47	1.34	
	TMR12	5.54	5.07	4.63	
	TMR13	3.59	3.31	3.01	
	TMR14	3.71	3.42	3.12	
	WWDT	0.79	0.73	0.67	
	SPI2/I^2S2	10.21	9.34	8.52	
	SPI3/I^2S3	7.80	7.16	6.53	

Peripheral		Typ			Unit
		LDO = 1.3 V	LDO = 1.2 V	LDO = 1.1 V	
APB1	USART2	3.14	2.87	2.62	μA/MHz
	USART3	3.09	2.83	2.58	
	UART4	3.04	2.78	2.53	
	UART5	2.96	2.72	2.47	
	I^2C1	7.28	6.66	6.07	
	I^2C2	7.31	6.69	6.09	
	I^2C3	7.25	6.64	6.06	
	CAN1	4.92	4.51	4.11	
	CAN2	4.56	4.18	3.81	
	PWC	0.55	0.54	0.48	
	DAC	2.72	2.50	2.28	
	UART7	3.06	2.80	2.56	
	UART8	3.07	2.80	2.56	
APB2	TMR1	13.26	12.11	11.04	
	TMR8	13.44	12.28	11.21	
	USART1	3.24	2.97	2.71	
	USART6	3.44	3.15	2.87	
	ADC1	15.11	13.80	12.56	
	ADC2	15.02	13.70	12.49	
	ADC3	14.95	13.65	12.44	
	SPI1/I^2S1	5.70	5.22	4.77	
	SPI4/I^2S4	3.67	3.36	3.07	
	SCFG	0.95	0.88	0.80	
	TMR9	5.89	5.40	4.93	
	TMR10	3.72	3.41	3.12	
	TMR11	3.97	3.63	3.31	
	TMR20	12.88	11.74	10.69	
	ACC	1.12	1.02	0.93	

5.3.6 External clock source characteristics

High-speed external clock generated from a crystal / ceramic resonator

The high-speed external (HEXT) clock can be supplied with a 4 to 25 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in the table below. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

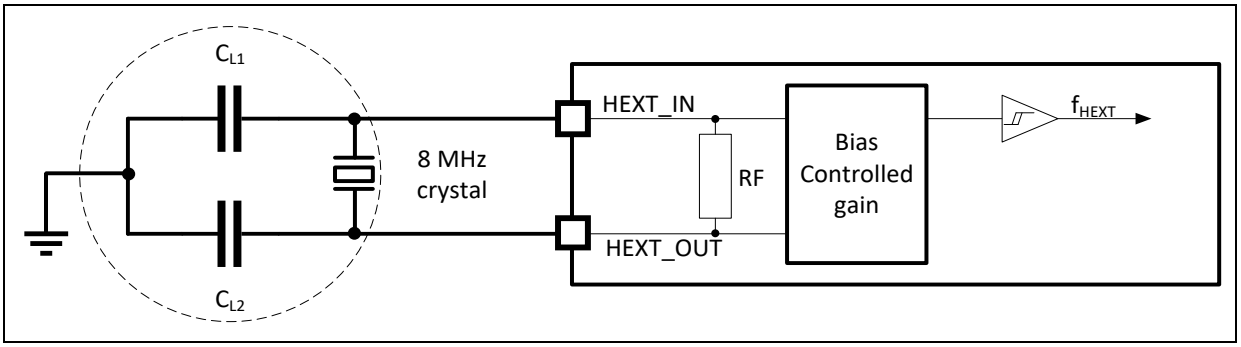
Table 27. HEXT 4 ~ 25 MHz crystal characteristics (1)(2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HEXT_IN}	Oscillator frequency	-	4	8	25	MHz
$t_{SU(HEXT)}$(3)	Startup time	V_{DD} is stabilized	-	2	-	ms

(1) Oscillator characteristics given by the crystal/ceramic resonator manufacturer.
(2) Guaranteed by characterization results, not tested in production.
(3) $t_{SU(HEXT)}$ is the startup time measured from the moment HEXT is enabled (by software) to a stabilized 8 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer.

For C_{L1} and C_{L2}, it is recommended to use high-quality external ceramic capacitors in the 5 pF to 33 pF range (typ.), designed for high-frequency applications, and select to match the requirements of the crystal or resonator. C_{L1} and C_{L2} are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of C_{L1} and C_{L2}. PCB and MCU pin capacitance must be included when sizing C_{L1} and C_{L2}. The load capacitance C_L is based on the following formula: CL = CL1 x CL2 / (CL1 + CL2) + Cstray, where Cstray is the pin capacitance and board or PCB-related capacitance. Typically, it is between 2 pF and 7 pF.

Figure 16. HEXT typical application with an 8 MHz crystal



High-speed external clock generated from an external source

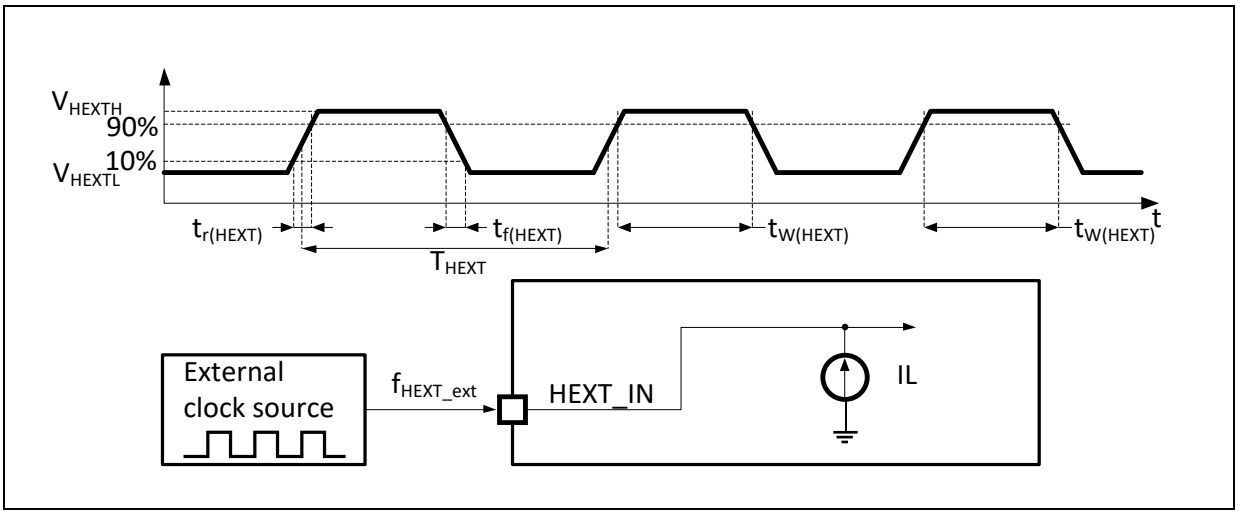
The characteristics given in the table below result from tests performed using a high-speed external clock source.

Table 28. HEXT external source characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HEXT_ext}	User external clock source frequency (1)	-	1	8	25	MHz
V_{HEXTH}	HEXT_IN input pin high level voltage		$0.7V_{DD}$	-	V_{DD}	V
V_{HEXTL}	HEXT_IN input pin low level voltage		V_{SS}	-	$0.3V_{DD}$	
$t_{w(HEXT)}$ $t_{w(HEXT)}$	HEXT_IN high or low time (1)		5	-	-	ns
$t_{r(HEXT)}$ $t_{f(HEXT)}$	HEXT_IN rise or fall time (1)		-	-	20	
$C_{in(HEXT)}$	HEXT_IN input capacitance (1)	-	-	5	-	pF
$Duty_{(HEXT)}$	Duty cycle	-	45	-	55	%
I_L	HEXT_IN input leakage current	$V_{SS} \le V_{IN} \le V_{DD}$	-	-	±1	μA

(1) Guaranteed by design, not tested in production.

Figure 17. HEXT external source AC timing diagram



Low-speed external clock generated from a crystal / ceramic resonator

The low-speed external (LEXT) clock can be supplied with a 32.768 kHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in the table below. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Table 29. LEXT 32.768 kHz crystal characteristics (1)(2)

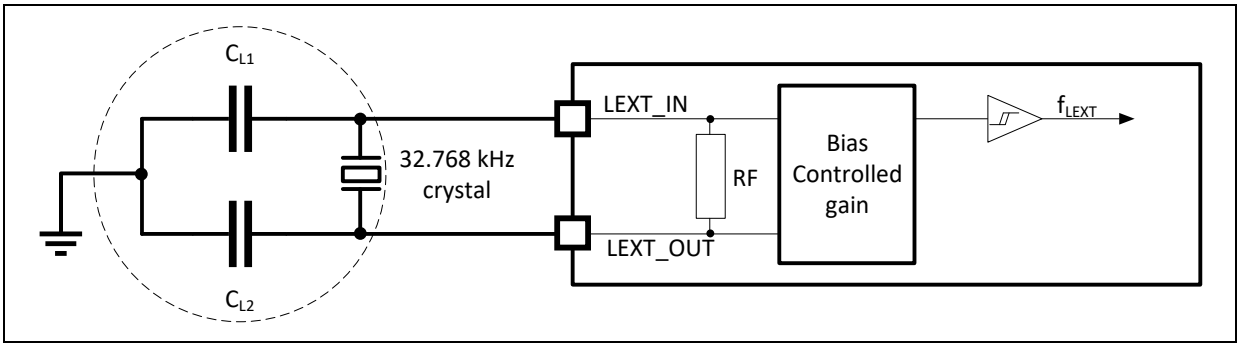
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{SU(LEXT)}$	Startup time	V_{DD} is stabilized	-	200	-	ms

(1) Oscillator characteristics given by the crystal/ceramic resonator manufacturer.
(2) Guaranteed by characterization results, not tested in production.

For C_{L1} and C_{L2}, it is recommended to use high-quality ceramic capacitors in the 5 pF to 20 pF range selected to meet the requirements of the crystal or resonator. C_{L1} and C_{L2}, are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of C_{L1} and C_{L2}.

Load capacitance C_L is based on the following formula: $C_L = C_{L1} \times C_{L2} / (C_{L1} + C_{L2}) + C_{stray}$, where C_{stray} is the pin capacitance and board or trace PCB-related capacitance. Typically, it is between 2 pF and 7 pF.

Figure 18. LEXT typical application with a 32.768 kHz crystal



Note: No external resistor is required between LEXT_IN and LEXT_OUT, and it is also prohibited to add it.

Low-speed external clock generated from an external source

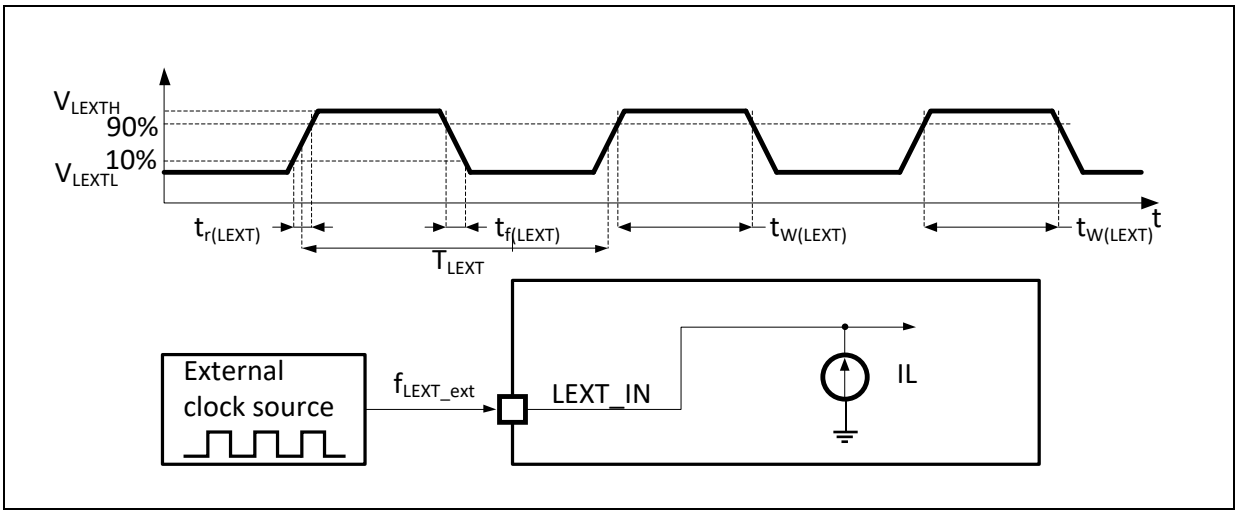
The characteristics given in the table below come from tests performed using a low-speed external clock source.

Table 30. LEXT external source characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LEXT_ext}	User external clock source frequency (1)	-	-	32.768	1000	kHz
V_{LEXTH}	LEXT_IN input pin high level voltage		$0.7V_{DD}$	-	V_{DD}	V
V_{LEXTL}	LEXT_IN input pin low level voltage		V_{SS}	-	$0.3V_{DD}$	
$t_{w(LEXT)}$ $t_{w(LEXT)}$	LEXT_IN high or low time (1)		450	-	-	ns
$t_{r(LEXT)}$ $t_{f(LEXT)}$	LEXT_IN rise or fall time (1)		-	-	50	
$C_{in(LEXT)}$	LEXT_IN input capacitance (1)	-	-	5	-	pF
$Duty_{(LEXT)}$	Duty cycle	-	30	-	70	%
I_L	LEXT_IN input leakage current	$V_{SS} \le V_{IN} \le V_{DD}$	-	-	±1	μA

(1) Guaranteed by design, not tested in production.

Figure 19. LEXT external source AC timing diagram



5.3.7 Internal clock source characteristics

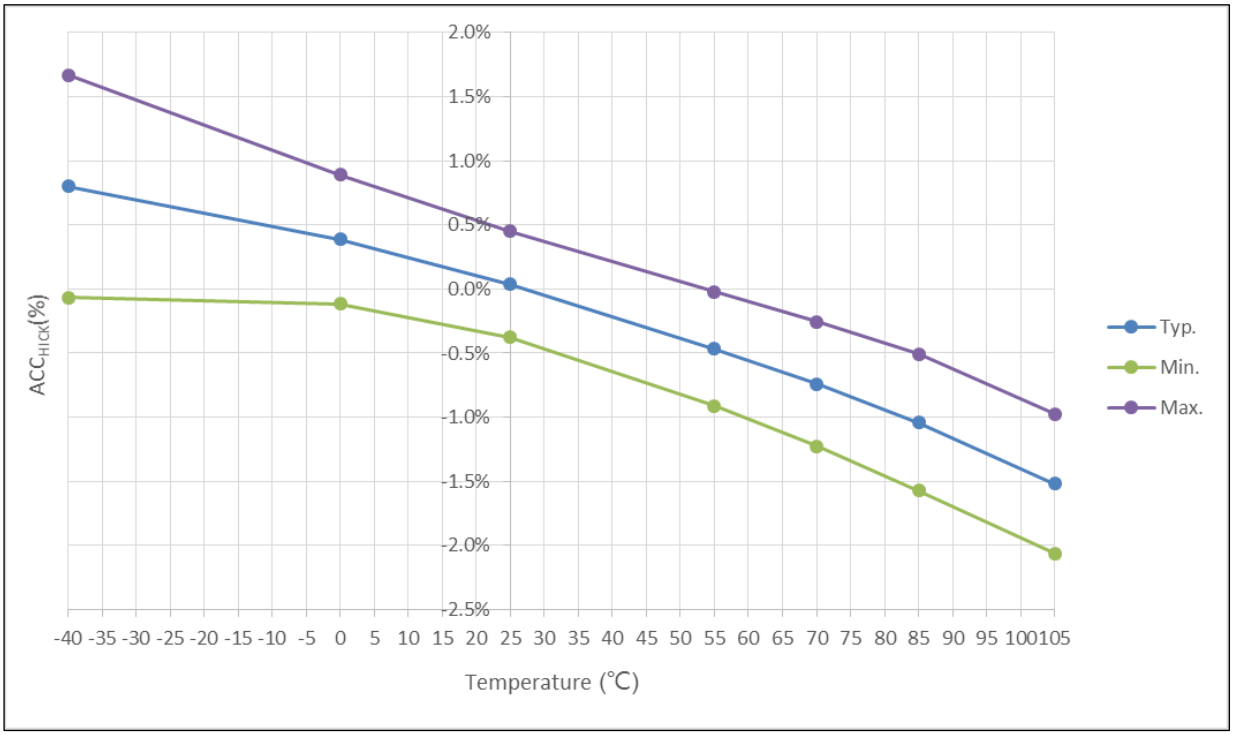
High-speed internal clock (HICK)

Table 31. HICK clock characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_{HICK}	Frequency	-		-	48	-	MHz
$DuCy_{(HICK)}$	Duty cycle	-		45	-	55	%
ACC_{HICK}	Accuracy of the HICK oscillator	User-trimmed with the CRM_CTRL register		-	-	1(1)	%
		ACC-trimmed		-	-	0.25(1)	
		Factory-calibrated (2)	T_A = -40 ~ 105 °C	-2.5	-	2.5	
			T_A = -40 ~ 85 °C	-2	-	2	
			T_A = 0 ~ 70 °C	-1.5	-	1.5	
			T_A = 25 °C	-1	0.5	1	
$t_{SU(HICK)}$(2)	HICK oscillator startup time	-		-	-	10	μs
$I_{DD(HICK)}$(2)	HICK oscillator power consumption	-		-	255	325	μA

(1) Guaranteed by design, not tested in production.
(2) Guaranteed by characterization results, not tested in production.

Figure 20. HICK clock frequency accuracy vs. temperature



Low-speed internal clock (LICK)

Table 32. LICK clock characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LICK}(1)	Frequency	-	30	40	60	kHz

(1) Guaranteed by characterization results, not tested in production.

5.3.8 PLL characteristics

Table 33. PLL characteristics

Symbol	Parameter	Min(1)	Typ	Max(1)	Unit
f_{PLL_IN}	PLL input clock (2)	2	8	16	MHz
	PLL input clock duty cycle	40	-	60	%
f_{PLL_OUT}	PLL multiplier output clock	16	-	288	MHz
t_{LOCK}	PLL lock time	-	-	200	μs
Jitter	Cycle-to-cycle jitter	-	-	300	ps

(1) Guaranteed by design, not tested in production.
(2) Take care of using the appropriate multiplier factors to ensure that PLL input clock values are compatible with the range defined by f_{PLL_OUT}.

5.3.9 Wakeup time from low-power mode

The wakeup times given in the table below is measured on a wakeup phase with the HICK. The clock source used to wake up the device depends from the current operating mode:

- Sleep mode: the clock source is the clock that was configured before entering Sleep mode.
- Deepsleep or Standby mode: the clock source is the HICK.

Table 34. Low-power mode wakeup time

Symbol	Parameter	Conditions	Typ	Unit
$t_{WUSLEEP}$	Wakeup from Sleep mode	-	1.8	μs
$t_{WUDEEPSLEEP}$	Wakeup from Deepsleep mode	LDO in normal mode	330	μs
		LDO in low-power mode	360	
$t_{WUSTDBY}$	Wakeup from Standby mode	ZW = 128 Kbytes	5	ms
		ZW = 256 Kbytes	10	
		ZW = 512 Kbytes	20	

5.3.10 EMC characteristics

Susceptibility tests are performed on a sample basis during device characterization.

Functional EMS (electromagnetic susceptibility)

- **EFT:** A Burst of Fast Transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a coupling/decoupling network, until a functional disturbance occurs. This test is compliant with the IEC 61000-4-4 standard.

Table 35. EMS characteristics

Symbol	Parameter	Conditions	Level/Class
V_{EFT}	Fast transient voltage burst limits to be applied through coupling/decoupling network conforms to IEC 61000-4-4 on V_{DD} and V_{SS} pins to induce a functional disturbance, V_{DD} and V_{SS} input has one 47 μF capacitor and each V_{DD} and V_{SS} pin pair 0.1 μF.	V_{DD} = 3.3 V, LQFP144, T_A = +25 °C, f_{HCLK} = 288 MHz, LDO = 1.3 V, NZW_BST = 0, conforming to IEC 61000-4-4	4A (±4 kV)
		V_{DD} = 3.3 V, LQFP144, T_A = +25 °C, f_{HCLK} = 160 MHz, LDO = 1.2 V, NZW_BST = 1, conforming to IEC 61000-4-4	

EMC characterization and optimization are performed at component level with a typical application environment. It should be noted that good EMC performance is highly dependent on the user application and the software in particular. Therefore, it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

5.3.11 GPIO port characteristics

General input/output characteristics

All GPIOs are CMOS and TTL compliant.

Table 36. GPIO static characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	GPIO input low level voltage	-	–0.3	-	0.28 x V_{DD} + 0.1	V
V_{IH}	TC input high level voltage	-	0.31 x V_{DD} + 0.8	-	V_{DD} + 0.3	V
	FTa input high level voltage	Analog mode				
	FT and FTf input high level voltage	-		-	5.5	
	FTa input high level voltage	Input floating, input pull-up, or input pull-down mode				
V_{hys}	Schmitt trigger voltage hysteresis (1)	-	200	-	-	mV
			5% V_{DD}	-	-	-
I_{lkg}	Input floating leakage current (2)	$V_{SS} \le V_{IN} \le V_{DD}$ TC GPIO	-	-	±1	µA
		$V_{SS} \le V_{IN} \le 5.5$ V FT, FTf and FTa GPIOs	-	-	±1	
R_{PU}	Weak pull-up equivalent resistor (3)	$V_{IN} = V_{SS}$	60	70	100	kΩ
R_{PD}	Weak pull-down equivalent resistor 3)(4)	$V_{IN} = V_{DD}$	60	70	100	kΩ
C_{IO}	GPIO pin capacitance	-	-	9	-	pF

(1) Hysteresis voltage between Schmitt trigger switching levels. Guaranteed by characterization results, not tested in production.
(2) Leakage could be higher than max if negative current is injected on adjacent pins.
(3) Internal pull-up/pull-down resistors must be disabled when the FT, FTf and FTa input voltage is higher than V_{DD} + 0.3 V.
(4) The pull-down resistor of BOOT0 exists permanently.

All GPIOs are CMOS and TTL compliant (no software configuration required). Their characteristics take into account the strict CMOS-technology or TTL parameters.

Output driving current

In the user application, the number of GPIO pins which can drive current must be controlled to respect the absolute maximum rating defined in Section *5.2.1*.

- The sum of the currents sourced by all GPIOs on V_{DD}, plus the maximum Run consumption of the MCU sourced on V_{DD}, cannot exceed the absolute maximum rating I_{VDD} (see *Table 11*).

- The sum of the currents sunk by all GPIOs on V_{SS}, plus the maximum Run consumption of the MCU sunk on V_{SS}, cannot exceed the absolute maximum rating I_{VSS} (see *Table 11*).

Output voltage levels

All GPIOs are CMOS and TTL compliant.

Table 37. Output voltage characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
Maximum sourcing/sinking strength					
V_{OL}	Output low level voltage	CMOS standard, I_{IO} = 15 mA	-	0.4	V
V_{OH}	Output high level voltage		V_{DD}-0.4	-	
V_{OL}	Output low level voltage	TTL standard, I_{IO} = 6 mA	-	0.4	V
V_{OH}	Output high level voltage		2.4	-	
Large sourcing/sinking strength					
V_{OL}	Output low level voltage	CMOS standard, I_{IO} = 6 mA	-	0.4	V
V_{OH}	Output high level voltage		V_{DD}-0.4	-	
V_{OL}	Output low level voltage	TTL standard, I_{IO} = 3 mA	-	0.4	V
V_{OH}	Output high level voltage		2.4	-	
V_{OL}(1)	Output low level voltage	I_{IO} = 20 mA	-	1.3	V
V_{OH}(1)	Output high level voltage		V_{DD}-1.3	-	
Normal sourcing/sinking strength					
V_{OL}	Output low level voltage	CMOS standard, I_{IO} = 4 mA	-	0.4	V
V_{OH}	Output high level voltage		V_{DD}-0.4	-	
V_{OL}	Output low level voltage	TTL standard, I_{IO} = 2 mA	-	0.4	V
V_{OH}	Output high level voltage		2.4	-	
V_{OL}(1)	Output low level voltage	I_{IO} = 10 mA	-	1.3	V
V_{OH}(1)	Output high level voltage		V_{DD}-1.3	-	
Ultra high sourcing/sinking strength (2)					
V_{OL}	Output low level voltage	I_{IO} = 20 mA	-	0.4	V

(1) Guaranteed by characterization results, not tested in production.
(2) When GPIO ultra high sinking strength is enabled, its V_{OH} is the same as that of maximum sourcing strength.

Input AC characteristics

The definition and values of input AC characteristics are given as follows.

Table 38. Input AC characteristics

Symbol	Parameter	Min	Max	Unit
$t_{EXINTpw}$	Pulse width of external signals detected by EXINT controller	10	-	ns

5.3.12 NRST pin characteristics

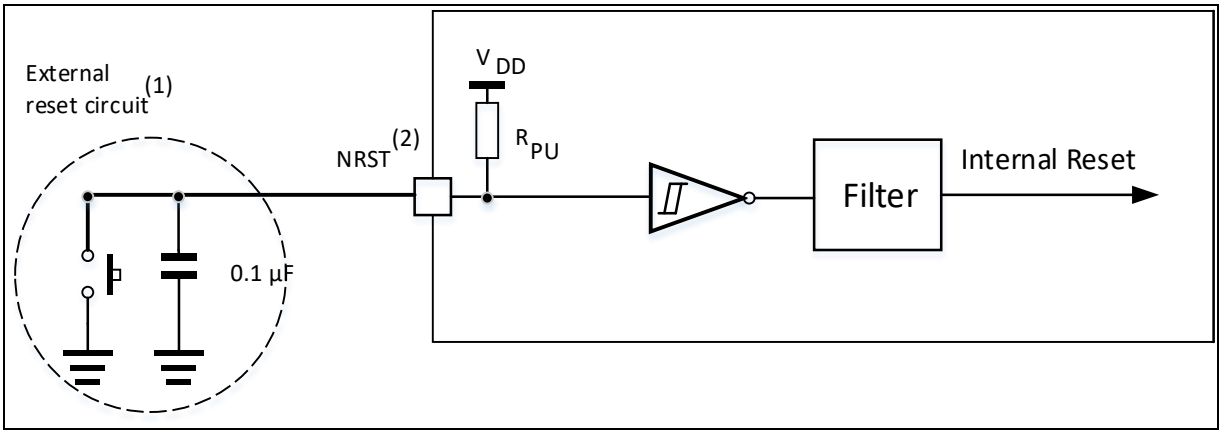
The NRST pin input driver uses CMOS technology. It is connected to a permanent pull-up resistor, R_{PU} (see the table below).

Table 39. NRST pin characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IL(NRST)}$(1)	NRST input low level voltage	-	-0.5	-	0.8	V
$V_{IH(NRST)}$(1)	NRST input high level voltage	-	2	-	V_{DD} + 0.3	
$V_{hys(NRST)}$	NRST Schmitt trigger voltage hysteresis	-	-	500	-	mV
R_{PU}	Weak pull-up equivalent resistor	$V_{IN} = V_{SS}$	30	40	50	kΩ
$t_{ILV(NRST)}$(1)	NRST input low level invalid time	-	-	-	33.3	μs
$t_{ILNV(NRST)}$(1)	NRST input low level valid time	-	66.7	-	-	μs

(1) Guaranteed by design, not tested in production.

Figure 21. Recommended NRST pin protection



(1) The reset network protects the device against parasitic resets.
(2) The user must ensure that the level on the NRST pin can go below the $V_{IL(NRST)}$ max level specified in NRST *Table 39*. Otherwise the reset will not be performed by the device.

5.3.13 XMC (SDRAM included) characteristics

Parameters listed in the table below are guaranteed by design, not tested in production.

Asynchronous waveforms and timings of SRAM/PSRAM/NOR

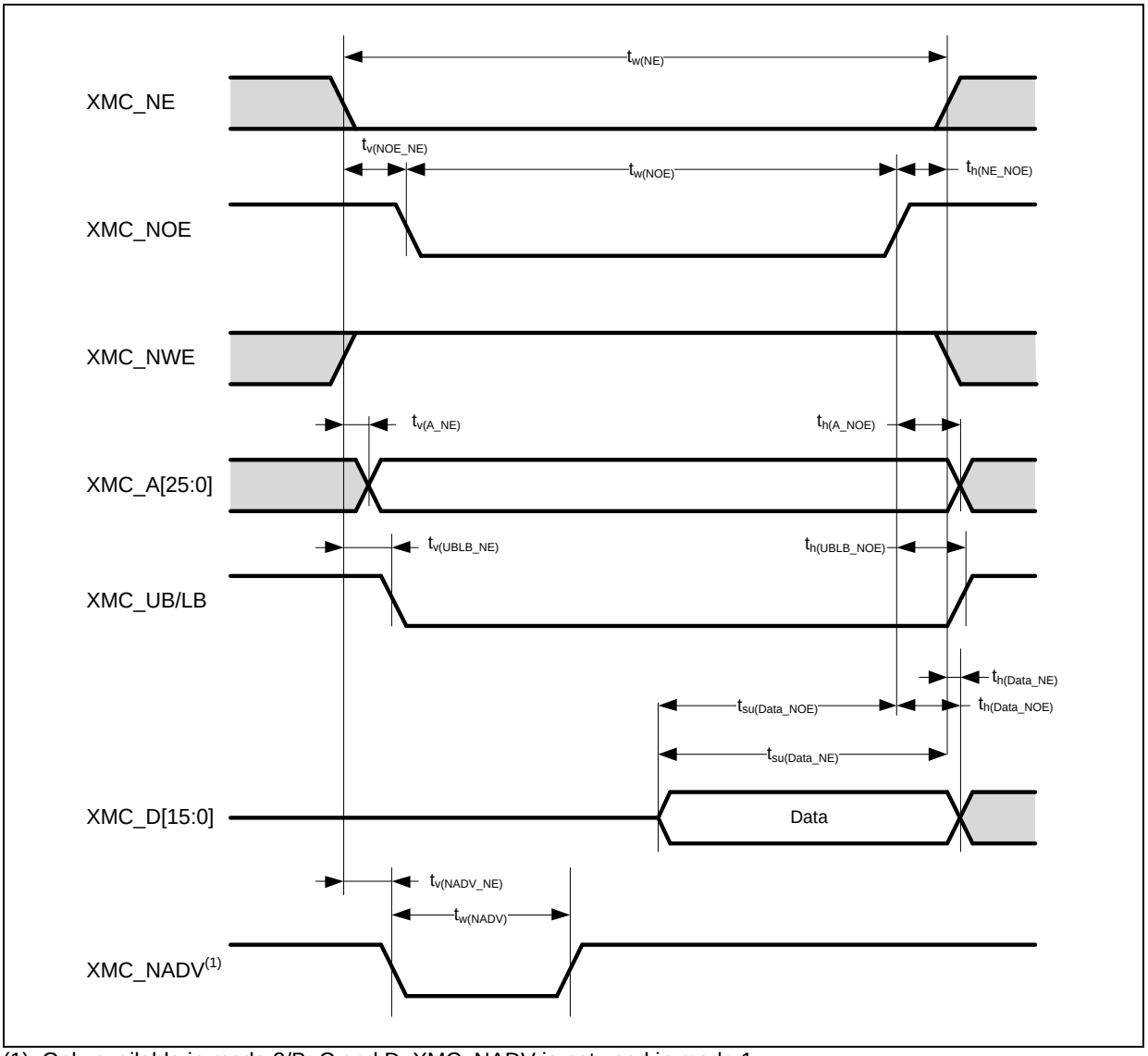
The results given in these tables are obtained with the following XMC configuration:

- AddressSetupTime = 0
- AddressHoldTime = 1
- DataSetupTime = 1

Table 40. Asynchronous non-multiplexed SRAM/PSRAM/NOR read timings

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	XMC_NE low time	$5t_{HCLK}$ - 1.5	$5t_{HCLK}$ + 2	ns
$t_{v(NOE_NE)}$	XMC_NE low to XMC_NOE low valid time	0.5	1.5	ns
$t_{w(NOE)}$	XMC_NOE low time	$5t_{HCLK}$ - 1.5	$5t_{HCLK}$ + 1.5	ns
$t_{h(NE_NOE)}$	XMC_NOE high to XMC_NE high hold time	-1.5	-	ns
$t_{v(A_NE)}$	XMC_NE low to XMC_A valid time	-	7	ns
$t_{h(A_NOE)}$	Address hold time after XMC_NOE high	2.5	-	ns
$t_{v(UBLB_NE)}$	XMC_NE low to XMC_UB/LB valid time	-	0	ns
$t_{h(UBLB_NOE)}$	XMC_UB/LB hold time after XMC_NOE high	2.5	-	ns
$t_{su(Data_NE)}$	Data to XMC_NE high setup time	$2t_{HCLK}$ + 25	-	ns
$t_{su(Data_NOE)}$	Data to XMC_NOE high setup time	$2t_{HCLK}$ + 25	-	ns
$t_{h(Data_NOE)}$	Data hold time after XMC_NOE high	0	-	ns
$t_{h(Data_NE)}$	Data hold time after XMC_NE high	0	-	ns
$t_{v(NADV_NE)}$	XMC_NE low to XMC_NADV low valid time	-	5	ns
$t_{w(NADV)}$	XMC_NADV low time	-	t_{HCLK} + 1.5	ns

Figure 22. Asynchronous non-multiplexed SRAM/PSRAM/NOR read waveforms

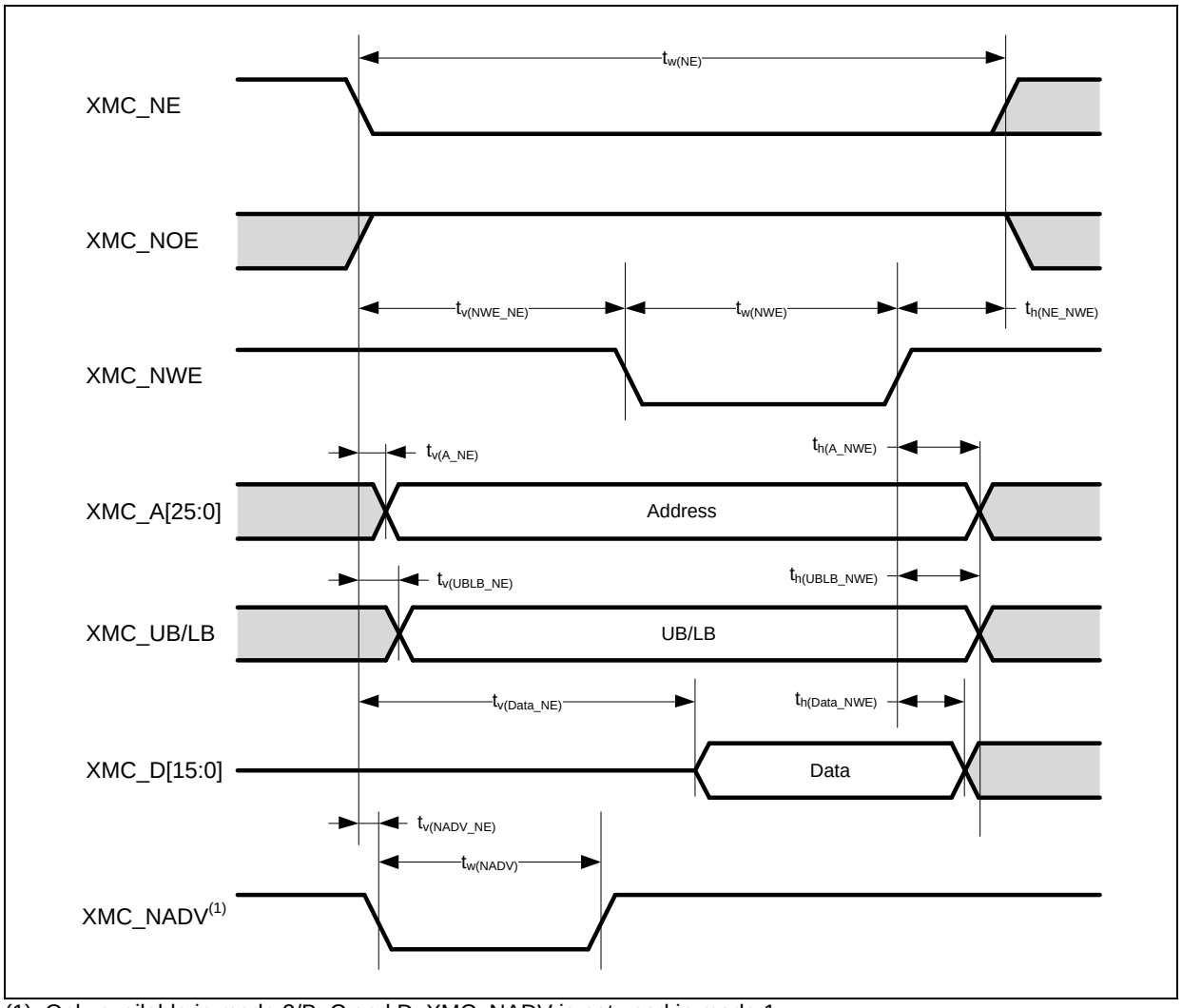


(1) Only available in mode 2/B, C and D. XMC_NADV is not used in mode 1.

Table 41. Asynchronous non-multiplexed SRAM/PSRAM/NOR write timings

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	XMC_NE low time	$4t_{HCLK} – 1.5$	$4t_{HCLK} + 2$	ns
$t_{v(NWE_NE)}$	XMC_NE low to XMC_NWE low valid time	$t_{HCLK} - 0.5$	$t_{HCLK} + 1.5$	ns
$t_{w(NWE)}$	XMC_NWE low time	$2t_{HCLK} - 0.5$	$2t_{HCLK} + 1.5$	ns
$t_{h(NE_NWE)}$	XMC_NWE high to XMC_NE high hold time	$t_{HCLK}- 0.5$	-	ns
$t_{v(A_NE)}$	XMC_NE low to XMC_A valid time	-	7.5	ns
$t_{h(A_NWE)}$	Address hold time after XMC_NWE high	$t_{HCLK} + 2$	-	ns
$t_{v(UBLB_NE)}$	XMC_NE low to XMC_UB/LB valid time	-	1.5	ns
$t_{h(UBLB_NWE)}$	XMC_UB/LB hold time after XMC_NWE high	$t_{HCLK} - 0.5$	-	ns
$t_{v(Data_NE)}$	XMC_NE low to data valid	-	$t_{HCLK} + 7$	ns
$t_{h(Data_NWE)}$	Data hold time after XMC_NWE high	$t_{HCLK} + 3$	-	ns
$t_{v(NADV_NE)}$	XMC_NE low to XMC_NADV low valid time	-	5.5	ns
$t_{w(NADV)}$	XMC_NADV low time	-	$t_{HCLK} + 1.5$	ns

Figure 23. Asynchronous non-multiplexed SRAM/PSRAM/NOR write waveforms



(1) Only available in mode 2/B, C and D. XMC_NADV is not used in mode 1.

Table 42. Asynchronous multiplexed PSRAM/NOR read timings

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	XMC_NE low time	$8t_{HCLK}$ - 2	$8t_{HCLK}$ + 2	ns
$t_{v(NOE_NE)}$	XMC_NE low to XMC_NOE low valid time	$4t_{HCLK}$ - 0.5	$4t_{HCLK}$ + 1.5	ns
$t_{w(NOE)}$	XMC_NOE low time	$4t_{HCLK}$ - 1	$4t_{HCLK}$ + 2	ns
$t_{h(NE_NOE)}$	XMC_NOE high to XMC_NE high hold time	-1	-	ns
$t_{v(A_NE)}$	XMC_NE low to XMC_A valid time	-	7	ns
$t_{v(NADV_NE)}$	XMC_NE low to XMC_NADV low valid time	3	5	ns
$t_{w(NADV)}$	XMC_NADV low time	t_{HCLK} - 1.5	t_{HCLK} + 1.5	ns
$t_{h(AD_NADV)}$	XMC_AD (address) valid hold time after XMC_NADV high	t_{HCLK} + 3	-	ns
$t_{h(A_NOE)}$	Address hold time after XMC_NOE high	t_{HCLK} + 3	-	ns
$t_{h(UBLB_NOE)}$	XMC_UB/LB hold time after XMC_NOE high	0	-	ns
$t_{v(UBLB_NE)}$	XMC_NE low to XMC_UB/LB valid time	-	0	ns
$t_{su(Data_NE)}$	Data to XMC_NE high setup time	$2t_{HCLK}$ + 24	-	ns
$t_{su(Data_NOE)}$	Data to XMC_NOE high setup time	$2t_{HCLK}$ + 25	-	ns
$t_{h(Data_NE)}$	Data hold time after XMC_NE high	0	-	ns
$t_{h(Data_NOE)}$	Data hold time after XMC_NOE high	0	-	ns

Figure 24. Asynchronous multiplexed PSRAM/NOR read waveforms

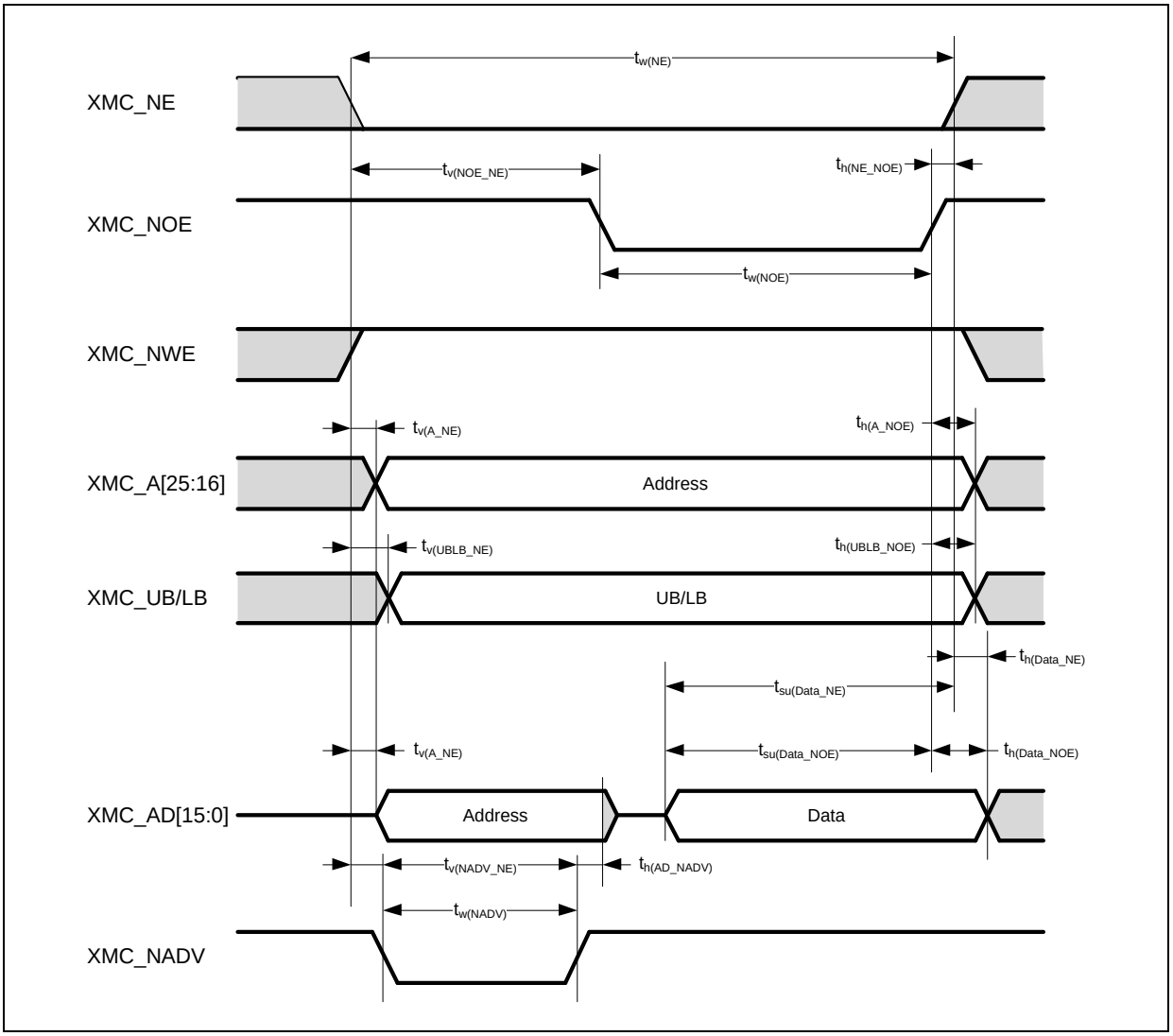
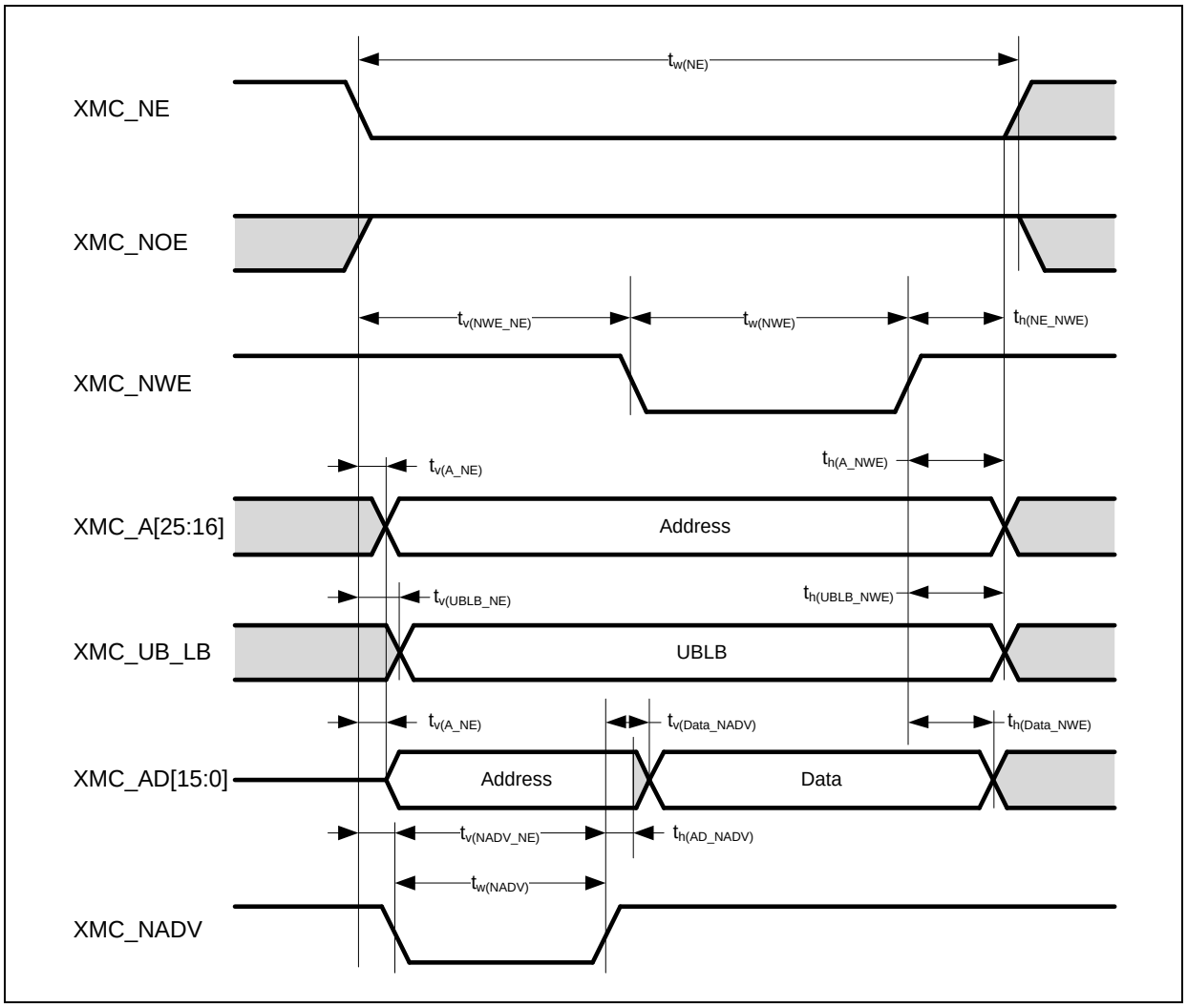


Table 43. Asynchronous multiplexed PSRAM/NOR write timings

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	XMC_NE low time	$7t_{HCLK}$ - 1	$7t_{HCLK}$ + 2	ns
$t_{v(NWE_NE)}$	XMC_NE low to XMC_NWE low valid time	t_{HCLK}- 1	t_{HCLK} + 1	ns
$t_{w(NWE)}$	XMC_NWE low time	$5t_{HCLK}$ - 1	$5t_{HCLK}$ + 2	ns
$t_{h(NE_NWE)}$	XMC_NWE high to XMC_NE high hold time	t_{HCLK} - 1	-	ns
$t_{v(A_NE)}$	XMC_NE low to XMC_A valid time	-	7	ns
$t_{v(NADV_NE)}$	XMC_NE low to XMC_NADV low valid time	3	5	ns
$t_{w(NADV)}$	XMC_NADV low time	t_{HCLK} - 1	t_{HCLK} + 1	ns
$t_{h(AD_NADV)}$	XMC_AD (address) hold time after XMC_NADV high	t_{HCLK} - 3	-	ns
$t_{h(A_NWE)}$	Address hold time after XMC_NWE high	t_{HCLK} - 1.5	-	ns
$t_{h(UBLB_NWE)}$	XMC_UB/LB hold time after XMC_NWE high	t_{HCLK} - 1.5	-	ns
$t_{v(UBLB_NE)}$	XMC_NE low to XMC_UB/LB valid time	-	1.6	ns
$t_{v(Data_NADV)}$	XMC_NADV high to data valid time	-	$2t_{HCLK}$ + 1.5	ns
$t_{h(Data_NWE)}$	Data hold time after XMC_NWE high	t_{HCLK} - 5	-	ns

Figure 25. Asynchronous multiplexed PSRAM/NOR write waveforms



Synchronous waveforms and timings of PSRAM/NOR

The results given in these tables are obtained with the following XMC configuration:

- BurstAccessMode = XMC_BurstAccessMode_Enable
- MemoryType = XMC_MemoryType_CRAM
- WriteBurst = XMC_WriteBurst_Enable
- CLKPrescale = 1 (1 memory cycle = 2 HCLK cycles) (note: CLKPrescale is the CLKPSC bit in the XMC_BK1TMGx register; refer to AT32F435/437 series reference manual)
- DataLatency = 1 for NOR Flash; DataLatency = 0 for PSRAM (note: DataLatency is the DATLAT bit in the XMC_BK1TMGx register; refer to AT32F435/437 series reference manual)

Table 44. Synchronous non-multiplexed PSRAM/NOR read timings

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	XMC_CLK period	20	-	ns
$t_{d(CLKL-NEL)}$	XMC_CLK low to XMC_NE low	-	2	ns
$t_{d(CLKL-NEH)}$	XMC_CLK low to XMC_NE high	1	-	ns
$t_{d(CLKL-NADVL)}$	XMC_CLK low to XMC_NADV low	-	4	ns
$t_{d(CLKL-NADVH)}$	XMC_CLK low to XMC_NADV high	1	-	ns
$t_{d(CLKL-AV)}$	XMC_CLK low to XMC_A valid	-	2	ns
$t_{d(CLKL-AIV)}$	XMC_CLK low to XMC_A invalid	0	-	ns
$t_{d(CLKH-NOEL)}$	XMC_CLK high to XMC_NOE low	-	2	ns
$t_{d(CLKL-NOEH)}$	XMC_CLK low to XMC_NOE high	0.5	-	ns
$t_{su(DV-CLKH)}$	XMC_D valid data before XMC_CLK high	6.5	-	ns
$t_{h(CLKH-DV)}$	XMC_D valid data after XMC_CLK high	7	-	ns
$t_{su(NWAITV-CLKH)}$	XMC_NWAIT valid before XMC_CLK high	7	-	ns
$t_{h(CLKH-NWAITV)}$	XMC_NWAIT valid after XMC_CLK high	2	-	ns

Figure 26. Synchronous non-multiplexed PSRAM/NOR read waveforms

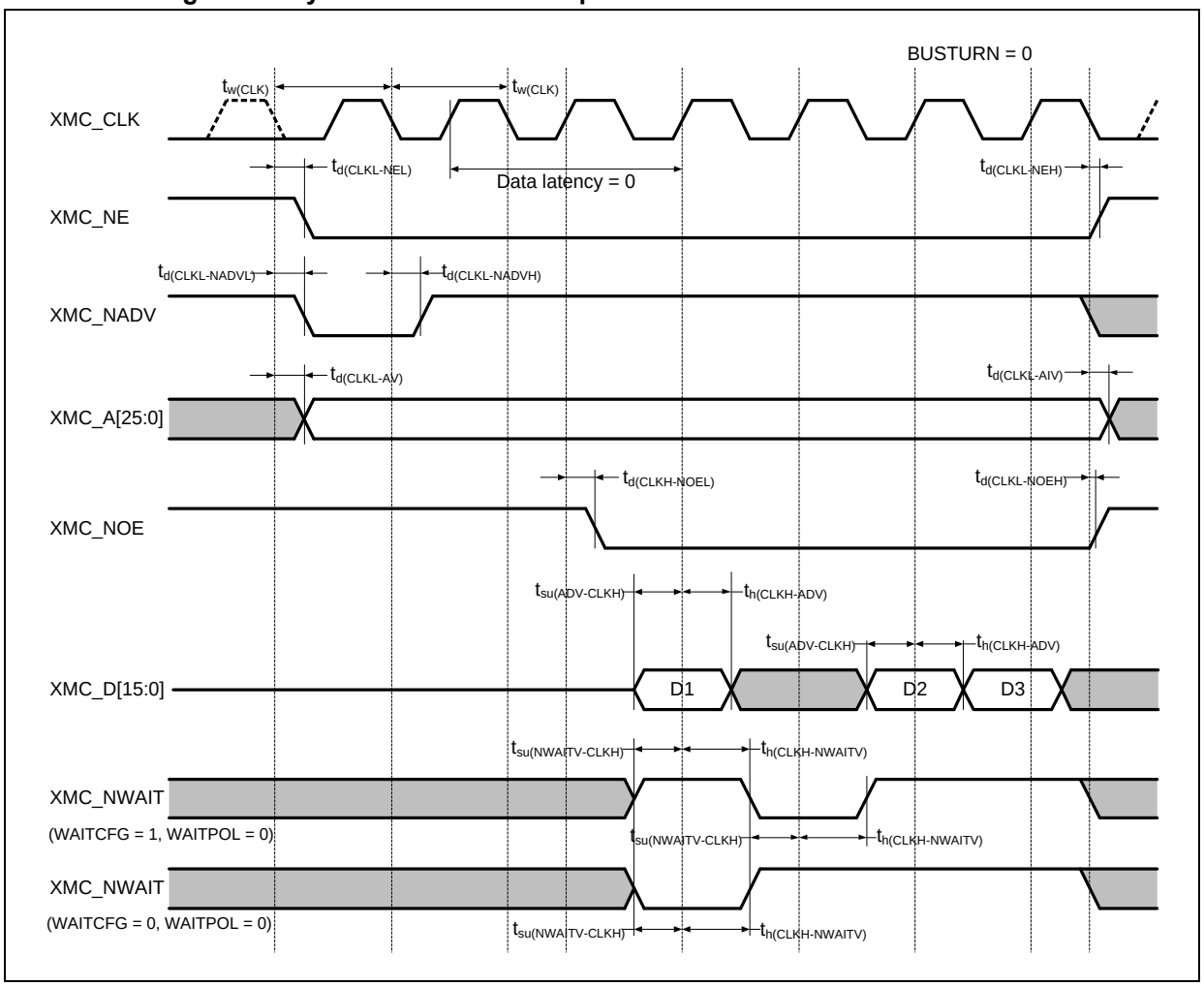


Table 45. Synchronous non-multiplexed PSRAM write timings

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	XMC_CLK period	20	-	ns
$t_{d(CLKL-NEL)}$	XMC_CLK low to XMC_NE low	-	2	ns
$t_{d(CLKL-NEH)}$	XMC_CLK low to XMC_NE high	1	-	ns
$t_{d(CLKL-NADVL)}$	XMC_CLK low to XMC_NADV low	-	4	ns
$t_{d(CLKL-NADVH)}$	XMC_CLK low to XMC_NADV high	1	-	ns
$t_{d(CLKL-AV)}$	XMC_CLK low to XMC_A valid	-	2	ns
$t_{d(CLKL-AIV)}$	XMC_CLK low to XMC_A invalid	0	-	ns
$t_{d(CLKL-NWEL)}$	XMC_CLK low to XMC_NWE low	-	1	ns
$t_{d(CLKL-NWEH)}$	XMC_CLK low to XMC_NWE high	0.5	-	ns
$t_{d(CLKL-Data)}$	XMC_D after XMC_CLK low	-	6	ns
$t_{d(CLKL-UBLBH)}$	XMC_CLK low to XMC_UB/LB high	1.5	-	ns
$t_{su(NWAITV-CLKH)}$	XMC_NWAIT valid before XMC_CLK high	7	-	ns
$t_{h(CLKH-NWAITV)}$	XMC_NWAIT valid after XMC_CLK high	2	-	ns

Figure 27. Synchronous non-multiplexed PSRAM write waveforms

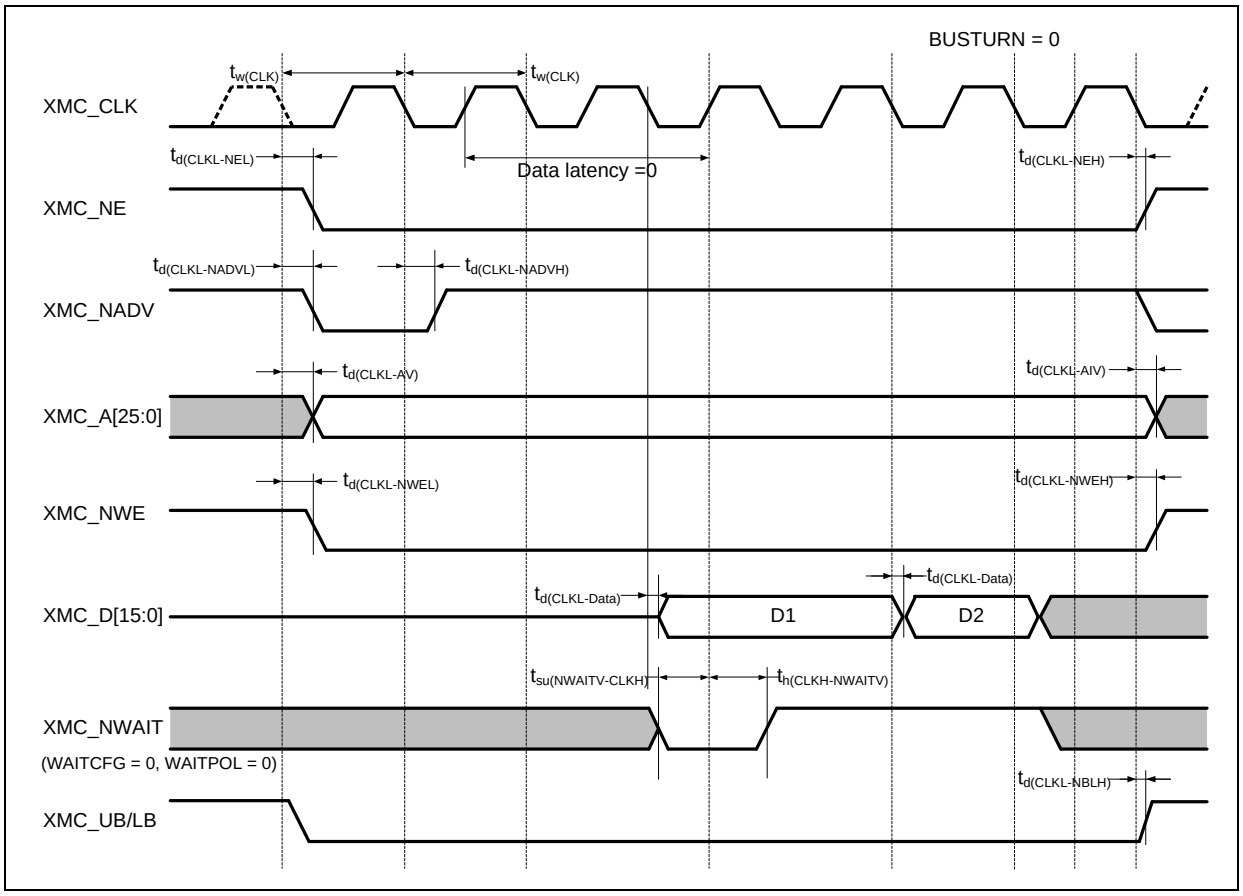


Table 46. Synchronous multiplexed PSRAM/NOR read timings

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	XMC_CLK period	20	-	ns
$t_{d(CLKL-NEL)}$	XMC_CLK low to XMC_NE low	-	2	ns
$t_{d(CLKL-NEH)}$	XMC_CLK low to XMC_NE high	1	-	ns
$t_{d(CLKL-NADVL)}$	XMC_CLK low to XMC_NADV low	-	4	ns
$t_{d(CLKL-NADVH)}$	XMC_CLK low to XMC_NADV high	1	-	ns
$t_{d(CLKL-AV)}$	XMC_CLK low to XMC_A valid	-	2	ns
$t_{d(CLKL-AIV)}$	XMC_CLK low to XMC_A invalid	0	-	ns
$t_{d(CLKH-NOEL)}$	XMC_CLK high to XMC_NOE low	-	1	ns
$t_{d(CLKL-NOEH)}$	XMC_CLK low to XMC_NOE high	0.5	-	ns
$t_{d(CLKL-ADV)}$	XMC_CLK low to XMC_AD valid	-	12	ns
$t_{d(CLKL-ADIV)}$	XMC_CLK low to XMC_AD invalid	0	-	ns
$t_{su(ADV-CLKH)}$	XMC_AD valid before XMC_CLK high	6	-	ns
$t_{h(CLKH-ADV)}$	XMC_AD valid after XMC_CLK high	6	-	ns
$t_{su(NWAITV-CLKH)}$	XMC_NWAIT valid before XMC_CLK high	8	-	ns
$t_{h(CLKH-NWAITV)}$	XMC_NWAIT valid after XMC_CLK high	6	-	ns

Figure 28. Synchronous multiplexed PSRAM/NOR read waveforms

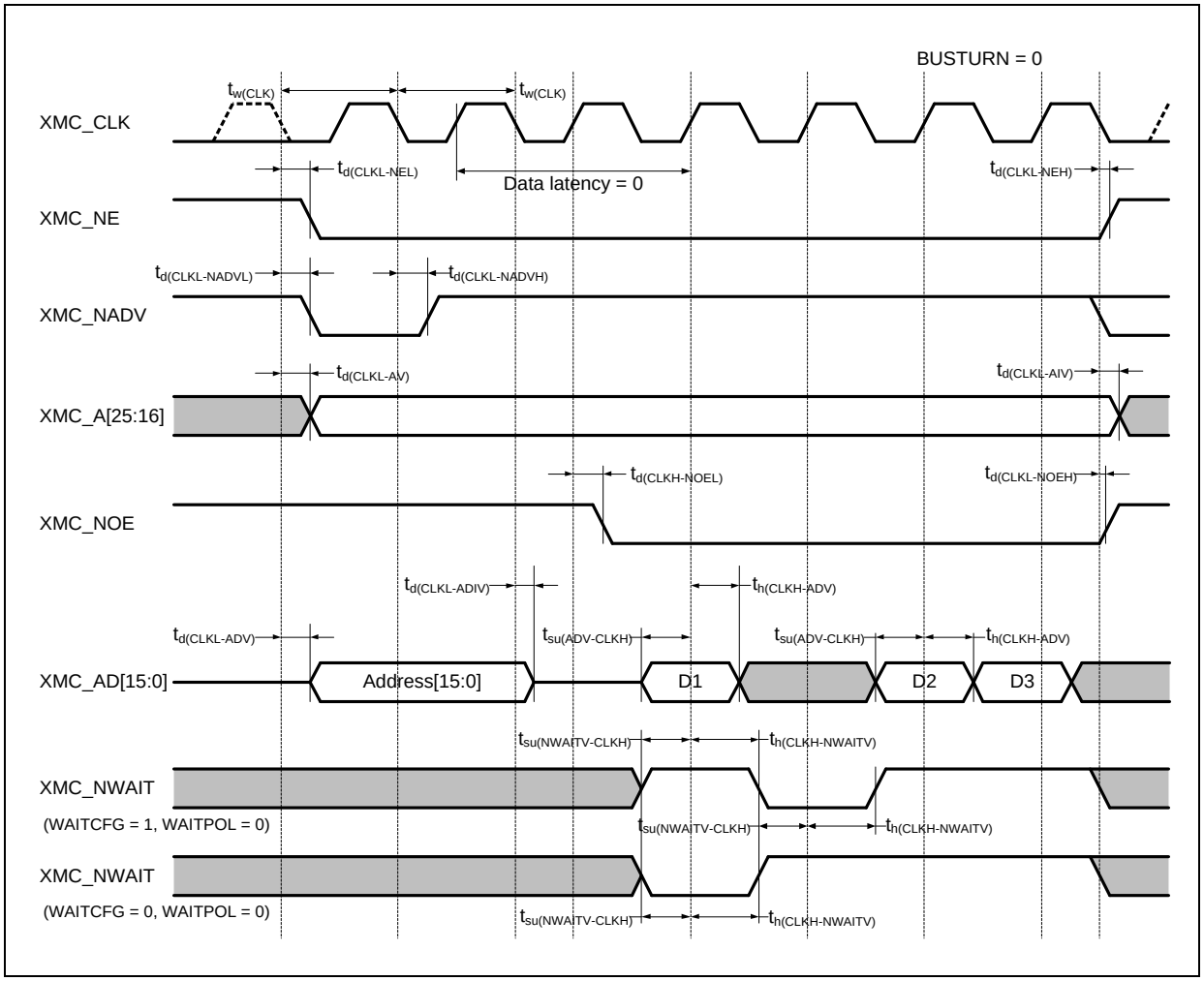
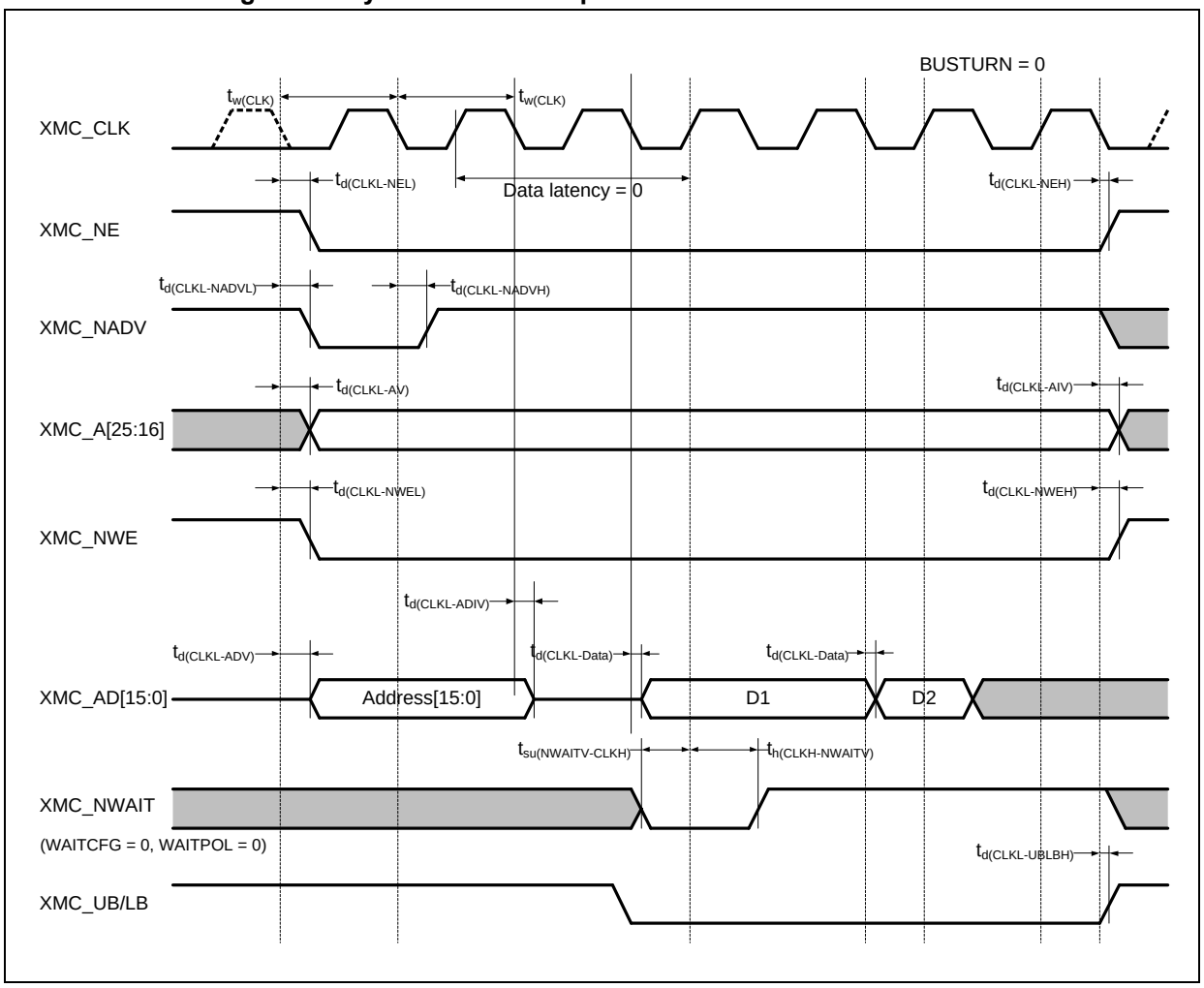


Table 47. Synchronous multiplexed PSRAM write timings

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	XMC_CLK period	20	-	ns
$t_{d(CLKL-NEL)}$	XMC_CLK low to XMC_NE low	-	2	ns
$t_{d(CLKL-NEH)}$	XMC_CLK low to XMC_NE high	1	-	ns
$t_{d(CLKL-NADVL)}$	XMC_CLK low to XMC_NADV low	-	4	ns
$t_{d(CLKL-NADVH)}$	XMC_CLK low to XMC_NADV high	1	-	ns
$t_{d(CLKL-AV)}$	XMC_CLK low to XMC_A valid	-	2	ns
$t_{d(CLKL-AIV)}$	XMC_CLK low to XMC_A invalid	0	-	ns
$t_{d(CLKL-NWEL)}$	XMC_CLK low to XMC_NWE low	-	1	ns
$t_{d(CLKL-NWEH)}$	XMC_CLK low to XMC_NWE high	0.5	-	ns
$t_{d(CLKL-ADV)}$	XMC_CLK low to XMC_AD valid	-	12	ns
$t_{d(CLKL-ADIV)}$	XMC_CLK low to XMC_AD invalid	3	-	ns
$t_{d(CLKL-Data)}$	XMC_AD after XMC_CLK low	-	6	ns
$t_{d(CLKL-UBLBH)}$	XMC_CLK low to XMC_UB/LB high	1	-	ns
$t_{su(NWAITV-CLKH)}$	XMC_NWAIT valid before XMC_CLK high	8	-	ns
$t_{h(CLKH-NWAITV)}$	XMC_NWAIT valid after XMC_CLK high	6	-	ns

Figure 29. Synchronous multiplexed PSRAM write waveforms



NAND controller waveforms and timings

The results given in the table below are obtained with the following XMC configuration:

- COM.XMC_SetupTime = 0x01 (note: STP in XMC_BKxTMGMEM)
- COM.XMC_WaitSetupTime = 0x03 (note: OP in XMC_BKxTMGMEM)
- COM.XMC_HoldSetupTime = 0x02 (note: HLD in XMC_BKxTMGMEM)
- COM.XMC_HiZSetupTime = 0x01 (note: WRSTP in XMC_BKxTMGMEM)
- ATT.XMC_SetupTime = 0x01 (note: STP in XMC_BKxTMGATT)
- ATT.XMC_WaitSetupTime = 0x03 (note: OP in XMC_BKxTMGATT)
- ATT.XMC_HoldSetupTime = 0x02 (note: HLD in XMC_BKxTMGATT)
- ATT.XMC_HiZSetupTime = 0x01 (note: WRSTP in XMC_BKxTMGATT)
- Bank = XMC_Bank_NAND
- MemoryDataWidth = XMC_MemoryDataWidth_16b (note: memory data width = 16 bits)
- ECC = XMC_ECC_Enable (note: enable ECC calculation)
- ECCPageSize = XMC_ECCPageSize_512Bytes (note: ECC page size = 512 bytes)
- DLYCRSetupTime = 0 (note: DLYCR in XMC_BKxCTRL)
- DLYARSetupTime = 0 (note: DLYAR in XMC_BKxCTRL)

Table 48. NAND Flash read and write timings

Symbol	Parameter	Min	Max	Unit
$t_{w(NOE)}$	XMC_NOE low width	$4t_{HCLK}$ - 1.5	$4t_{HCLK}$ + 1.5	ns
$t_{su(D-NOE)}$	XMC_Dx valid data before XMC_NOE high	25	-	ns
$t_{h(NOE-D)}$	XMC_Dx valid data after XMC_NOE high	14	-	ns
$t_{d(ALE-NOE)}$	XMC_ALE valid before XMC_NOE low	-	$3t_{HCLK}$ + 2	ns
$t_{h(NOE-ALE)}$	XMC_NOE high to XMC_ALE invalid	$3t_{HCLK}$ + 4.5	-	ns
$t_{w(NWE)}$	XMC_NWE low width	$4t_{HCLK}$ - 1	$4t_{HCLK}$ + 2.5	ns
$t_{v(NWE-D)}$	XMC_NWE low to XMC_Dx valid	-	0	ns
$t_{h(NWE-D)}$	XMC_NWE high to XMC_Dx invalid	$10t_{HCLK}$ + 4	-	ns
$t_{d(D-NWE)}$	XMC_Dx valid data before XMC_NWE high	$6t_{HCLK}$ + 12	-	ns
$t_{d(ALE-NWE)}$	XMC_ALE valid before XMC_NWE low	-	$3t_{HCLK}$ + 1.5	ns
$t_{h(NWE-ALE)}$	XMC_NWE high to XMC_ALE invalid	$3t_{HCLK}$ + 4.5	-	ns

Figure 30. NAND controller read waveforms

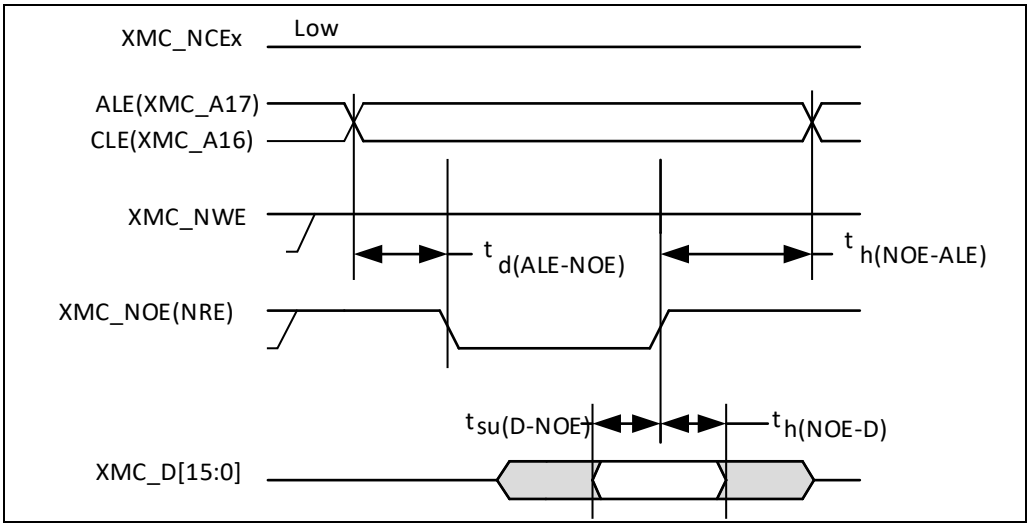


Figure 31. NAND controller write waveforms

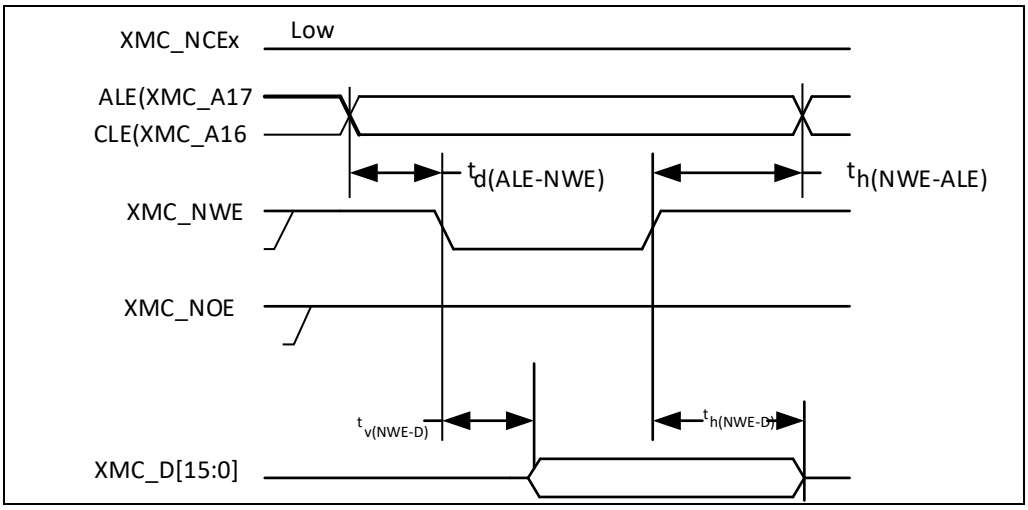


Figure 32. NAND controller common memory read waveforms

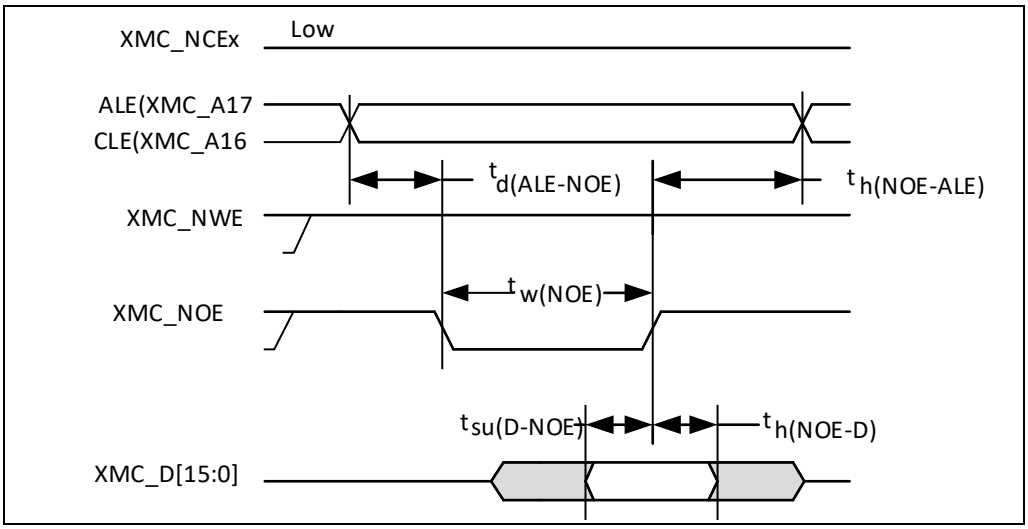
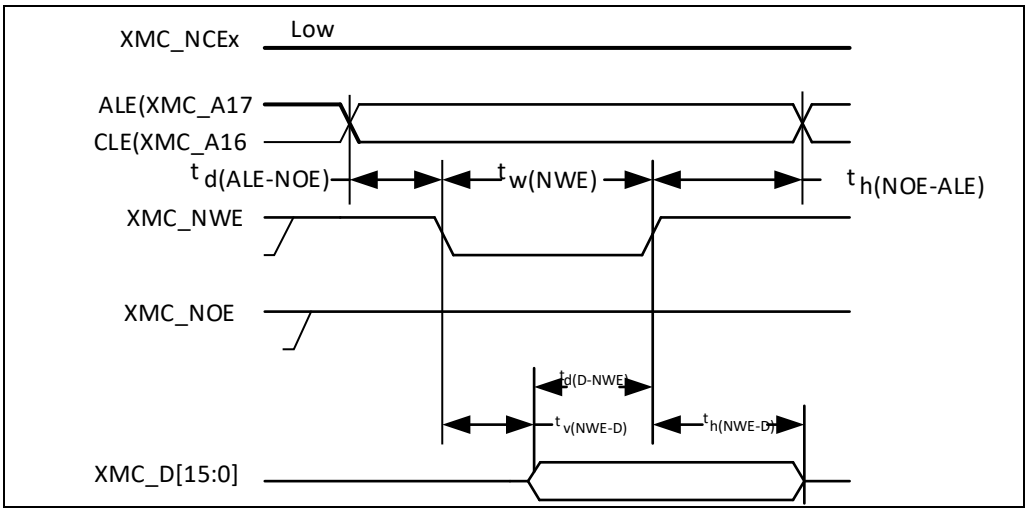


Figure 33. NAND controller for common memory write waveforms



PC card /CF card controller timings and waveforms

The results given in the table below are obtained with the following XMC configuration:

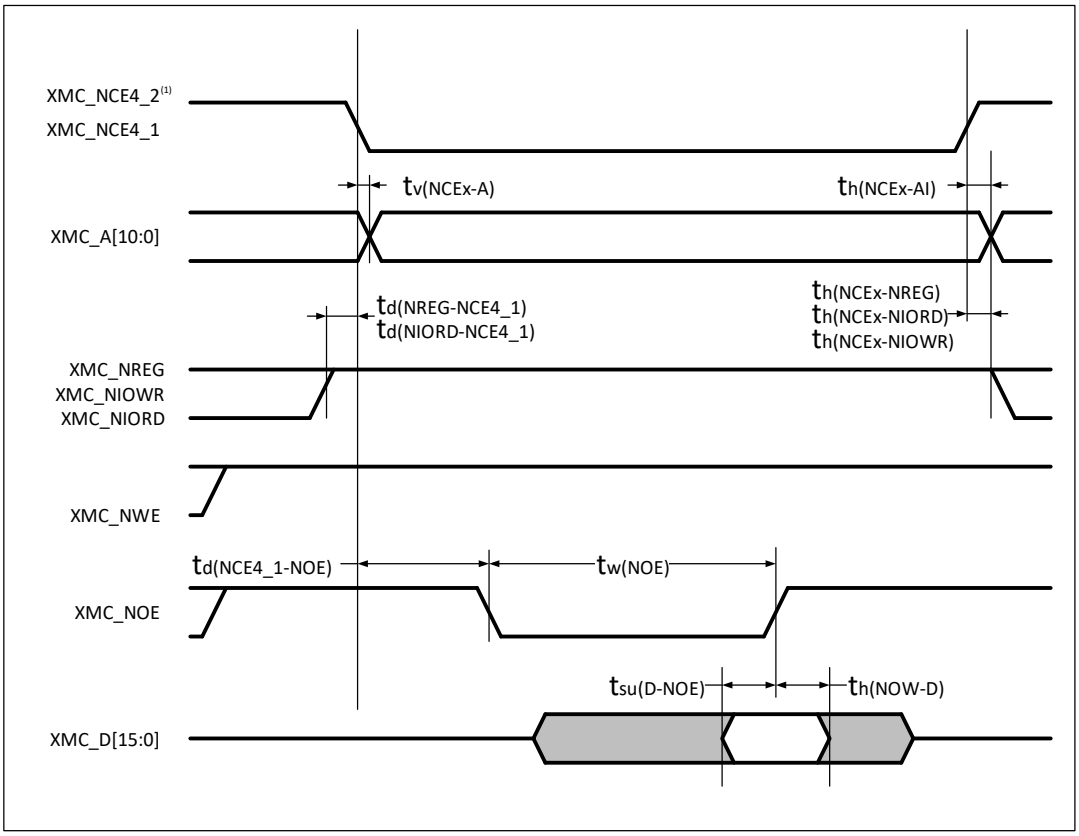
- COM.XMC_SetupTime = 0x04 (note: STP in XMC_BKxTMGMEM, x = 2…4)
- COM.XMC_WaitSetupTime = 0x07 (note: OP in XMC_BKxTMGMEM, x = 2…4)
- COM.XMC_HoldSetupTime = 0x04 (note: HLD in XMC_BKxTMGMEM, x = 2…4)
- COM.XMC_HiZSetupTime = 0x00 (note: WRSTP in XMC_BKxTMGMEM, x = 2…4)
- ATT.XMC_SetupTime = 0x04 (note: STP in XMC_BKxTMGATT, x = 2…4)
- ATT.XMC_WaitSetupTime = 0x07 (note: OP in XMC_BKxTMGATT, x = 2…4)
- ATT.XMC_HoldSetupTime = 0x04 (note: HLD in XMC_BKxTMGATT, x = 2…4)
- ATT.XMC_HiZSetupTime = 0x00 (note: WRSTP in XMC_BKxTMGATT, x = 2…4)
- IO.XMC_SetupTime = 0x04 (note: STP in XMC_BKxTMGIO, x = 4)
- IO.XMC_WaitSetupTime = 0x07 (note: OP in XMC_BKxTMGIO, x = 4)
- IO.XMC_HoldSetupTime = 0x04 (note: HLD in XMC_BKxTMGIO, x = 4)
- IO.XMC_HiZSetupTime = 0x00 (note: WRSTP in XMC_BKxTMGIO, x = 4)
- DLYCRSetupTime = 0 (note: DLYCR in XMC_BKxCTRL)
- DLYARSetupTime = 0 (note: DLYAR in XMC_BKxCTRL)

Note: Refer to the AT32F435/437 reference manual about the description of registers above (XMC_BKXTMGMEMx, XMC_BKxTMGATT, XMC_BKxTMGIO and XMC_BKxCTRL).

Table 49. PC card /CF read and write timings

Symbol	Parameter	Min	Max	Unit
$t_{v(NCEx-A)}$	XMC_NCEx low to XMC_Ax valid	-	0	ns
$t_{h(NCEx-AI)}$	XMC_NCEx high to XMC_Ax invalid	0	-	ns
$t_{d(NREG-NCEx)}$	XMC_NCEx low to XMC_NREG valid	-	2	ns
$t_{h(NCEx-NREG)}$	XMC_NCEx high to XMC_NREG invalid	t_{HCLK} + 4	-	ns
$t_{d(NCEx-NWE)}$	XMC_NCEx low to XMC_NWE low	-	$5t_{HCLK}$ + 1	ns
$t_{d(NCEx-NOE)}$	XMC_NCEx low to XMC_NOE low	-	$5t_{HCLK}$ + 1	ns
$t_{w(NOE)}$	XMC_NOE low width	$8t_{HCLK}$ - 0.5	$8t_{HCLK}$ + 1	ns
$t_{d(NOE -NCEx)}$	XMC_NOE high to XMC_NCEx high	$5t_{HCLK}$ – 0.5	-	ns
$t_{su(D-NOE)}$	XMC_Dx valid data before XMC_NOE high	32	-	ns
$t_{h(NOE-D)}$	XMC_Dx invalid data after XMC_NOE high	t_{HCLK}	-	ns
$t_{w(NWE)}$	XMC_NWE low width	$8t_{HCLK}$ - 1	$8t_{HCLK}$ + 4	ns
$t_{d(NWE-NCEx)}$	XMC_NWE high to XMC_NCEx high	$5t_{HCLK}$ + 1.5	-	ns
$t_{d(NCEx-NWE)}$	XMC_NCEx low to XMC_NWE low	-	$5t_{HCLK}$ + 1	ns
$t_{v(NWE-D)}$	XMC_NWE low to XMC_Dx valid	-	0	ns
$t_{h(NWE-D)}$	XMC_NWE high to XMC_Dx invalid	$11t_{HCLK}$	-	ns
$t_{d(D-NWE)}$	XMC_Dx valid data before XMC_NWE high	$13t_{HCLK}$ + 2.5	-	ns
$t_{w(NIOWR)}$	XMC_NIOWR low width	$8t_{HCLK}$	-	ns
$t_{v(NIOWR-D)}$	XMC_NIOWR low to XMC_Dx valid	-	$5t_{HCLK}$ - 4	ns
$t_{h(NIOWR-D)}$	XMC_NIOWR high to XMC_Dx invalid	$11t_{HCLK}$	-	ns
$t_{d(NCEx-NIOWR)}$	XMC_NCEx low to XMC_NIOWR valid			
$t_{h(NCEx-NIOWR)}$	XMC_NCEx high to XMC_NIOWR invalid	$5t_{HCLK}$ - 7	-	ns
$t_{d(NIORD-NCEx)}$	XMC_NCEx low to XMC_NIORD valid	-	$5t_{HCLK}$ + 1	ns
$t_{h(NCEx-NIORD)}$	XMC_NCEx high to XMC_NIORD invalid	$5t_{HCLK}$ – 0.5	-	ns
$t_{w(NIORD)}$	XMC_NIORD low width	$8t_{HCLK}$	-	ns
$t_{su(D-NIORD)}$	XMC_Dx valid before XMC_NIORD high	28	-	ns
$t_{d(NIORD-D)}$	XMC_Dx valid after XMC_NIORD high	3	-	ns

Figure 34. PC card/CF controller waveforms for common memory read access



(1) XMC_NCE4_2 remains low (inactive during 8-bit access).

Figure 35. PC card/CF controller waveforms for common memory write access

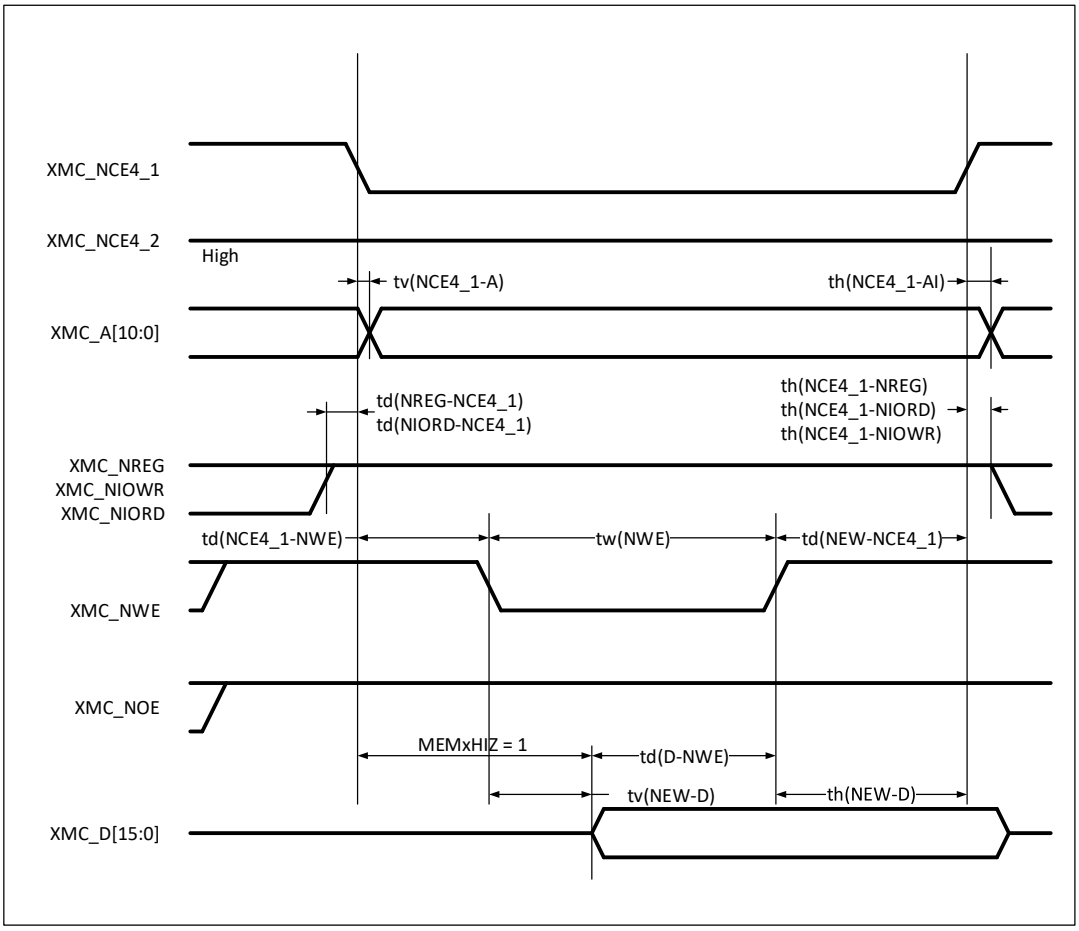
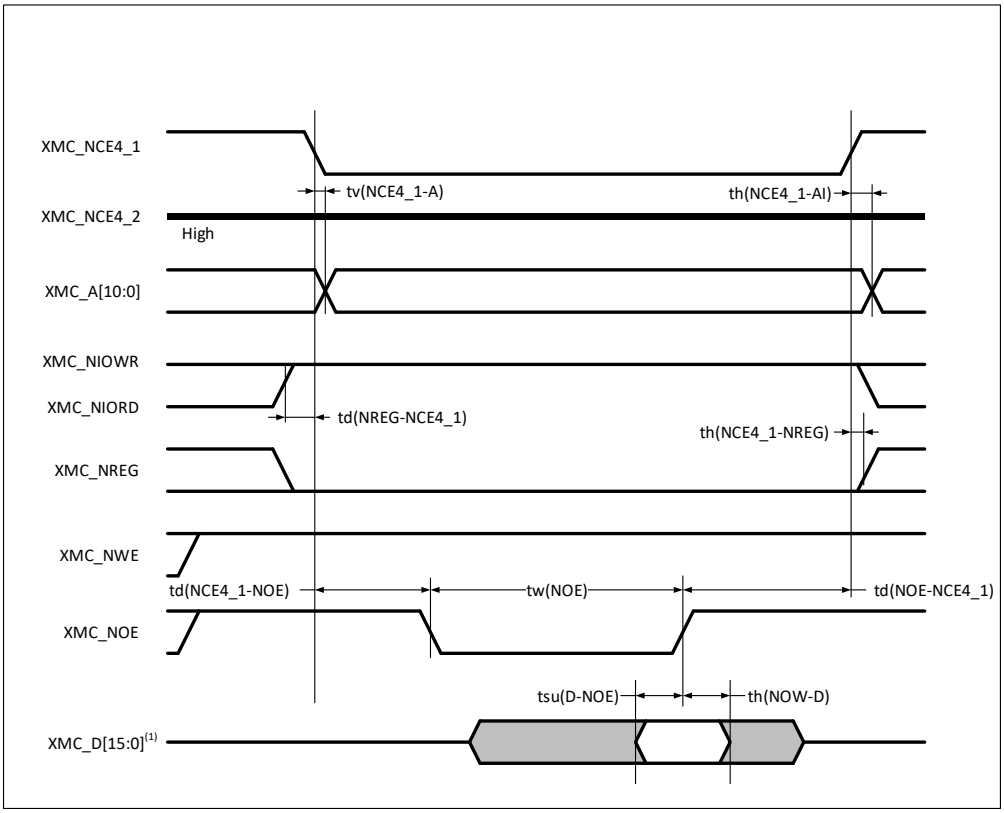
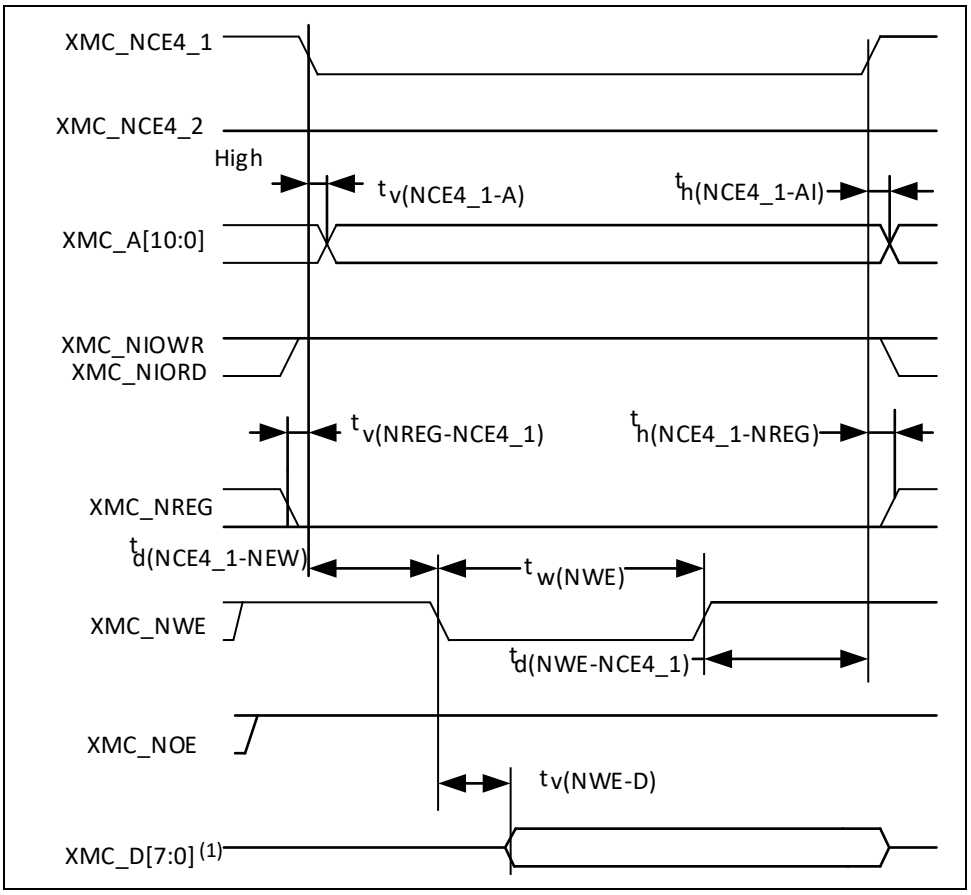


Figure 36. PC card/CF controller waveforms for attribute memory read access



(1) Only data bits 0~7 are read (bits 8~15 disregarded).

Figure 37. PC card/CF controller waveforms for attribute memory write access



(1) Only data bits 0~7 are driven (bits 8~15 remains HiZ).

Figure 38. PC card /CF controller waveforms for I/O space read access

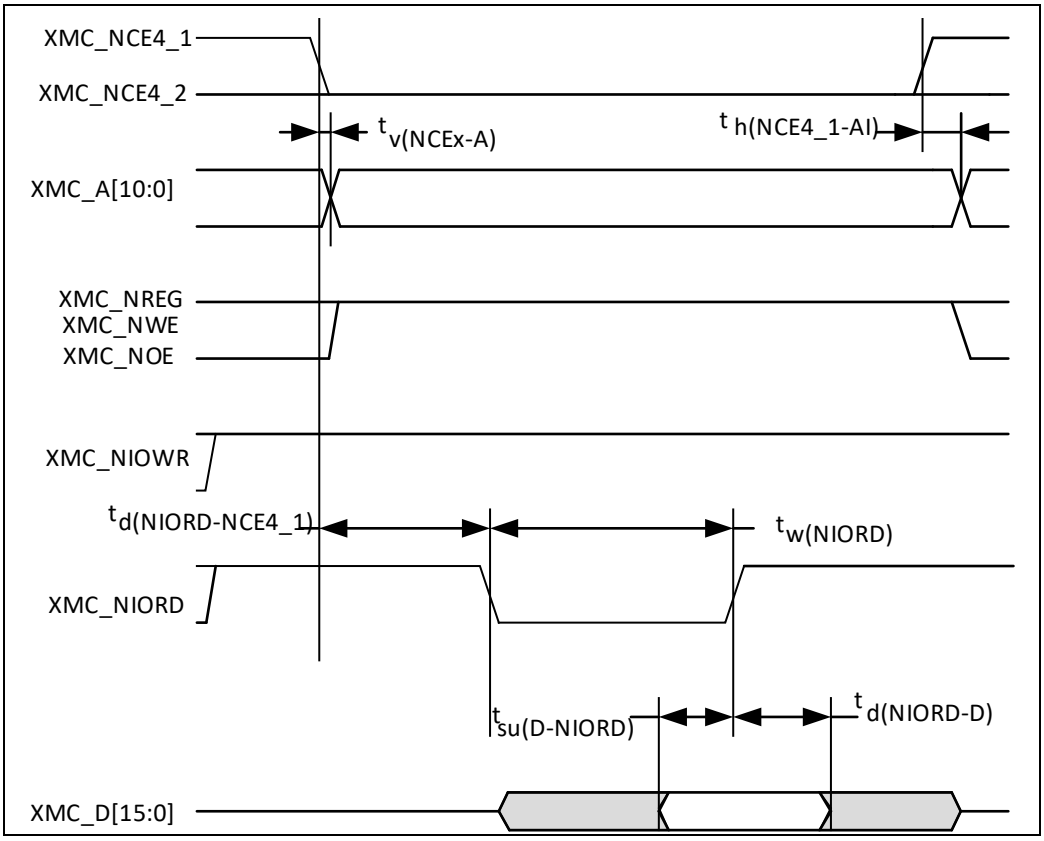
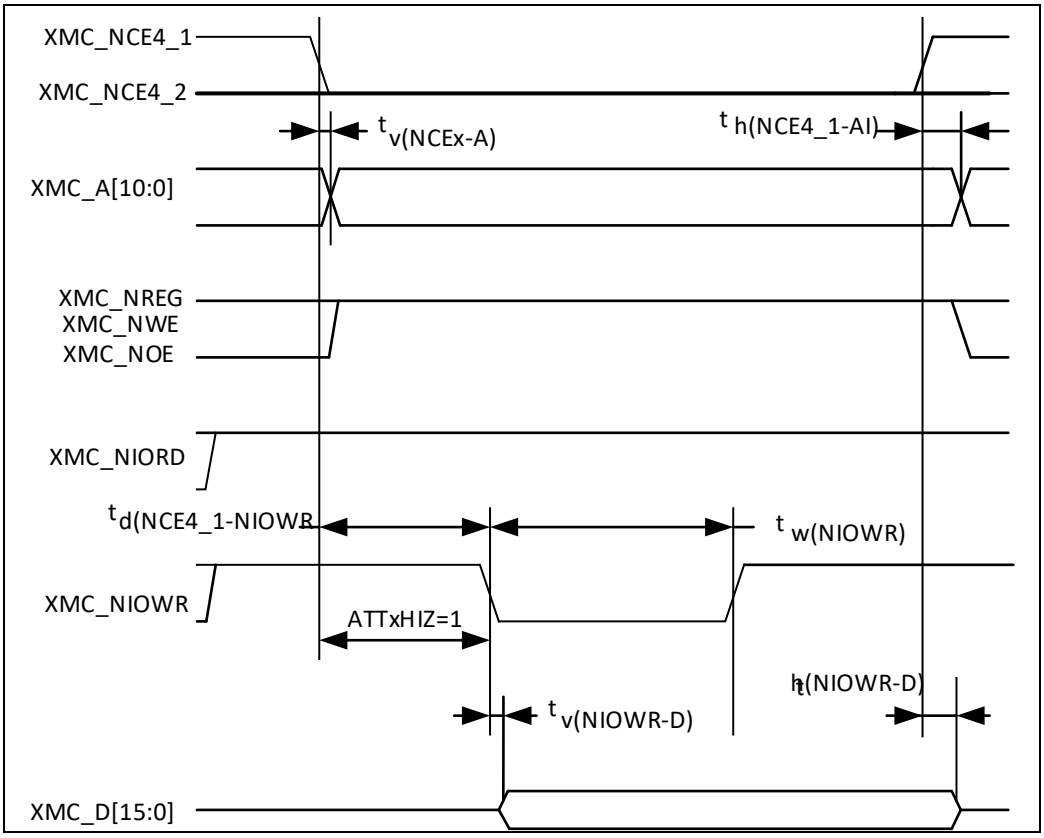


Figure 39. PC card/CF controller waveforms for I/O space write access



SDRAM controller timings and waveforms

Table 50. SDRAM read timings

Symbol	Parameter	Min	Max	Unit
$1/t_{w(SDCLK)}$	SDCLK frequency	-	100	MHz
$t_{su(SDCLKH_Data)}$	Input data setup time	2	-	ns
$t_{h(SDCLKH_Data)}$	Input data hold time	0	-	ns
$t_{d(SDCLKL_Add)}$	Address valid time	-	1.5	ns
$t_{d(SDCLKL_SDCS)}$	SDCS valid time	-	1	ns
$t_{h(SDCLKL_SDCS)}$	SDCS hold time	0	-	ns
$t_{d(SDCLKL_SDNRAS)}$	SDNRAS valid time	-	1	ns
$t_{h(SDCLKL_SDNRAS)}$	SDNRAS hold time	0	-	ns
$t_{d(SDCLKL_SDNCAS)}$	SDNCAS valid time	-	1	ns
$t_{h(SDCLKL_SDNCAS)}$	SDNCAS hold time	0	-	ns

Figure 40. SDRAM read waveforms

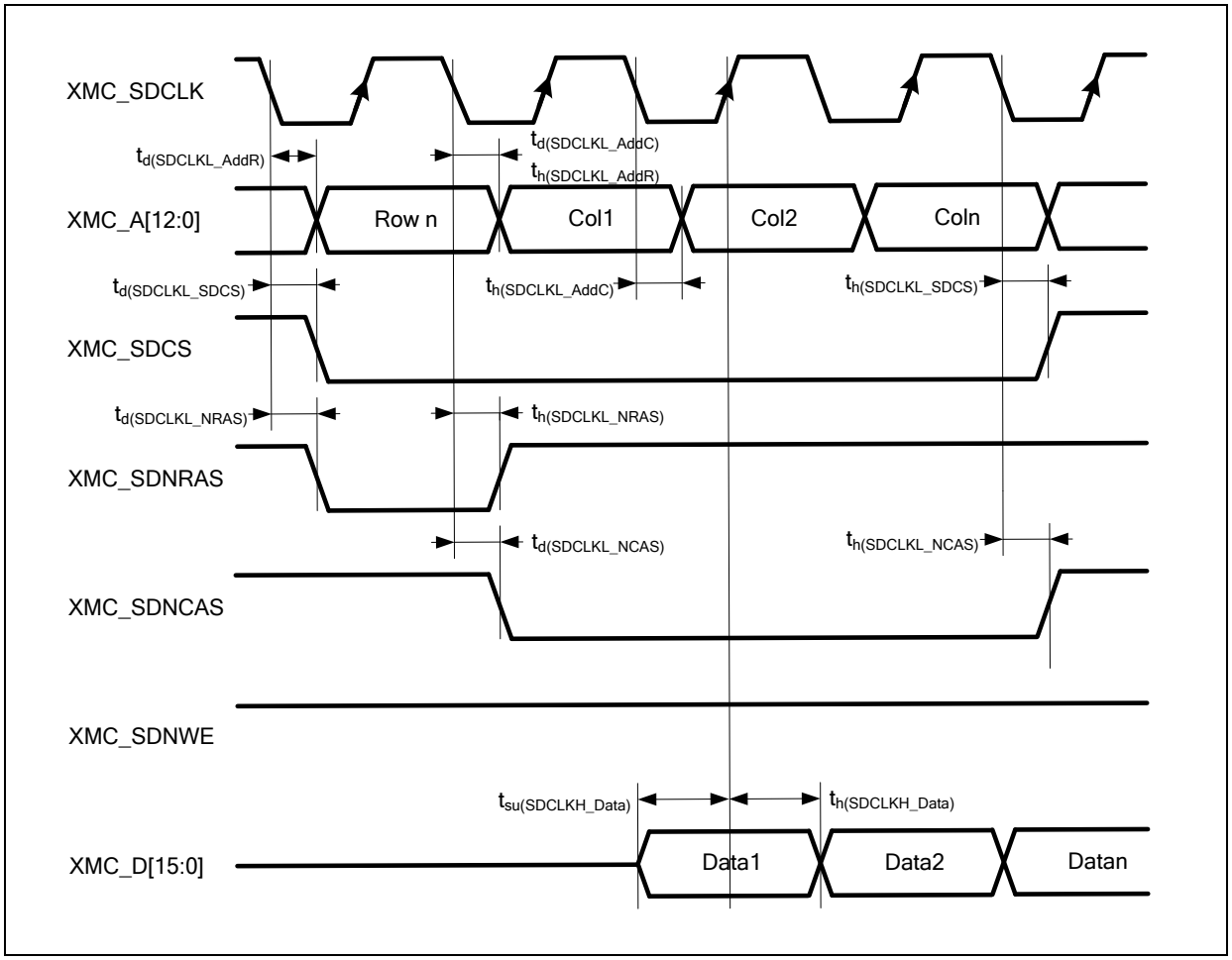
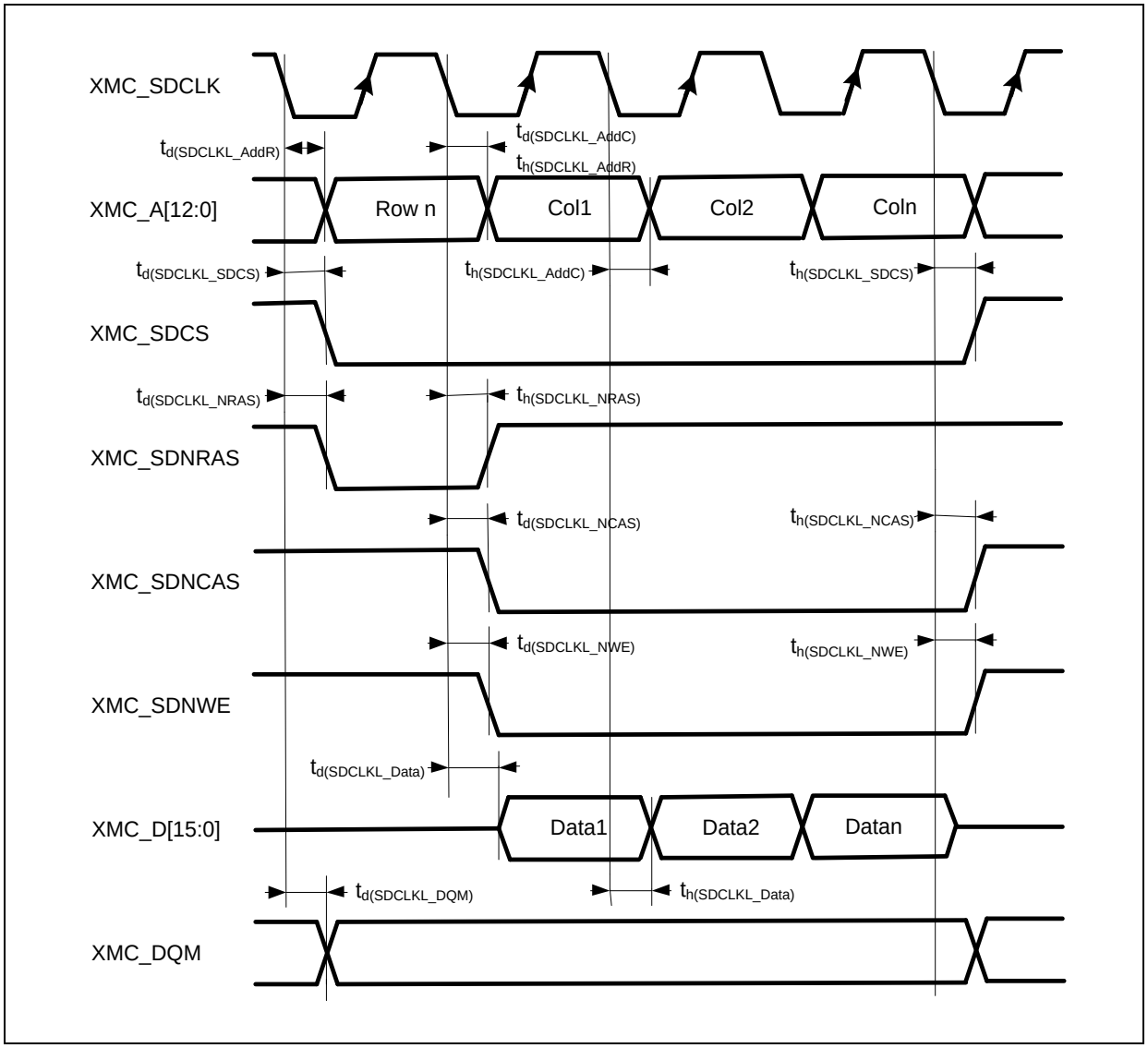


Table 51. SDRAM write timings

Symbol	Parameter	Min	Max	Unit
$1/t_{w(SDCLK)}$	SDCLK frequency	-	100	MHz
$t_{d(SDCLKL_Data)}$	Output data valid time	-	2.5	ns
$t_{h(SDCLKL_Data)}$	Output data hold time	-1	-	ns
$t_{d(SDCLKL_Add)}$	Address valid time	-	1.5	ns
$t_{d(SDCLKL_SDNWE)}$	SDNWE valid time	-	1	ns
$t_{h(SDCLKL_SDNWE)}$	SDNWE hold time	0	-	ns
$t_{d(SDCLKL_SDCS)}$	SDCS valid time	-	1	ns
$t_{h(SDCLKL_SDCS)}$	SDCS hold time	0	-	ns
$t_{d(SDCLKL_SDNRAS)}$	SDNRAS valid time	-	1	ns
$t_{h(SDCLKL_SDNRAS)}$	SDNRAS hold time	0	-	ns
$t_{d(SDCLKL_SDNCAS)}$	SDNCAS valid time	-	1	ns
$t_{h(SDCLKL_SDNCAS)}$	SDNCAS hold time	0	-	ns
$t_{d(SDCLKL_DQM)}$	DQM valid time	-	1	ns
$t_{h(SDCLKL_DQM)}$	DQM hold time	0	-	ns

Figure 41. SDRAM write waveforms



5.3.14 TMR characteristics

The parameters given in the table below are guaranteed by design.

Table 52. TMR characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{res(TMR)}$	Timer resolution time	-	1	-	$t_{TMRxCLK}$
		$f_{TMRxCLK}$ = 288 MHz	3.47	-	ns
f_{EXT}	Timer external clock frequency on CH1 to CH4	-	0	$f_{TMRxCLK}/2$	MHz

5.3.15 SPI characteristics

The t_{PCLK} refers to the APB clock cycle (APB1 or PAB2) connected with SPI.

Table 53. SPI characteristics(1)

Symbol	Parameter	Conditions		Min	Max	Unit
f_{SCK} $(1/t_{c(SCK)})$(2)(3)	SPI clock frequency	Master mode	Prescaler ≠ 3	-	50	MHz
			Prescaler = 3	-	40	
		Slave receive mode	Prescaler ≠ 3	-	36	
			Prescaler = 3	-	32	
		Slave transmit mode		-	32	
$t_{su(CS)}$	CS setup time	Slave mode		$2t_{PCLK}$	-	ns
$t_{h(CS)}$	CS hold time	Slave mode		$2t_{PCLK}$	-	ns
$t_{w(SCKH)}$ $t_{w(SCKL)}$	SCK high and low time	Master mode, prescaler factor = N		(N / 2) x t_{PCLK} - 3	(N / 2) x t_{PCLK} + 3	ns
$Duty_{(SCK)}$	SCK duty cycle	Master mode	$f_{PCLK} = f_{HCLK}$	45	55	%
			$f_{PCLK} = f_{HCLK}$ / 2, prescaler ≠ 3			
			$f_{PCLK} = f_{HCLK}$ / 2, prescaler = 3	40	60	
$t_{su(MI)}$	Data input setup time	Master mode		6	-	ns
$t_{su(SI)}$		Slave mode		5	-	
$t_{h(MI)}$	Data input hold time	Master mode		4	-	ns
$t_{h(SI)}$		Slave mode		5	-	
$t_{a(SO)}$(4)	Data output access time	Slave mode		t_{PCLK}	$2t_{PCLK}$ + 25	ns
$t_{dis(SO)}$(5)	Data output disable time	Slave mode		t_{PCLK}	$2t_{PCLK}$ + 25	ns
$t_{v(SO)}$	Data output valid time	Slave mode (after enable edge)		-	25	ns
$t_{v(MO)}$	Data output valid time	Master mode (after enable edge)		-	10	ns
$t_{h(SO)}$	Data output hold time	Slave mode (after enable edge)		9	-	ns
$t_{h(MO)}$		Master mode (after enable edge)		2	-	

(1) Guaranteed by design, not tested in production.
(2) The maximum SPI clock frequency should not exceed $f_{PCLK}/2$.
(3) Guaranteed by characterization results, not tested in production. The maximum SPI clock frequency is highly related with devices and the PCB layout. For more details about the complete solution, please contact your local Artery sales representative.
(4) Min time is for the minimum time to drive the output and the max time is for the maximum time to validate the data.
(5) Min time is for the minimum time to invalidate the output and the max time is for the maximum time to put the data in Hi-Z.

Figure 42. SPI timing diagram – slave mode and CPHA = 0

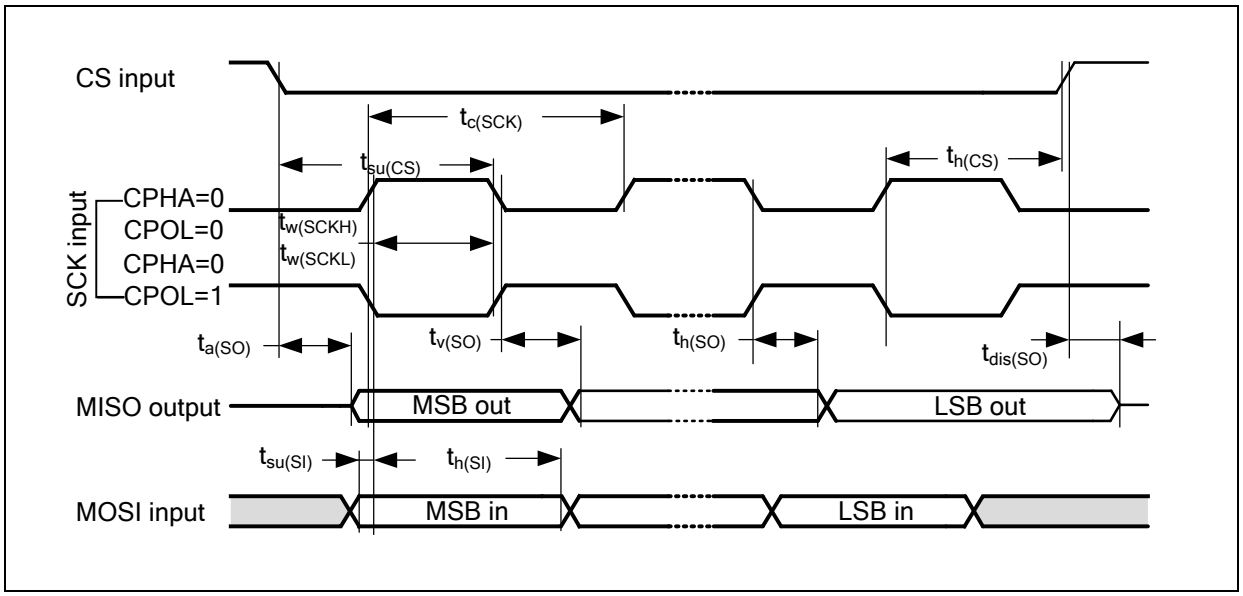


Figure 43. SPI timing diagram – slave mode and CPHA = 1

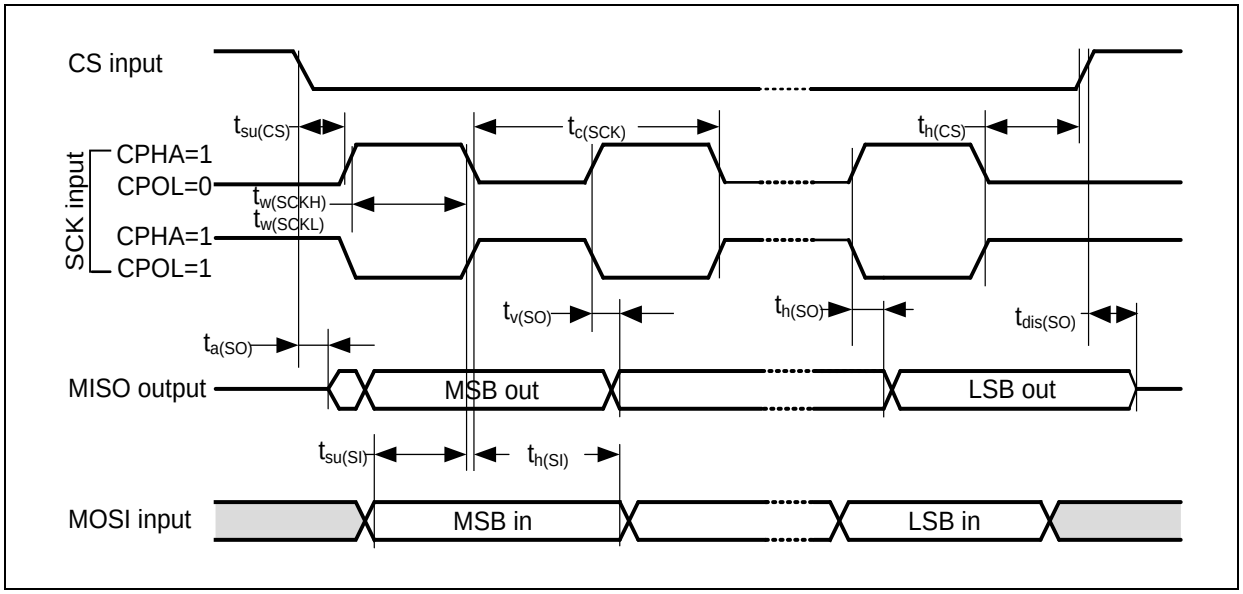
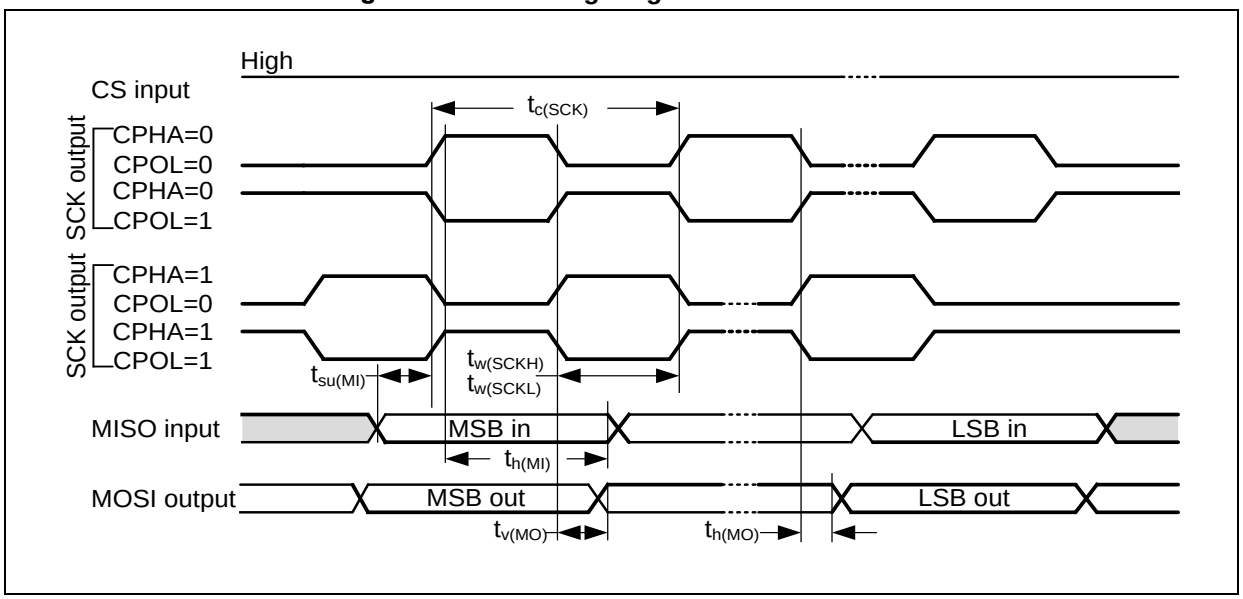


Figure 44. SPI timing diagram – master mode



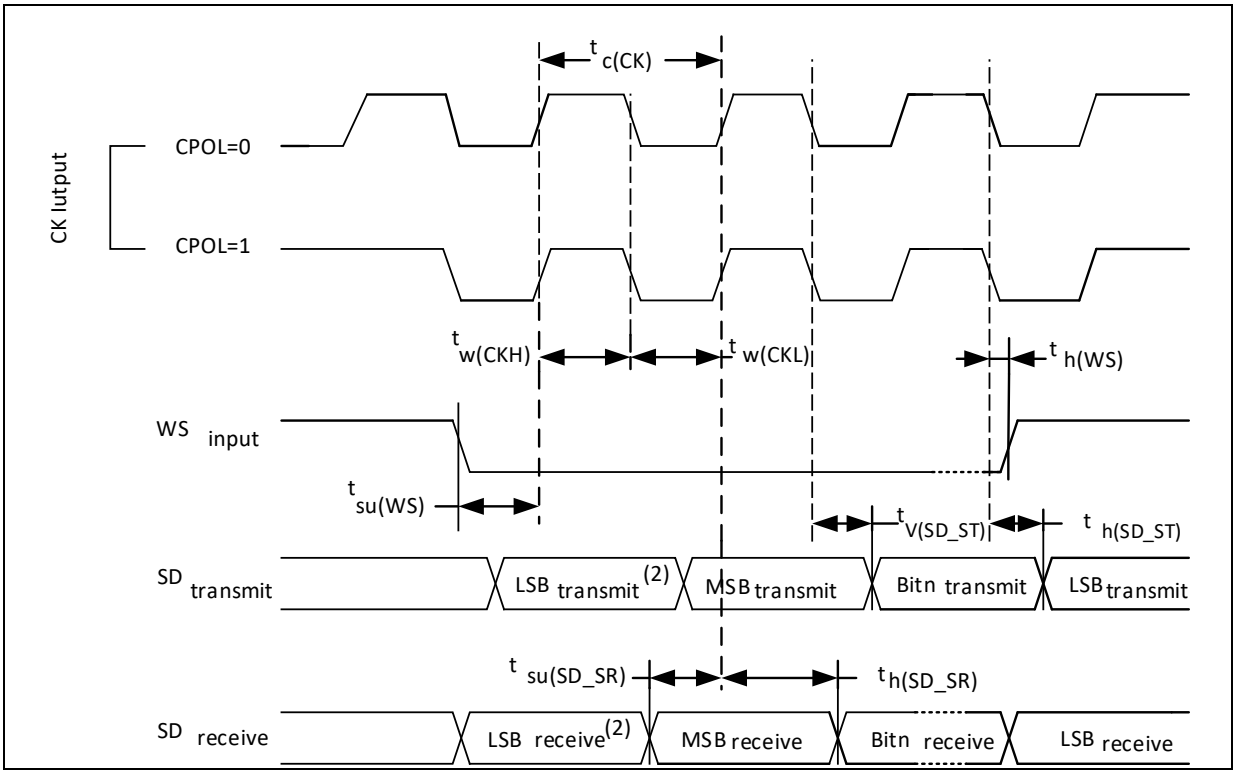
5.3.16 I²S characteristics

Table 54. I²S characteristics(1)

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{r(CK)}$ $t_{f(CK)}$	I²S clock rise and fall time	Capacitive load: C = 15 pF	-	12	ns
$t_{v(WS)}$	WS valid time	Master mode	0	4	
$t_{h(WS)}$	WS hold time	Master mode	0	4	
$t_{su(WS)}$	WS setup time	Slave mode	9	-	
$t_{h(WS)}$	WS hold time	Slave mode	0	-	
$t_{su(SD_MR)}$	Data input setup time	Master receiver	6	-	
$t_{su(SD_SR)}$		Slave receiver	2	-	
$t_{h(SD_MR)}$	Data input hold time	Master receiver	0.5	-	
$t_{h(SD_SR)}$		Slave receiver	0.5	-	
$t_{v(SD_ST)}$	Data output valid time	Slave transmitter (after enable edge)	-	20	
$t_{h(SD_ST)}$	Data output hold time	Slave transmitter (after enable edge)	9	-	
$t_{v(SD_MT)}$	Data output valid time	Master transmitter (after enable edge)	-	15	
$t_{h(SD_MT)}$	Data output hold time	Master transmitter (after enable edge)	0	-	

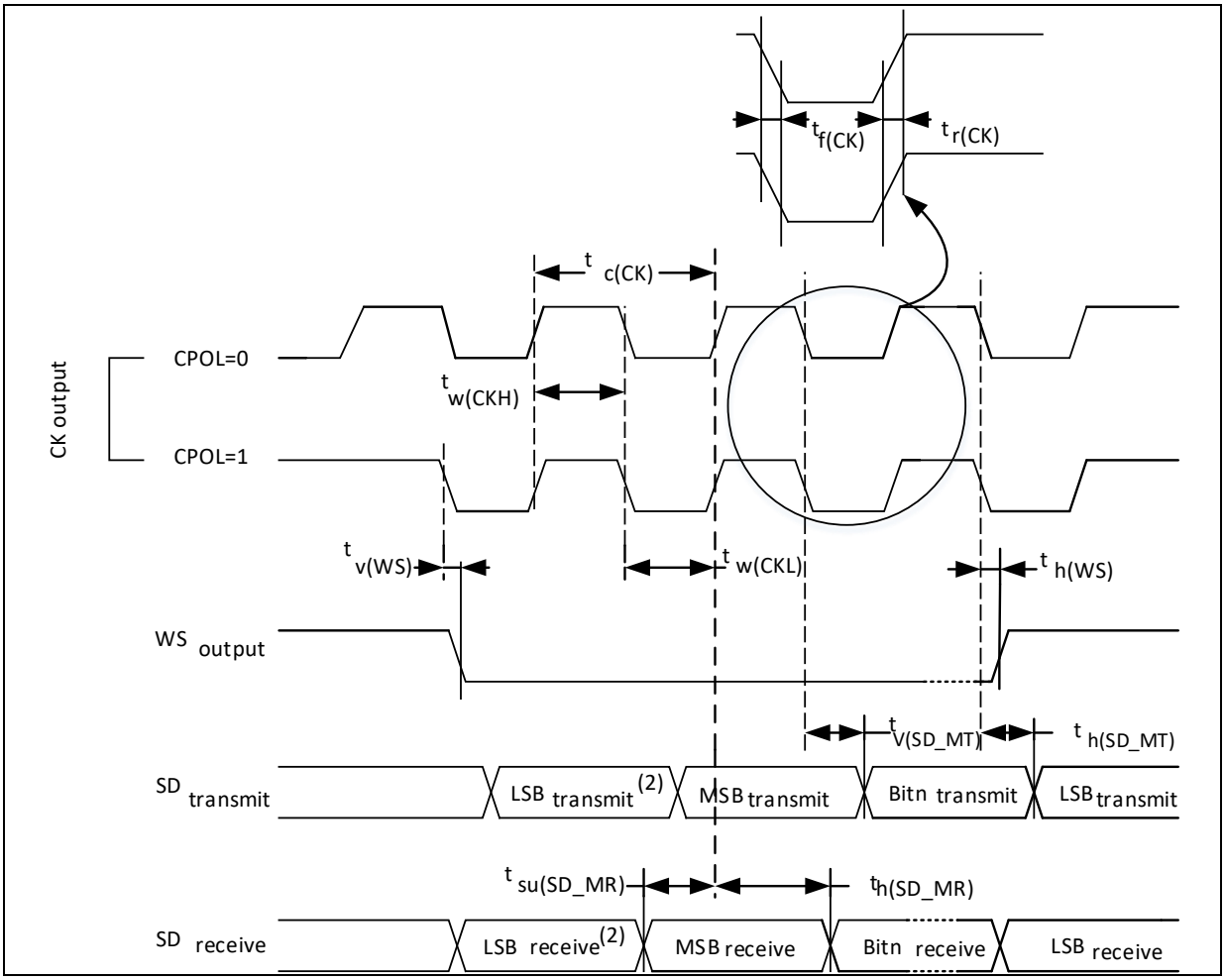
(1) Guaranteed by design, not tested in production.

Figure 45. I²S slave timing diagram (Philips protocol)



(1) LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

Figure 46. I²S master timing diagram (Philips protocol)



(1) LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

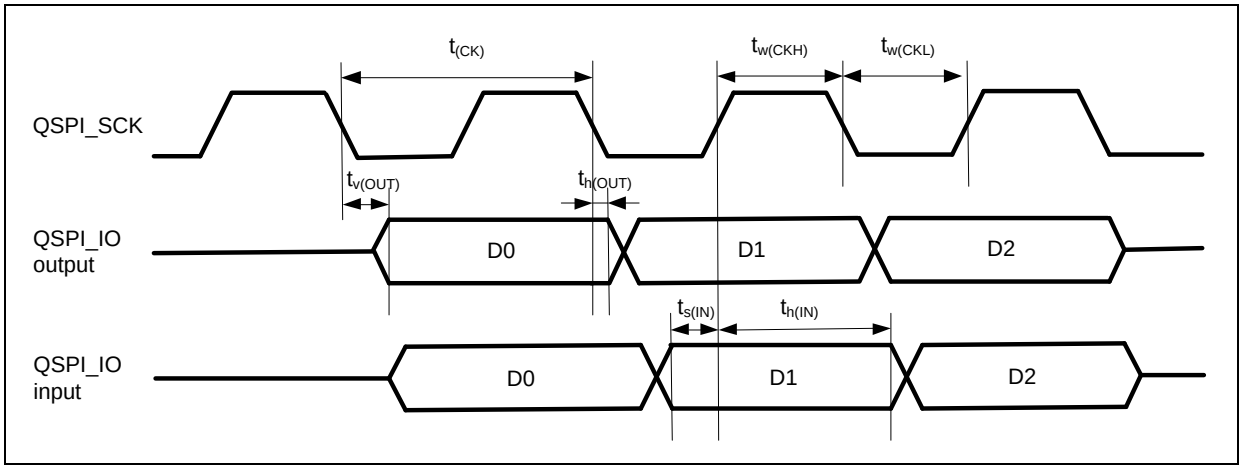
5.3.17 QSPI characteristics

Table 55. QSPI characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{SCK} $1/t_{(CK)}$ (2)	QSPI clock frequency	-	-	-	96	MHz
$t_{w(CKH)}$ $t_{w(CKL)}$	QSPI clock high and low time	-	$(t_{(CK)} / 2) - 3$	-	$(t_{(CK)} / 2) + 3$	ns
$t_{s(IN)}$	Data input setup time	-	2	-	-	ns
$t_{h(IN)}$	Data input hold time	-	4.5	-	-	ns
$t_{v(OUT)}$	Data output valid time	-	-	1.5	3	ns
$t_{h(OUT)}$	Data output hold time	-	0	-	-	ns

(1) Guaranteed by design, not tested in production.
(2) Guaranteed by characterization results, not tested in production.

Figure 47. QSPI timing diagram



5.3.18 I²C characteristics

GPIO pins SDA and SCL have limitation as follows: they are not “true” open-drain. When configured as open-drain, the PMOS connected between the GPIO pin and V_{DD} is disabled, but is still present.

I²C bus interface can support standard mode (max. 100 kHz), fast mode (max. 400 kHz), and fast mode plus (max. 1 MHz).

5.3.19 SDIO characteristics

Table 56. SD/MMC characteristics(1)

Symbol	Parameter	Conditions	Min	Max	Unit
f_{PP}	Clock frequency in data transfer mode	-	0	48	MHz
$t_{W(CKL)}$	Clock low time	f_{PP} = 48 MHz	8.5	-	ns
$t_{W(CKH)}$	Clock high time	f_{PP} = 48 MHz	8.5	-	
CMD, D inputs (referenced to CK)					
t_{ISU}	Clock setup time	f_{PP} = 48 MHz	7	-	ns
t_{IH}	Clock hold time	f_{PP} = 48 MHz	-4.5	-	
CMD, D outputs (referenced to CK)					
t_{OV} t_{OVD}	Output valid time	f_{PP} = 48 MHz	-	4	ns
t_{OH} t_{OHD}	Output hold time	f_{PP} = 48 MHz	0.5	-	

(1) Guaranteed by design, not tested in production.

Figure 48. SDIO high-speed mode

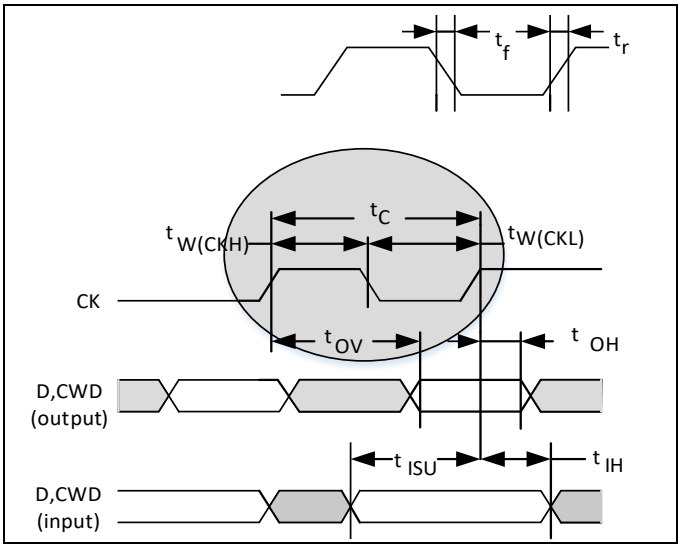
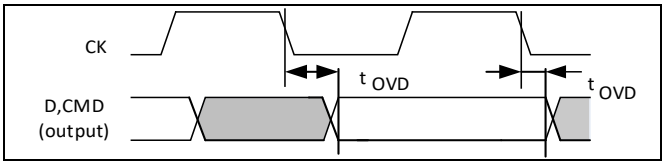


Figure 49. SD default mode



5.3.20 OTGFS characteristics

Table 57. OTGFS startup time

Symbol	Parameter	Max	Unit
$t_{STARTUP}$(1)	OTGFS transceiver startup time	1	μs

(1) Guaranteed by design, not tested in production.

Table 58. OTGFS DC electrical characteristics (1)(2)

Symbol		Parameter	Conditions	Min	Typ	Max	Unit
Input levels	V_{DD}	OTGFS operating voltage	-	3.0(3)		3.6	V
	V_{DI}	Differential input sensitivity	I (OTGFS_D+/D-)	0.2		-	V
	V_{CM}	Differential common mode range	Include V_{DI} range	0.8		2.5	
	V_{SE}	Single ended receiver threshold	-	1.3		2.0	
Output levels	V_{OL}	Static output level low	R_L of 1.24 kΩ to 3.6 V(4)	-		0.3	V
	V_{OH}	Static output level high	R_L of 15 kΩ to V_{SS}(4)	2.8		3.6	
R_{PU}		OTGFS_D+ internal pull-up	Idle, V_{IN} = V_{SS}	0.97	1.24	1.58	kΩ
			Receive, V_{IN} = V_{SS}	1.66	2.26	3.09	
R_{PD}		OTGFS_D+/D- internal pull-down	V_{IN} = V_{DD}	15	19	25	kΩ

(1) All the voltages are measured from the local ground potential.
(2) Guaranteed by design, not tested in production.
(3) The AT32F435/437 USB functionality is ensured down to 2.7 V but not the full USB electrical characteristics which are degraded in the 2.7 to 3.0 V V_{DD} voltage range.
(4) R_L is the load connected on the USB drivers.

Figure 50. OTGFS timings: definition of data signal rise and fall time

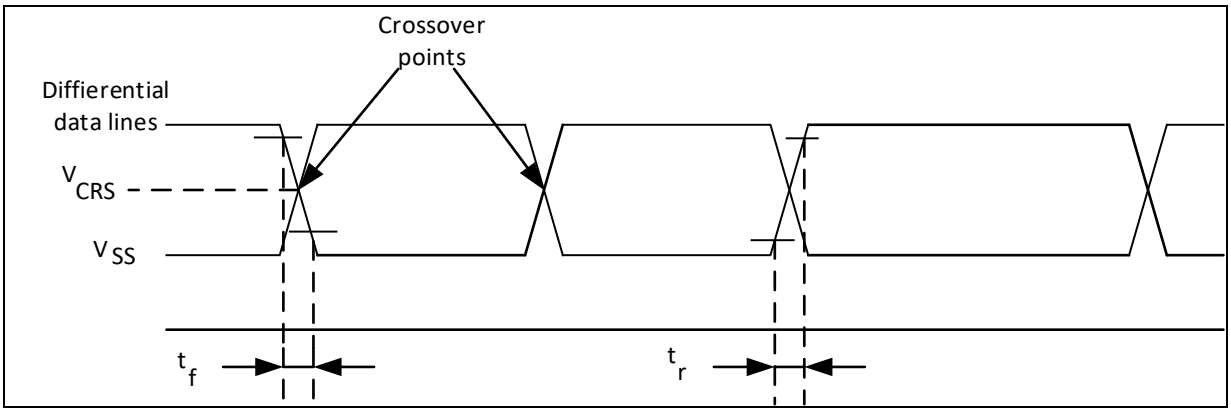


Table 59. OTGFS electrical characteristics (1)

Symbol	Parameter	Conditions	Min	Max	Unit
t_r(2)	Rise time	C_L ≤ 50 pF	4	20	ns
t_f(2)	Fall time	C_L ≤ 50 pF	4	20	ns
t_{rfm}	Rise/fall time matching	t_r/t_f	90	110	%
V_{CRS}	Output signal crossover voltage	-	1.3	2.0	V

(1) Guaranteed by design, not tested in production.
(2) Measured from 10% to 90% of the data signal. For more detailed information, please refer to USB Specification Chapter 7 (version 2.0).

5.3.21 EMAC characteristics

Operating voltage

Table 60. EMAC DC electrical characteristics(1)

Symbol	Parameter	Min	Max	Unit
V_{DD}	EMAC operating voltage	3.0	3.6	V

(1) Guaranteed by design, not tested in production. All the voltages are measured from the local ground potential.

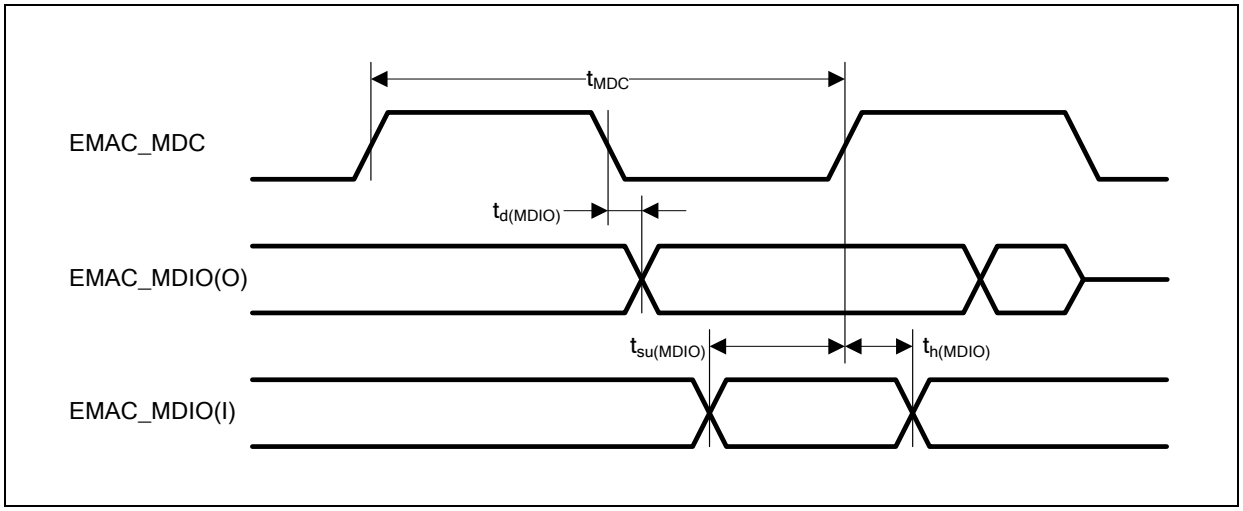
SMI (station management interface)

Table 61. Dynamic characteristics: EMAC signals for SMI(1)

Symbol	Parameter	Min	Typ	Max	Unit
t_{MDC}	MDC cycle time (1.96 MHz)	509	510	511	ns
$t_{d(MDIO)}$	MDIO write data valid time	12	14.5	17	
$t_{su(MDIO)}$	Read data setup time	35	-	-	
$t_{h(MDIO)}$	Read data hold time	15	-	-	

(1) Guaranteed by design, not tested in production.

Figure 51. EMAC SMI timing diagram



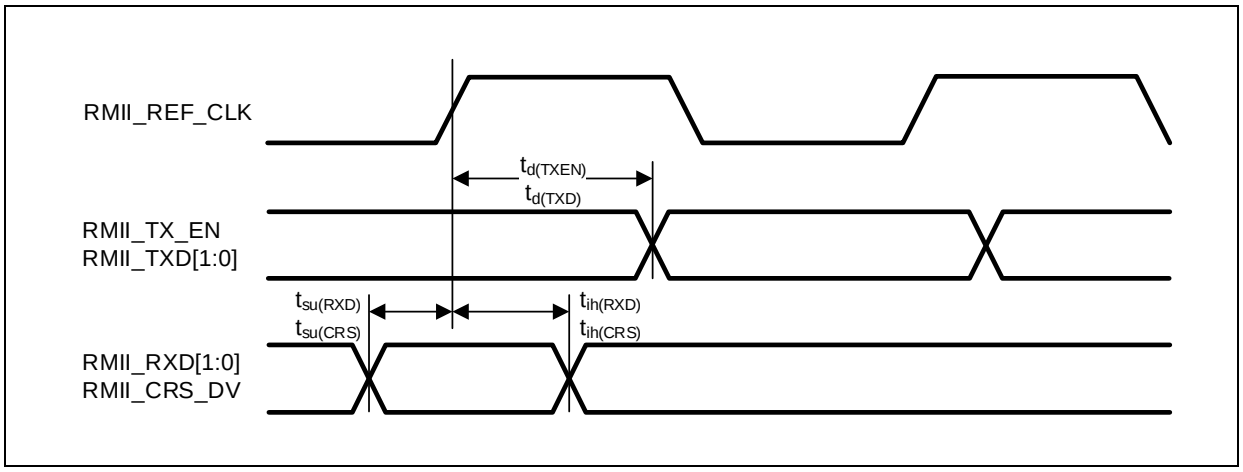
RMII

Table 62. Dynamic characteristics: EMAC signals for RMII(1)

Symbol	Parameter	Min	Typ	Max	Unit
$t_{su(RXD)}$	Receive data setup time	4	-	-	ns
$t_{ih(RXD)}$	Receive data hold time	2	-	-	
$t_{su(DV)}$	Carrier sense set-up time	6	-	-	
$t_{ih(DV)}$	Carrier sense hold time	1	-	-	
$t_{d(TXEN)}$	Transmit enable valid delay time	8	10	16	
$t_{d(TXD)}$	Transmit data valid delay time	7	10	16	

(1) Guaranteed by design, not tested in production.

Figure 52. EMAC RMII timing diagram



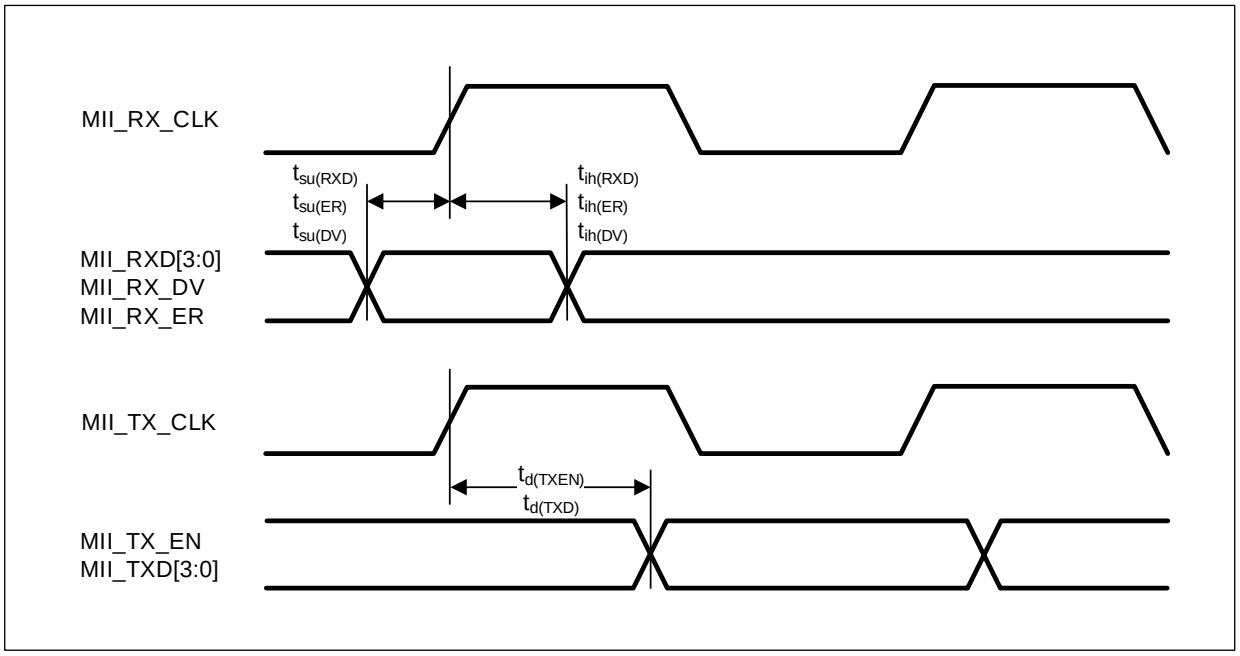
MII

Table 63. Dynamic characteristics: EMAC signals for MII(1)

Symbol	Parameter	Min	Typ	Max	Unit
$t_{su(RXD)}$	Receive data setup time	8	-	-	ns
$t_{ih(RXD)}$	Receive data hold time	2	-	-	
$t_{su(DV)}$	Data valid setup time	6	-	-	
$t_{ih(DV)}$	Data valid hold time	1	-	-	
$t_{su(ER)}$	Error setup time	3	-	-	
$t_{ih(ER)}$	Error hold time	1	-	-	
$t_{d(TXEN)}$	Transmit enable valid delay time	14	16	18	
$t_{d(TXD)}$	Transmit data valid delay time	13	16	20	

(1) Guaranteed by design, not tested in production.

Figure 53. EMAC MII timing diagram



5.3.22 DVP characteristics

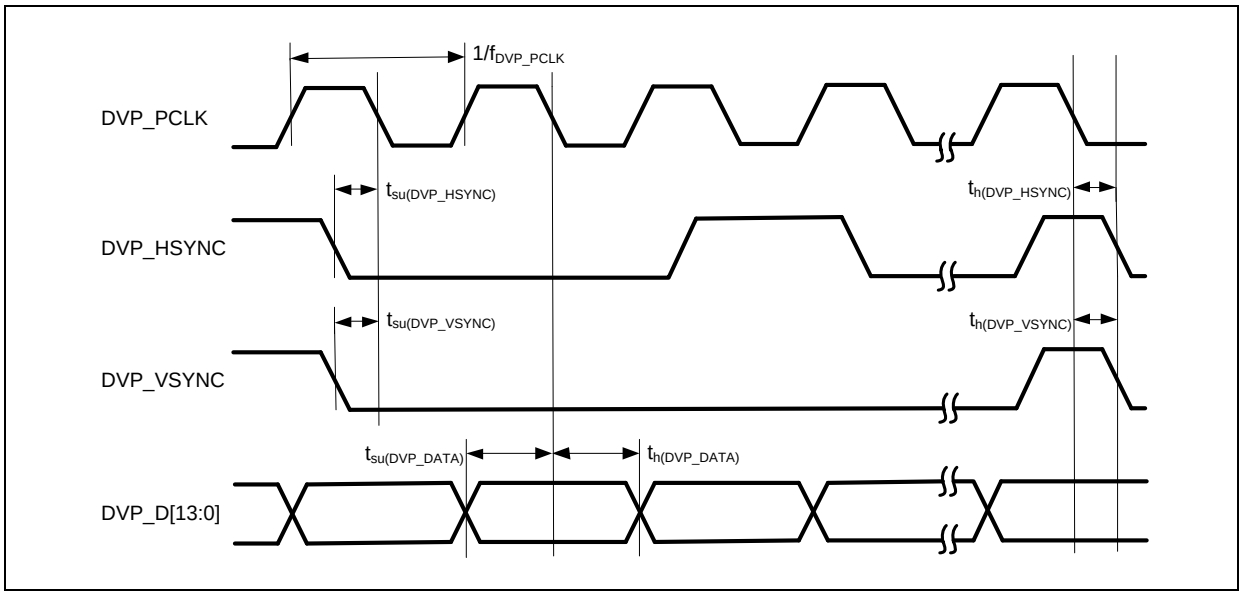
DVP_PCLK polarity: falling edge; DVP_HSYNC and DVP_VSYNC polarity: high level.

Table 57. DVP characteristics(1)

Symbol	Parameter	Min	Max	Unit
f_{DVP_PCLK}	Frequency of the input pixel clock	-	54	MHz
$Duty_{DVP_PCLK}$	Duty cycle of the input pixel clock	30	70	%
$t_{su(DVP_DATA)}$	Input data setup time	1	-	ns
$t_{h(DVP_DATA)}$	Input data hold time	3.5	-	ns
$t_{su(DVP_HSYNC)}$ $t_{su(DVP_VSYNC)}$	Input HSYNC/VSYNC setup time	2	-	ns
$t_{h(DVP_HSYNC)}$ $t_{h(DVP_VSYNC)}$	Input HSYNC/VSYNC hold time	0	-	ns

(1) Guaranteed by design, not tested in production.

Figure 54. DVP timing diagram



5.3.23 12-bit ADC characteristics

Unless otherwise specified, the parameters given in the table below are preliminary values derived from tests performed under ambient temperature, f_{PCLK2} frequency and V_{DDA} supply voltage conditions summarized in *Table 15*.

Note: It is recommended to perform a calibration after each power-up.

Table 64. ADC characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DDA}	Power supply	-		2.6	-	3.6	V
V_{REF+} (3)	Positive reference voltage	-		2.0	-	V_{DDA}	V
V_{REF-} (3)	Negative reference voltage	Must be the same potential as V_{SSA}		0	-	0	V
V_{SSA}	Ground	-		0	-	0	V
I_{DDA}	Current on V_{DDA} input pin	-		-	1280(1)	1560	μA
I_{VREF+} (3)	Current on V_{REF+} input pin	-		-	400(1)	480	μA
f_{ADC}	ADC clock frequency	$V_{REF+} \geq 2.6$ V		0.6	-	80	MHz
		$V_{REF+} < 2.6$ V		0.6	-	30	
f_S(2)	Sampling rate	12-bit resolution	Fast channels	0.04	-	5.33	MSPS
			Slow channels			4.21	
		10-bit resolution	Fast channels	0.047	-	6.15	
			Slow channels			4.71	
		8- bit resolution	Fast channels	0.055	-	7.27	
			Slow channels			5.33	
		6- bit resolution	Fast channels	0.067	-	8.88	
			Slow channels			6.15	
f_{TRIG}(2)	External trigger frequency	f_{ADC} = 80 MHz		-	-	4.44	MHz
		-		-	-	18	$1/f_{ADC}$
V_{AIN} (3)	Conversion voltage range	-		V_{REF-}	-	V_{REF+}	V
R_{AIN}(2)	External input impedance	-		See *Table 65*			Ω
C_{ADC}(2)	Internal sample and hold capacitor	-		-	10	-	pF
t_{CAL}(2)	Calibration time	f_{ADC} = 80 MHz		2.56			μs
		-		205			$1/f_{ADC}$
t_{lat}(2)	Preemptive trigger conversion latency	f_{ADC} = 80 MHz		-	-	37.5	ns
		-		-	-	3(4)	$1/f_{ADC}$
t_{latr}(2)	Ordinary trigger conversion latency	f_{ADC} = 80 MHz		-	-	25	ns
		-		-	-	2(4)	$1/f_{ADC}$
t_S(2)	Sampling time	f_{ADC} = 80 MHz		0.031	-	8.006	μs
		-		2.5	-	640.5	$1/f_{ADC}$
t_{STAB}(2)	Power-up time	-		45			$1/f_{ADC}$
t_{CONV}(2)	Total conversion time (including sampling time)	f_{ADC} = 80 MHz, 12-bit resolution		0.188	-	8.163	μs
		12-bit resolution		15 ~ 653 (t_S for sampling+ 12.5 for successive approximation)			$1/f_{ADC}$

(1) Guaranteed by characterization results, not tested in production.
(2) Guaranteed by design, not tested in production.
(3) V_{REF+} and V_{REF-} can be internally connected to V_{DDA} and V_{SSA} respectively, depending on the package.
(4) For external triggers, a delay of $1/f_{PCLK2}$ must be added to the latency specified in *Table 64*.

Table 65 are used to define the maximum external impedance allowed for an error below 1 of LSB in 12-bit resolution.

Table 65. R_{AIN} max for f_{ADC} = 80 MHz

T_S (cycle)	t_S (μs)	R_{AIN} max (Ω)(1)	
		Fast channels	Slow channels
2.5	0.031	30	-
6.5	0.081	200	50
12.5	0.156	400	350
24.5	0.306	800	700
47.5	0.594	1700	1500
92.5	1.156	3000	2600
247.5	3.094	9000	8500
640.5	8.006	20000	19000

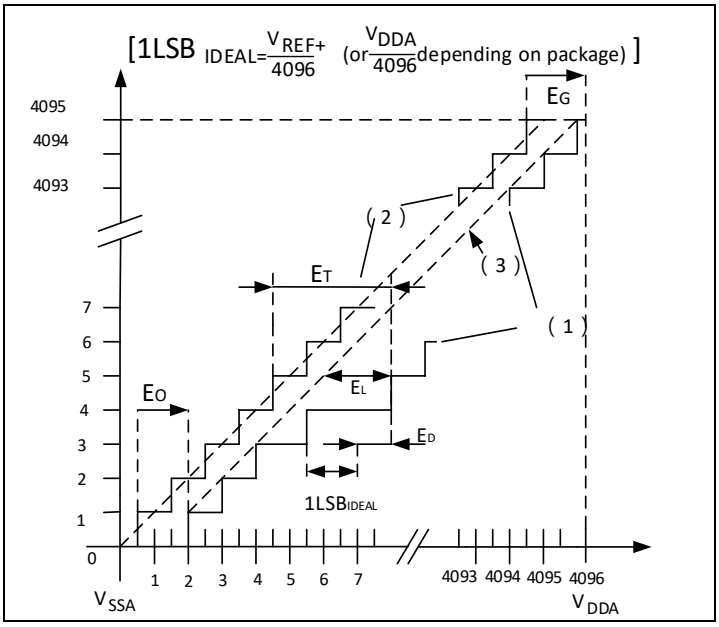
(1) Guaranteed by design.

Table 66. ADC accuracy (1)(2)

Symbol	Parameter	Test conditions	Typ	Max	Unit
ET	Total unadjusted error	f_{ADC} = 80 MHz, R_{AIN} < 20 kΩ, V_{DDA} = 3.0~3.6 V, T_A = 25 °C, V_{REF+} = V_{DDA}	±1.5	±3	LSB
EO	Offset error		±0.5	±1.5	
EG	Gain error		±0.5	±1.5	
ED	Differential linearity error		±1	+1.5/-1	
EL	Integral linearity error		±1.5	±3	
ET	Total unadjusted error	f_{ADC} = 15 ~ 80 MHz, R_{AIN} < 20 kΩ, V_{DDA} = 2.6~3.6 V, T_A = -40 ~ 105 °C, V_{REF+} = 2.0~3.6 V	±2	±4.5	LSB
EO	Offset error		±0.5	±3	
EG	Gain error		+1.5	+4/-2	
ED	Differential linearity error		±1	+2/-1	
EL	Integral linearity error		±1.5	±3.5	

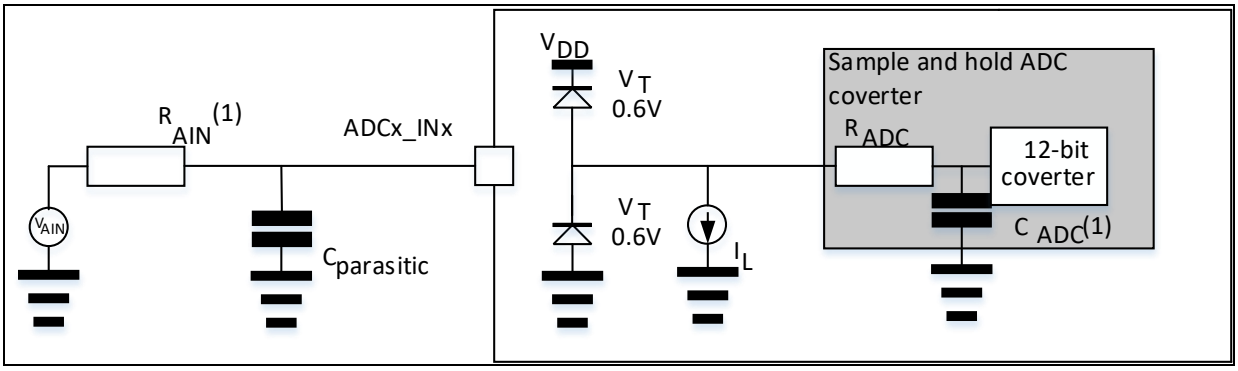
(1) ADC DC accuracy values are measured after internal calibration.
(2) Guaranteed by characterization results, not tested in production.

Figure 55. ADC accuracy characteristics



(1) Example of an actual transfer curve.
(2) Ideal transfer curve.
(3) End point correlation line.
(4) ET = Maximum deviation between the actual and the ideal transfer curves.
EO = Deviation between the first actual transition and the first ideal one.
EG = Deviation between the last ideal transition and the last actual one.
ED = Maximum deviation between actual steps and the ideal one.
EL = Maximum deviation between any actual transition and the end point correlation line.

Figure 56. Typical connection diagram using the ADC



(1) Refer to *Table 64* for the values of R_{AIN} and C_{ADC}.
(2) $C_{parasitic}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (roughly 7 pF).

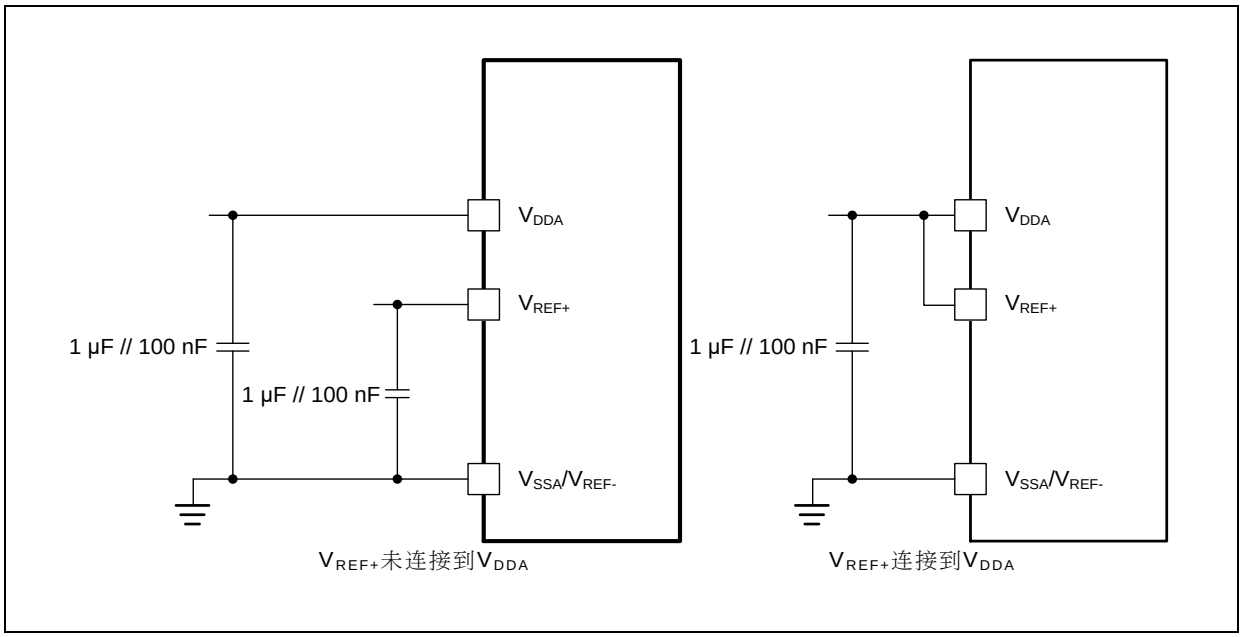
General PCB design guidelines

Power supply decoupling should be performed as shown in *Figure 57* or *Figure 58*, depending on whether V_{REF+} is connected to V_{DDA} or not. The 100 nF capacitors should be ceramic (good quality). They should be placed them as close as possible to the chip.

If HEXT is enabled while ADC uses any input channel of ADC3_IN4~8 and ADC123_IN10~13, following PCB layout guide line below benefits to isolate the high frequency interference from HEXT emitting to ADC input signals nearby.

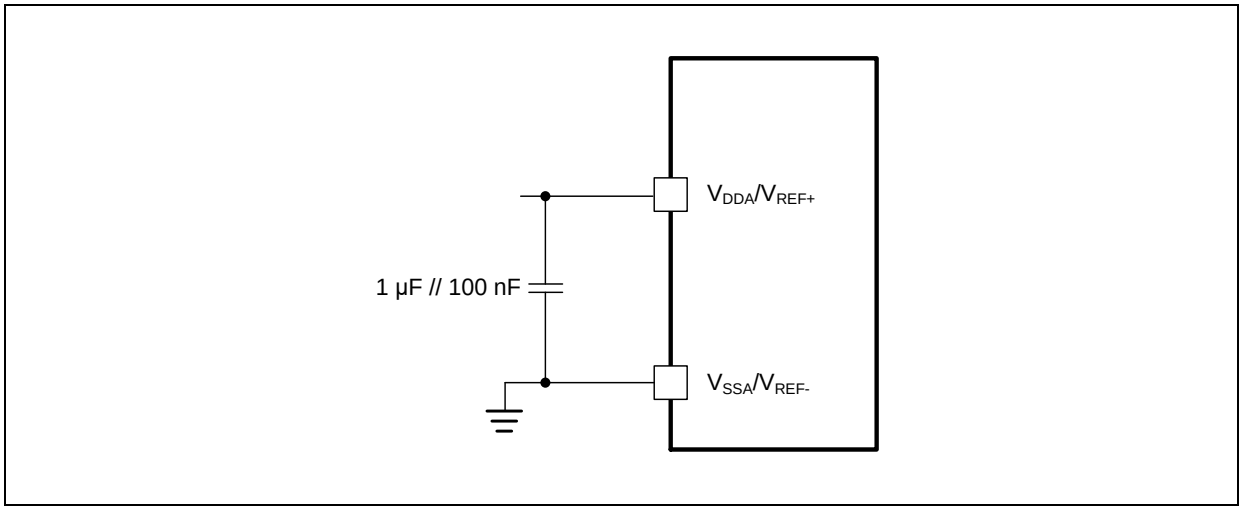
- Use different PCB layers to route ADC_IN signal apart from HEXT path
- Do not route ADC_IN signals and HEXT path parallel

Figure 57. Power supply and reference decoupling (V_{REF+} connected to V_{DDA})



(1) V_{REF+} input is available only on 100-pin package.

Figure 58. Power supply and reference decoupling (V_{REF+} not connected to V_{DDA})



(1) V_{REF+} input is available only on 100-pin package.

5.3.24 Internal reference voltage (V_{INTRV}) characteristics

Table 67. Internal reference voltage characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{INTRV}(1)	Internal reference voltage	-	1.16	1.20	1.24	V
T_{Coeff}(1)	Temperature coefficient	-	-	50	100	ppm/°C
T_{S_VINTRV}(2)	ADC sampling time when reading the internal reference voltage	-	5	-	-	µs

(1) Guaranteed by characterization results, not tested in production.
(2) Guaranteed by design, not tested in production.

5.3.25 Temperature sensor (V_{TS}) characteristics

Table 68. Temperature sensor characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_L(1)	V_{TS} linearity with temperature	T_A = -20 ~ +85 °C	-	±1	±2	ºC
		T_A = -40 ~ +105 °C	-	-	±3	
Avg_Slope(1)(2)	Average slope	-	-4.00	-4.13	-4.25	mV/ºC
V_{25}(1)(2)	Voltage at 25 ºC	-	1.21	1.27	1.34	V
t_{START}(3)	Setup time	-	-	-	100	µs
T_{S_temp}(3)	ADC sampling time when reading the temperature	-	5	-	-	µs

(1) Guaranteed by characterization results, not tested in production.
(2) The temperature sensor output voltage changes linearly with temperature. The offset of this line varies from chip to chip due to process variation (up to 50 °C from one chip to another). The internal temperature sensor is more suited to applications that detect temperature variations instead of absolute temperatures. If accurate temperature readings are needed, an external temperature sensor part should be used.
(3) Guaranteed by design, not tested in production.

Obtain the temperature using the following formula:

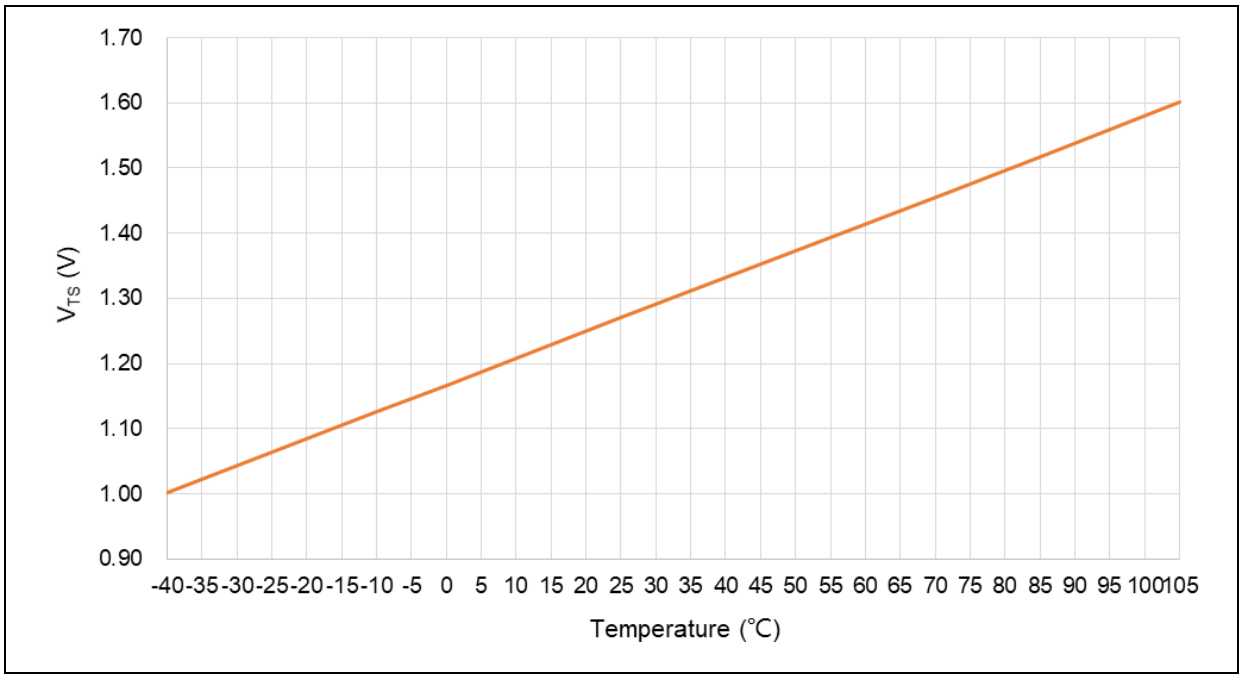
Temperature (°C) = {(V_{25} – V_{TS}) / Avg_Slope} + 25

where,

V_{25} = V_{TS} value for 25 °C

Avg_Slope = Average Slope for curve between Temperature vs. V_{TS} (given in mV/° C)

Figure 59. Ideal curve of V_{TS} vs. temperature



5.3.26 V_{BAT} voltage monitor characteristics

Table 69. V_{BAT} voltage monitor characteristics

Symbol	Parameter	Min	Typ	Max	Unit
R_{VBATM}(1)	String resistor value of the V_{BAT} monitor	-	45	-	kΩ
Q	Dividing factor of the V_{BAT} monitor	-	4	-	-
Q_{ET}(1)	Total error of Q	-1	-	+1	%
T_{S_VBATM}(2)	ADC sampling time when reading the voltage of the V_{BAT} monitor	5	-	-	μs

(1) Guaranteed by characterization results, not tested in production.
(2) Guaranteed by design, not tested in production.

5.3.27 12-bit DAC characteristics

Table 70. DAC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage	-	2.6	-	3.6	V
V_{REF+}(3)	Positive reference voltage	-	2.0	-	3.6	V
V_{REF-}(3)	Negative reference voltage	Must be the same potential as V_{SSA}	0	-	0	V
V_{SSA}	Ground	-	0	-	0	V
R_{LOAD}(1)	Load resistance with buffer ON	-	5	-	-	kΩ
R_O(2)	Impedance output with buffer OFF	-	-	13.2	16	kΩ
C_{LOAD}(1)	Capacitive load (buffer ON)	-	-	-	50	pF
DAC_OUT(1)	Lower DAC_OUT voltage with buffer ON	-	0.15	-	-	V
	Higher DAC_OUT voltage with buffer ON	-	-	-	V_{REF+} - 0.15	V
	Lower DAC_OUT voltage with buffer OFF	-	-	0.5	5	mV
	Higher DAC_OUT voltage with buffer OFF	-	-	-	V_{REF+} - 2 mV	V
I_{DDA}	DAC DC current consumption in quiescent mode	With no load, V_{REF+} = 3.6 V	-	460	625	μA
I_{VREF+}(3)	DAC AC current consumption in quiescent mode	With no load, V_{REF+} = 3.6 V	-	270	310	μA
DNL(2)	Differential non linearity	-	-	±0.4	±0.8	LSB
INL(2)	Integral non linearity (difference between measured value from code i and a line drawn between DAC_OUT min and DAC_OUT max)	-	-	±1	±3	LSB
Offset(2)	Offset error (difference between measured value at Code (0x800) and the ideal value = V_{REF+}/2)	-	-	10	15	mV
			-	10	25	LSB
Gain error(2)	Gain error	-	-	0.1	0.25	%
$t_{SETTLING}$	Setting time	R_{LOAD} ≥ 5 kΩ C_{LOAD} ≤ 50 pF	-	1	4	μs
Update rate	Max frequency for a correct DAC_OUT change when small variation in the input code (from code i to i+1 LSB)	R_{LOAD} ≥ 5 kΩ C_{LOAD} ≤ 50 pF	-	-	1	MSPS
t_{WAKEUP}	Wakeup time from off state (setting the EN bit in the DAC Control register)	R_{LOAD} ≥ 5 kΩ C_{LOAD} ≤ 50 pF	-	1.2	4	μs

(1) Guaranteed by design, not tested in production.
(2) Guaranteed by characterization results, not tested in production.
(3) V_{REF+} and V_{REF-} can be internally connected to V_{DDA} and V_{SSA} respectively, depending on the package.

6 Package information

6.1 LQFP144

Figure 60. LQFP144 – 20 x 20 mm 144 pin low-profile quad flat package outline

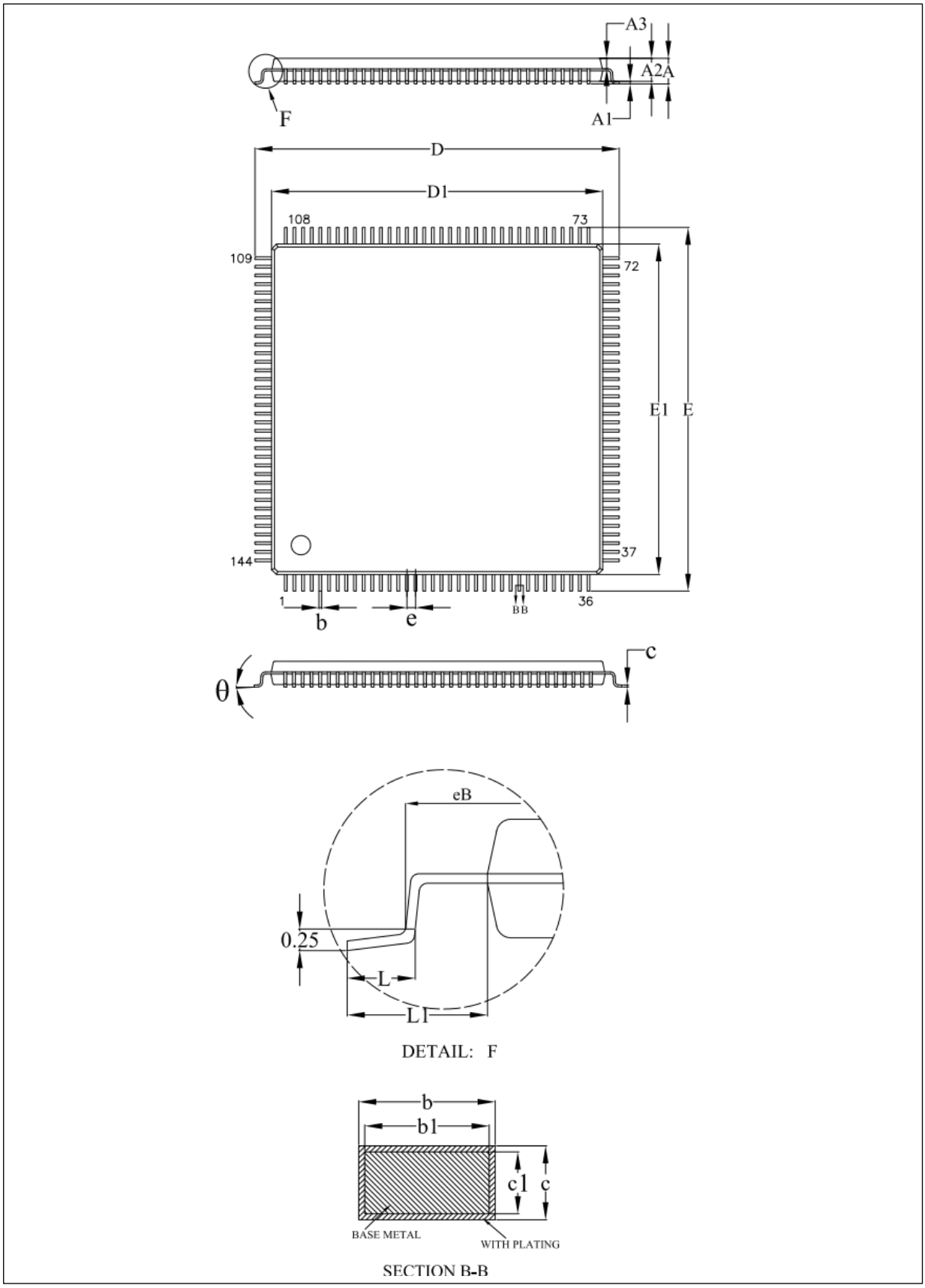


Table 71. LQFP144 – 20 x 20 mm 144 pin low-profile quad flat package mechanical data

Symbol	millimeters		
	Min	Typ	Max
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18	-	0.26
b1	0.17	0.20	0.23
c	0.13	-	0.17
c1	0.12	0.13	0.14
D	21.80	22.00	22.20
D1	19.90	20.00	20.10
E	21.80	22.00	22.20
E1	19.90	20.00	20.10
e	0.50 BSC.		
L	0.45	0.60	0.75
L1	1.00 REF.		
θ	0°	3.5°	7°

6.2 LQFP100

Figure 61. LQFP100 – 14 x 14 mm 100 pin low-profile quad flat package outline

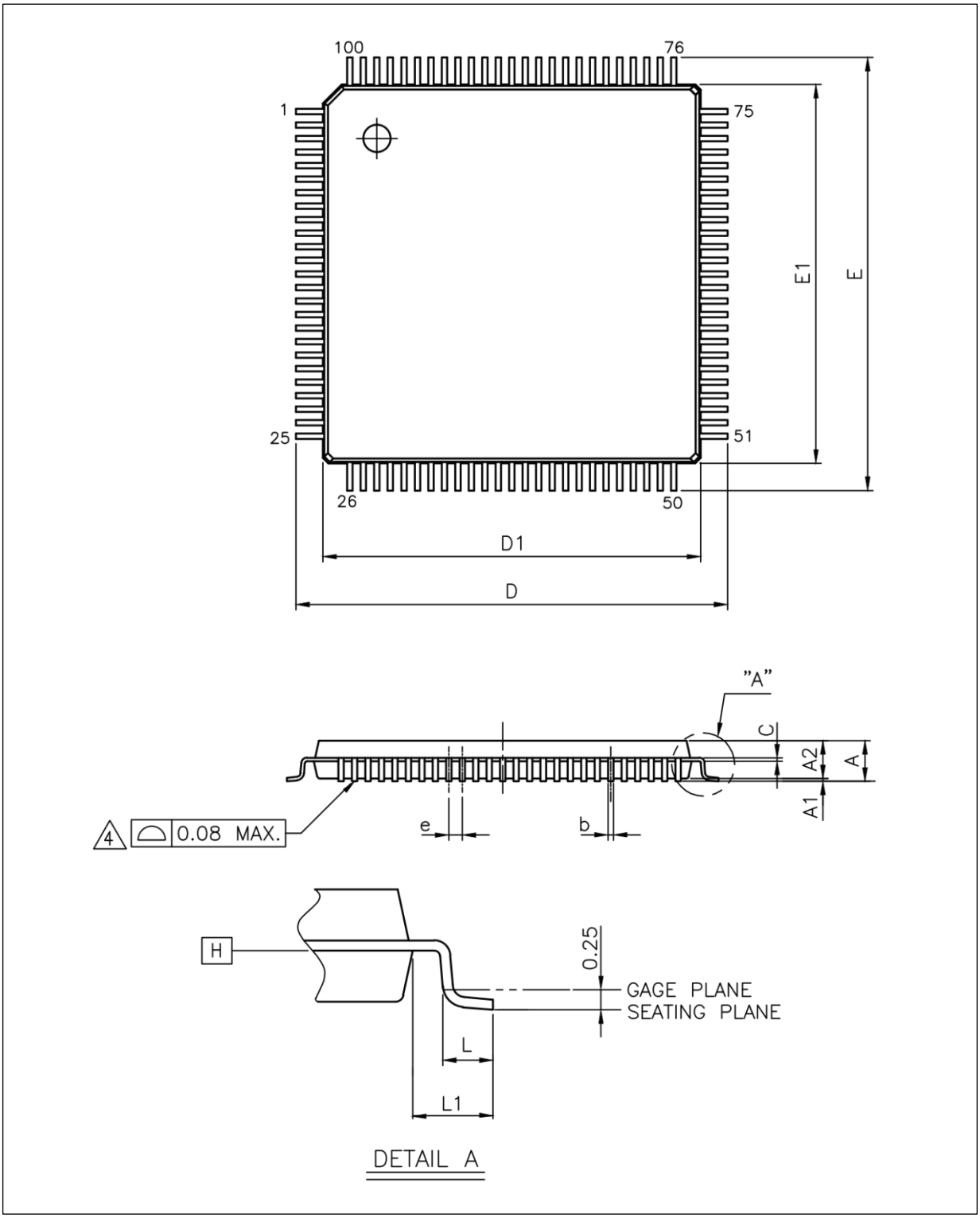


Table 72. LQFP100 – 14 x 14 mm 100 pin low-profile quad flat package mechanical data

Symbol	millimeters		
	Min	Typ	Max
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
b	0.17	0.20	0.26
c	0.10	0.127	0.20
D	15.75	16.00	16.25
D1	13.90	14.00	14.10
E	15.75	16.00	16.25
E1	13.90	14.00	14.10
e	0.50 BSC.		
L	0.45	0.60	0.75
L1	1.00 REF.		

6.3 BGA100

Figure 62. BGA100 – 7 x 7 mm 100 solder balls array package outline

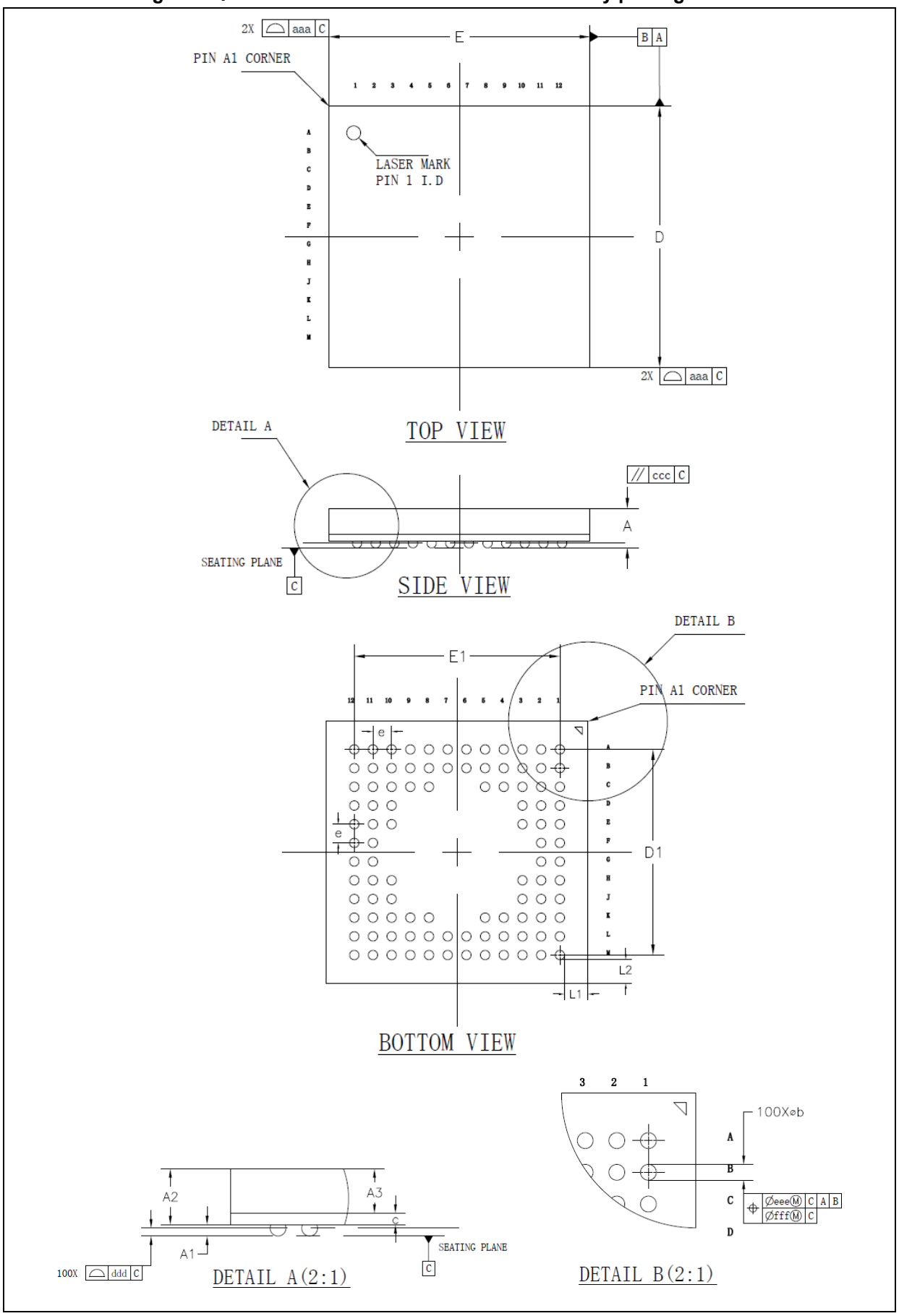


Table 73. BGA100 – 7 x 7 mm 100 solder balls array package mechanical data

Symbol	millimeters		
	Min	Typ	Max
A	0.99	1.06	1.13
A1	0.13	0.18	0.23
A2	0.84	0.88	0.92
A3	0.70 BSC.		
b	0.20	0.25	0.30
c	0.15	0.18	0.21
D	6.90	7.00	7.10
D1	5.50 BSC.		
E	6.90	7.00	7.10
E1	5.50 BSC.		
e	0.50 BSC.		
L1	0.55	0.625	0.70
L2	0.55	0.625	0.70
aaa	0.15		
ccc	0.20		
ddd	0.08		
eee	0.15		
fff	0.05		

6.4 LQFP64

Figure 63. LQFP64 – 10 x 10 mm 64 pin low-profile quad flat package outline

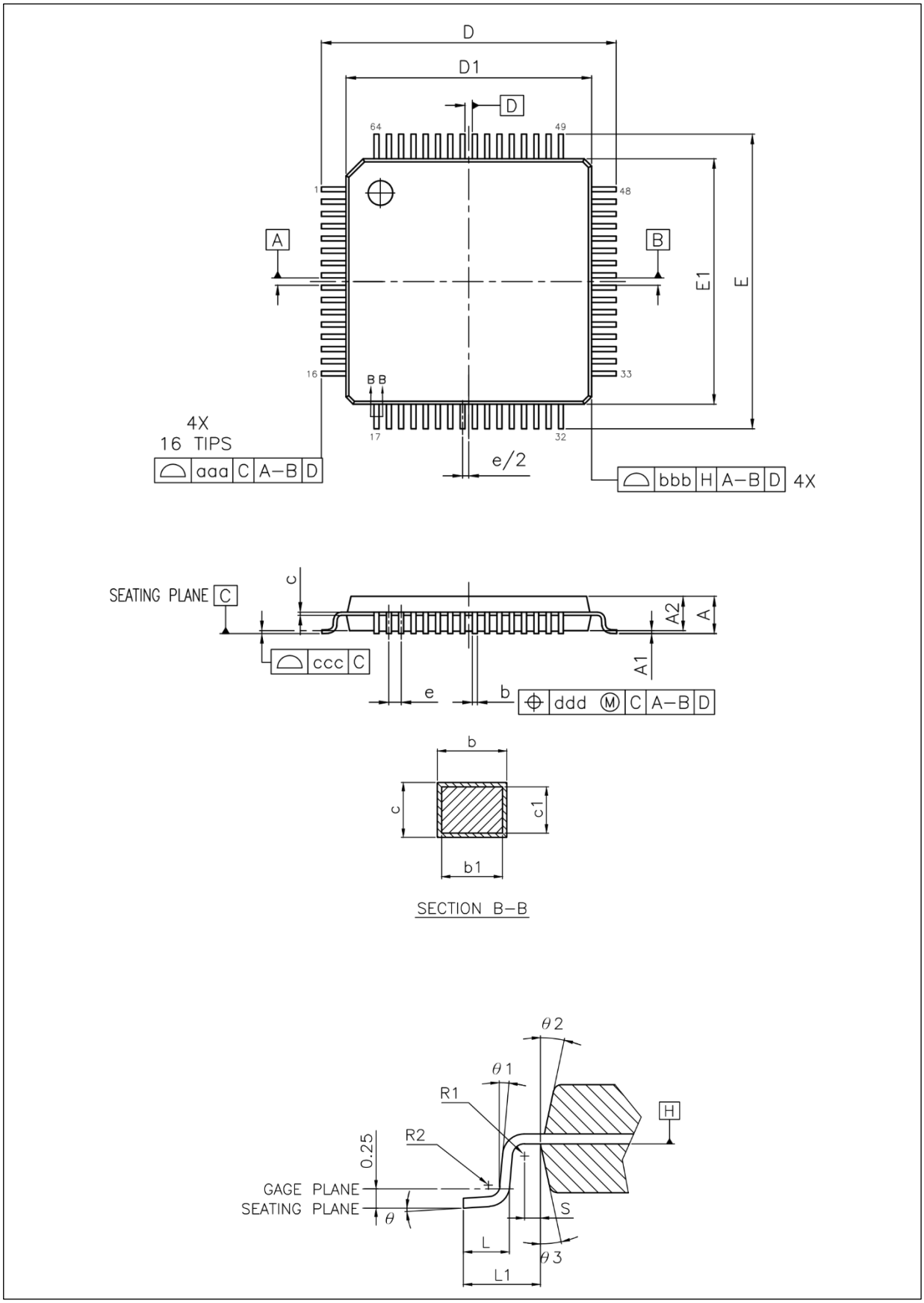


Table 74. LQFP64 – 10 x 10 mm 64 pin low-profile quad flat package mechanical data

Symbol	millimeters		
	Min	Typ	Max
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
b	0.17	0.20	0.27
c	0.09	-	0.20
D	11.75	12.00	12.25
D1	9.90	10.00	10.10
E	11.75	12.00	12.25
E1	9.90	10.00	10.10
e	0.50 BSC.		
Θ	3.5° REF.		
L	0.45	0.60	0.75
L1	1.00 REF.		
ccc	0.08		

6.5 LQFP48

Figure 64. LQFP48 – 7 x 7 mm 48 pin low-profile quad flat package outline

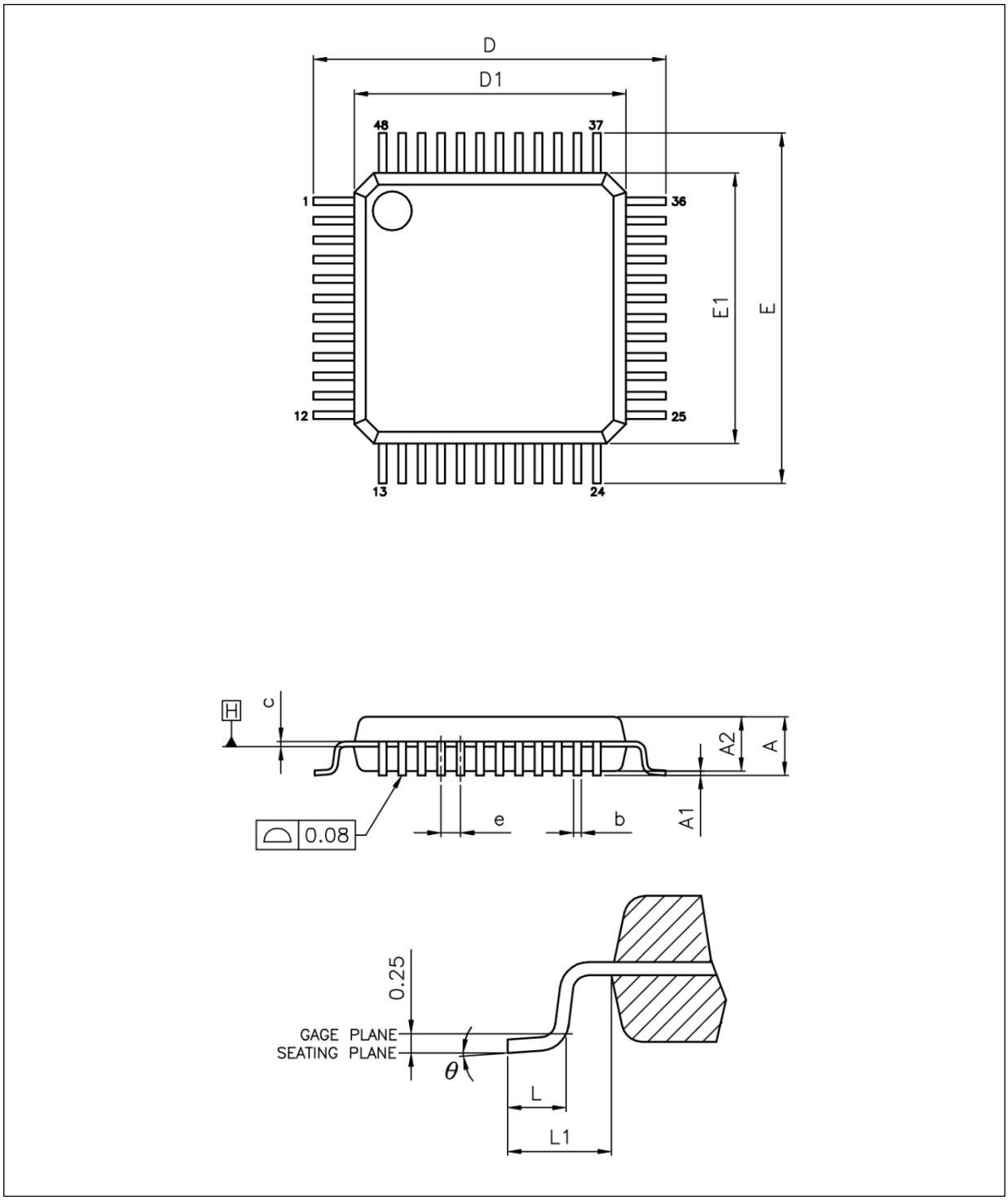


Table 75. LQFP48 – 7 x 7 mm 48 pin low-profile quad flat package mechanical data

Symbol	millimeters		
	Min	Typ	Max
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
b	0.17	0.22	0.27
c	0.09	-	0.20
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
e	0.50 BSC.		
Θ	0°	3.5°	7°
L	0.45	0.60	0.75
L1	1.00 REF.		

6.6 QFN48

Figure 65. QFN48 – 6 x 6 mm 48 pin quad flat no-leads package outline

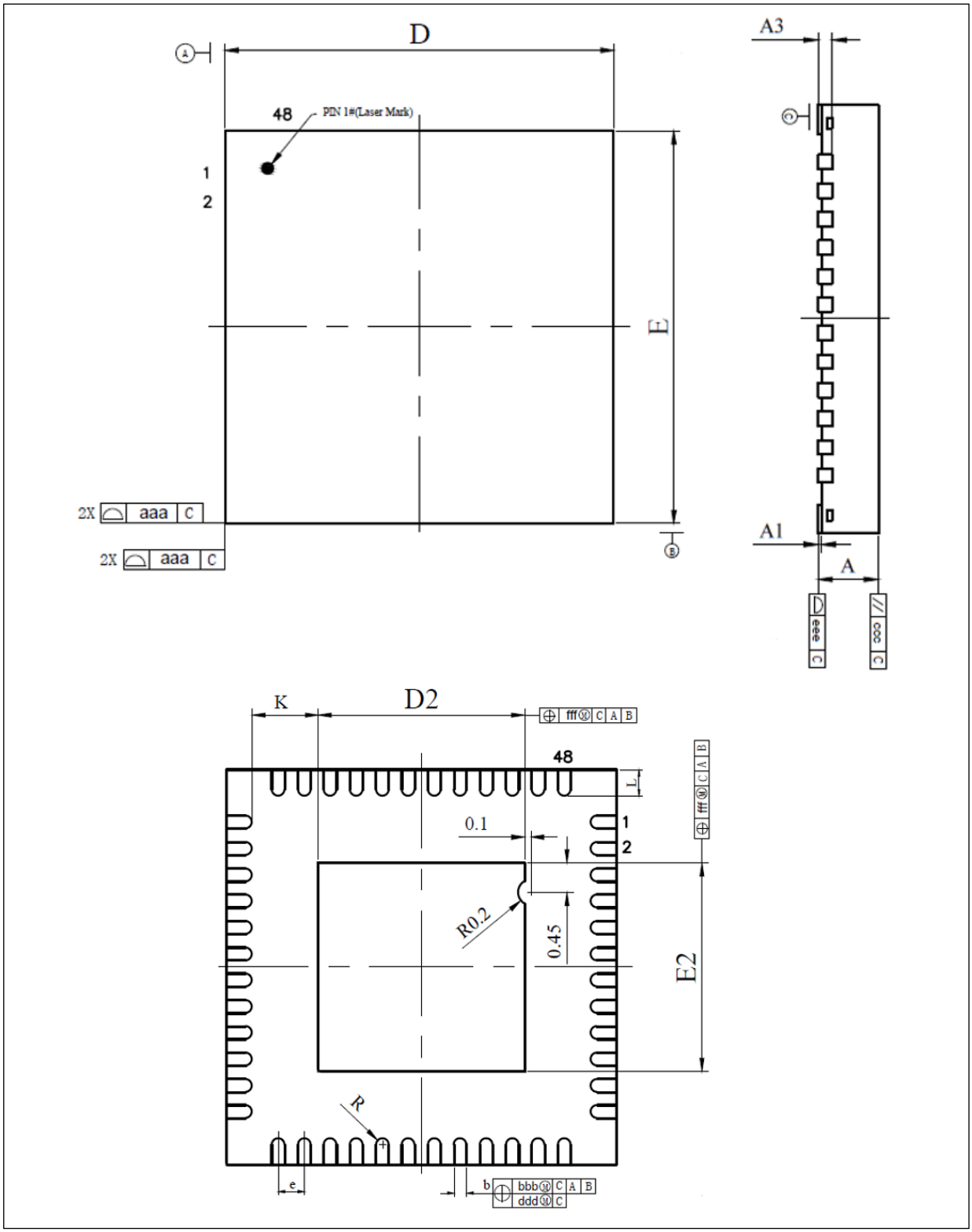
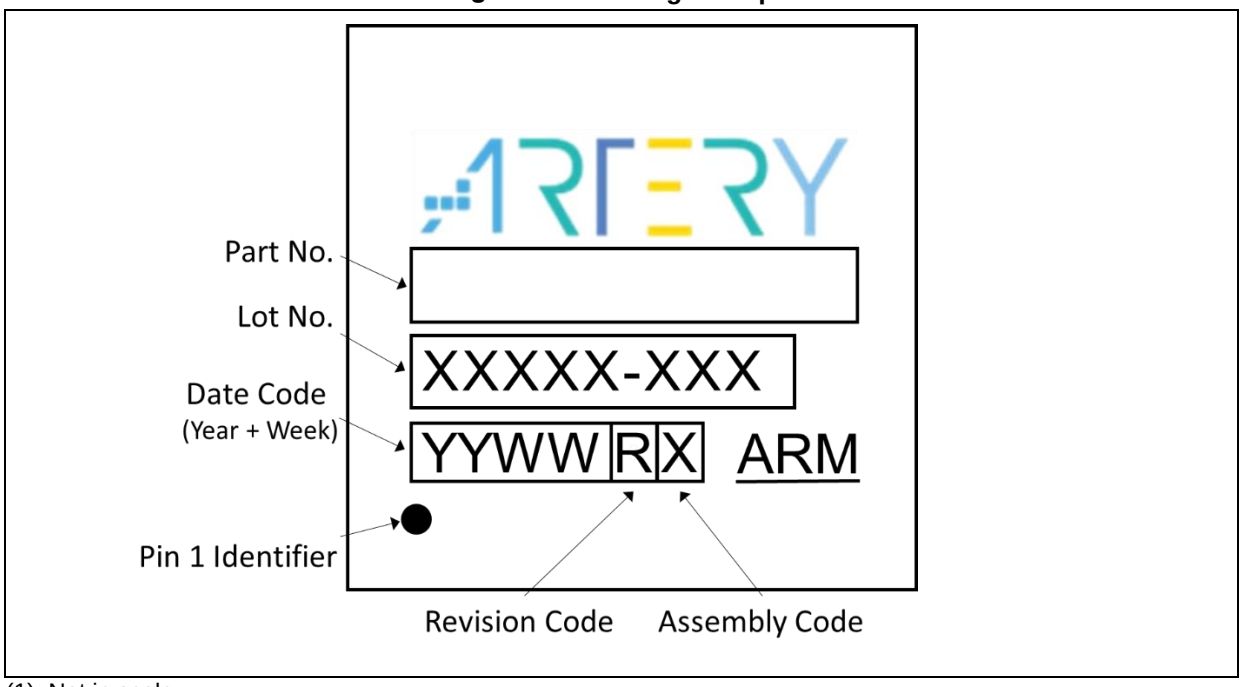


Table 76. QFN48 – 6 x 6 mm 48 pin quad flat no-leads package mechanical data

Symbol	millimeters		
	Min	Typ	Max
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
A3	0.203 REF.		
b	0.15	0.20	0.25
D	5.90	6.00	6.10
D2	3.07	3.17	3.27
E	5.90	6.00	6.10
E2	3.07	3.17	3.27
e	0.40 BSC.		
K	0.20	-	-
L	0.35	0.40	0.45

6.7 Device marking

Figure 66. Marking example



(1) Not in scale.

6.8 Thermal characteristics

Thermal characteristics are calculated based on two-layer board that uses FR-4 material in 1.6mm thickness. They are guaranteed by design, not tested in production.

Table 77. Package thermal characteristics

Symbol	Parameter	Values	Unit
Θ_{JA}	Thermal resistance junction-ambient —LQFP144 – 20 x 20 mm/0.5 mm	49.7	°C/W
	Thermal resistance junction-ambient —LQFP100 – 14 x 14 mm/0.5 mm	63.2	
	Thermal resistance junction-ambient —BGA100 – 7 x 7 mm/0.5 mm	52.0	
	Thermal resistance junction-ambient —LQFP64 – 10 x 10 mm/0.5 mm	64.4	
	Thermal resistance junction-ambient —LQFP48 – 7 x 7 mm/0.5 mm	62.5	
	Thermal resistance junction-ambient —QFN48 – 6 x 6 mm/0.4 mm	40.0	

7 Part numbering

Table 78. AT32F435/437 series part numbering

Example: AT32 F 4 3 7 Z M T 7

Product family

AT32 = ARM®-based 32-bit microcontroller

Product type

F = General-purpose

Core

4 = Cortex®-M4F

Product series

3 = High performance

Product application

7 = Ethernet EMAC series

5 = OTGFS series

Pin count

Z = 144 pins

V = 100 pins

R = 64 pins

C = 48 pins

Internal Flash memory size

M = 4 Mbytes of the internal Flash memory

G = 1 Mbytes of the internal Flash memory

D = 448 Kbytes of the internal Flash memory

C = 256 Kbytes of the internal Flash memory

Package

T = LQFP

U = QFN

H = BGA

Temperature range

7 = -40 °C to +105 °C

For a list of available options (speed, package, etc.) or for more information concerning this device, please contact your local Artery sales office.

8 Document revision history

Table 79. Document revision history

Date	Version	Revision note
2021.10.27	2.00	Initial release.
2022.1.13	2.01	1. Updated *Figure 65.* 2. Modified contents in the original *Table 16.*
2022.6.13	2.02	1. Added max values at T_A = 25 °C and notes of *Table 24* and *Table 25*. 2. Added max and min values of D, D1, E, E1 for each package.
2023.3.24	2.10	1. Added AT32F435/437xD. 2. Added pins for USART3 in *Table 5*. 3. Modified V_{DD} and T_A in *Table 15* and deleted the original *Table 16*. 4. Modified current values in *Table 22*, *Table 23* and *Table 24*. 5. Modified SPI clock frequency in *Table 53*. 6. Modified current values in *Table 64*, and updated *Figure 57* and *Figure 58.* 7. Modified thermal characteristic values of QFN48 in *Table 77*.
2023.10.17	2.11	1. Modified *Table 18*, *Table 44*, *Table 45*, *Table 46*, *Table 47*, *The tPCLK* refers to the APB clock cycle (APB1 or PAB2) connected with SPI. Table 53 and *Table 54.* 2. Added note (3) of *Table 36*. 3. Added contents in *2.13.6*. 4. Modified the fourth paragraph in IMPORTANT NOTICE.
2024.4.1	2.12	Updated the end address of internal Flash memory bank 2 in *Figure 7*
2024.11.1	2.20	1. LDO 1.0V not supported. Modified the maximum frequency at LDO 1.1V in *Table 15*, and modified test conditions and data in *5.3.5*. 2. Modified the condition and values of OTGFS_D+ internal pull-up in *Table 58*. 3. Modified *Table 41, Table 42, Table 43, Table 44, Table 45, Table 46, Table 47, Table 50, Table 51, The tPCLK* refers to the APB clock cycle (APB1 or PAB2) connected with SPI. Table 53*, Table 55, Table 56, Table 61*, *Table 62* and *Table 63*.
2026.3.23	2.30	Added BGA100 package.

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