YXW9361

Dual-Channel SDR RF Transceiver

DATASHEET

1 Overview

YXW9361ModelThe2T2RSDR RF transceiver is a high-performance, highly integrated RF transceiver, pin-to-pin compatible withtheAD9361chip,allowing for direct replacement without modifying external circuitry. Its excellent programmability and bandwidth capabilities make it suitable for various RF transceiver systems, including communications, radio, and data links. This device achieves full integration of RF,frequencysynthesizer, AD&DA, and mixed-signal baseband, providing a configurable digital interface for the processor and significantly simplifying system design.

TheYXW9361coversanoperatingfrequency range of 70 MHz to 6.0 GHz and supports adjustablesignalbandwidthfrom200 kHz to 56 MHz.

2 Features

Key features of the chip are as follows:

1) Pin-to-pincompatiblewith theoriginalAD9361 chip, direct replacement without changing external circuitry

2) Frequency band: 70MHz to 6.0GHz

3) Tunable signal bandwidth: 200kHz to 56MHz

4) EVM loss ≤3% (transmit/receive loopback mode, 40Msps; QPSK modulation)

5) 128preset local oscillator frequency points, enabling ultra-fastfrequencyhopping of 7μs;

6) Integrated 12-bit DAC and ADC

Power consumption ≤4W (2T2R, 56MHz bandwidth)

8) Supports TDD and FDD

9) Multi-device baseband synchronization

10) Integrated fractional N Frequency divider synthesizer, also supports external local oscillator input.

11) RX has automatic gain control and manual gain control modes.

12) CMOS/LVDS digital interface.

3 Parameter specifications.

VDD_GPO=3.3V, VDD_INTER=1.8V, VDD_CORE=1.3V, TA=25° C, Fref (reference clock frequency)=50MHz, Pref (reference clock level)=3dBm, internal local oscillator, test frequencies are 108M, 2400M, 4200M

Parameters		Symbols	Minimum Value	Typical Value	Maximum Value	Units	Conditions
Receiver Performance							
Center Frequency		*fLORX*	70		6000	MHz	
RxBandwidth		*BWSIGRX*	0.2		56	MHz	
Channel Gain Range		GRX-D		60		dB	
Gain Step		△ GRX-D		1		dB	
Full Scale Level	108MHz	Pfull		-60		dBm	ChannelGain73,Digital Domain Power6dBfs Conversion
	2400MHz			-54			
	4200MHz			-46			
Noise Figure	108MHz	NF		8		dB	Maximum Channel Gain
	2400MHz			5			
	4200MHz			8			
Third-Order Intermodulation	108MHz	IIP3		-9.5		dBm	Test Dual-Tone Width2M-10dBm/tone
	2400MHz			-6			
	4200MHz			-2			
Image Suppression	108MHz	IIR		62		dBc	Quadrature Correction Algorithm Enabled, Channel Gain 50dB
	2400MHz			66			
	4200MHz			70			
DC Suppression	108MHz	DCR		55		dBc	DCSuppression Algorithm Enabled,Channel Gain50dB
	2400MHz			60			
	4200MHz			57			
Spurious Suppression		SFDR		55		dBc	-50dBmInput Power,Channel Gain 50dB
InputS11		S11			-5	dB	70MHz~6GHz
Transmit Performance							
S22		S22			-4	dB	70MHz~6GHz
Maximum Output Power	108MHz	Pout		5		dBm	TestSignalCW,DigitalDomain Power6dBfs Conversion
	2400MHz			3			
	4200MHz			0			
Output Third Order Intermodulation	108MHz	OIP3		23		dBm	Test Dual-Tone Width 2M, -9dBfs/tone
	2400MHz			22		dBm	
	4200MHz			15		dBm	
Modulation Accuracy	108MHz	EVMTx		1		%	64QAMmodulationLTE 20M
	2400MHz			1.6			
	4200MHz			2			

TxCarrier Suppression	108MHz	LOITx		65		dBc	Calibration Algorithm Enabled, Maximum Channel Gain
	2400MHz			53			
	4200MHz			50			
Image Suppression	108MHz	IMRTx		60		dBc	Calibration Algorithm Enabled, Maximum Channel Gain
	2400MHz			55			
	4200MHz			55			
Emit Noise Floor	108MHz	Pnoise		-147		dBm/Hz	
	2400MHz			-145			
	4200MHz			-144			
Adjacent Channel Leakage Ratio	108MHz	ACLR		45		dB	64QAMModulation LTE20M
	2400MHz			45			
	4200MHz			45			
LoopbackEVMLoss		EEVMRX-T x		3		%	QPSKModulation
Emit Spurious Suppression	108MHz	SpurTX		70		dBc	
	2400MHz			55			
	4200MHz			55			
Local Oscillator Frequency Synthesizer							
Local Oscillator Frequency Stepping				2.4		Hz	
Local Oscillator Spurious Suppression				50		dBc	
Frequency Switching Time				80		us	Frequency Variation Range 2GHz
Phase noise	108MHz	10 KHz	PN	-127.8		dBc/Hz	
		100KHz		-121.8			
		1MHz		-132.5			
	2400MHz	10 KHz		-97.3			
		100KHz		-98.5			
		1MHz		-110.5			
	4200MHz	10 kHz		-94.1			
		100kHz		-95.8			
		1MHz		-106.4			
	108MHz			0.15			

Integral Phase Noise	2400MHz	INTnoise		0.74		Degree	
	4200MHz			1.0			
Reference Clock							
Reference Input	Frequency Range	*Fref*	19		50	MHz	
			10		80		
	Signal Level	*Fref*		1.3		dBm	VP-P
AuxiliaryADC							
Resolution		*BADC*		12		bit	
Input Voltage Range		*VIN_ADC*	0.1		VDDA1P3_BB - 0.1	V	
AuxiliaryDAC							
Resolution		*BDAC*		10		bit	
Output Voltage Range		*VO_DAC*	0.5		VDDA3P3 - 0.3	V	
Output Current		*IO_DAC*		10		mA	
Digital Specifications(CMOS)							
Input Voltage	high	*VIH*	VDD_INTER × 0.8		VDD_INTER	V	
	low	*VIL*	0		VDD_INTER × 0.2		
Input current	high	*IIH*	-10		10	uA	
	low	*IIL*	-10		10		
Output voltage	high	*VOH*	VDD_INTER × 0.8			V	
	low	*VOL*			VDD_INTER × 0.2		
SPItiming(1.8V)							
SPI_CLK	cycle	tcp	20			ns	
	pulse width	tMP	9				
SPI_ENBis established to the firstSPI_CLK rising edge		tsc	1				
LastSPI_CLKfalling edge SPI_ENBhold		tHC	0				
SPI_DIdata	Digital input hold toSPI_CLK	tS	2				
	data entry hold toSPI_CLK	tH	1				
	4-wiremode	tCO	3		8		

SPI_CLKon Rising edge to output data delay	3-wiremode	tCO	3		8		
	bus turnaround time time to read	htK	tH		tCO (max)		
	bus turnaround time time to read	htK	0		tCO (max)		
Digital data clock (CMOS,1.8V)							
DATA_CLKclock cycle		tcp	4.069			ns	
DATA_CLK andFB_CLK pulse Width		tMP	45% of tcp		55% of tcp		
Txdata	Create to FB_CLK	tx	1				
	keep until FB_CLK	tx	0				
DATA_CLKto data bus output delay late		tDDRX	0.25		1.25		
DATA_CLKtoRX_FEAMEdelay		tD	0.25		1.25		
pulse width	enable	t t	tcp				
	TxNRX	tTXNRXPW	tcp				
TXNRXESTABLISHED TOENABLE		tTXNRXSU	0				
bus turnaround time room	BeforeRX	tRPR	2*tcp				
	AfterRX	tRPST	2*tcp				
capacitive load				3		pF	
capacitive input				3			
Power characteristics							
1.3V supply voltage			1.267	1.3	1.33	V	
VDD_INTER power Source rated settings	CMOS		1.2		2.5		
	LVDS						
VDD_INTER Tolerance			-5		5	%	
VDD_GPOPower Supply Nominal Setting			1.3		3.3	V	
VDD_GPOTolerance			-5		5	%	
Current Consumption	Sleep Mode			180		uA	
	VDD_GPO			50			

Return Flow Temperature				260	℃	
Operating Temperature Range		-40		85		
Storage Temperature Range		-65		150		
ESD			500		V	
Maximum Junction Temperature	Tj			115	℃	
Maximum Input Port Power Capacity				2.5	dBm	

4 Functional Block Diagram

TheYXW9361 system functional block diagram is shown below:

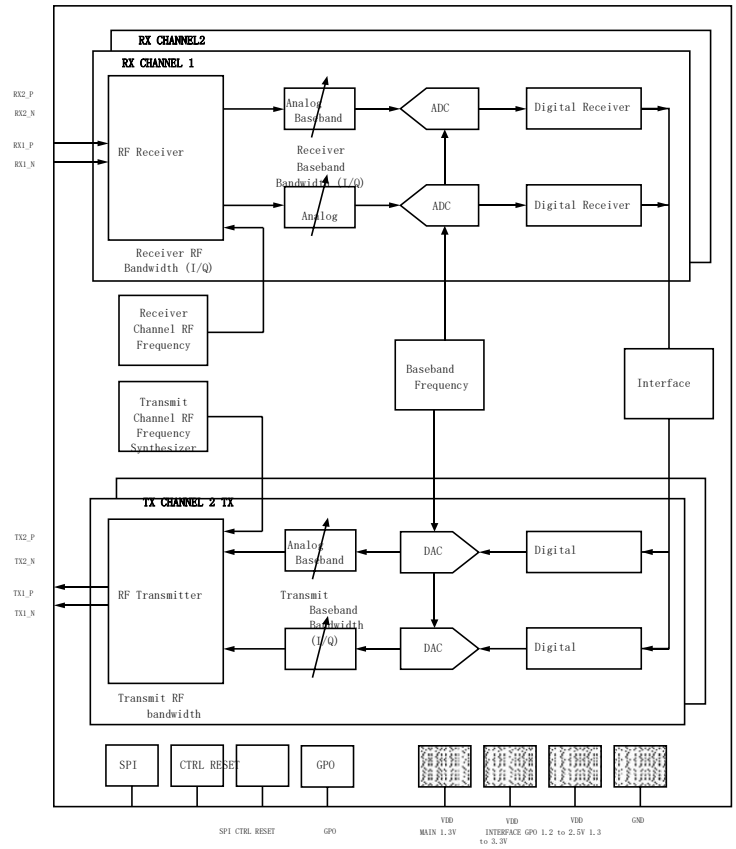


Figure 1 Functional block diagram

YXW9361 is mainly divided into two parts: receiving and transmitting.

The receiving part mainly includes: RF receiving front-end, analog baseband filter, receiving channel RF frequency synthesizer, ADC, digital receiving front-end, and baseband frequency synthesizer.

The transmitting part mainly includes: digital transmitting front-end, DAC, transmitting channel RF frequency synthesizer, RF transmitting front-end; as well as interface circuits and peripheral interface modules such as SPI.

Receive module:

1) The input receives two radio frequency signals;

2) The input signal is sent to the mixer after low-noise amplifier processing;

3) The mixer receives the input signal and multiplies the local oscillator signaltogenerate I analog signal;

4) The input signal is multiplied by the localoscillatorwith a phase shift

of90degrees to generate a Q-channel analog signal;

5）TheIandQ signals are fed into the subsequent filter after passing through the transconductance amplifier;

6）The signal is fed into the AD pre-processing stageafterpassing through the low-pass filter;

7）After gain processing, the signal is senttothe ADC module for analog-to-digital conversion;

8）The data after analog-to-digital conversionisdecimated by a 3-stage half-band filter, then processed bytheFIR filter, and finally output to theBBPfor further processing;

Transmitting Module:

1）TheBBP signal is senttothe FIR chip chip. The filter performs filtering;

2）TheFIR filter signal isfedinto three half-band filters for filtering;

3）The filtered signal isfedintoa12-bit DAC for digital-to-analog conversion;

4）The converted analog signal is fedintoan RF filter for analog filtering;

5）The filteredI/Qsignal is fed into a mixer for frequency conversion;

6）The two signals are added together and output;

5 Package and Pin Function Description

This deviceusesa BGA144 package. The dimensionsshouldconform to GB/T 7092. The outline is shown below:

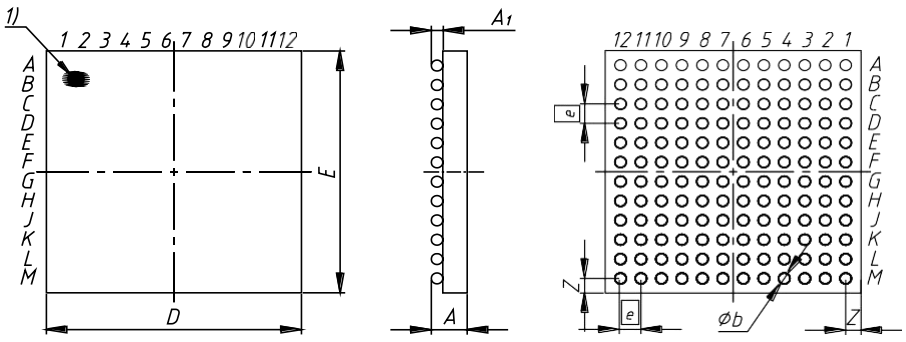


Figure 2: Outer Dimensions

Note1:Pin identification mark.

Unit: Millimeters

Table 1: Housing Dimensions

Dimension Symbols	Values		
	Mini mum	Nomi nal	Maxi mum

A	—	—	1.61
A1	0.20	—	0.60
b	0.35	0.45	0.55
D	9.90	—	10.10
e	—	0.80	—
D	9.90	—	10.10
Z	—	0.60	—

Chip pinout is shown below.

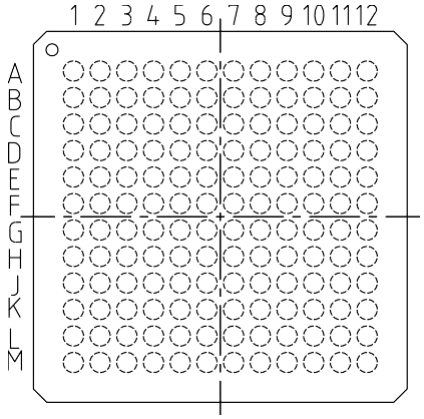


Figure 3 Terminal arrangement

Detailed description of the pin functions of the chip:

Table 2 Pin function description

Terminal serial number	symbol	Function description	Terminal serial number	symbol	Function description
A1, A2	RX2A_N, RX2A_P	Receive channel 2 differential input A	G1	RX_EXT_LO_IN	Receive LO external input
A3, M3	NC	hanging in the air	G2	RX_VCO_LDO_OUT	1.3v receive VCOLDO output filter
A5	TX_MON2	Transmit channel 2 power control output enter	G3	VDDA_RX_VCO	Receive VCO power
A7, A8	TX2A_N, TX2A_P	Transmit Channel 2 Differential Output A	G5	EN_AGC	Automatic gain enable
A9, A10	TX2B_N, TX2B_P	Transmit channel 2 differential output B	G6	ENABLE	control input
A11	VDDA_TX_VCO	Transmit VCO power supply	G7, G8	RX_FRAME_N, RX_FRAME_P	Receive Data Frame Input Signal
A12	TX_EXT_LO_IN	Transmit LO External Input	G9, H9	TX_FRAME_P, TX_FRAME_N	Transmit Data Frame Input Signal

B3	AUXDAC1	Auxiliary DAC1 Output	G11,H11	DATA_CLK_P, DATA_CLK_N	Receive Data Clock Output
B4 to B7	GPO3 to GPO0	General Output	H1,J1	RX1B_P,RX1B_N	Receive Channel 1 Differential Input B
B8	VDD_GPO	General Output Power	H4	TXNRX	Enable State Machine Control Signal
B9	VDDA1P3_TX_LO	1.3V Transmit Power	H5	SYNC_IN	Synchronization Input
B10	VDDA1P3_TX_VCO_LDO	Transmit VCO LDO 1.3V Input Input	H8	P1_D11/RX_D5_P	Bidirectional Digital Port
B11	TX_VCO_LDO_OUT	1.3V Transmit VCOLDO Output Filtering	H12	VDD_INTER	Digital IO Power Supply
C1, D1	RX2C_P, RX2C_N	Receive Channel 2 Differential Input C	J3	VDDA1P3_RX_SYNTH	1.3V Transmit Power Supply
Pin Serial Number	Symbol	Functional Description	Pin Serial Number	Symbol	Functional Description
C3	AUXDAC2	Auxiliary DAC2 Output	J4	SPI_DI	SPI Data Input
C4	TEST/ENABLE	Test Input	J5	SPI_CLK	SPI Clock Input
C5,C6 D5,D6	CTRL_IN0,CTRL_IN1,CTRL_IN3,CTRL_IN2	Gain Control Input	J6	CLK_OUT	Clock Output
D2	VDDA1P3_RX_RF	1.3V Receive Power	J7	P1_D10/RX_D5_N	Bidirectional Digital Port
D3	VDDA1P3_RX_TX	1.3V Power Supply	J8	P1_D9/RX_D4_P	Bidirectional Digital Port
D4, E4 to E6, F4 to F6, G4	CTR_OUT0, CTR_OUT1 to CTR_OUT3, CTR_OUT6 to CTR_OUT4 CTR_OUT7	Control Output	J9	P1_D7/RX_D3_P	Bidirectional Digital Port
			J10	P1_D5/RX_D2_P	Bidirectional Digital Port
			J11	P1_D3/RX _D1_P	Bidirectional Digital Port
			J12	P1_D1/RX_D0_P	Bidirectional Digital Port
D7	PO_D9/TX_D4_P	Bidirectional Digital Port	K1, L1	RX1C_P, RX1C_N	Receive Channel 1 Differential Input C
D8	PO_D7/TX_D3_P	Bidirectional Digital Port	K3	VDDA1P3_TX_SYNTH	1.3V Power Supply
D9	PO_D5/TX_D2_P	Bidirectional Digital Port	K4	VDDA1P3_BB	1.3V Baseband Power Supply
D10	PO_D3/TX_D1_P	Bidirectional Digital Port	K5	RESETB	Asynchronous Reset
D11	PO_D1/TX_D0_P	Bidirectional Digital Port	K6	SPI_ENB	SPI Enable Input
E1,F1	RX2B_P,RX2B_N	Receive Channel 2 Differential Input B	K7	P1_D8/RX_D4_N	Bidirectional Digital Port
E2	VDDA1P3_RX_LO	1.3v Analog Power Supply	K8	P1_D6/RX_D3_N	Bidirectional Digital Port

E3	VDDA1P3_TX_LO_BUFFER	1.3V Analog Power Supply	K9	P1_D4/RX_D2_N	Bidirectional Digital Port
E7	P0_D11/TX_D5_P	Bidirectional Digital Port	K10	P1_D2/RXD1_N	Bidirectional Digital Port
E8	P0_D8/TX_D4_N	Bidirectional Digital Port	K11	P1_D0/RX_D0_N	Bidirectional Digital Port
E9	P0_D6/TXD3_N	Bidirectional Digital Port	L4	RBIAS	Reference Offset Input
E10	P0_D4/TX_D2_N	Bidirectional Digital Port	L5	AUXADC	Auxiliary ADC Input
E11	P0_D2/TX_D1_N	Bidirectional Digital Port	L6	SPI_DO	SPI Data Output
E12	P0_D0/TX_D0_N	Bidirectional Digital Port	M1, M2	RX1A_P, RX1A_N	Receive Channel 1 Differential Input A
F2	VDDA1P3_RX_VCO_LDO	1.3V Receive VCO LDO Output Filter	M5	TX_MON1	Transmit Channel 1 Power Control Input
F8	P0_D10/TX_D5_N	Bidirectional Digital Port	M7,M8	TX1A_P,TX1A_N	Transmit Channel 1 Differential Output A
F10, G10	FB_CLK_P, FB_CLK_N	Feedback Clock	M9, M10	TX1B_P, TX1B_N	Transmit Channel 1 Differential Output B
F12	VDDD1P3_DIG	1.3V Digital Power Supply	M11, M12	XTALP,XTALN	Reference crystal input
A4, A6, B1, B2, B12, C2, C7 to C12,F3, H2, H3, H6, J2, K2, L2, L3, L7 to	VSSA	Analogly	D12, F7, F9, F11, G12, H7, H10, K12	VSSD	digitally
Terminal serial number	symbol	Function description	Terminal serial number	symbol	Function description
L12, M4, M6					

6 Detailed function description of the chip

6.1 General characteristics

YXW9361is a highly integrated radio frequency (RF) transceiver that integrates all necessary transceiver functions into a single device.

RF, of Mixed signal and digital processing modules. Its excellent programmability enables YXW9361 to be applied to a variety of communication standards.

Including frequency division duplex (FDD) and time division duplex (TDD) systems. In addition, the YXW9361 also allows interfaces with various baseband processors (BBPs) through a single-channel 12-bit parallel data port, dual-channel 12-bit parallel data port, or 12-bit low-voltage differential signaling (LVDS)
connected.

TheYXW9361 also provides a self-calibration and automatic gain control (AGC) system that maintains high performance levels over a wide range of temperatures and input signal conditions. Additionally, the YXW9361 offers a test mode that allows system designers to insert test tones for use in debugging designs during prototyping and optimizing radio configurations for specific applications.

6.2 clock input

YXW9361 provides two options for using the reference clock. The first option uses a specialized crystal oscillator with a frequency of 19MH.
and 50MHz, connected between the XTALP and XTALN pins. The second option would be an external oscillator or clock divider
components to the XTALN pin (where the XTALP pin remains disconnected). If an external oscillator is used, the frequency can vary between 10MHz and 80MHz. This reference clock is used to provide a reference for the frequency synthesizer blocks that generate all data clocks, sample clocks, and local oscillators internally within the device.

6.3 digital data interface

TheYXW9361 data interface can be configured as single-ended CMOS format or differential LVDS format.

Both formats can be configured in various ways to meet system requirements for data sequencing and data port connectivity. Specifically, this includes single-port data bus, dual-port data bus, single data rate, dual data rate, and various data sequencing combinations to transmit data from different channels across the bus at the appropriate time.

Bus transmission is controlled by a simple hardware handshake signal. Both

ports can operate in bidirectional (TDD) mode or full-duplex (FDD) mode. In the latter mode, half the bits are used for transmitting data and half for receiving data. The interface can also be configured so that one of the data ports is used for applications that do not require high data rates and prefer to use fewer interface pins.

6.3.1 CMOS Format Transmission Modes

Data transmission between the device and the BBP through CMOS mode can be configured through simple hardware control signals to choose to use only one parallel data line or two data lines. These two data ports can operate in FDD mode or TDD mode. When in TDD mode, the same data port tx data and rx are used.Data is transmitted through time-sharing alternating transmission. The digital interface mainly includes signals: P0_D[11:0], P1_D[11:0], DATA_CLK, FB_CLK, RX_FRAME, TX_FRAME, TXNRX, ENABLE.

working mode

In CMOS transmission mode, there are 4 different transmission mode settings according To the system structure and data rate.

Table 3 Working modes

Transmission mode	YXW9361state machine mode	data rate
Single port half duplex	TDD	Less than61.44MOXz
Single port full duplex	FDD	Less than30.72MOXz
Dual port half duplex	TDD	Greater than122.88MOXz
Dual port full duplex	FDD	Less than61.44MOXz

Single-Port Half-Duplex Mode

Single-channel half-duplex mode is used in TDD mode with data ratesbelow61.44MHz. In this mode, the data bus can be manually configured as a bidirectional data bus, allowing both data reception and transmission. Depending on the channel selection, four modes can be configured for reception and transmission:1R1T,2R1T, 1R2T,and 2R2T. The data bus can operate at single-edge and dual-edge data rates.

During data reception, the data bus is driven by the YXW9361, meeting the

set up and hold time requirements for data and DATA_CLK. The BBP captures data through DATA_CLK. During data transmission, the data bus is driven by the BBP, meeting the setup and hold time requirements for data and FB_CLK. TheYXW9361 captures data through FB_CLK. During data transmission, ENABLE can have two modes: level mode and pulse mode.

The direction of data transmission is determined by TXNRX.When the TXNRX signal is low and in RX or FDD state, the data bus is configured for receiving (datafromYXW9361toBBP); correspondingly, when the TXNRX signal is high and not in RX or FDD state, the data bus is configured for transmitting (data from BBP toYXW9361).

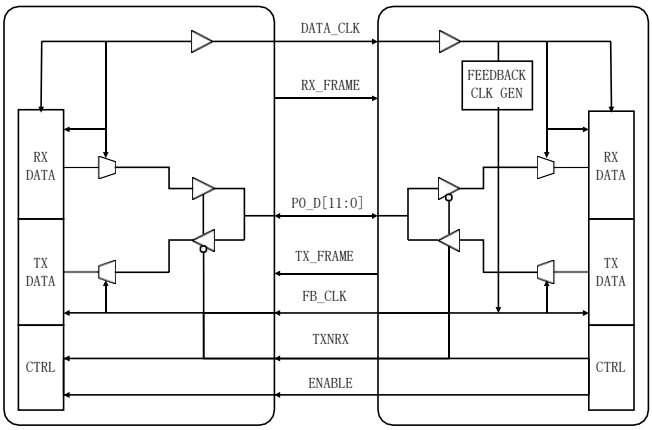


Figure 4 Single-channel half-duplex mode

RX_FRAME and TX_FRAME indicate the start of data sampling. The RX_FRAME signal can be set to go high once during each transmission or to go high at the beginning of each data frame and then repeat with a 50% duty cycle until data transmission is complete. TX_FRAME is similar.

During the transmission process,the BBP drives the data on the data bus through FB_CLK and TX_FRAME. During the reception process,theYXW9361drivesthedata on the data bus through DATA_CLK and RX_FRAME. In this mode, IQ data appears on the data bus in a time-division multiplexing manner. The four transmission modes are shown in the figure below:

- The1R1T's dual-edge transmission mode and single-edge transmission mode are selected through configuration register 0x12. The relevant registers are 0x010, 0x011, and0x012. In this transmission mode, the system use sone RX/TX channel.The IQ data transmission format is: I,Q,I,Q,I,Q,I,Q,……

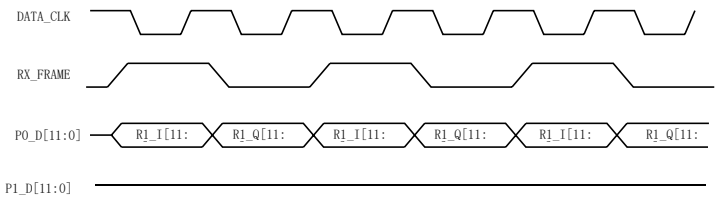


Figure 5 1R1T Single-port single-edge receive

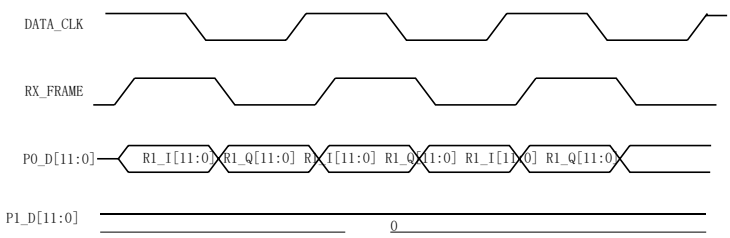


Figure 6 1R1T Single-port Single-edge Reception

- 2R2TSingle-port Dual-channel Dual-edge Transmission Mode, this mode uses 2 sets of RX/TX channels, and the IQ of the two RX/TX channels

Data transmission format is: I1,Q1,I2,Q2,I1,Q1,I2,Q2,…. The receive timing diagram is as follows, and the transmit timing diagram is similar.

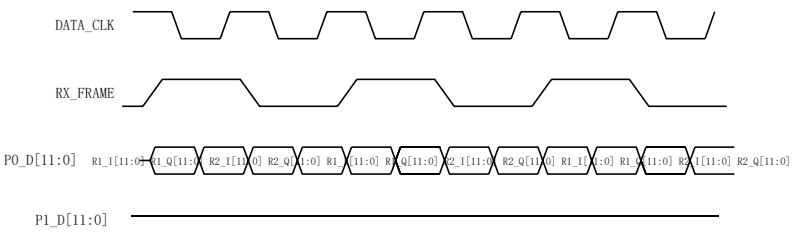


Figure 7 2R2T Single-Port Dual-Edge Receiver

- 1R2T and 2R1T are single-port dual-edge transmission modes. In this mode, the clock frequency, sampling period, and data capture time are the same as in the 2R2T mode. This mode uses one set of RX/TX channels to transmit correct data and an other set of RX/TX channels to transmit arbitrary data. Arbitrary data will notbereceivedbyYXW9361. The IQ data transmission format is: I, Q, X, X, I, Q, X, X,I,Q, ...

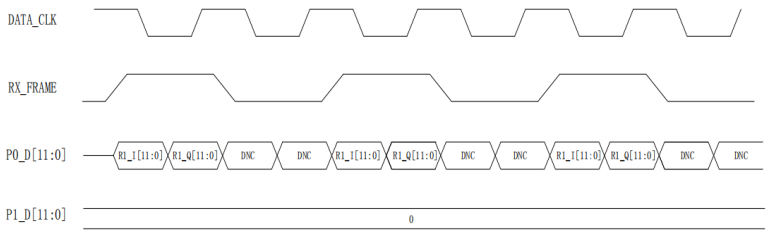


Figure 8 1R2T Single-Port Dual-Edge Receiver

Single-Port Full-Duplex Mode

Single-channel full-duplex mode is used in FDD operating mode and the data rate is lower than 30.72MOXz. In this mode, the data bus is divided into two parts,6bits transmit RX data and the other 6 bits transmit TX data.This mode also supports all RX -TX configurations. The data bus can operate in single-edge mode and dual-edge mode. In single-channel mode, only one parallel data port can be used.

In this mode, the sending data is output by BBPonP0_D[11:6],which meets the setup time and hold time of FB_CLK and P0_D[11:6]. YXW9361 grabs the data on the bus through FB_CLK; the receiving data is output by YXW9361 onP0_D[5:0],which meets the setup time and hold time of DATA_CLKandP0_D[5:0].BBP Grab the data on the bus through DATA_CLK.During the transmission process, the pulse signal (or rising edge) on the ENABLE pin triggers the start of the transmission, and another pulse signal (or falling edge) marks the end of the transmission.

The RX_FRAME and TXFRAME signals indicate the start of data sampling. RX_FRAME can be set to go high once at the start of each data transmission burst, or to go high at the start of each frame of data transmission and repeat with a50%duty cycle until the data transmission is complete. TX_FRAME is similar.

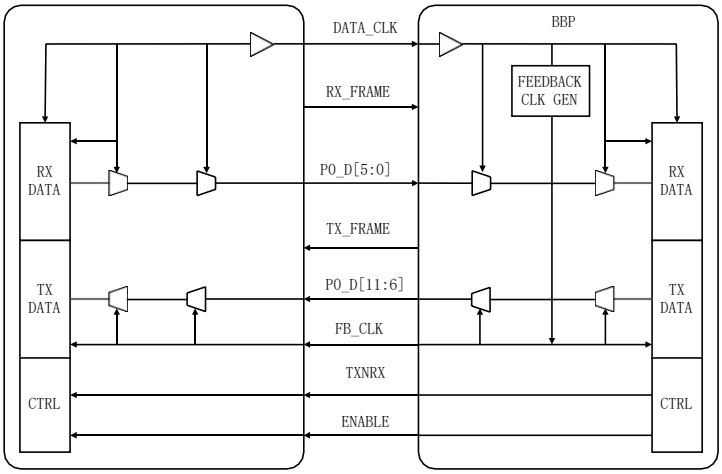


Figure 9 Single-port full-duplex YXW9361 and BBP

In this mode, the transmitted data is sampled and transmitted in two parts: the first group of 6 bits transmits the high-order bits, and the second group of 6 bits transmits the low-order bits. Similarly, received data is transmitted in the same manner. In this mode, one set of RX/TX channels is used for time-division multiplexing of IQ data transmission on the data bus. The data transmission format of IQ is: IMSB, QMSB, ILSB, QLSB, ...

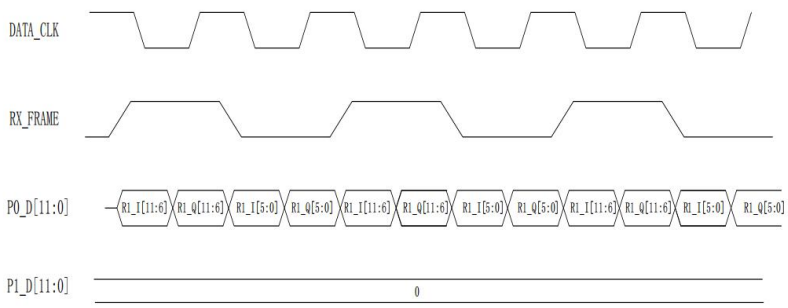


Figure 10 1R1T Single-port full-duplex dual-edge receiver

When using two RX/TX channels, IQ data is transmitted on the data bus in a time-division multiplexing manner. The clock frequency, sampling period, and data capture time are completely consistent with the 2R2T mode when the system

transmits data in 1R2T or 2R1T format. The IQ data transmission format is: I1MSB, Q1MSB, I1LSB,Q1LSB, I2MSB,Q2MSB, I2LSB,Q2LSB,……

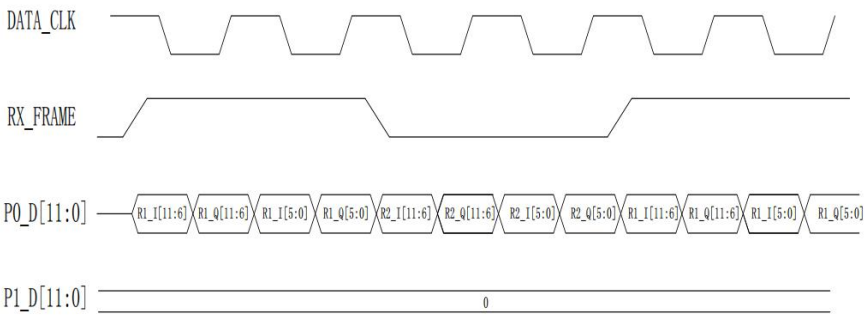


Figure 11 2R2T Single-channel full-duplex dual-edge receiver

Dual-port half-duplex mode

Dual-channel half-duplex mode is used in TDD mode with a data rate exceeding122.88MHz. This mode employs two parallel data ports: port P0transmitsI-channel data, and port P1transmitsQ-channel data. Both parallel data ports are bidirectional.

Both data ports can operate in single-edge or dual-edge mode. The direction of data transmission is primarily determined by

Theeffective range of the RX/TX channels.

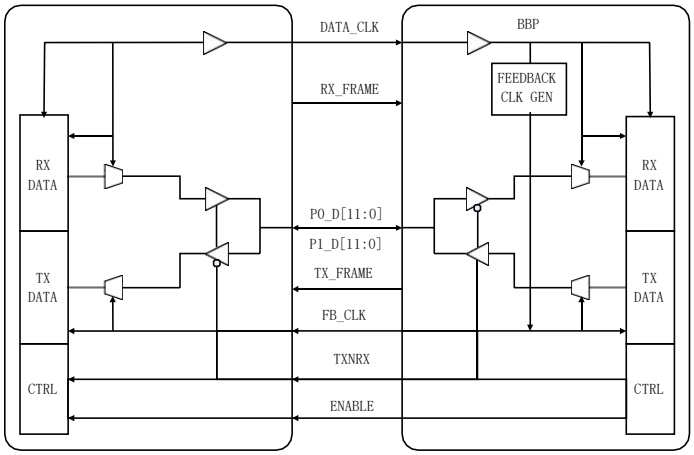


Figure 12 Dual-Port Half-Duplex

When RX is receiving and transmitting, the data on the two parallel data ports comes from YXW9361. When the setup time and hold time of data and DATA_CLK are met, BBP uses DATA_CLK to capture the data on the bus. When TX is transmitting and transmitting, the data on the two parallel data ports come from BBP. When the setup time and hold time of data and FB_CLK are met, YXW9361 uses FB_CLK to capture the data on the bus.

Data transfer begins with the first pulse of ENABLE (or pulled high) and ends with the next pulse of ENABLE (or pulled low). The direction of data transmission is determined by TXNRX. When the TXNRX signal is lowandYXW9361isinFDDor RX state, the data transmission is in the receiving direction(YXW9361toBBP). When the TXNRX signal is high and the YXW9361 is in other states, the data transmission is in the sending direction (BBP to YXW9361 ）。 During data transmission, RX_FRAME and TX_FRAME are used as indication signals for data sampling. This signal can

to set to level mode and pulse mode. There are four data transmission formats depending on the channel selection:

1R1T:P0:I,I,I,..... P1: Q,Q,Q,.....

1R2T/2R1T: P0: I1,X,I1,X,…… P1: Q1,X,Q1,X,…...

2R2T:P0: I1, I2, I1, I2, ... P1: Q1,Q2,Q1,Q2,……

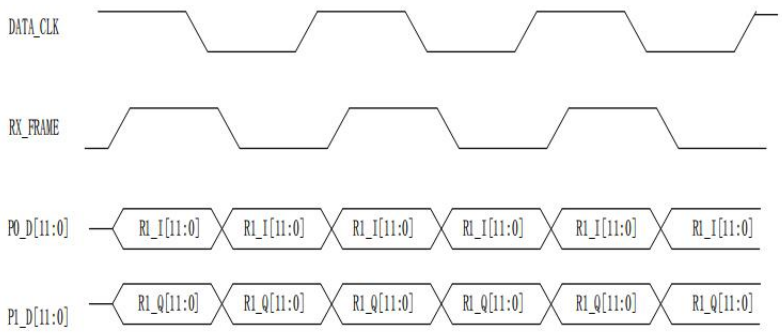


Figure 13 1R1T Dual-Port Half-Duplex Receiver

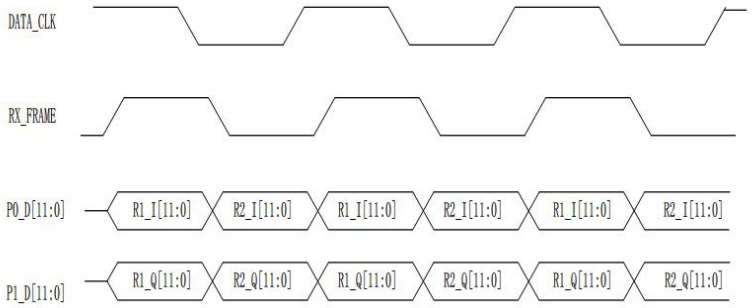


Figure 14 2R2T dual-port half-duplex reception

Dual port full duplex mode

The dual-channel full-duplex mode is used in FDD mode and the data rate is lower than 61.44MOXz. In this mode, two parallel data ports are used, where PO is used to transmit RX data andP1is used to transmit TX data. The data bus can ensure simultaneous operation of TX/RX direction transmission. Data is transmitted in full-duplex between BBP and YXW9361. Each data bus operates at twice the speed of dual-port TDD mode to achieve the same RX/TX data rate. Each data bus can operate in single-edge mode or dual-edge mode.

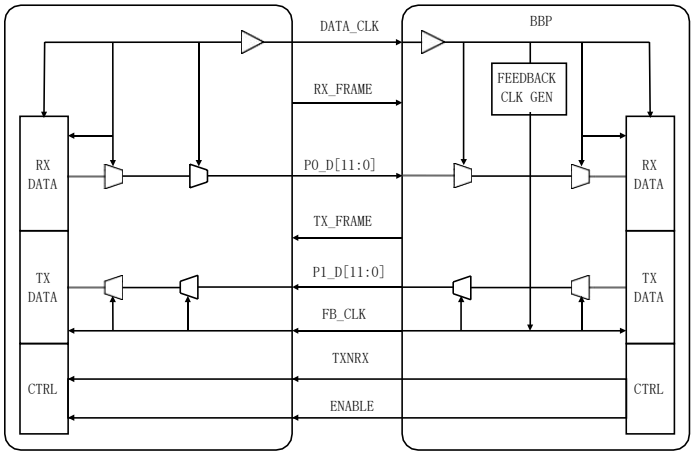


Figure 15 Dual-channel Full-Duplex

The data sent by TX is on the P1_D data bus. When the setup and hold times of data and FB_CLK are satisfied,

YXW9361uses FB_CLK to capture data on the bus. RX receives data onthePO_D data bus. When the setup and hold times of data and DATA_CLK are satisfied,

BBP uses DATA_CLK. Capture data on the bus. Data transmission begins with the first pulse signal (or pull-high) of ENABLE and ends with the next pulse signal (or pull-low) of ENABLE.

During data transmission, RX_FRAME and TX_FRAME are used as indicator signals for data sampling. These signals can be set to level mode and pulse mode.

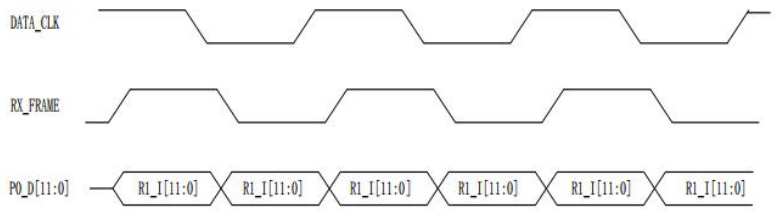


Figure 16 1R1T Dual-Port Full-Duplex Receiver

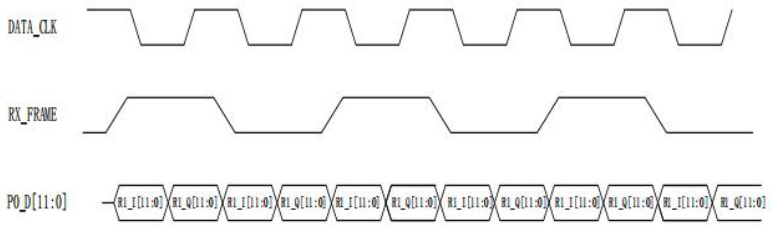


Figure 17 2R2T Dual-Port Full-Duplex Receiver

6.3.2 LVDS Format Transmission Mode

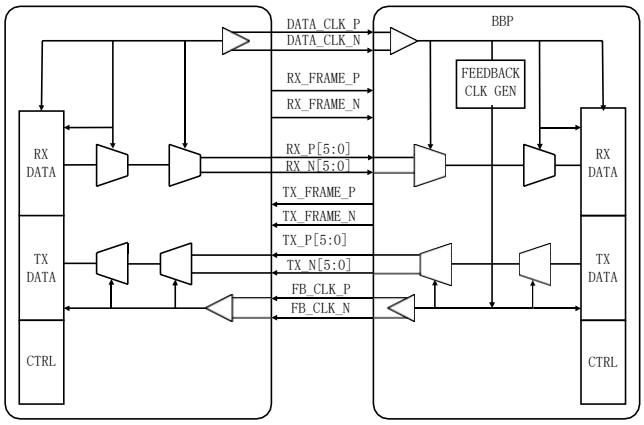


Figure 18 Dual-channel full-duplex LVDS mode

LVDS transmission method

LVDS transmission mode only has dual-channel full-duplex mode. The dual-channel full-duplex mode is enabled by writing the SPI register. In this mode, thePOandP1parallel data ports are LVDS differential signals, and the data bus is divided into RX_D[5:0] and TX_D[5:0]two parts of the bus, these two parts of the bus operate simultaneously to ensure full-duplex data transmission and reception between BBP and YXW9361.

The data transmission(TX_D[5:0]),FB_CLK,and TX_FRAME signals are driven by BBP. Under the premise of meeting the requirements of setup time and hold time between data, TX_FRAME, and FB_CLK, YXW9361 uses FB_CLK to captured at a and TX_FRAME signal. The sampled data is sent through the TX_FRAME signal set on the TX_D[5:0] bus and sent in two parts: first, the high 6 bits of data are sent and then thelow6 bits of data are sent.

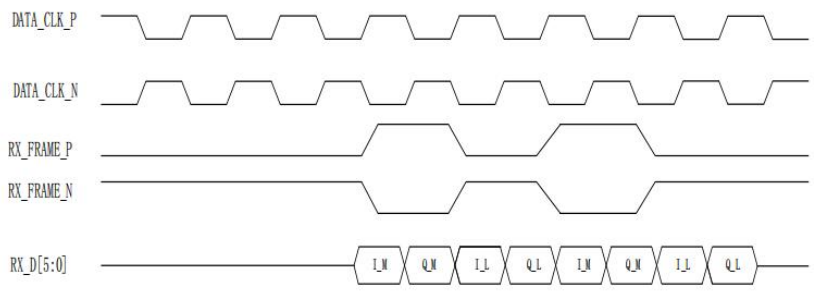


Figure 19 Receive Timing Diagram

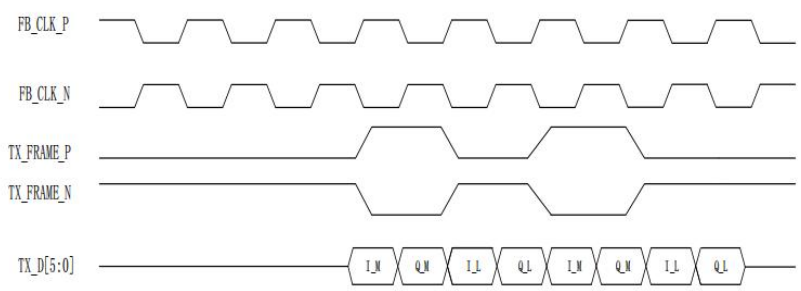


Figure 20 Transmit Timing Diagram

Receive data(RX_D[5:0]),DATA_CLK and RX_FRAME signals are drivenbyYXW9361. Under the requirement of meeting the setup time and hold time between RX_D[5:0], RX_FRAME and DATA_CLK, BBP uses DATA_CLK to captured at a and RX_FRAME signal.

The received sampled data is set at RX_FRAME signal. On the RX_D[5:0] bus, the transmission is divided into two parts. The high 6-bit data is sent first and then the low 6-bit data is sent. There are 4 corresponding channel configurations:1R1T, 2R1T,1R2Tand 2R2T.

- In the 1R1T channel configuration,IQ data appears on the data bus in a time-division multiplexing manner. In this mode,the conversion of TX_FRAME and RX_FRAME signals and data is consistent.IMSB and QMSB portions are transmitted when TX_FRAME and RX_FRAME are high, and ILSB and QLSB are transmitted when TX_FRAME and RX_FRAME are low. The TX_FRAME and RX_FRAME signals have a 50% duty cycle. The IMSB indicates the start of each frame of data. Data transmission format: IMSB, QMSB, ILSB, QLSB,…..

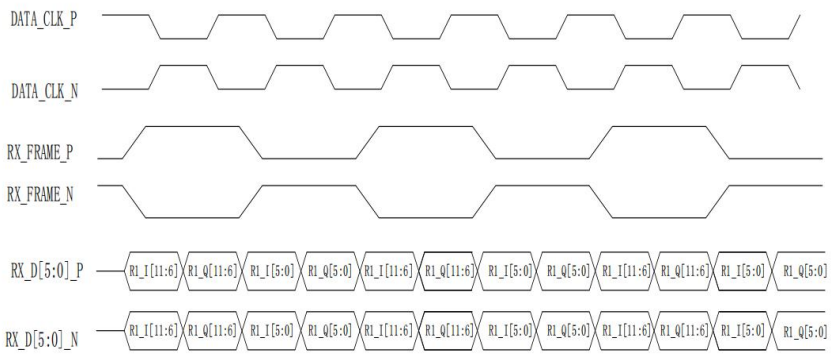


Figure 21 1R1T Dual-Channel Full-Duplex Receiver

- 2R2T Channel Configuration, IQ data is upsampled from RF channel 1/2, data transmission format is: I1MSB,Q1MSB, I1LSB,Q1LSB, I2MSB,Q2MSB,I2LSB,Q2LSB,…..

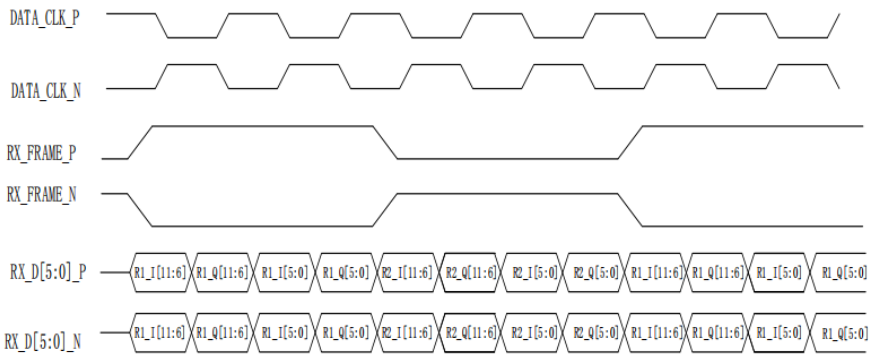


Figure 22 2R2T Dual-Channel Full-Duplex Receiver

- The1R2T/2R1T channel configuration has the same clock frequency, sampling period, bus data rate, and data capture time asthe2R2T. In this configuration mode, only one channel is used to transmit correct data, and the other channel transmitting arbitrary data will beignoredby YXW9361. Forexample,in the 2R1T channel configuration, the transmittingchanneluses TX1, and the data transmission format is: I1MSB,Q1MSB, I1LSB,Q1LSB, X,X,X,X,.....

6.4 Enable state machine

TheYXW9361 transceiver includes an enable state machine (ENSM) that allows real-time control of the device's current state. During normal operation, the device can be placed in a number of different states, including:

•SLEEP:Sleep state, except for SPI - related circuits, all others are turned off.

•WAIT: Standby state, the frequency synthesizer is turned off (the sleep and wait states in the original film are one state, and the design is also like this).

•CALIBRATION: Perform various calibrations.

•ALERT: The frequency synthesizer is turned on. It will jump to the next state after the frequency synthesizer performs correct calibration to ensure the wireless spectrum sent and received by the chip.

ENSM has two control methods: SPI control and pin control.

In SPI control mode, asynchronous control of ENSM is achieved by writing to the SPI register to enter the next state from the current state. SPI control is an asynchronous control method. When real-time control is not required, it is recommended to use SPI to control ENSM. If the BBIC can accurately perform SPI write operations, SPI control can also be used in synchronous control scenarios.

In pin control mode, the current status can be controlled in real time through the ENABLE pin and TXNRX pin. ENSM supports TDD or FDD operation mode, depending on the configuration of the corresponding SPI register. If the BBIC has a GPIO output that can be controlled in real time, it is recommended to use the ENABLE and TXNRX pin control methods. In order to make the current state of ENSM enter the next state, the enable function of the ENABLE pin can be driven by a pulse or level.

When using pulses, the minimum pulse width must be one FB_CLK period. In level mode, the ENABLE and TXNRX pins are also detected by YXW9361 on their edges, and must meet the minimum pulse width requirement of one FB_CLK period. 。 In FDD mode, the ENABLE and TXNRX pins must be remapped as real-time RX and TX data transfer control signals. In this mode, the ENABLE pin enables or disables the receive signal, and the TXNRX pin enables or disables the transmit signal. In this mode, ENSM is no longer valid, allowing these pins to control all data flow.

6.5 SPI Interface

6.5.1 SPI Interface Register and Timing Description

The chip's internal registers have an 11-bit address width, ranging from 0x000 to 0x5FF, and an 8-bit data width. The SPI interface supports writing and reading 1 to 8 bytes of data, and supports both MSB and LSB modes.

1. MSB Mode

When performing multi-byte operations, the register address is decremented. For example, if the starting register address is 0x02A, and four consecutive bytes are operated on, the addresses of the subsequent three bytes will be 0x029, 0x028, and 0x027, respectively. Furthermore, the frame order for the SPI

instruction section is D15~D0, and the frame order for the data section is D7~D0.

2. LSB Mode

When performing multi-byte operations, the register address increments. For example, if the starting register address is 0x02A, and four consecutive bytes are operated on, the addresses of the subsequent three bytes are 0x02B, 0x02C, and 0x02D, respectively. Furthermore, the frame order for the SPI instruction section is D0~D15, and the frame order for the data section is D0~D7.

The following table lists the timing specifications for each signal line. The relationship between these parameters is shown in Figure (23), taking the three-wire mode as an example.

Table 4 Timing Specifications

Parameters	Minimum Value	Maximum Value	Description
TCP	20ns		SPI_CLK Clock Cycle
TMP	9ns	8ns	SPI_CLK Pulse Width
TSC	1ns		SPI_ENB Setup Time to First Rising Clock Edge
THC	0ns		Last SPI Clock Falling Edge to SPI_ENB Disabling hold time
TS	2ns		SPI_DI data setup time
TH	1ns		SPI_DI data hold time
TCO	3ns	TCO (max)	SPI_CLK clock rising edge to output data delay, bus rotation time after the last address bit of the master controller
THZM	TH		

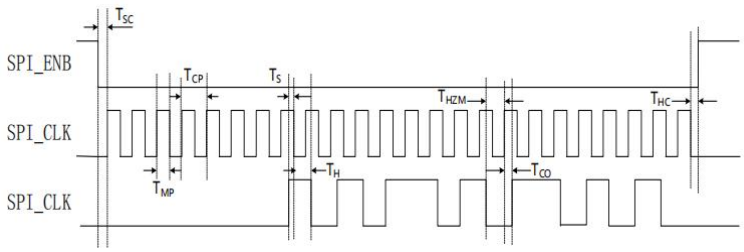


Figure 23 SPI Interface Timing Diagram

6.5.2 SPI Write Timing (Single Byte Write Example)

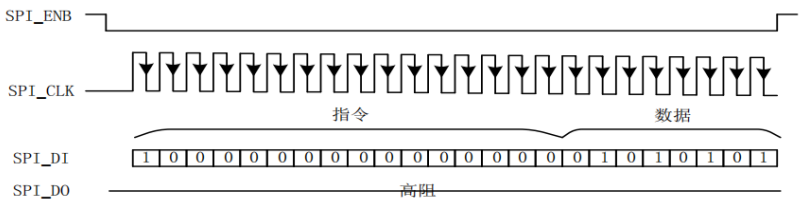


Figure 24 0x000 register writing 0x55 timing diagram

It should be noted that this timing is to send data (data on DI) to Spi_control on the rising edge of the clock.

Spi_control samples on the falling edge.

6.5.3 SPI read timing (take single-byte read as an example)

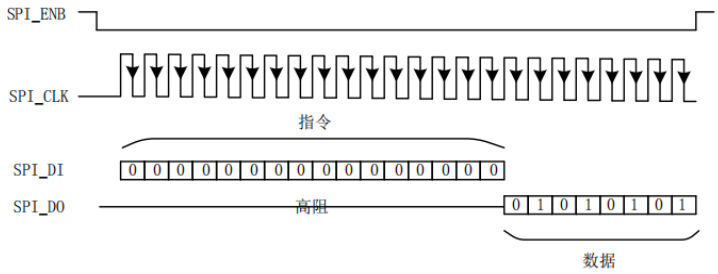


Figure 25 0x000 register read back timing diagram

Read the 0x55 information previously written to the 0x000 register through SPI_DO. It should be noted that in SPI_DO

Before data is output, its logic value remains in a high-impedance state. Similarly, DI and DO send out data on the rising edge and sample the data on the falling edge.

6.6 control pin

6.6.1 Control output (CTRL_OUT[7:0])

YXW9361 provides 8 synchronous real-time output signals, which are used as BBP interrupts. These outputs can be configured to output some internal settings and measurements. These settings and measurements can be used by the BBP to monitor the transceiver's performance under different conditions. The control output pointer register selects which information is output to these pins, while the control output enable register determines which signals the BBP will activate for monitoring. Signals for manual gain mode, calibration flags, state machine status, and ADC output are some of the outputs that can be monitored on these pins.

6.6.2 Control Inputs (CTRL_IN[3:0])

The YXW9361 provides four edge-detected control input pins. In manual gain mode, the BBP can use these pins to change the gain table index in real time. In transmit mode, the BBP can use these pins to change the transmit gain in real time.

6.7 GPO Pins (GPO_3 to GPO_0)

The YXW9361 provides four general-purpose logic output pins supporting 3.3V: GPO_3, GPO_2, GPO_1, and GPO_0. These pins can be used to control other peripheral devices, such as voltage regulators and switches, via the YXW9361 SPI bus, or they can act as slave devices to the internal YXW9361 state machine.

6.8 Auxiliary Converter

6.8.1 AUXADC

The YXW9361 contains an auxiliary ADC that can be used to monitor system functions such as temperature and power output. AUXADC is 12 bits wide

, the input range is 0 V to 1.25 V. When enabled, the ADC is free running. An

SPI read operation provides the last value latched at the ADC output. A multiplexer placed before the ADC allows the user to select between the AUXADC input pin and the built-in temperature sensor.

6.8.2 AUXDAC1 and AUXDAC2

The YXW9361 contains two identical auxiliary DACs that can provide power amplifier (PA) bias or other system functions.

。 The auxiliary DAC is 10 bits wide, has an output voltage range of 0.5VtoVDD_GPO-0.3V, a current drive of 10mA, and can be controlled directly through the internal enable state machine.

6.9 power supply

The chip is powered by the following three power supplies: analog power supply (VDDD1P3_DIG/VDDAx = 1.3 V), interface power supply (VDD_INTER

= 1.8 V) and GPO power supply (VDD_GPO = 3.3 V).

For applications requiring optimized noise performance, it is recommended to use a low-noise, low-dropout (LDO) regulator to separate and provide the 1.3 V power supply. The following diagram illustrates the recommended approach.

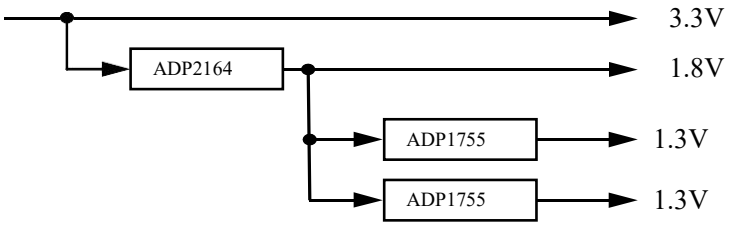


Figure 26 Power Supply Block Diagram

For applications where board space is limited and optimal noise performance is not an absolute requirement, the 1.3 V module power supply can be directly provided by a switch, and a more integrated power management unit (PMU) can be used. The following diagram illustrates this approach.

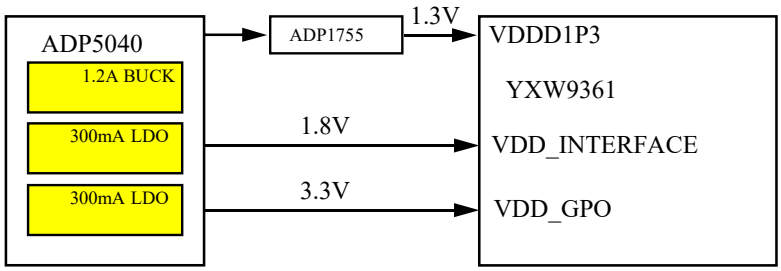
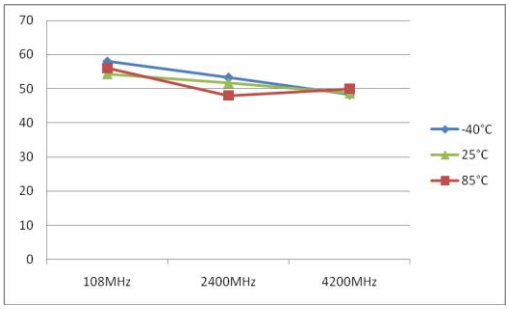


Figure 27 Power Management Block Diagram

7 Product Measured Results

Partial measured results are shown below (VDD_GPO=3.3V, VDD_INTER=1.8V, VDD_CORE=1.3V, Fref (reference clock frequency)
=50MHz,Pref(reference clock level) =3dBm, internal local oscillator, testfrequency points are 108M, 2400M, 4200M)



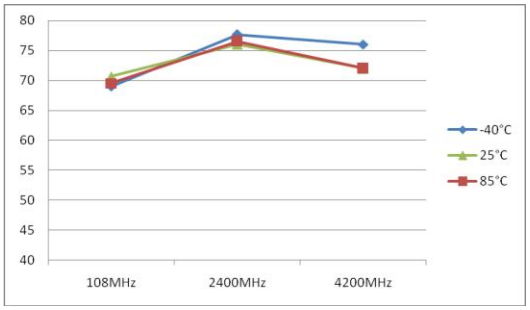
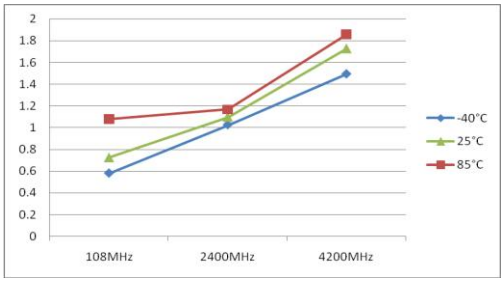


Figure28RX SFDR diagram Figure 29 RX image suppression diagram



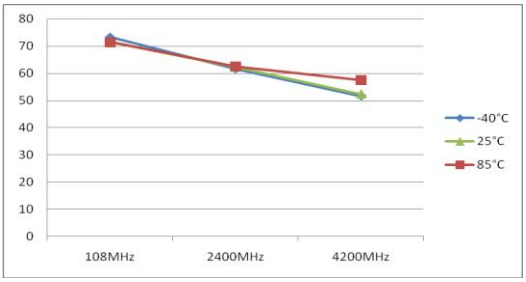
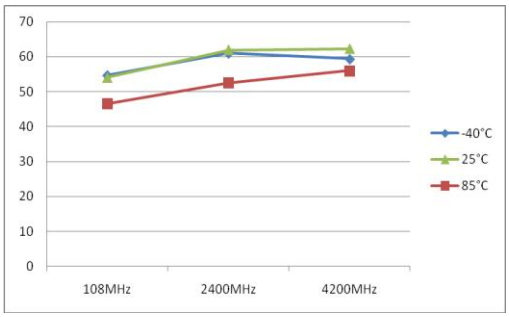


Figure30TX EVMdiagramFigure 31 TX spurious suppression diagram



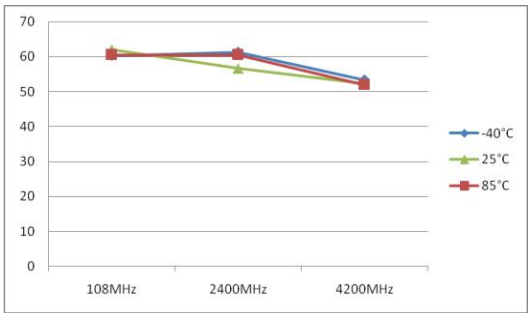


Figure32TX ACLR diagram Figure 33 TX image suppression diagram

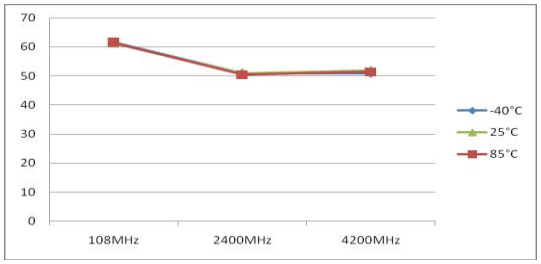
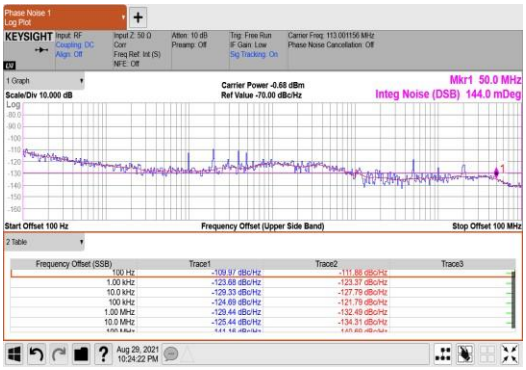
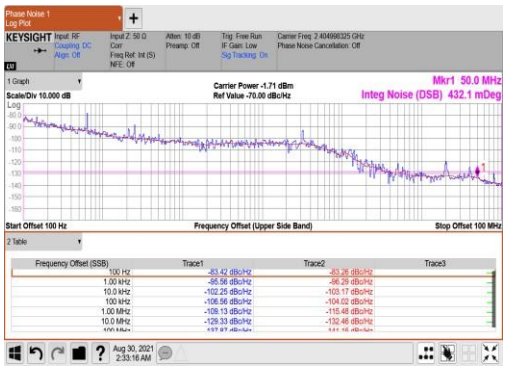


Figure34Schematic diagram of carrier suppression



(a) 108MHz



(b) 2400MHz



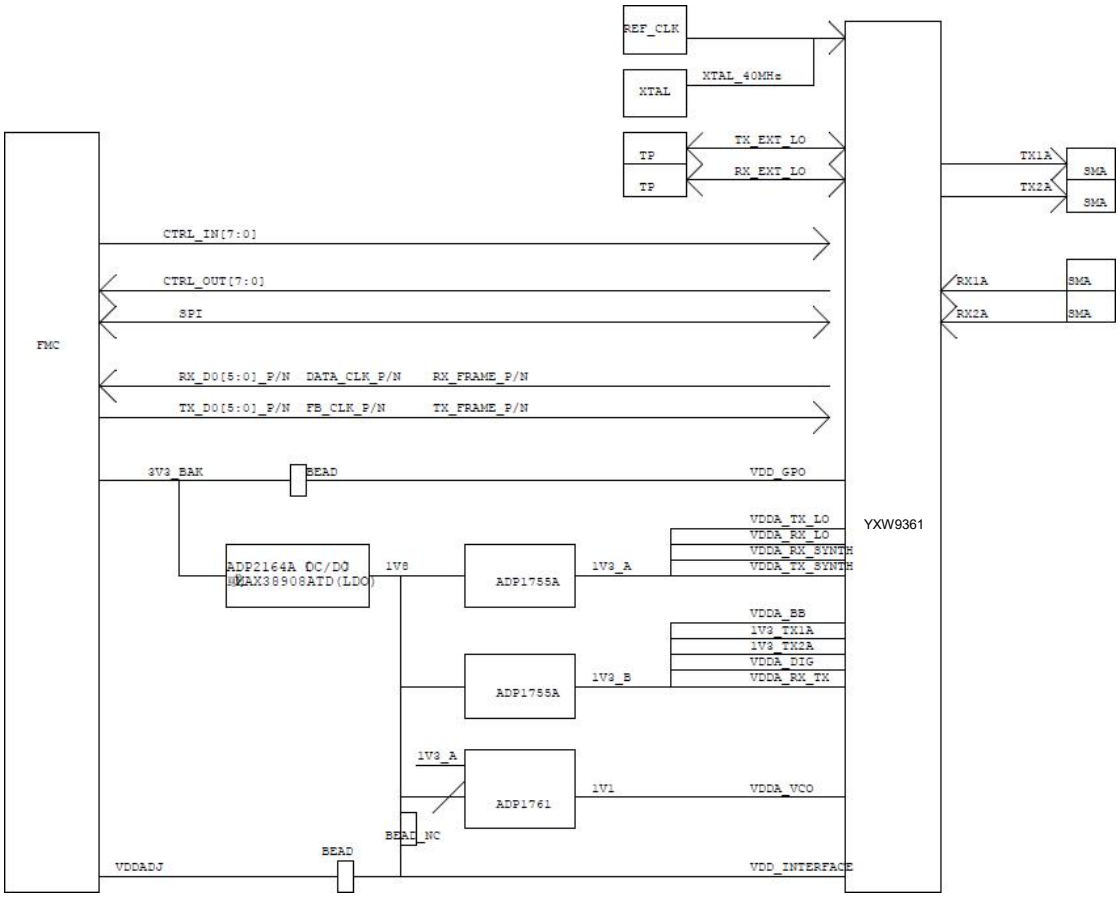
(c) 4200MHz

Figure35TX phase noise diagram

8 Product application information

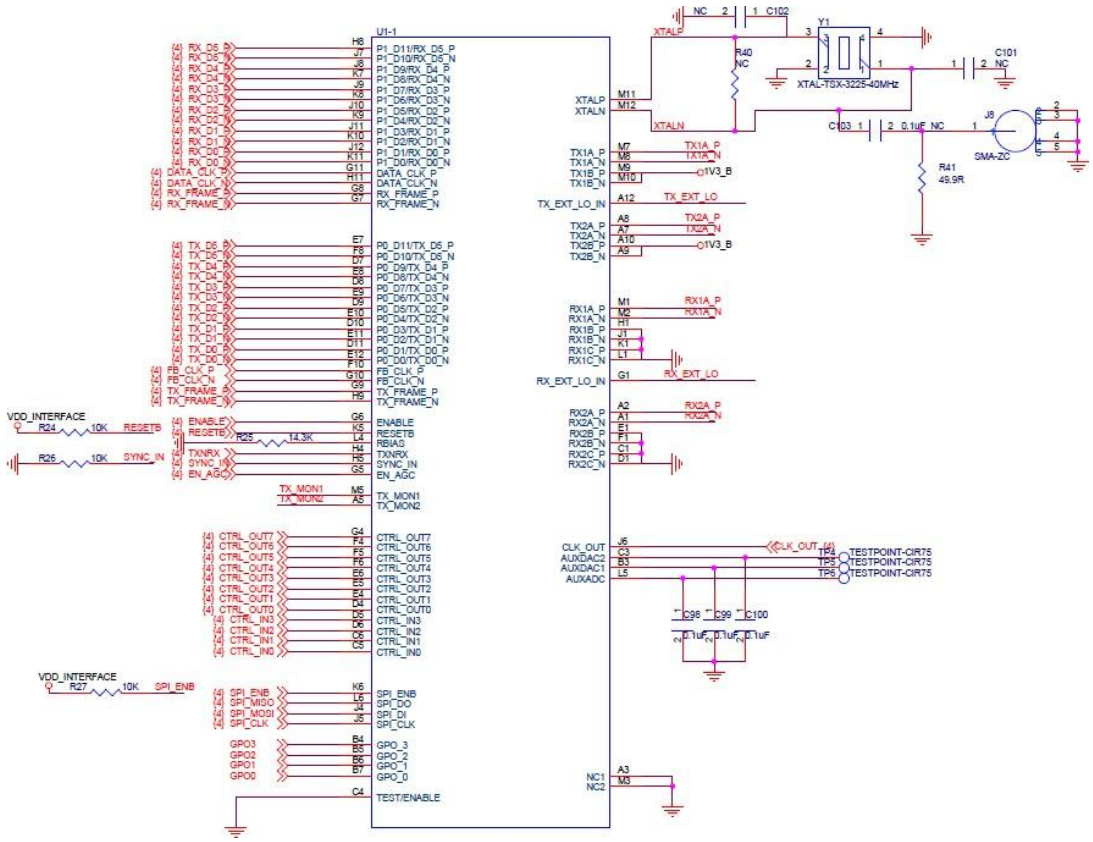
8.1 Topology reference schematic

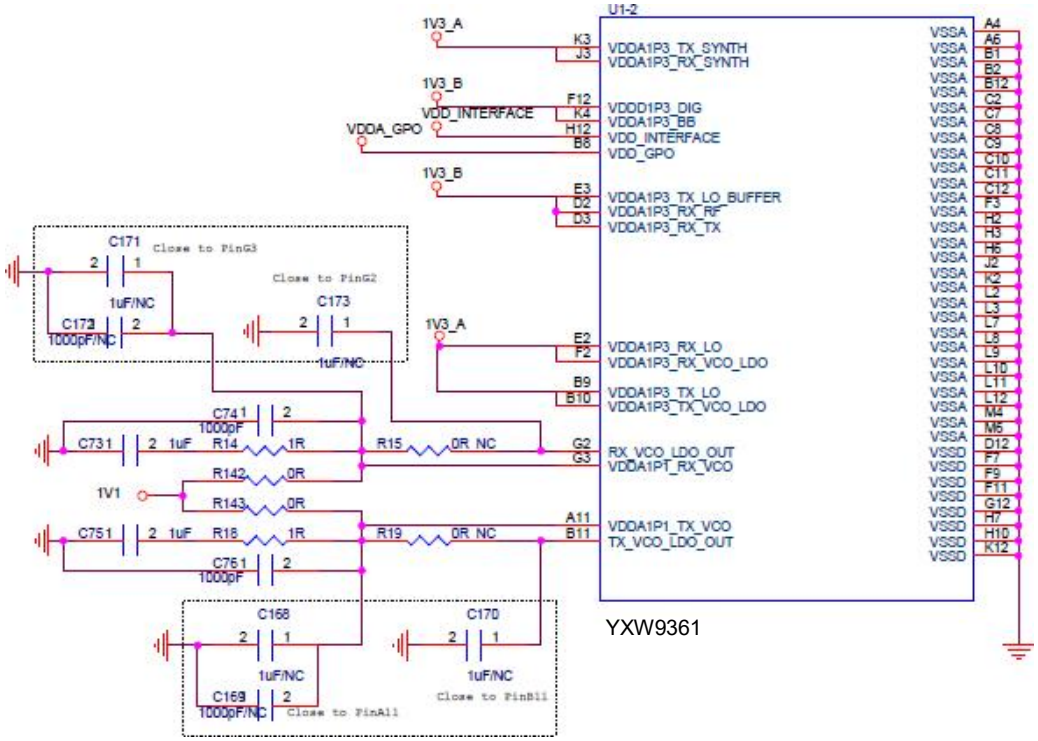
The topology diagram of the overall schematic design can completely refer to the AD9361 original chip design.



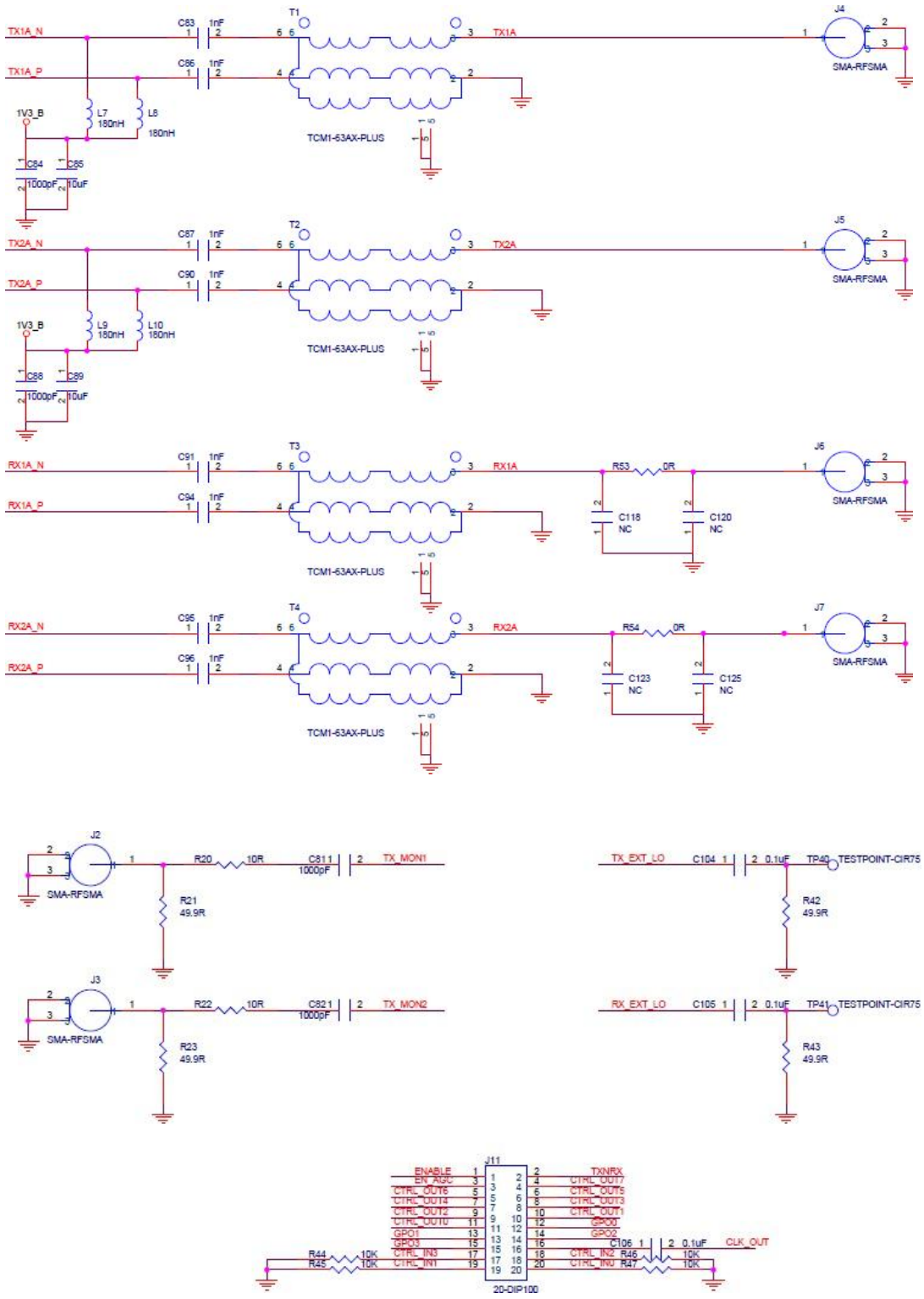
Main chip and power supply reference circuit diagram

The recommended circuit is as follows, and you can completely refer to the YXW9361 original chip design.

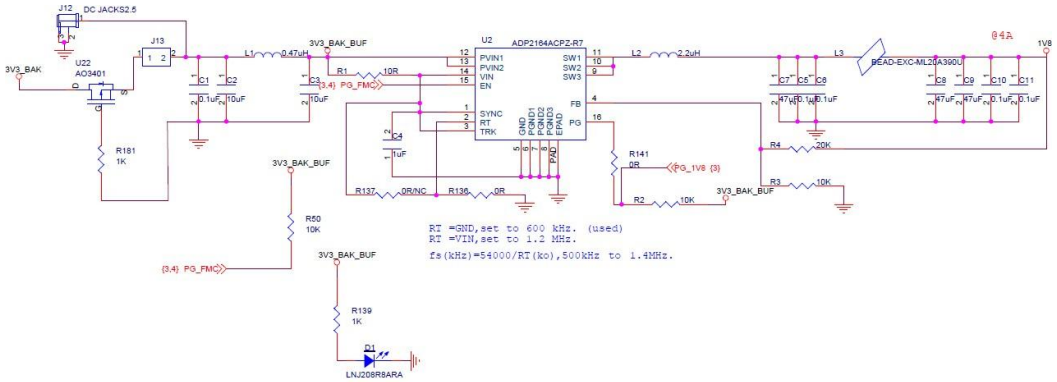




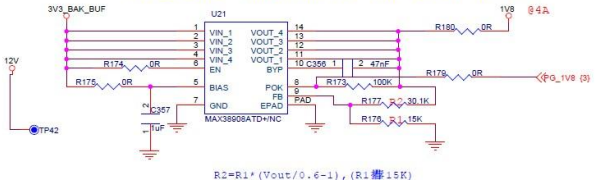
Antenna and test interface reference circuit diagram



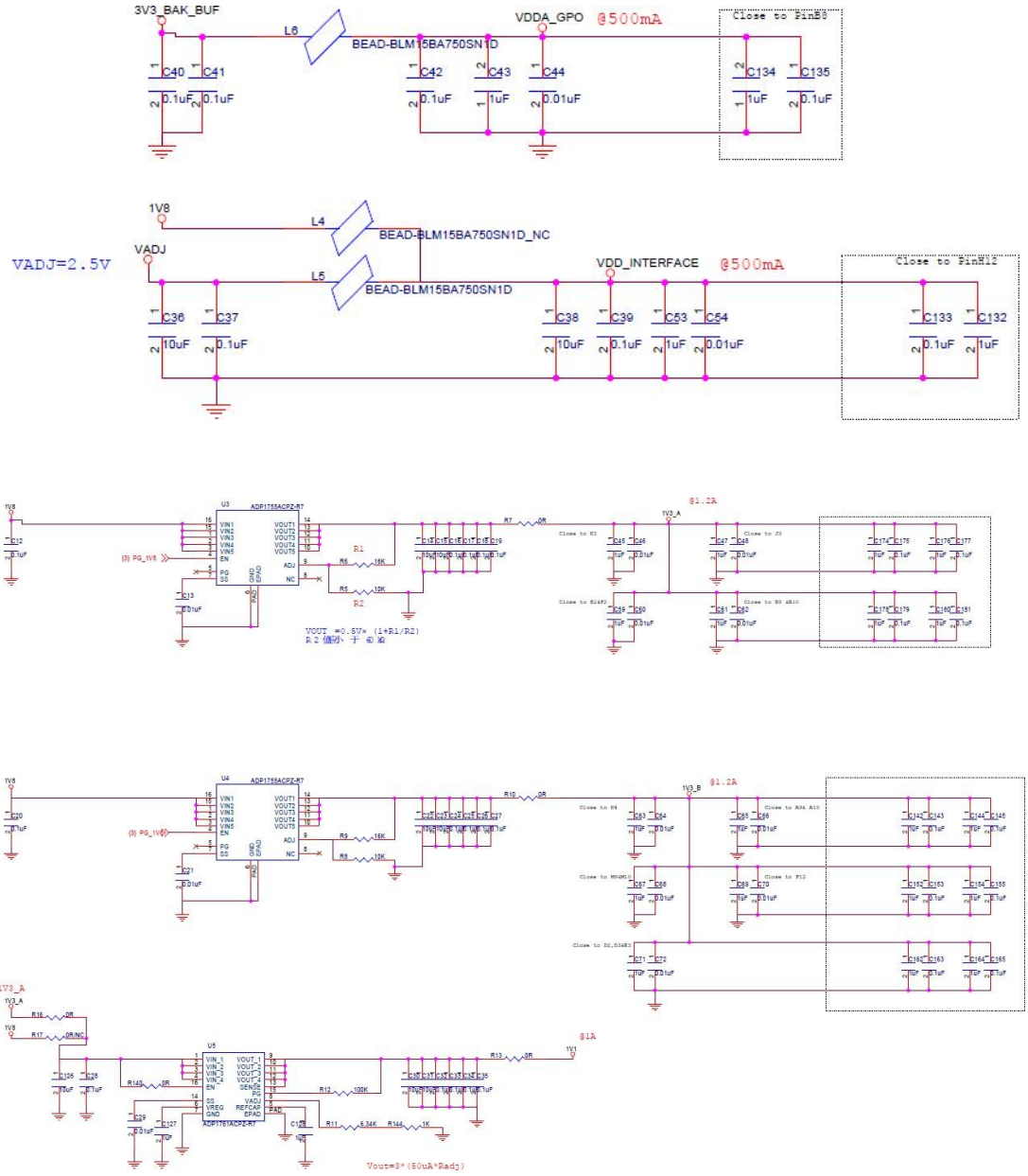
Power chip reference circuit powered by chip power supply: ADP2164ACPZ-R7 and MAX38908ATD+ are in a choice



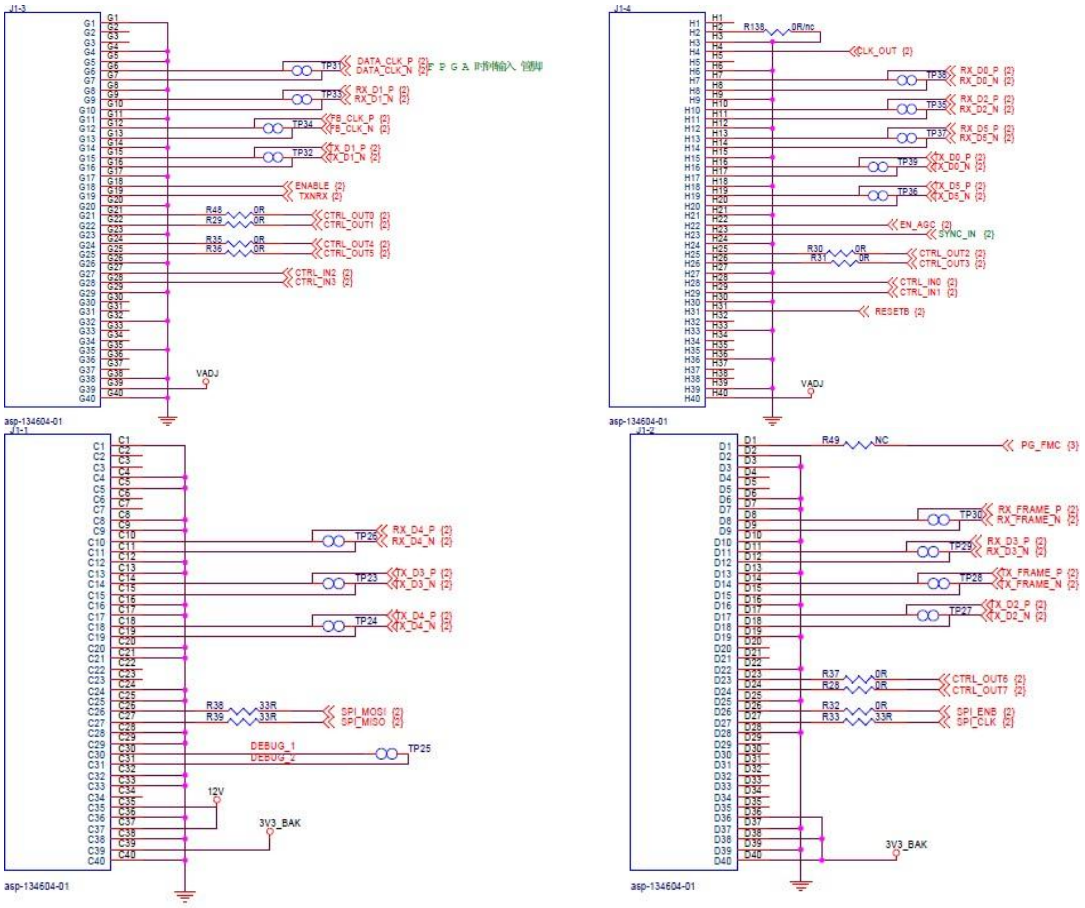
MAX38908ATD+(LDO)稳定测试
对替ADP2164ACPZ-R7(DC/DC)
(MAX38908ATD+(LDO)避免超过 1W，
将导致转换 温升超40 度不宜 长时工作)



R2=R1*(Vout/0.6-1),(R1推荐15K)


3V3_BAK_BUF
L6
BEAD-BLM15BA750SN1D
VDDA_GPO @500mA
Close to PinB9
C40 C41 C42 C43 C44 C134 C135
0.1uF 0.1uF 0.1uF 1uF 0.01uF 1uF 0.1uF
1V8
L4
BEAD-BLM15BA750SN1D_NC
VADJ
VADJ=2.5V
L5
BEAD-BLM15BA750SN1D
VDD_INTERFACE @500mA
Close to PinH12
C36 C37 C38 C39 C53 C54 C133 C132
10uF 0.1uF 10uF 0.1uF 1uF 0.01uF 0.1uF 1uF
U3 ADP1755ACPZ-R7
U4 ADP1755ACPZ-R7
U5 ADP197SACPZ-R7
R1 16K
R2 10K
R5 10K
R7 0R
R8 10K
R9 16K
R10 0R
R11 5.34K
R12 100K
R13 0R
R144 1K
R148 0R
R16 0R
R17 0R/NC
@1.2A
@1A
1V3_A
1V3_B
1V1
Vout=3*(50uA*Radj)

FMC Interface Signals:



FMC CONNECTOR (LPC)