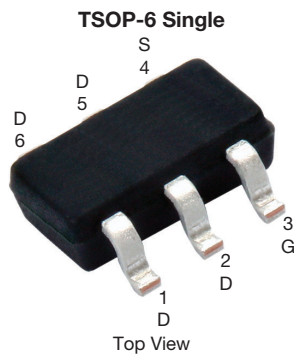


P-Channel 2.5 V (G-S) MOSFET

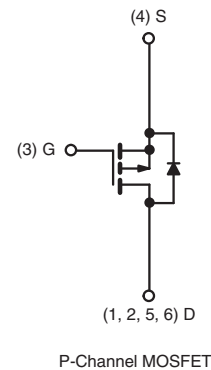


FEATURES

- TrenchFET® power MOSFET
- 100 % R_g tested
- Material categorization:
for definitions of compliance please see
www.vishay.com/doc?99912



RoHS
COMPLIANT
HALOGEN
FREE
Available



Marking Code: 3B

PRODUCT SUMMARY	
V_{DS} (V)	-20
$R_{DS(on)}$ max. (Ω) at $V_{GS} = -4.5$ V	0.060
$R_{DS(on)}$ max. (Ω) at $V_{GS} = -2.7$ V	0.090
$R_{DS(on)}$ max. (Ω) at $V_{GS} = -2.5$ V	0.100
Q_g typ. (nC)	6
I_D (A) ^a	-4.7
Configuration	Single

ORDERING INFORMATION	
Package	TSOP-6
Lead (Pb)-free	Si3443BDV-T1-E3
Lead (Pb)-free and halogen-free	Si3443BDV-T1-GE3

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$, unless otherwise noted)				
PARAMETER		SYMBOL	LIMIT	UNIT
Drain-source voltage		V_{DS}	-20	V
Gate-source voltage		V_{GS}	± 12	
Continuous drain current ($T_J = 150^\circ\text{C}$) ^a	$T_A = 25^\circ\text{C}$	I_D	-3.6	A
	$T_A = 70^\circ\text{C}$		-2.8	
Pulsed drain current		I_{DM}	-20	
Continuous source current (diode conduction) ^a		I_S	-0.9	
Maximum power dissipation ^a	$T_A = 25^\circ\text{C}$	P_D	1.1	W
	$T_A = 70^\circ\text{C}$		0.7	
Operating junction and storage temperature range		T_J, T_{stg}	-55 to +150	$^\circ\text{C}$

THERMAL RESISTANCE RATINGS					
PARAMETER		SYMBOL	TYPICAL	MAXIMUM	UNIT
Maximum junction-to-ambient ^a	$t \leq 5$ s	R_{thJA}	50	62.5	$^\circ\text{C/W}$
	Steady state		90	110	
Maximum junction-to-foot (drain)	Steady state	R_{thJF}	30	36	

Note

a. Surface mounted on FR4 board, $t \leq 5$ s



SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static						
Gate threshold voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = -250 μA	-0.6	-	-1.4	V
Gate-body leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 12 V	-	-	± 100	nA
Zero gate voltage drain current	I _{DSS}	V _{DS} = -20 V, V _{GS} = 0 V	-	-	-1	μA
		V _{DS} = -20 V, V _{GS} = 0 V, T _J = 70 °C	-	-	-5	
On-state drain current ^a	I _{D(on)}	V _{DS} = -5 V, V _{GS} = -4.5 V	-15	-	-	A
Drain-source on-state resistance ^a	R _{DS(on)}	V _{GS} = -4.5 V, I _D = -4.7 A	-	0.048	0.060	Ω
		V _{GS} = -2.7 V, I _D = -3.8 A	-	0.070	0.090	
		V _{GS} = -2.5 V, I _D = -1 A	-	0.080	0.100	
Forward transconductance ^a	g _{fs}	V _{DS} = -10 V, I _D = -4.7 A	-	11	-	S
Diode forward voltage ^a	V _{SD}	I _S = -1.7 A, V _{GS} = 0 V	-	-0.8	-1.2	V
Dynamic ^b						
Total gate charge	Q _g	V _{DS} = - 10 V, V _{GS} = - 4.5 V, I _D = - 4.7 A	-	6	9	nC
Gate-source charge	Q _{gs}		-	1.4	-	
Gate-drain charge	Q _{gd}		-	1.9	-	
Gate resistance	R _g	f = 1 MHz	5	9.5	16.2	Ω
Turn-on delay time	t _{d(on)}	V _{DD} = - 10 V, R _L = 10 Ω I _D ≡ - 1.0 A, V _{GEN} = - 4.5 V, R _g = 6 Ω	-	22	35	ns
Rise time	t _r		-	35	55	
Turn-off delay time	t _{d(off)}		-	45	70	
Fall time	t _f		-	25	40	
Source-drain reverse recovery time	t _{rr}	I _F = - 1.7 A, dI/dt = 100 A/μs	-	25	50	

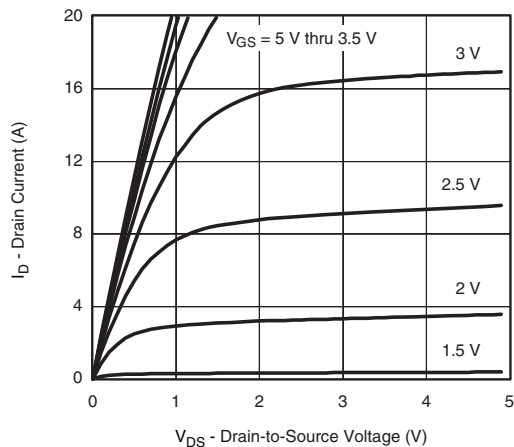
Notes

- a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2 %
b. Guaranteed by design, not subject to production testing

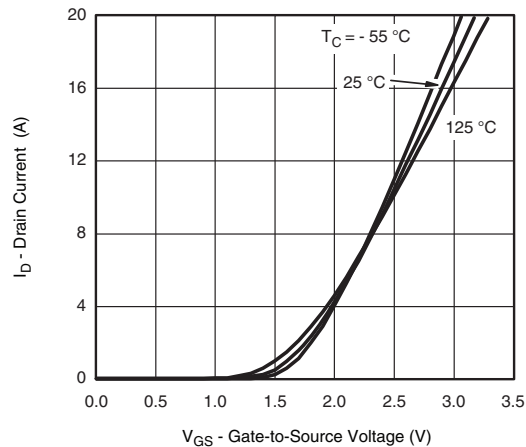
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



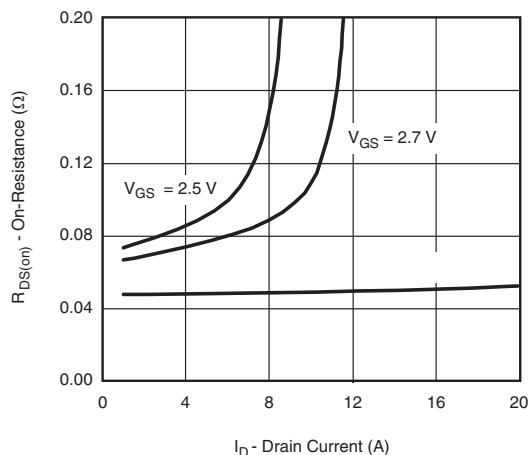
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



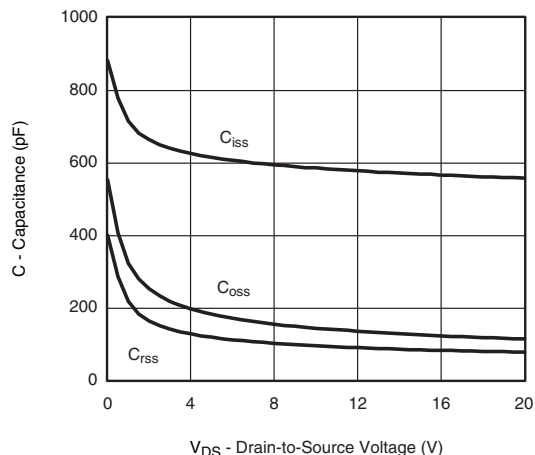
Output Characteristics



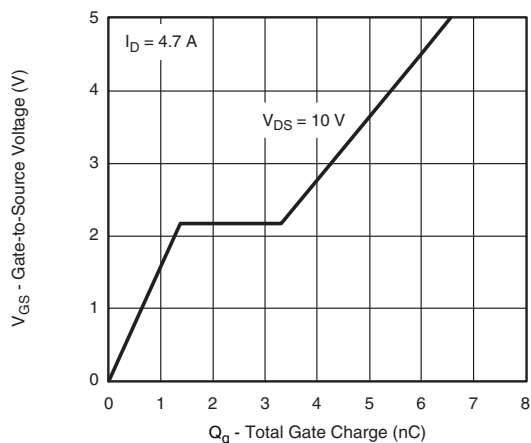
Transfer Characteristics



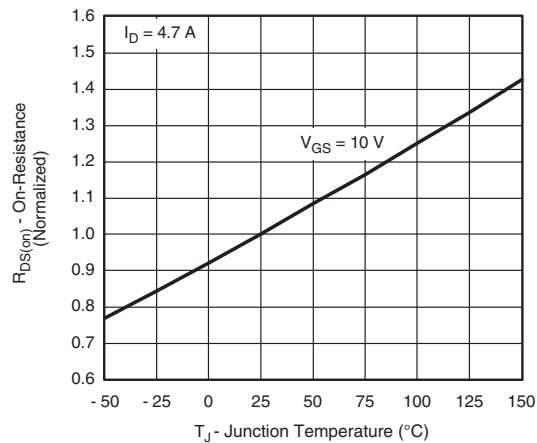
On-Resistance vs. Drain Current



Capacitance



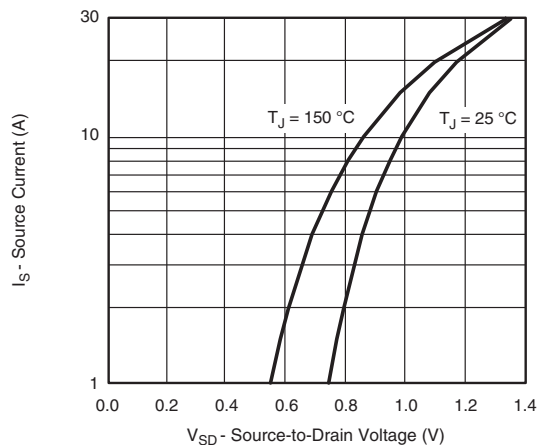
Gate Charge



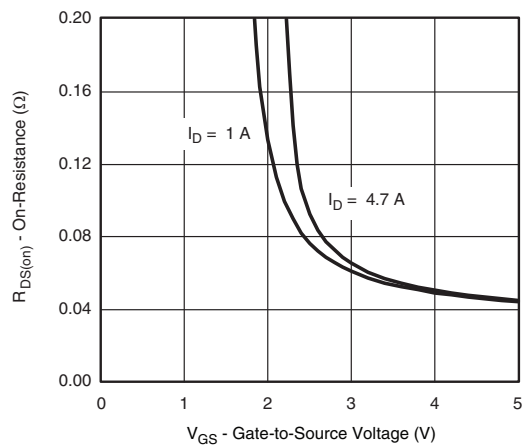
On-Resistance vs. Junction Temperature



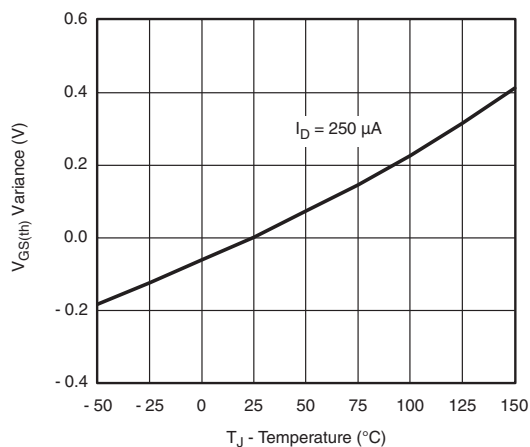
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



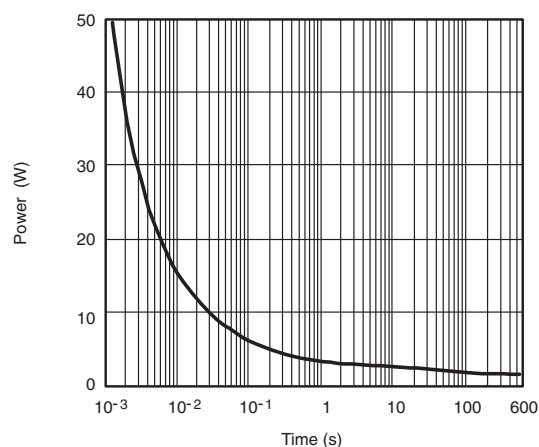
Source-Drain Diode Forward Voltage



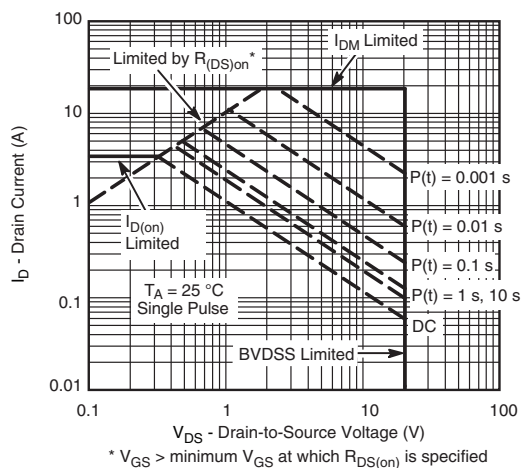
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



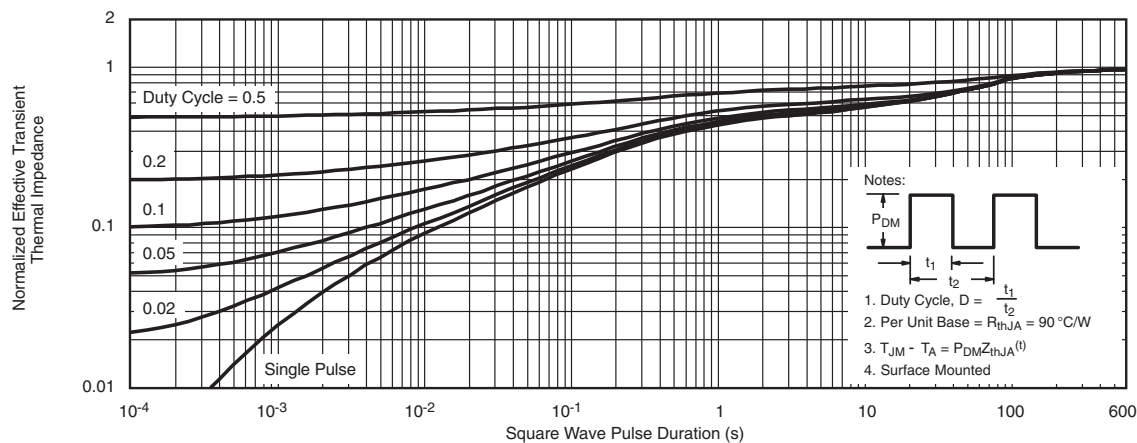
Single Pulse Power



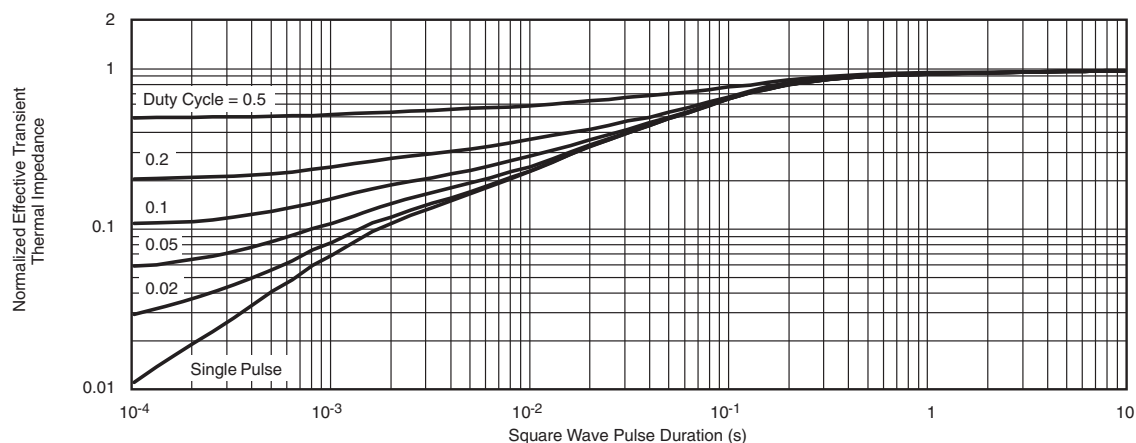
Safe Operating Area



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Ambient



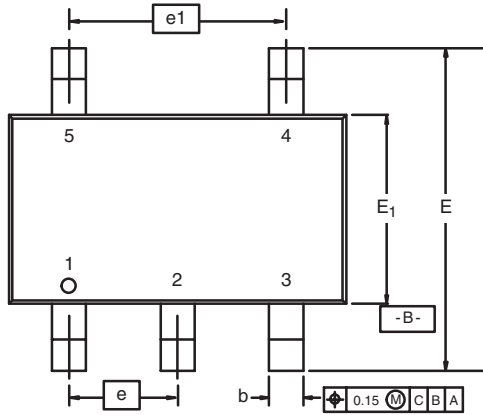
Normalized Thermal Transient Impedance, Junction-to-Foot

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package / tape drawings, part marking, and reliability data, see www.vishay.com/ppg?72749.

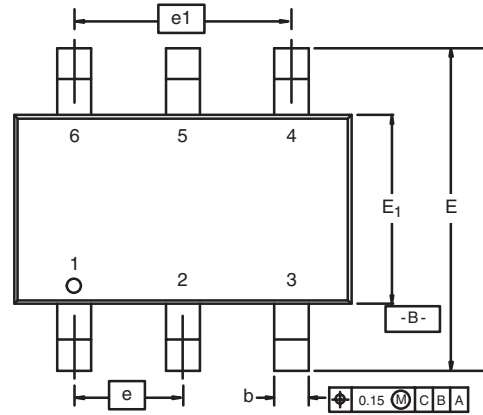


TSOP: 5/6-LEAD

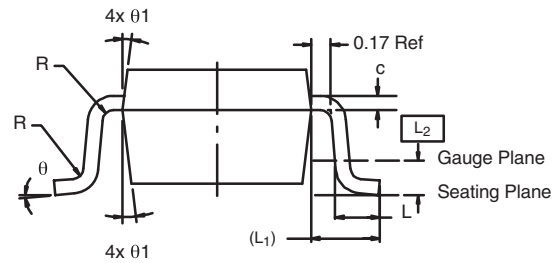
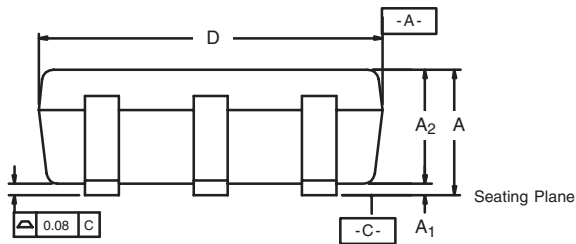
JEDEC Part Number: MO-193C



5-LEAD TSOP

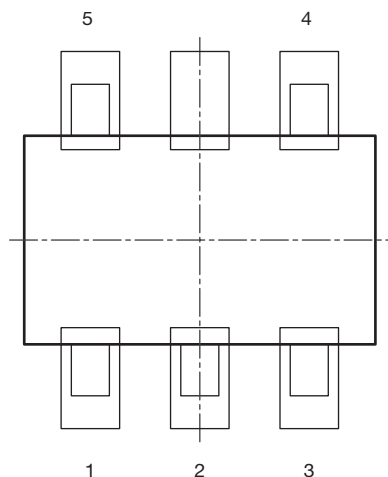


6-LEAD TSOP

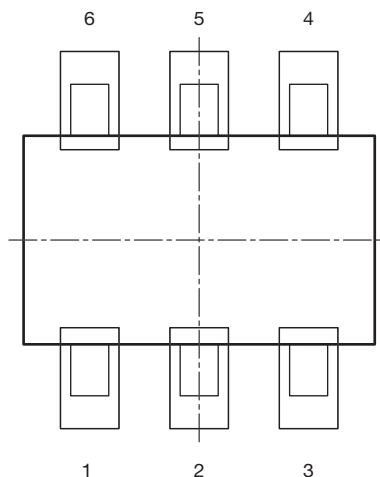


	MILLIMETERS			INCHES		
Dim	Min	Nom	Max	Min	Nom	Max
A	0.91	-	1.10	0.036	-	0.043
A ₁	0.01	-	0.10	0.0004	-	0.004
A ₂	0.90	-	1.00	0.035	0.038	0.039
b	0.30	0.32	0.45	0.012	0.013	0.018
c	0.10	0.15	0.20	0.004	0.006	0.008
D	2.95	3.05	3.10	0.116	0.120	0.122
E	2.70	2.85	2.98	0.106	0.112	0.117
E ₁	1.55	1.65	1.70	0.061	0.065	0.067
e	0.95 BSC			0.0374 BSC		
e ₁	1.80	1.90	2.00	0.071	0.075	0.079
L	0.32	-	0.50	0.012	-	0.020
L ₁	0.60 Ref			0.024 Ref		
L ₂	0.25 BSC			0.010 BSC		
R	0.10	-	-	0.004	-	-
θ	0°	4°	8°	0°	4°	8°
θ ₁	7° Nom			7° Nom		
ECN: C-06593-Rev. I, 18-Dec-06						
DWG: 5540						

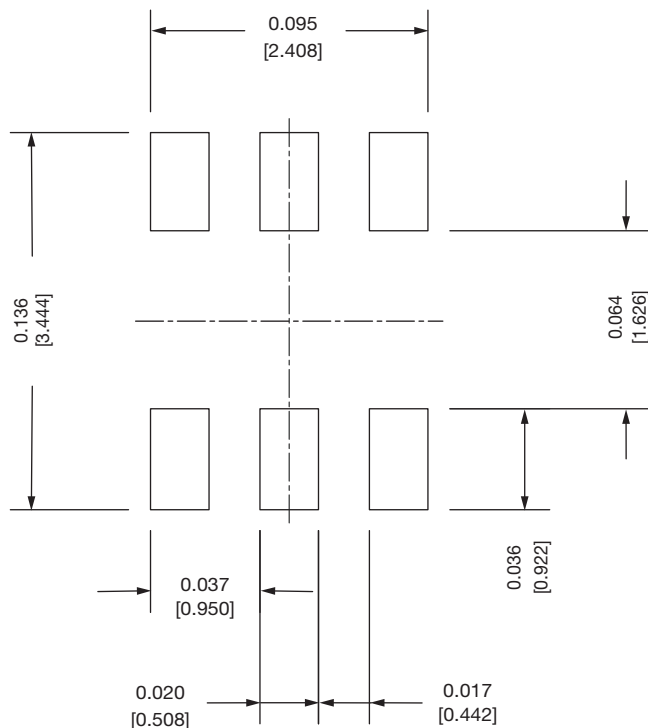
Recommended Land Pattern For TSOP-5L / TSOP-6L



TSOP 5L



TSOP 6L


Note

- All dimensions are in inches (millimeter)

ECN: C22-0860-Rev. B, 24-Oct-2022
DWG: 3010



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