

7th Generation Intel® Processor Families for U/Y Platforms and 8th Generation Intel® Processor Family for U Quad-Core and Y Dual Core Platforms

Datasheet, Volume 1 of 2

Supporting 7th Generation Intel® Core™ Processor Families, Intel® Pentium® Processors, Intel® Celeron® Processors for U/Y Platforms and8th Generation Intel® Processor Family for U Quad Core formerly known as Kaby Lake Refresh and 8th Generation Intel® Processor Family for Y Dual Core formerly known as Amber Lake 2-Core

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Revision History

Revision Number	Description	Revision Date
001	• Initial release	August 2016
002	• Minor updates throughout for clarity • Added support for the following processors — 7th Generation Intel® Core™ processors i7-7600U, i5-7300U, i7-7Y75, i5 -7Y57, i7-7660U, i7-7567U, i7-7560U, i5-7360U, i5-7287U, i5-7267U, i5-7260U, i3-7167U — Intel® Celeron® processors 3965U, 3865U — Intel® Pentium® processors 4415U, 4410Y • Supporting new processor SKUs, added support for on-package cache, GT3 • Updated table 2-24, “HDCP Display supported Implications” maximum resolutions for HDMI2.0 changed from 4K@30 to 4K@60. • Updated Section 5.1, “Processor Thermal Management”. • Updated Section 5.1.1-”Thermal Considerations”. • Updated Section 5.1.5.1.1, “TCC Activation Offset”. • Updated table 5-2, “TDP Specifications (U/Y-Processor Line)”. • Updated table 5-3, “Package Turbo Specifications (U/Y-Processor Line)” + Added note. • Updated Table 7-2, “Processor IA core (Vcc) Active and Idle Mode DC Voltage and Current Specifications”. • Updated Table 7-3, “Processor Graphics (VccGT and VccGTX) Supply DC Voltage and Current Specifications”. • Updated table 7-5, “System Agent (VccSA) Supply DC Voltage and Current Specifications”.	January 2017
003	• Added support for 8th Generation Intel® Processor Family for U Quad Core Platforms • Updated Table 2-18, “Display Resolutions and Link Bandwidth for Multi-Stream Transport Calculations”. • Updated TOB parameter in Chapter 7. • Updated Table 7-2, “Processor IA core (Vcc) Active and Idle Mode DC Voltage and Current Specifications”, Note 14. • Updated Table 7-3, “Processor Graphics (VccGT and VccGTX) Supply DC Voltage and Current Specifications”, Note 10. • Updated Table 7-5, “System Agent (VccSA) Supply DC Voltage and Current Specifications“. Added Note 8.	August 2017
004	• Added Section 1.6,”Operating Systems Support”	September 2018
005	• Updated document title	December 2018
006	• Updated Section 1.6,”Operating Systems Support”	January 2019
007	• Updated Section 7.1.2,”V_{CC} Voltage Identification (VID)”	August 2020
008	• Added note in Section 1.6,”Operating Systems Support”	February 2022

1 Introduction

Processor Volatility statement:

Intel® Kaby Lake processor families does not retain any end user data when powered down and/or when the processor is physically removed.

Note: *Power down refers to state which all processor power rails are off.*

The 7th Generation Intel® Core™ processor, Intel® Pentium® processor, Intel® Celeron® processor families and 8th Generation Intel® Processor Family for U 4-Core and Y-2 Core family are 64-bit, multi-core processors built on 14-nanometer process technology.

The U-Processor Line and Y-Processor Line are offered in a 1-Chip Platform that includes the 7th Generation Intel® processor families I/O Platform Controller Hub (PCH) die on the same package as the processor die. See the following figure.

Some of the processor SKUs are offered with On-Package Cache.

The following table describes the processor lines covered in this document.

Table 1-1. Processor Lines

Processor Line[1]	Package	Base TDP	Processor IA Cores	Graphics Configuration	On-Package Cache	Platform Type
KBL Y-Processor Line	BGA1515	4.5W	2	GT2	N/A	1-Chip
KBL Y-Processor Line With Integrated HDCP2.2	BGA1515	4.5W	2	GT2	N/A	1-Chip
KBL Y-Pentium/Celeron Processor Line	BGA1515	6W	2	GT2	N/A	1-Chip
AML-Y Processor Line (2-Cores)	BGA1515	5W	2	GT2	N/A	1-Chip
KBL U-Processor Line	BGA1356	15W	2	GT2	N/A	1-Chip
KBL U-Processor Line With Integrated HDCP2.2	BGA1356	15W	2	GT2	N/A	1-Chip
		15W, 28W	2	GT3	64 MB	1-Chip
KBL U-Pentium/Celeron Processor Line	BGA1356	15W	2	GT1	N/A	1-Chip

Throughout this document, the 7th Generation Intel® Core™ processor, Intel® Pentium® processor, Intel® Celeron® processor, and 8th Generation Intel® Processor Family for U 4-Core family (known as KBL-U Refresh) and Y 2-Core (named Amber Lake)may be referred to simply as “processor”. The 7th Generation Intel® processor families I/O and 8th Generation Intel® Processor Family for U 4-Core and Y 2-Core family I/O Platform Controller Hub (PCH) may be referred to simply as “PCH”.

This document is for the following U/Y-Processor SKUs:

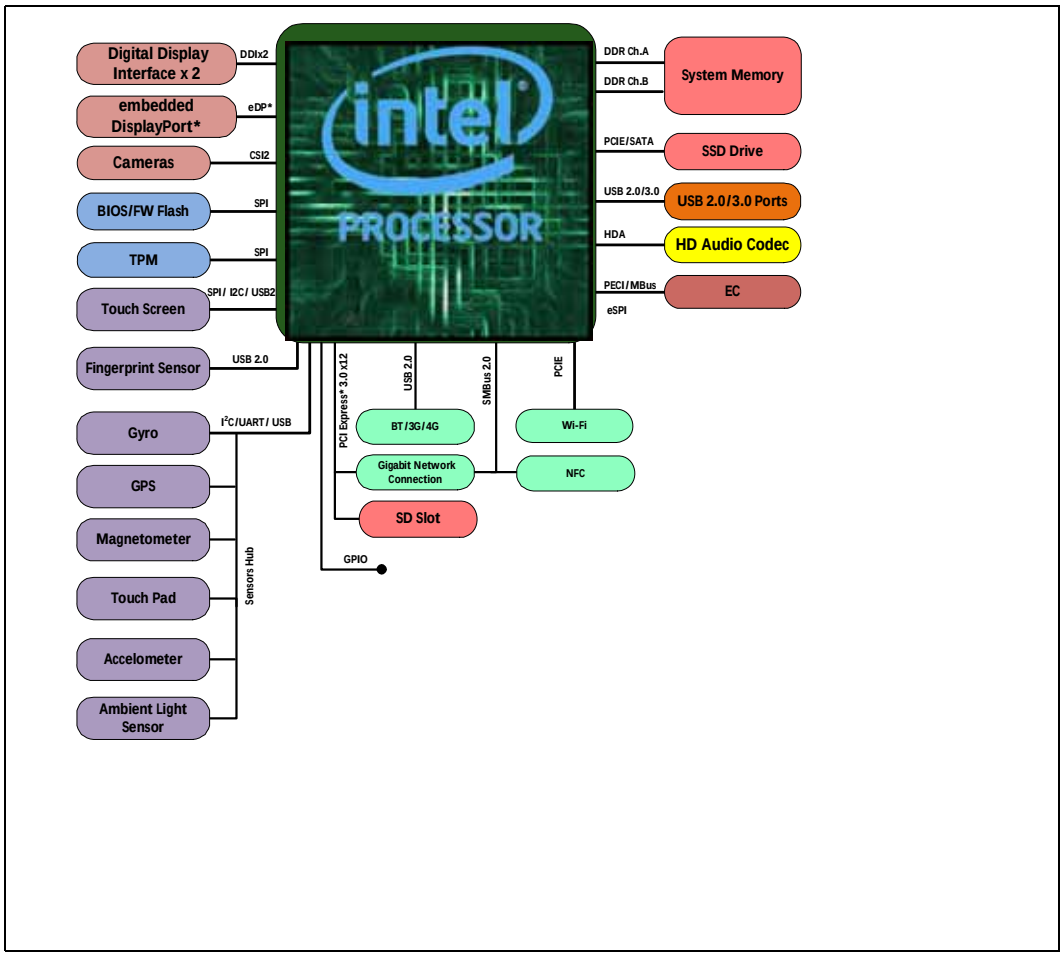
- 7th Generation Intel® Core™ processor family U-Processors

— i7-7500U, i5-7200U, i3-7100U, i7-7600U, i5-7300U, i7-7660U, i7-7567U, i7-7560U, i5-7360U, i5-7287U, i5-7267U, i5-7260U, i3-7167U

- 7th Generation Intel® Core™ processor family Y-Processors
  — i7-7Y75, i5-7Y54, m3-7Y30, i7-7Y75 with vPro™ support, i5-7Y57
- Intel® Pentium® processors
  — 4415U, 4410Y
- Intel® Celeron® processors
  — 3965U, 3865U
- 8th Generation Intel® Processor Family for U Quad Core family
  — i7-8550U, i5-8250U

Refer to the processor Specification Update for additional SKU details.

Figure 1-1. KBL Y/U/U 4-Core and AML-Y22 Processor Line Platforms



1.1 Supported Technologies

- Intel® Virtualization Technology (Intel® VT)
- Intel® Active Management Technology 11.0 (Intel® AMT 11.0)
- Intel® Trusted Execution Technology (Intel® TXT)
- Intel® Streaming SIMD Extensions 4.2 (Intel® SSE4.2)
- Intel® Hyper-Threading Technology (Intel® HT Technology)
- Intel® 64 Architecture
- Execute Disable Bit
- Intel® Turbo Boost Technology 2.0
- Intel® Advanced Vector Extensions 2 (Intel® AVX2)
- Intel® Advanced Encryption Standard New Instructions (Intel® AES-NI)
- PCLMULQDQ (Perform Carry-Less Multiplication Quad word) Instruction
- Intel® Secure Key
- Intel® Transactional Synchronization Extensions (Intel® TSX-NI)
- PAIR – Power Aware Interrupt Routing
- SMEP – Supervisor Mode Execution Protection
- Intel® Boot Guard
- On-package Cache Memory
- Intel® Software Guard Extensions (Intel® SGX)
- Intel® Memory Protection Extensions (Intel® MPX)
- GMM Scoring Accelerator
- Intel® Image Signal Processor (Intel® ISP)
- Intel® Processor Trace
- High-bandwidth Digital Content Protection (HDCP)

Note: The availability of the features may vary between processor SKUs.

Refer to Chapter 3, “Technologies” for more information.

1.2 Power Management Support

1.2.1 Processor Core Power Management

- Full support of ACPI C-states as implemented by the following processor C-states:
  - C0, C1, C1E, C3, C6, C7, C8, C9, C10
- Enhanced Intel SpeedStep® Technology

Refer to Section 4.2, “Processor IA Core Power Management” for more information.

1.2.2 System Power Management

- S0/S0ix, S3, S4, S5

Refer to Chapter 4, “Power Management” for more information.

1.2.3 Memory Controller Power Management

- Disabling Unused System Memory Outputs
- DRAM Power Management and Initialization
- Initialization Role of CKE
- Conditional Self-Refresh
- Dynamic Power Down
- DRAM I/O Power Management
- DDR Electrical Power Gating (EPG)
- Power training

Refer to Section 4.3, “Integrated Memory Controller (IMC) Power Management” for more information.

1.2.4 Processor Graphics Power Management

1.2.4.1 Memory Power Savings Technologies

- Intel Rapid Memory Power Management (Intel RMPM)
- Intel Smart 2D Display Technology (Intel S2DDT)

1.2.4.2 Display Power Savings Technologies

- Intel (Seamless & Static) Display Refresh Rate Switching (DRRS) with eDP port
- Intel Automatic Display Brightness
- Smooth Brightness
- Intel Display Power Saving Technology (Intel DPST 6)
- Panel Self-Refresh 2 (PSR 2)
- Low Power Single Pipe (LPSP)

1.2.4.3 Graphics Core Power Savings Technologies

- Intel Graphics Dynamic Frequency
- Intel Graphics Render Standby Technology (Intel GRST)
- Dynamic FPS (Intel DFPS)

Refer to Section 4.4, “Processor Graphics Power Management” for more information.

1.3 Thermal Management Support

- Digital Thermal Sensor
- Intel Adaptive Thermal Monitor
- THERMTRIP# and PROCHOT# support
- On-Demand Mode
- Memory Open and Closed Loop Throttling
- Memory Thermal Throttling
- External Thermal Sensor (TS-on-DIMM and TS-on-Board)
- Render Thermal Throttling
- Fan speed control with DTS
- Intel Turbo Boost Technology 2.0 Power Control

Refer to Chapter 5, “Thermal Management” for more information.

1.4 Package Support

The processor is available in the following packages:

- A 20.5 mm x 16.5 mm BGA package (BGA1515) for Y/ AML- Y22 Processor Line
- A 42 mm x 24 mm BGA package (BGA1356) for U/U-4 Core Processor Line

1.5 Processor Testability

An XDP on-board connector is warmly recommended to enable full debug capabilities. For the processor SKUs, a merged XDP connector is highly recommended to enable lower C-state debug.

Note: When separate XDP connectors will be used at C8–C10 states, the processor will need to be waked up using the PCH.

The processor includes boundary-scan for board and system level testability.

1.6 Operating Systems Support

(7th Gen)				
Processor Line	**Windows* 10 64-bit**	**OS X**	**Linux* OS**	**Chrome* OS**
U-processor line	Yes	Yes	Yes	Yes
Y-processor line	Yes	Yes	Yes	Yes

(8th Gen)				
Processor Line	**Windows* 10 64-bit**	**OS X**	**Linux* OS**	**Chrome* OS**
U-processor line	Yes	Yes	Yes	Yes
Y-processor line	Yes	Yes	Yes	Yes

Note: Refer to OS Vendor site for more information regarding latest OS revision support.

1.7 Terminology

Table 1-2. Terminology

Term	Description
4K	Ultra High Definition (UHD)
AES	Advanced Encryption Standard
AGC	Adaptive Gain Control
BLT	Block Level Transfer
BPP	Bits per pixel
CDR	Clock and Data Recovery
CTLE	Continuous Time Linear Equalizer
DDI	Digital Display Interface for DP or HDMI/DVI
DDR3	Third-generation Double Data Rate SDRAM memory technology
DDR3L/RS	DDR3 Low Voltage Reduced Standby Power
DDR4/DDR4-RS	Fourth-Generation Double Data Rate SDRAM Memory Technology RS - Reduced Standby Power
DFE	decision feedback equalizer
DMA	Direct Memory Access
DMI	Direct Media Interface
DP	DisplayPort*
DTS	Digital Thermal Sensor
eDP*	embedded DisplayPort*
EU	Execution Unit in the Processor Graphics
GSA	Graphics in System Agent
HDCP	High-bandwidth Digital Content Protection
HDMI*	High Definition Multimedia Interface
IMC	Integrated Memory Controller
Intel® 64 Technology	64-bit memory extensions to the IA-32 architecture
Intel® DPST	Intel Display Power Saving Technology
Intel® PTT	Intel Platform Trust Technology
Intel® TSX-NI	Intel Transactional Synchronization Extensions
Intel® TXT	Intel Trusted Execution Technology
Intel® VT	Intel Virtualization Technology. Processor virtualization, when used in conjunction with Virtual Machine Monitor software, enables multiple, robust independent software environments inside a single platform.
Intel® VT-d	Intel Virtualization Technology (Intel VT) for Directed I/O. Intel VT-d is a hardware assist, under system software (Virtual Machine Manager or OS) control, for enabling I/O device virtualization. Intel VT-d also brings robust security by providing protection from errant DMAs by using DMA remapping, a key feature of Intel VT-d.
IOV	I/O Virtualization
ISP	Image Signal Processor
LFM	Low Frequency Mode. corresponding to the Enhanced Intel SpeedStep® Technology's lowest voltage/frequency pair. It can be read at MSR CEh [47:40].
LLC	Last Level Cache
LPDDR3	Low Power Third-generation Double Data Rate SDRAM memory technology

Term	Description
LPM	Low-Power Mode.The LPM Frequency is less than or equal to the LFM Frequency. The LPM TDP is lower than the LFM TDP as the LPM configuration limits the processor to single thread operation
LPSP	Low-Power Single Pipe
LSF	Lowest Supported Frequency.This frequency is the lowest frequency where manufacturing confirms logical functionality under the set of operating conditions.
MCP	Multi Chip Package - includes the processor and the PCH. In some SKUs it might have additional On-Package Cache.
MFM	Minimum Frequency Mode. MFM is the minimum ratio supported by the processor and can be read from MSR CEh [55:48].
MLC	Mid-Level Cache
NCTF	Non-Critical to Function. NCTF locations are typically redundant ground or non-critical reserved balls/lands, so the loss of the solder joint continuity at end of life conditions will not affect the overall product functionality.
OPC	On-Package Cache
PAG	Platform Power Architecture Guide (formerly PDDG)
PCH	Platform Controller Hub. The chipset with centralized platform capabilities including the main I/O interfaces along with display connectivity, audio features, power management, manageability, security, and storage features. The PCH may also be referred as “chipset”.
PECI	Platform Environment Control Interface
PEG	PCI Express Graphics
PL1, PL2, PL3	Power Limit 1, Power Limit 2, Power Limit 3
Processor	The 64-bit multi-core component (package)
Processor Core	The term “processor core” refers to Si die itself, which can contain multiple execution cores. Each execution core has an instruction cache, data cache, and 256-KB L2 cache. All execution cores share the LLC.
Processor Graphics	Intel Processor Graphics
PSR	Panel Self-Refresh
Rank	A unit of DRAM corresponding to four to eight devices in parallel, ignoring ECC. These devices are usually, but not always, mounted on a single side of a SODIMM.
SCI	System Control Interrupt. SCI is used in the ACPI protocol.
SDP	Scenario Design Power
SGX	Software Guard Extension
SHA	Secure Hash Algorithm
SSC	Spread Spectrum Clock
Storage Conditions	A non-operational state. The processor may be installed in a platform, in a tray, or loose. Processors may be sealed in packaging or exposed to free air. Under these conditions, processor landings should not be connected to any supply voltages, have any I/Os biased, or receive any clocks. Upon exposure to “free air” (that is, unsealed packaging or a device removed from packaging material), the processor should be handled in accordance with moisture sensitivity labeling (MSL) as indicated on the packaging material.
STR	Suspend to RAM
TAC	Thermal Averaging Constant
TCC	Thermal Control Circuit
TDP	Thermal Design Power
TOB	Tolerance Budget
TTV TDP	Thermal Test Vehicle TDP
V_{CC}	Processor core power supply

Term	Description
V_{CCGT}	Processor Graphics Power Supply
V_{CCIO}	I/O Power Supply
V_{CCSA}	System Agent Power Supply
V_{CCST}	Vcc Sustain Power Supply
V_{DDQ}	DDR Power Supply
VLD	Variable Length Decoding
VPID	Virtual Processor ID
V_{SS}	Processor Ground

1.8 Related Documents

Table 1-3. Related Documents

Document	Document Number / Location
7th Generation Intel® Processor Families for U/Y-Platforms Datasheet Volume 2 of 2	334662
7th Generation Intel® Processor Families Specification Update	334663
7th Generation Intel® Processor Families I/O Platform Datasheet Volume 1 of 2	334658
7th Generation Intel® Processor Families I/O Platform Datasheet Volume 2 of 2	334659
Advanced Configuration and Power Interface 3.0	http://www.acpi.info/
DDR3L SDRAM Specification	http://www.jedec.org
LPDDR3 Specification	http://www.jedec.org
DDR4 Specification	http://www.jedec.org
High Definition Multimedia Interface specification revision 1.4	http://www.hdmi.org/manufacturer/specification.aspx
Embedded DisplayPort* Specification revision 1.4	http://www.vesa.org/vesa.standards/
DisplayPort* Specification revision 1.2	http://www.vesa.org/vesa.standards/
PCI Express* Base Specification Revision 3.0	http://www.pcisig.com/specifications
Intel® 64 and IA-32 Architectures Software Developer's Manuals	http://www.intel.com/products/processor/manuals/index.htm

2 Interfaces

2.1 System Memory Interface

- Two channels of DDR3L/-RS, LPDDR3 and DDR4 memory with a maximum of two DIMMs per channel. DDR technologies, number of DIMMs per channel, number of ranks per channel are SKU dependent.
- UDIMM, SO-DIMM, and Memory Down support (based on SKU)
- Single-channel and dual-channel memory organization modes
- Data burst length of eight for all memory organization modes
- DDR3L/-RS I/O Voltage of 1.35V - based on Processor Line
- LPDDR3 I/O voltage of 1.2V
- DDR4 I/O Voltage of 1.2V
- 64-bit wide channels
- Non-ECC UDIMM and SODIMM DDR4/DDR3L/-RS support (based on SKU)
- Theoretical maximum memory bandwidth of:
  - — 20.8 GB/s in dual-channel mode assuming 1333 MT/s
  - — 25.0 GB/s in dual-channel mode assuming 1600 MT/s
  - — 29.1 GB/s in dual-channel mode assuming 1866 MT/s
  - — 33.3 GB/s in dual-channel mode assuming 2133 MT/s
  - — 37.5 GB/s in dual-channel mode assuming 2400 MT/s

Note: Memory down of all technologies (DDR3L/DDR4/LPDDR3) should be implemented homogeneously, which means that all DRAM devices should be from the same vendor and have the same part number. Implementing a mix of DRAM devices may cause serious signal integrity and functional issues.

2.1.1 System Memory Technology Supported

The Integrated Memory Controller (IMC) supports DDR3L/-RS, LPDDR3 andDDR4 protocols with two independent, 64-bit wide channels.

Table 2-1. Processor DRAM Support Matrix

Processor Line	DPC[1]	DDR3L/-RS [MT/s]	DDR4 [MT/s]	LPDDR3 [MT/s]
U-Processor Line	1	1333/1600	1866/2133	1600/1866
Y/AML-Y22 Processor Line	1	N/A	N/A	1600/1866

Notes:
1. DPC = DIMM Per Channel
2. N/A
3. N/A

- DDR3L/-RS Data Transfer Rates:
  - 1333 MT/s (PC3-10600)
  - 1600 MT/s (PC3-12800)
- DDR4 Data Transfer Rates:
  - 1866 MT/s (PC4-1866)
  - 2133 MT/s (PC4-2133)
- LPDDR3 Data Transfer Rates:
  - 1600 MT/s
  - 1866 MT/s
- SODIMM Modules:

  DDR3L/-RS SODIMM/UDIMM Modules:

  - Standard 4-Gb technology and addressing are supported for x8 and x16 devices.

  DDR4 SODIMM/UDIMM Modules:

  - Standard 4-Gb and 8-Gb technologies and addressing are supported for x8 and x16 devices.

  There is no support for memory modules with different technologies or capacities on opposite sides of the same memory module. If one side of a memory module is populated, the other side is either identical or empty.
- DDR3L/-RS Memory Down: Single and dual rank x8, x16 (based on SKU)
- DDR4 Memory Down: Single rank x8, x16 (based on SKU)
- LPDDR3 Memory Down: Single and Dual Rank x32/x64 (based on SKU)

2.1.1.1 DDR3L/-RS Supported Memory Modules and Devices

Table 2-2. Supported DDR3L/-RS Non-ECC SO-DIMM Module Configurations (U-Processor Line)

Raw Card Version	DIMM Capacity	DRAM Device Technology	DRAM Organization	# of DRAM Devices	# of Ranks	# of Row/Col Address Bits	# of Banks Inside DRAM	Page Size
A	4GB	4Gb	256M x 16	8	2	15/10	8	8K
B	4GB	4Gb	512M x 8	8	1	16/10	8	8K
C	2GB	4Gb	256M x 16	4	1	15/10	8	8K
F	8GB	4Gb	512M x 8	16	2	16/10	8	8K

Table 2-3. Supported DDR3L/-RS Memory Down Module Configurations (U-Processor Line)

PKG Type (Dies bits x PKG bits)	Max System Capacity	DRAM Device Technology	DRAM Organization	Die Density	Dies Per Channel	PKGs per channel	# of DRAM Ranks	# of Banks Inside DRAM	Page Size
SDP 8x8	16GB	4Gb	512M x 8	4 Gb	16	16	1	16	8K
SDP 16x16	8GB	4Gb	256M x 16	4 Gb	8	8	1	16	8K
DDP 16x16	8GB	8Gb	256M x 16	4 Gb	8	4	2	16	8K
Note: Maximum system capacity is referred to 2 channels populated with 2 ranks per channel.									

2.1.1.2 DDR4 Supported Memory Modules and Devices

Table 2-4. Supported DDR4 Non-ECC SODIMM Module Configurations (U/U-4 Core Processor Line)

Raw Card Version	DIMM Capacity	DRAM Device Technology	DRAM Organization	# of DRAM Devices	# of Ranks	# of Row/Col Address Bits	# of Banks Inside DRAM	Page Size
A	4GB	4Gb	512M x 8	8	1	15/10	16	8K
A	8GB	8Gb	1024M x 8	8	1	16/10	16	8K
B	8GB	4Gb	512M x 8	16	2	15/10	16	8K
B	16GB	8Gb	1024M x 8	16	2	16/10	16	8K
C	2GB	4Gb	256M x 16	4	1	15/10	8	8K
C	4GB	8Gb	512M x 16	4	1	16/10	8	8K
E	8GB	4Gb	512M x 8	16	2	15/10	16	8K
E	16GB	8Gb	1024M x 8	16	2	16/10	16	8K

Table 2-5. Supported DDR4 Memory Down Device Configurations (U/U-4 Core Processor Line)

Max System Capacity	PKG Type (Die bits x PKG bits)	DRAM Organization / PKG Type	PKG Density	Die Density	Die Per Channel	Rank Per Channel	PKGs Per channel	Physical Device Rank	Banks Inside DRAM	Page Size
16GB	SDP 8x8	512M x 8	4Gb	4Gb	16	2	16	1	16	8K
32GB	SDP 8x8	1024M x 8	8Gb	8Gb	16	2	16	1	16	8K
4GB	SDP 16x16	256M x 16	4Gb	4Gb	4	1	4	1	8	8K
8GB	SDP 16x16	512M x 16	8Gb	8Gb	4	1	4	1	8	8K
16GB	DDP 8x16	1024M x 16	16Gb	8Gb	8	1	4	1	16	8K

Notes:
1. The maximum system capacity for x8 devices refers to 2 channels, 2 ranks systems
2. The maximum system capacity for x16 devices refers to 2 channels, 1 rank systems

2.1.1.3 LPDDR3 Supported Memory Devices

Table 2-6. Supported LPDDR3 x32 DRAMs Configurations (KBL Y/H/U/U-4 Core and AML-Y22 Processor Lines) (Sheet 1 of 2)

Max System Capacity	PKG Type (Dies bits x PKG bits)	DRAM Organization / PKG Type	Die Density	PKG Density	Dies Per Channel	PKGs Per Channel	Physical Device Rank	Banks Inside DRAM	Page Size
2 GB	SDP 32x32	128Mx32	4 Gb	4Gb	2	2	1	8	8K
4 GB	DDP 32x32	256Mx32	4 Gb	8Gb	4	2	2	8	8K
8 GB	QDP 16x32	512Mx32	4 Gb	16Gb	8	2	2	8	8K
4 GB	SDP 32x32	256Mx32	8 Gb	8Gb	2	2	1	8	8K
8 GB	DDP 32x32	512Mx32	8 Gb	16Gb	4	2	2	8	8K
16 GB	QDP 16x32	1024Mx32	8 Gb	32Gb	8	2	2	8	8K

Table 2-6. Supported LPDDR3 x32 DRAMs Configurations (KBL Y/H/U/U-4 Core and AML-Y22 Processor Lines) (Sheet 2 of 2)

Max System Capacity	PKG Type (Dies bits x PKG bits)	DRAM Organization / PKG Type	Die Density	PKG Density	Dies Per Channel	PKGs Per Channel	Physical Device Rank	Banks Inside DRAM	Page Size
Notes: 1. x32 devices are 178 balls. 2. SDP = Single Die Package, DDP = Dual Die Package, QDP = 4 Die Package									

Table 2-7. Supported LPDDR3 x64 DRAMs Configurations (KBL Y/U and AML-Y22 Processor Lines)

Max System Capacity	PKG Type (Dies bits x PKG bits)	DRAM Organization / PKG Type	Die Density	PKG Density	Dies Per Channel	PKGs Per Channel	Physical Device Rank	Banks Inside DRAM	Page Size
2 GB	DDP 32x64	128Mx64	4 Gb	8 Gb	2	1	1	8	8K
4 GB	QDP 32x64	256Mx64	4 Gb	16 Gb	4	1	2	8	8K
4 GB	DDP 32x64	256Mx64	8 Gb	16 Gb	2	1	1	8	8K
8 GB	QDP 32x64	512Mx64	8 Gb	32 Gb	4	1	2	8	8K
Notes: 1. x64 devices are 253 balls. 2. SDP = Single Die Package, DDP = Dual Die Package, QDP = 4 Die Package									

2.1.2 System Memory Timing Support

The IMC supports the following DDR Speed Bin, CAS Write Latency (CWL), and command signal mode timings on the main memory interface:

- tCL = CAS Latency
- tRCD = Activate Command to READ or WRITE Command delay
- tRP = PRECHARGE Command Period
- CWL = CAS Write Latency
- Command Signal modes:
  - — 1N indicates a new DDR3L/DDR4 command may be issued every clock
  - — 2N indicates a new DDR3L/DDR4 command may be issued every 2 clocks

Table 2-8. DRAM System Memory Timing Support

DRAM Device	Transfer Rate (MT/s)	tCL (tCK)	tRCD (tCK)	tRP (tCK)	CWL (tCK)	DPC (SODIMM Only)	CMD Mode
DDR3L/-RS	1333	8/9	8/9	8/9	7	1 or 2	1N/2N
	1600	10/11	10/11	10/11	8	1 or 2	1N/2N
DDR4	1866	13/14	12/13/14	13/14	10/12/12	1 or 2	1N/2N
DDR4	2133	15/16	14/15/16	15/16	11/14/14	1 or 2	1N/2N

Table 2-9. DRAM System Memory Timing Support (LPDDR3)

DRAM Device	Transfer Rate (MT/s)	tCL (tCK)	tRCD (tCK)	tRPpb[1] (tCK)	tRPab[2] (tCK)	CWL (tCK)
LPDDR3	1600	12	15	15	18	9
LPDDR3	1866	14	17	17	20	11

Notes:
1. tRPpb = Row Precharge typical time (single bank)
2. tRPab = Row Precharge typical time (all banks)

2.1.3 System Memory Organization Modes

The IMC supports two memory organization modes, single-channel and dual-channel. Depending upon how the DDR Schema and DIMM Modules are populated in each memory channel, a number of different configurations can exist.

Single-Channel Mode

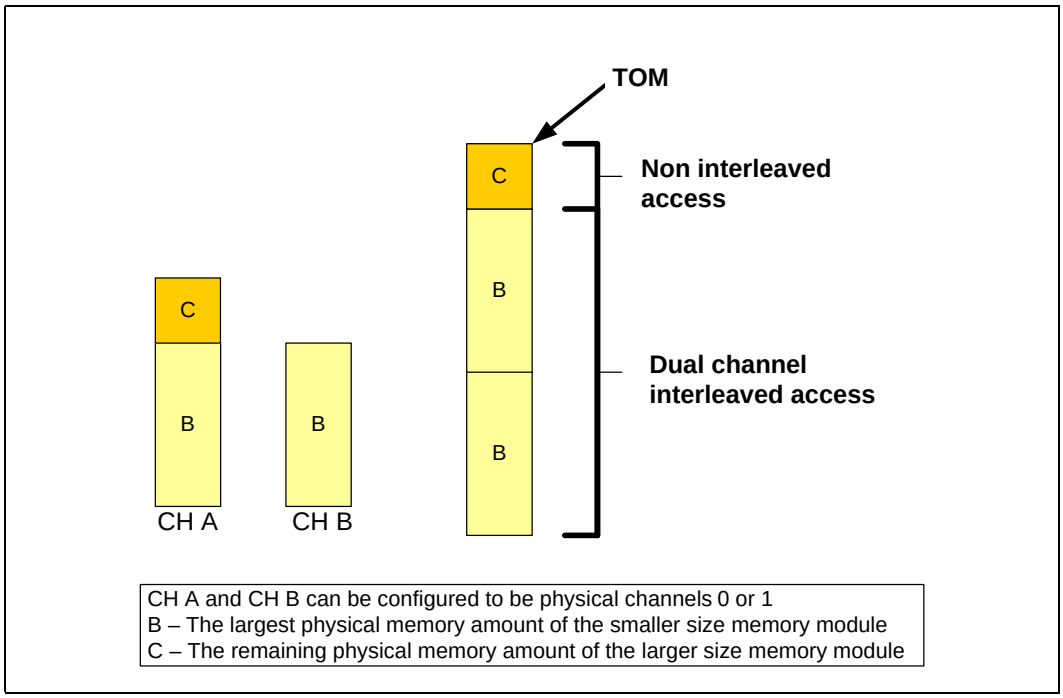
In this mode, all memory cycles are directed to a single channel. Single-Channel mode is used when either the Channel A or Channel B DIMM connectors are populated in any order, but not both.

Dual-Channel Mode – Intel® Flex Memory Technology Mode

The IMC supports Intel Flex Memory Technology Mode. Memory is divided into a symmetric and asymmetric zone. The symmetric zone starts at the lowest address in each channel and is contiguous until the asymmetric zone begins or until the top address of the channel with the smaller capacity is reached. In this mode, the system runs with one zone of dual-channel mode and one zone of single-channel mode, simultaneously, across the whole memory array.

Note: Channels A and B can be mapped for physical channel 0 and 1 respectively or vice versa. However, channel A size should be greater or equal to channel B size.

Figure 2-1. Intel® Flex Memory Technology Operations



Dual-Channel Symmetric Mode (Interleaved Mode)

Dual-Channel Symmetric mode, also known as interleaved mode, provides maximum performance on real world applications. Addresses are ping-ponged between the channels after each cache line (64-byte boundary). If there are two requests, and the second request is to an address on the opposite channel from the first, that request can be sent before data from the first request has returned. If two consecutive cache lines are requested, both may be retrieved simultaneously, since they are ensured to be on opposite channels. Use Dual-Channel Symmetric mode when both Channel A and Channel B DIMM connectors are populated in any order, with the total amount of memory in each channel being the same.

When both channels are populated with the same memory capacity and the boundary between the dual channel zone and the single channel zone is the top of memory, IMC operates completely in Dual-Channel Symmetric mode.

Note: The DRAM device technology and width may vary from one channel to the other.

2.1.4 System Memory Frequency

In all modes, the frequency of system memory is the lowest frequency of all memory modules placed in the system, as determined through the SPD registers on the memory modules. The system memory controller supports up to two DIMM connectors per channel. If DIMMs with different latency are populated across the channels, the BIOS will use the slower of the two latencies for both channels. For Dual-Channel modes both channels should have a DIMM connector populated. For Single-Channel mode, only a single channel can have a DIMM connector populated.

2.1.5 Technology Enhancements of Intel® Fast Memory Access (Intel® FMA)

The following sections describe the Just-in-Time Scheduling, Command Overlap, and Out-of-Order Scheduling Intel FMA technology enhancements.

Just-in-Time Command Scheduling

The memory controller has an advanced command scheduler where all pending requests are examined simultaneously to determine the most efficient request to be issued next. The most efficient request is picked from all pending requests and issued to system memory Just-in-Time to make optimal use of Command Overlapping. Thus, instead of having all memory access requests go individually through an arbitration mechanism forcing requests to be executed one at a time, they can be started without interfering with the current request allowing for concurrent issuing of requests. This allows for optimized bandwidth and reduced latency while maintaining appropriate command spacing to meet system memory protocol.

Command Overlap

Command Overlap allows the insertion of the DRAM commands between the Activate, Pre-charge, and Read/Write commands normally used, as long as the inserted commands do not affect the currently executing command. Multiple commands can be issued in an overlapping manner, increasing the efficiency of system memory protocol.

Out-of-Order Scheduling

While leveraging the Just-in-Time Scheduling and Command Overlap enhancements, the IMC continuously monitors pending requests to system memory for the best use of bandwidth and reduction of latency. If there are multiple requests to the same open page, these requests would be launched in a back to back manner to make optimum use of the open memory page. This ability to reorder requests on the fly allows the IMC to further reduce latency and increase bandwidth efficiency.

2.1.6 Data Scrambling

The system memory controller incorporates a Data Scrambling feature to minimize the impact of excessive di/dt on the platform system memory VRs due to successive 1s and 0s on the data bus. Past experience has demonstrated that traffic on the data bus is not random and can have energy concentrated at specific spectral harmonics creating high di/dt which is generally limited by data patterns that excite resonance between the package inductance and on die capacitances. As a result, the system memory controller uses a data scrambling feature to create pseudo-random patterns on the system memory data bus to reduce the impact of any excessive di/dt.

2.1.7 DDR I/O Interleaving

The processor supports I/O interleaving, which has the ability to swap DDR bytes for routing considerations. BIOS configures the I/O interleaving mode before DDR training.

Note: The KBL Y and AML-Y22 Processor Lines package is optimized only for Non-Interleaving (NIL) mode.

There are 2 supported modes:

- Interleave (IL)

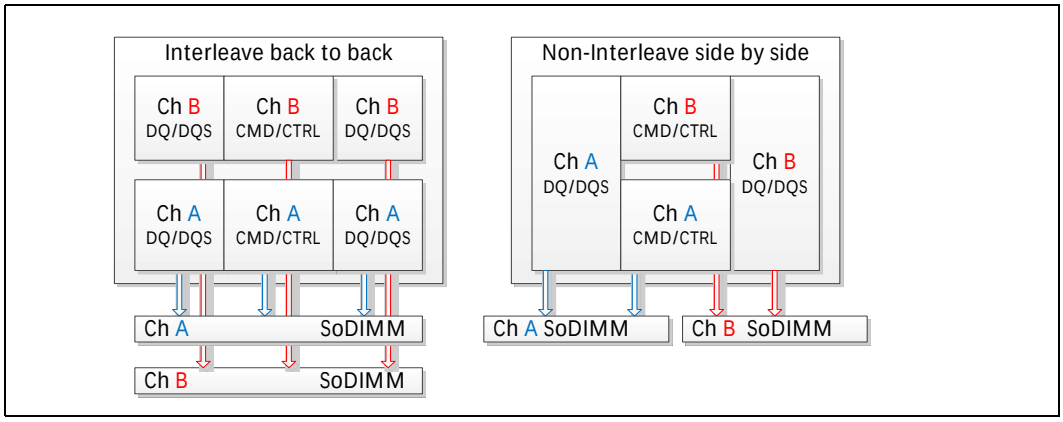
- Non-Interleave (NIL)

The following table and figure describe the pin mapping between the IL and NIL modes.

Table 2-10. Interleave (IL) and Non-Interleave (NIL) Modes Pin Mapping

IL		NIL	
Channel	**Byte**	**Channel**	**Byte**
DDR0	Byte0	DDR0	Byte0
DDR0	Byte1	DDR0	Byte1
DDR0	Byte2	DDR0	Byte4
DDR0	Byte3	DDR0	Byte5
DDR0	Byte4	DDR1	Byte0
DDR0	Byte5	DDR1	Byte1
DDR0	Byte6	DDR1	Byte4
DDR0	Byte7	DDR1	Byte5
DDR1	Byte0	DDR0	Byte2
DDR1	Byte1	DDR0	Byte3
DDR1	Byte2	DDR0	Byte6
DDR1	Byte3	DDR0	Byte7
DDR1	Byte4	DDR1	Byte2
DDR1	Byte5	DDR1	Byte3
DDR1	Byte6	DDR1	Byte6
DDR1	Byte7	DDR1	Byte7

Figure 2-2. Interleave (IL) and Non-Interleave (NIL) Modes Mapping



2.1.8 Data Swapping

By default, the processor supports on-board data swapping in two manners (for all segments and DRAM technologies):

- byte (DQ+DQS) swapping between bytes in the same channel.
- bit swapping within specific byte.

2.1.9 DRAM Clock Generation

Every supported rank has a differential clock pair. There are a total of four clock pairs driven directly by the processor to DRAM.

2.1.10 DRAM Reference Voltage Generation

The memory controller has the capability of generating the DDR3L/-RS, LPDDR3 and DDR4 Reference Voltage (VREF) internally for both read and write operations. The generated VREF can be changed in small steps, and an optimum VREF value is determined for both during a cold boot through advanced training procedures in order to provide the best voltage to achieve the best signal margins.

2.1.11 Data Swizzling

All Processor Lines does not have die-to-package DDR swizzling.

2.2 Processor Graphics

Note: Processor graphics is not supported on the X-Processor.

The processor graphics is based on Gen 9 LP (generation 9 Low Power) graphics core architecture that enables substantial gains in performance and lower-power consumption over prior generations. Gen 9 LP architecture supports up to 72 Execution Units (EUs) with On-Package Cache depending on the processor SKU.

The processor graphics architecture delivers high dynamic range of scaling to address segments spanning low power to high power, increased performance per watt, support for next generation of APIs. Gen 9 LP scalable architecture is partitioned by usage domains along Render/Geometry, Media, and Display. The architecture also delivers very low-power video playback and next generation analytic and filters for imaging-related applications. The new Graphics Architecture includes 3D compute elements, Multi-format HW assisted decode/encode pipeline, and Mid-Level Cache (MLC) for superior high definition playback, video quality, and improved 3D performance and media.

The Display Engine handles delivering the pixels to the screen. GSA (Graphics in System Agent) is the primary channel interface for display memory accesses and PCI-like traffic in and out.

The display engine supports the latest display standards such as eDP* 1.4, DP* 1.2, HDMI* 1.4, HW support for blend, scale, rotate, compress, high PPI support, and advanced SRD2 display power management.

2.2.1 Operating Systems Support

Windows* 10 x64,OS X, Linux* OS, Chrome* OS.

Note: The processor supports only 64-bit operating systems.

2.2.2 API Support (Windows*)

- Direct3D* 2015, Direct3D 11.2, Direct3D 11.1, Direct3D 9, Direct3D 10, Direct2D
- OpenGL* 4.4
- OpenCL* 2.1, OpenCL 2.0, OpenCL 1.2

DirectX* extensions:

- PixelSync, InstantAccess, Conservative Rasterization, Render Target Reads, Floating-point De-norms, Shared Virtual memory, Floating Point atomics, MSAA sample-indexing, Fast Sampling (Coarse LOD), Quilted Textures, GPU Enqueue Kernels, GPU Signals processing unit. Other enhancements include color compression.

Gen 9 LP architecture delivers hardware acceleration of Direct X* 11 Render pipeline comprising of the following stages: Vertex Fetch, Vertex Shader, Hull Shader, Tesselation, Domain Shader, Geometry Shader, Rasterizer, Pixel Shader, Pixel Output.

2.2.3 Media Support (Intel® QuickSync & Clear Video Technology HD)

Gen 9 LP implements multiple media video codecs in hardware as well as a rich set of image processing algorithms.

Note: All supported media codecs operate on 8 bpc, YCbCr 4:2:0 video profiles.

2.2.3.1 Hardware Accelerated Video Decode

Gen 9 LP implements a high-performance and low-power HW acceleration for video decoding operations for multiple video codecs.

The HW decode is exposed by the graphics driver using the following APIs:

- Direct3D* 9 Video API (DXVA2)
- Direct3D11 Video API
- Intel Media SDK
- MFT (Media Foundation Transform) filters.

Gen 9 LP supports full HW accelerated video decoding for AVC/VC1/MPEG2/HEVC/VP8/JPEG.

Table 2-11. Hardware Accelerated Video Decoding (Sheet 1 of 2)

Codec	Profile	Level	Maximum Resolution
MPEG2	Main	Main High	1080p
VC1/WMV9	Advanced	L3	3840x3840
	Main	High	
	Simple	Simple	
AVC/H264	High Main MVC & stereo	L5.1	2160p(4K)

Table 2-11. Hardware Accelerated Video Decoding (Sheet 2 of 2)

Codec	Profile	Level	Maximum Resolution
VP8	0	Unified level	1080p
JPEG/MJPEG	Baseline	Unified level	16k x16k
HEVC/H265 (8 bits)	Main	L5.1	2160(4K)
HEVC/H265 (10 bits)	Main BT2020, isolate Dec	L5.1	2160(4K)
VP9	0 (4:2:0 Chroma 8-10bit)	Unified level	2160(4K)

Expected performance:

- More than 16 simultaneous decode streams @ 1080p.

Note: Actual performance depends on the processor SKU, content bit rate, and memory frequency. Hardware decode for H264 SVC is not supported.

2.2.3.2 Hardware Accelerated Video Encode

Gen 9 LP implements a high-performance and low-power HW acceleration for video decoding operations for multiple video codecs.

The HW encode is exposed by the graphics driver using the following APIs:

- Intel Media SDK
- MFT (Media Foundation Transform) filters

Gen 9 LP supports full HW accelerated video encoding for AVC/MPEG2/HEVC/VP8/JPEG.

Table 2-12. Hardware Accelerated Video Encode

Codec	Profile	Level	Maximum Resolution
MPEG2	Main	High	1080p
AVC/H264	High Main	L5.1	2160p(4K)
VP8	Unified profile	Unified level	—
JPEG	Baseline	—	16Kx16K
HEVC/H265	Main	L5.1	2160p(4K)
VP9	Support 8 bits 4:2:0 BT2020 may be obtained the pre/post processing	—	—

Note: Hardware encode for H264 SVC is not supported.

2.2.3.3 Hardware Accelerated Video Processing

There is hardware support for image processing functions such as De-interlacing, Film cadence detection, Advanced Video Scaler (AVS), detail enhancement, image stabilization, gamut compression, HD adaptive contrast enhancement, skin tone enhancement, total color control, Chroma de-noise, SFC pipe (Scalar and Format Conversion), memory compression, Localized Adaptive Contrast Enhancement (LACE), spatial de-noise, Out-Of-Loop De-blocking (from AVC decoder), 16 bpc support for de-noise/de-mosaic.

There is support for Hardware assisted Motion Estimation engine for AVC/MPEG2 encode, True Motion, and Image stabilization applications.

The HW video processing is exposed by the graphics driver using the following APIs:

- Direct3D* 9 Video API (DXVA2).
- Direct3D 11 Video API.
- Intel Media SDK.
- MFT (Media Foundation Transform) filters.
- Intel CUI SDK.

Note: Not all features are supported by all the above APIs. Refer to the relevant documentation for more details.

2.2.3.4 Hardware Accelerated Transcoding

Transcoding is a combination of decode video processing (optional) and encode. Using the above hardware capabilities can accomplish a high-performance transcode pipeline. There is not a dedicated API for transcoding.

The processor graphics supports the following transcoding features:

- Low-power and low-latency AVC encoder for video conferencing and Wireless Display applications.
- Lossless memory compression for media engine to reduce media power.
- HW assisted Advanced Video Scaler.
- Low power Scaler and Format Converter.

Expected performance:

- KBL Y and AML-Y22 Processor Lines: 10x 1080p30 RT (previous generation is 5x 1080p30 RT).
- U/U 4 Core Processor Line: 12x 1080p30 RT (same as previous generation).

Note: Actual performance depends on the processor Line, video processing algorithms used, content bit rate, and memory frequency.

2.2.4 Camera Pipe Support

Camera pipe functions such as de-mosaic, white balance, defect pixel correction, black level correction, gamma correction, LGCA, vignette control, Front end Color Space Converter (CSC), Image Enhancement Color Processing (IECP).

2.2.5 Switchable / Hybrid Graphics

The processor supports Switchable/Hybrid graphics.

Switchable graphics: The Switchable Graphics feature allows you to switch between using the Intel integrated graphics and a discrete graphics card. The Intel Integrated Graphics driver will control the switching between the modes. In most cases it will operate as follows: when connected to AC power - Discrete graphic card; when connected to DC (battery) - Intel integrated GFX.

Hybrid graphics: Intel integrated graphics and a discrete graphics card work cooperatively to achieve enhanced power and performance.

Table 2-13. Switchable / Hybrid Graphics Support

Operating System	Hybrid Graphics	Switchable Graphics[2]
Windows* 10 (64 bit)	Yes[1]	N/A

Note:
1. Contact your graphics vendor to check for support.
2. Intel does not validate any SG configurations on Windows* 8.1 or Windows* 10.

2.2.6 Gen 9 LP Video Analytics

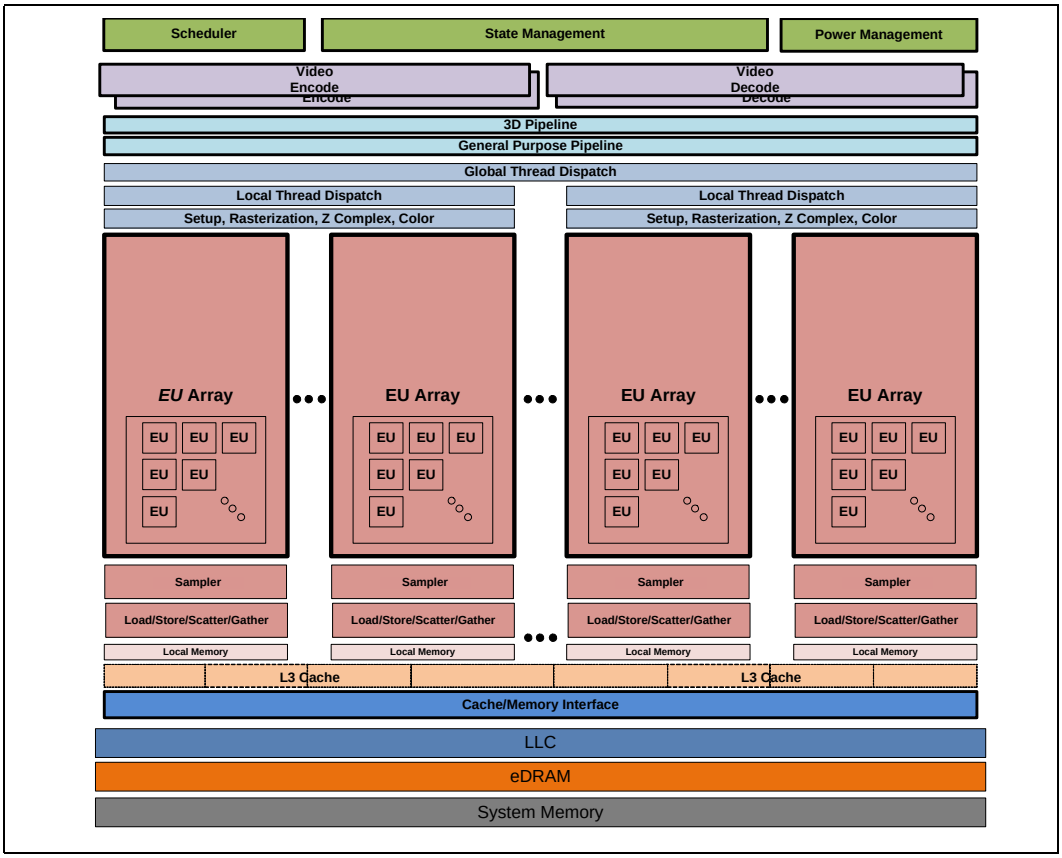
There is HW assist for video analytics filters such as scaling, convolve 2D/1D, minmax, 1P filter, erode, dilate, centroid, motion estimation, flood fill, cross correlation, Local Binary Pattern (LBP).

Figure 2-3. Video Analytics Common Use Cases

Usage	Scaling	Convolve 2D / 1D	MinMax Filter	Erode	Dilate	Centroid	Motion Estimation	Floodfill	Cross Correlation	LBP Creation
Face Detection	■	■	■	■	■	■				
Face Expressions	■	■	■			■				
Face Recognition	■	■				■				■
Face Tracking		■	■				■			
Gesture Detection	■	■	■	■	■	■		■		
Gesture Tracking		■	■				■			
Scene Identification	■	■	■			■				
2D to 3D Video	■	■	■				■			■
Object Detection	■	■	■	■	■	■			■	
Object Tracking		■	■				■			
Video Enhancement	■	■	■	■	■	■	■			
Video Segmentation	■	■	■				■			
Visual Search	■	■	■	■	■	■				
Stereo	■	■					■	■	■	■
Superes	■	■							■	

2.2.7 Gen 9 LP (9th Generation Low Power) Block Diagram

Figure 2-4. Gen 9 LP Block Diagram



2.2.8 GT2 / 3 Graphic Frequency

Table 2-14. GT2 / 3 Graphics Frequency (KBL U / Y and AML-Y22 Processor Line)

Segment	GT Unslice	GT Unslice + 1 GT Slice	GT Unslice + 2 GT Slice
Y-Processor Line and AML Y-Processor Line- 2 Core with GT2	GT Max Dynamic frequency	[GT Unslice only] - (1or2)BIN	—
U-Processor Line- 2 Core with GT2	GT Max Dynamic frequency	[GT Unslice only] - (1or2)BIN	—
U-Processor Line- 2 Core with GT3 and OPC	GT Max Dynamic frequency	[GT Unslice only] - (1or2)BIN	[GT Unslice + 1 Slice] - (1or2)BIN

2.3 Display Interfaces

The processor supports single eDP* interface and 2 DDI interfaces (depends on segment):

- DDI interface can be configured as DisplayPort* or HDMI*.
- Each DDI can support dual mode (DP++).
- Each DDI can support DVI (DVI max resolution is 1920x1200 @ 60 Hz).
- The DisplayPort* can be configured to use 1, 2, or 4 lanes depending on the bandwidth requirements and link data rate.
- DDI ports notated as: DDI B, C, D.
- Y-Processor /AML-Y22 ProcessorU/ support eDP and up to 2 DDI supporting DP/ HDMI.
- AUX/DDC signals are valid for each DDI Port. (Two for U/YProcessors)
- Total Five dedicated HPD (Hot plug detect signals) are valid for all processor SKUs.

Note: SSC is supported in eDP*/DP for all Processor Lines.

Note: The processor platform supports DP Type-C implementation with additional discrete components.

Table 2-15. VGA and Embedded DisplayPort* (eDP*) Bifurcation Summary

Port	U/Y-Processor Line
eDP - DDIA (eDP lower x2 lanes, [1:0])	N/A
VGA - DDIE[2] (DP upper x2 lanes, [3:2])	N/A

Notes:
1. N/A
2. DP-to-VGA converter on the processor ports is supported using external dongle only, display driver software for VGA dongles which configures the VGA port as a DP branch device.

The technologies supported by the processor are listed in the following table.

Table 2-16. Embedded DisplayPort (eDP*)/DDI Ports Availability (Sheet 1 of 2)

Ports	Port Name in VBT	U/U-Quad Core/Y-Processor Line[2,3]
DDI0 - eDP	Port A	Yes
DDI1	Port B	Yes
DDI2	Port C	Yes
DDI3	Port D	No[4]
DDI4 - eDP/VGA	Port E	No

Table 2-16. Embedded DisplayPort (eDP*)/DDI Ports Availability (Sheet 2 of 2)

Ports	Port Name in VBT	U/U-Quad Core/Y-Processor Line[2,3]
Notes: 1. Port E is bifurcated from eDP, when VGA is used need to use available AUX (if HDMI is in used). a. For example, DT can use eDP_AUX for VGA converter which is available as free Design but HPD should be used as DDPE_HPD3. 2. 3xDDC (DDPB, DDPC, DDPD) are valid for all the processor SKUs (for U/YProcessor Line DDC signals description, refer to the PCH Datasheet) (See Related Document section). 3. 5xHPD (PCH) inputs (eDP_HPD, DDPB_HPD0, DDPC_HPD1, DDPD_HPD2, DDPE_HPD3) are valid for all processor SKUs. 4. No Port D for Y/U-Processor Line. DDI3_AUX are exists as reserved. 5. VBT provides a configuration option to select the four AUX channels A/B/C/D for a given port, based on how the aux channel lines are connected physically on the board.		

Table 2-17. Display Technologies Support

Technology	Standard
eDP* 1.4	VESA* Embedded DisplayPort* Standard 1.4
DisplayPort* 1.2	VESA DisplayPort* Standard 1.2 VESA DisplayPort* PHY Compliance Test Specification 1.2 VESA DisplayPort* Link Layer Compliance Test Specification 1.2
HDMI* 1.4[1]	High-Definition Multimedia Interface Specification Version 1.4
Notes: 1. HDMI* 2.0/2.0a support is possible using LS-Pcon converter chip connected to the DP port. The LS-Pcon supports 2 modes: a. Level shifter for HDMI 1.4 resolutions. b. DP-HDMI 2.0 protocol converter for HDMI 2.0 resolutions.	

- The HDMI* interface supports HDMI with 3D, 4Kx2K @ 24 Hz, Deep Color, and x.v.Color.
- The processor supports High-bandwidth Digital Content Protection (HDCP) for high definition content playback over digital interfaces. HDCP is not supported for eDP.
- The processor supports eDP display authentication: Alternate Scrambler Seed Reset (ASSR).
- The processor supports Multi-Stream Transport (MST), enabling multiple monitors to be used via a single DisplayPort connector.

The maximum MST DP supported resolution for U/Y-Processors is shown in the following table.

Table 2-18. Display Resolutions and Link Bandwidth for Multi-Stream Transport Calculations (Sheet 1 of 2)

Pixels per line	Lines	Refresh Rate [Hz]	Pixel Clock [MHz]	Link Bandwidth [Gbps]
640	480	60	25.2	0.76
800	600	60	40	1.20
1024	768	60	65	1.95
1280	720	60	74.25	2.23
1280	768	60	68.25	2.05
1360	768	60	85.5	2.57
1280	1024	60	108	3.24
1400	1050	60	101	3.03
1680	1050	60	119	3.57

Table 2-18. Display Resolutions and Link Bandwidth for Multi-Stream Transport Calculations (Sheet 2 of 2)

Pixels per line	Lines	Refresh Rate [Hz]	Pixel Clock [MHz]	Link Bandwidth [Gbps]
1920	1080	60	148.5	4.46
1920	1200	60	154	4.62
2048	1152	60	156.75	4.70
2048	1280	60	174.25	5.23
2048	1536	60	209.25	6.28
2304	1440	60	218.75	6.56
2560	1440	60	241.5	7.25
3840	2160	30	262.75	7.88
2560	1600	60	268.5	8.06
2880	1800	60	337.5	10.13
3200	2400	60	497.75	14.93
3840	2160	60	533.25	16.00
4096	2160	60	556.75	16.70
4096	2304	60	605	18.15

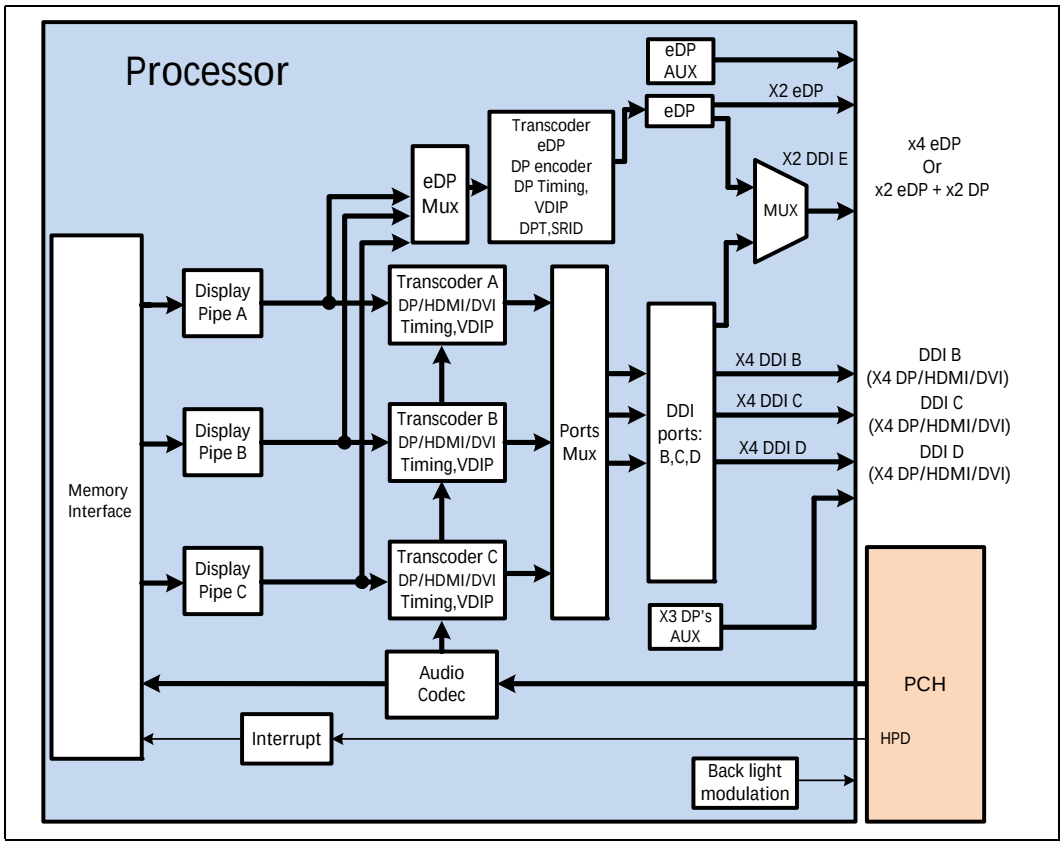
Notes:

1. All above is related to bit depth of 24.
2. The data rate for a given video mode can be calculated as: Data Rate = Pixel Frequency * Bit Depth.
3. The bandwidth requirements for a given video mode can be calculated as: Bandwidth = Data Rate * 1.25 (for 8B/10B coding overhead).
4. The Table above is partial List of the common Display resolutions, just for example.
   The Link Bandwidth depends if the standards is Reduced Blanking or not.
   If the Standard is Not reduced blanking, the expected Bandwidth will be higher.
   For more details, refer to VESA and Industry Standards and Guidelines for Computer Display Monitor Timing (DMT), Version 1.0, Rev. 13 February 8, 2013
5. To calculate the resolutions that can be supported in MST configurations, follow the below guidelines:
   a. Identify what is the Link Bandwidth (column right) according the requested Display resolution.
   b. Summarize the Bandwidth for Two of three Displays accordingly, and make sure the final result is below 21.6Gbps. (for HBR2, four lanes)
   c. For special cases when x2 lanes are used or HBR or RBR used, refer to the tables in Section 2.3.11, “Display Resolution per Link Width” accordingly.

   For examples:
   a. Docking Two displays: 3840x2160 @ 60 Hz + 1920x1200 @ 60 Hz = 16 + 4.62 = 20.62 Gbps [Supported]
   b. Docking Three Displays: 3840x2160 @ 30 Hz + 3840x2160 @ 30 Hz + 1920x1080 @ 60 Hz = 7.88 + 7.88 + 4.16 = 19.92 Gbps [Supported]
6. Consider also the supported resolutions as mentioned in Section 2.3.6, “Multiple Display Configurations (Dual Channel DDR)” and Section 2.3.7, “Multiple Display Configurations (Single Channel DDR)”.

- The processor supports only 3 streaming independent and simultaneous display combinations of DisplayPort*/eDP*/HDMI/DVI monitors. In the case where 4 monitors are plugged in, the software policy will determine which 3 will be used.
- Three High Definition Audio streams over the digital display interfaces are supported.
- For display resolutions driving capability, see Maximum Display Resolution table.
- DisplayPort* Aux CH supported by the processor, while DDC channel, Panel power sequencing, and HPD are supported through the PCH.

Figure 2-5. Processor Display Architecture (with 3 DDI ports as an example)



Note: U/Y Processors only have two DDI ports.

Display is the presentation stage of graphics. This involves:

- Pulling rendered data from memory
- Converting raw data into pixels
- Blending surfaces into a frame
- Organizing pixels into frames
- Optionally scaling the image to the desired size
- Re-timing data for the intended target
- Formatting data according to the port output standard

2.3.1 DisplayPort*

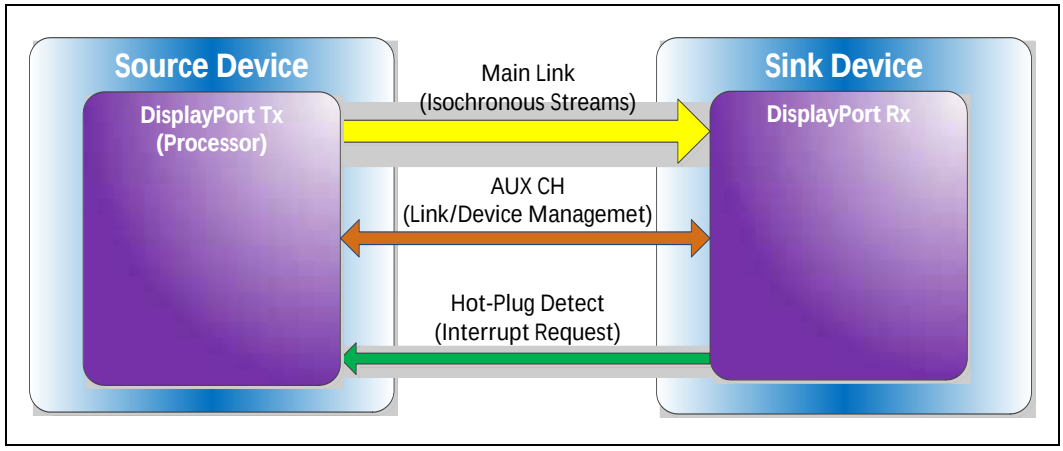
The DisplayPort* is a digital communication interface that uses differential signaling to achieve a high-bandwidth bus interface designed to support connections between PCs and monitors, projectors, and TV displays.

A DisplayPort* consists of a Main Link, Auxiliary channel, and a Hot-Plug Detect signal. The Main Link is a unidirectional, high-bandwidth, and low-latency channel used for transport of isochronous data streams such as uncompressed video and audio. The

Auxiliary Channel (AUX CH) is a half-duplex bidirectional channel used for link management and device control. The Hot-Plug Detect (HPD) signal serves as an interrupt request for the sink device.

The processor is designed in accordance to VESA* DisplayPort* specification. Refer to Table 2-17, “Display Technologies Support”.

Figure 2-6. DisplayPort* Overview



2.3.2 High-Definition Multimedia Interface (HDMI*)

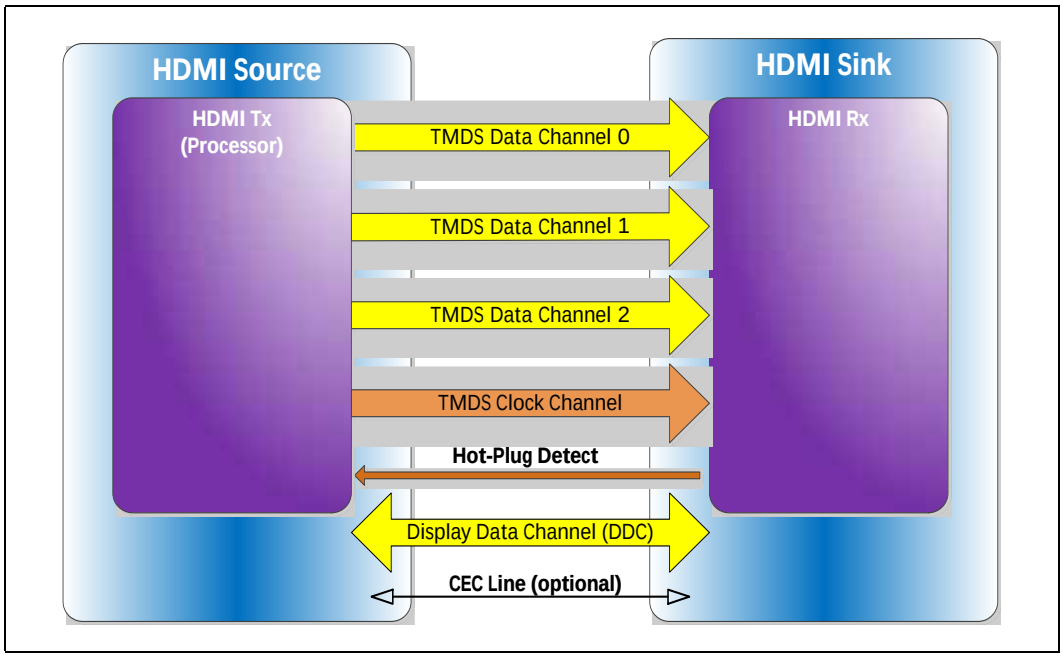
The High-Definition Multimedia Interface (HDMI*) is provided for transmitting uncompressed digital audio and video signals from DVD players, set-top boxes, and other audio-visual sources to television sets, projectors, and other video displays. It can carry high-quality multi-channel audio data and all standard and high-definition consumer electronics video formats. The HDMI display interface connecting the processor and display devices uses transition minimized differential signaling (TMDS) to carry audiovisual information through the same HDMI cable.

HDMI includes three separate communications channels: TMDS, DDC, and the optional CEC (consumer electronics control). CEC is not supported on the processor. As shown in the following figure, the HDMI cable carries four differential pairs that make up the TMDS data and clock channels. These channels are used to carry video, audio, and auxiliary data. In addition, HDMI carries a VESA DDC. The DDC is used by an HDMI Source to determine the capabilities and characteristics of the Sink.

Audio, video, and auxiliary (control/status) data is transmitted across the three TMDS data channels. The video pixel clock is transmitted on the TMDS clock channel and is used by the receiver for data recovery on the three data channels. The digital display data signals driven natively through the PCH are AC coupled and needs level shifting to convert the AC coupled signals to the HDMI compliant digital signals.

The processor HDMI interface is designed in accordance with the High-Definition Multimedia Interface.

Figure 2-7. HDMI* Overview



2.3.3 Digital Video Interface (DVI)

The processor Digital Ports can be configured to drive DVI-D. DVI uses TMDS for transmitting data from the transmitter to the receiver, which is similar to the HDMI protocol except for the audio and CEC. Refer to the HDMI section for more information on the signals and data transmission. The digital display data signals driven natively through the processor are AC coupled and need level shifting to convert the AC coupled signals to the HDMI compliant digital signals.

2.3.4 embedded DisplayPort* (eDP*)

The embedded DisplayPort* (eDP*) is an embedded version of the DisplayPort standard oriented towards applications, such as notebook and All-In-One PCs. Like DisplayPort, embedded DisplayPort* also consists of a Main Link, Auxiliary channel, and an optional Hot-Plug Detect signal.

2.3.5 Integrated Audio

- HDMI* and display port interfaces carry audio along with video.
- The processor supports 3 High Definition audio streams on 3 digital ports simultaneously (the DMA controllers are in the PCH).
- The integrated audio processing (DSP) is performed by the PCH, and delivered to the processor using the AUDIO_SDI and AUDIO_CLK inputs pins.
- AUDIO_SDO output pin is used to carry responses back to the PCH.
- Supports only the internal HDMI and DP CODECs.

Table 2-19. Processor Supported Audio Formats over HDMI and DisplayPort*

Audio Formats	HDMI*	DisplayPort*
AC-3 Dolby* Digital	Yes	Yes
Dolby Digital Plus	Yes	Yes
DTS-HD*	Yes	Yes
LPCM, 192 kHz/24 bit, 8 Channel	Yes	Yes
Dolby TrueHD, DTS-HD Master Audio* (Lossless Blu-Ray Disc* Audio Format)	Yes	Yes

The processor will continue to support Silent stream. Silent stream is an integrated audio feature that enables short audio streams, such as system events to be heard over the HDMI* and DisplayPort* monitors. The processor supports silent streams over the HDMI and DisplayPort interfaces at 44.1 kHz, 48 kHz, 88.2 kHz, 96 kHz, 176.4 kHz, and 192 kHz sampling rates.

2.3.6 Multiple Display Configurations (Dual Channel DDR)

The following multiple display configuration modes are supported (with appropriate driver software):

- Single Display is a mode with one display port activated to display the output to one display device.
- Intel Display Clone is a mode with up to three display ports activated to drive the display content of same color depth setting but potentially different refresh rate and resolution settings to all the active display devices connected.
- Extended Desktop is a mode with up to three display ports activated to drive the content with potentially different color depth, refresh rate, and resolution settings on each of the active display devices connected.

The digital ports on the processor can be configured to support DisplayPort/HDMI/DVI. The following table shows examples of valid three display configurations through the processor.

Table 2-20. Maximum Display Resolution (Sheet 1 of 2)

Standard	Y-Processor Line	U/U-Quad Core Processor Line	Notes
eDP*	2880x1800 @ 60Hz, 24bpp Or 3840x2160 @ 60Hz, 24bpp[4]	3840x2160 @ 60Hz, 24bpp[4] Or 4096x2304 @ 60Hz, 24bpp[4]	1,2,3,7
DP*	2880x1800 @ 60Hz, 24bpp Or 3840x2160 @ 60Hz, 24bpp[4]	3840x2160 @ 60Hz, 24bpp[4] Or 4096x2304 @ 60Hz, 24bpp[4]	1,2,3,7
HDMI* 1.4 (native)	4096x2160 @ 30 Hz, 24bpp[4]	4096x2160 @ 30 Hz, 24bpp[4]	1,2,3
HDMI 2.0/2.0a (Via LS-Pcon)	2880x1800 @ 60Hz, 24bpp Or 3840x2160 @ 60Hz, 24bpp[4]	3840x2160 @ 60Hz, 24bpp[4] Or 4096x2160 @ 60Hz, 24bpp[4]	1,2,3,6

Table 2-20. Maximum Display Resolution (Sheet 2 of 2)

Standard	Y-Processor Line	U/U-Quad Core Processor Line	Notes

Notes:
1. Maximum resolution is based on implementation of 4 lanes with HBR2 link data rate.
2. bpp - bit per pixel.
3. N/A
4. N/A
5. In the case of connecting more than one active display port, the processor frequency may be lower than base frequency at thermally limited scenario.
6. HDMI2.0 implemented using LSPCON device. Only one LSPCON with HDCP2.2 support is supported per platform.
7. Display resolution of 5120x2880@60Hz can be supported with 5K panels displays which have two ports. (with the GFX driver accordingly).

2.3.7 Multiple Display Configurations (Single Channel DDR)

Table 2-21. Y/AML Y22-Processor Lines Display Resolution Configuration

Minimum DDR speed [MT/s]	Maximum Resolution (Clone/ Extended mode)		
	eDP @ 60 Hz (Primary)	DP @ 60 Hz / HDMI @ 30 Hz (Secondary 1)	DP @ 60 Hz / HDMI @ 30 Hz (Secondary 2)
1333	2880 x 1800	Not Connected	Not Connected
	2880 x 1800	2880 x 1800	Not Connected
	2880 x 1800	2880 x 1800	2880 x 1800

Note: This resolution is limited by power.

Table 2-22. U/ Lines Display Resolution Configuration

Minimum DDR speed [MT/s]	Maximum Resolution (Clone/ Extended mode)		
	eDP @ 60 Hz (Primary)	DP @ 60 Hz / HDMI @ 30 Hz (Secondary 1)	DP @ 60 Hz / HDMI @ 30 Hz (Secondary 2)
1333	3840 x 2160	Not Connected	Not Connected
	3200 x 1800	3840 x 2160	Not Connected
1600	3840 x 2160	3840 x 2160	Not Connected
	2560 x 1440	3840 x 2160	3840 x 2160
1866	3200 x 1800	3840 x 2160	3840 x 2160
2133	3840 x 2160	3840 x 2160	3840 x 2160
2400	3840 x 2160	3840 x 2160	3840 x 2160

Table 2-23. U/U- 4 CoreProcessor Lines Display Resolution Configuration (DP @ 30 Hz) (Sheet 1 of 2)

Minimum DDR speed [MT/s]	Maximum Resolution (Clone/ Extended mode)		
	eDP @ 60 Hz (Primary)	DP @ 30 Hz (Secondary 1)	DP @ 30 Hz (Secondary 2)
1333	3840 x 2160	Not Connected	Not Connected
	3840 x 2160	3840 x 2160	Not Connected
	3200 x 1800	3840 x 2160	3840 x 2160
1600[1]	3840 x 2160	3840 x 2160	3840 x 2160

Table 2-23. U/U- 4 CoreProcessor Lines Display Resolution Configuration (DP @ 30 Hz) (Sheet 2 of 2)

Minimum DDR speed [MT/s]	Maximum Resolution (Clone/ Extended mode)		
	eDP @ 60 Hz (Primary)	DP @ 30 Hz (Secondary 1)	DP @ 30 Hz (Secondary 2)

Note:
1. eDP with 3840x2160 @ 60 Hz resolution is very close to maximum limit and may not be supported for U/U-4 Core Processor Line.

2.3.8 High-bandwidth Digital Content Protection (HDCP)

HDCP is the technology for protecting high-definition content against unauthorized copy or unreceptive between a source (computer, digital set top boxes, and so on) and the sink (panels, monitor, and TVs). The processor supports HDCP 2.2 for 4k Premium content protection over wired displays (HDMI*, DVI, and DisplayPort*).

The HDCP 2.2 keys are integrated into the processor and customers are not required to physically configure or handle the keys. HDCP2.2 for HDMI2.0 is covered by the LSPCON platform device.

Some minor difference will be between Integrated HDCP2.2 over HDMI1.4 compared to the HDCP2.2 over LSPCON in HDMI1.4 Mode. Also, LSPCON is needed for HDMI 2.0a which defines HDR over HDMI.

The HDCP 1.4 keys are integrated into the processor and customers are not required to physically configure or handle the keys.

Table 2-24. HDCP Display supported Implications Table

Topic	HDCP Revision	Maximum Resolution	HDR[1]	HDCP Solution[2]	BPC[3]	Comments
DP	HDCP1.4	4K@60	No	iHDCP	10 bit	Legacy Integrated for HDCP1.4
	HDCP2.2	4K@60	Yes	iHDCP	10 bit	New Integrated for HDCP2.2
HDMI1.4	HDCP1.4	4K@30	No	iHDCP	8 bit	Legacy Integrated for HDCP1.4
	HDCP2.2	4K@30	No	LSPCON	8 bit	LSPCON HDCP2.2 required
	HDCP2.2	4K@30	No	iHDCP[4]	8 bit	New Integrated for HDCP2.2
HDMI2.0	HDCP2.2	4K@60	No	LSPCON	12 bit (YUV 420)	LSPCON HDCP2.2 required
HDMI2.0a	HDCP2.2	4K@60	Yes	LSPCON	12 bit (YUV 420)	LSPCON HDCP2.2 required

Notes:
1. HDR - High Dynamic Range feature expands the range of both contrast and color significantly, HDR will be supported on DP and HDMI2.0a configuration only.
2. HDCP Solutions:
   a. iHDCP - Intel Silicon Integrated HDCP
   b. LSPCon - 3rd Party motherboard soldered down solution
3. BPC - Bits Per Channel.
4. HDMI1.4 with the Integrated HDCP2.2 solution will replace the LSPCON Solution at a later time.
5. HDCP2.2 is supported by KBL U/Y and AML Y22-Processors with integrated HDCP2.2 and by U-Processors 2+3e. HDCP2.2 is not supported by Y/U-Processors without integrated HDCP2.2.

2.3.9 Display Link Data Rate Support

Table 2-25. Display Link Data Rate Support

Technology	Link Data Rate
eDP*	RBR (1.62 GT/s) 2.16 GT/s 2.43 GT/s HBR (2.7 GT/s) 3.24 GT/s 4.32 GT/s HBR2 (5.4 GT/s)
DisplayPort*	RBR (1.62 GT/s) HBR (2.7 GT/s) HBR2 (5.4 GT/s)
HDMI*	1.65 Gb/s 2.97 Gb/s

Table 2-26. Display Resolution and Link Rate Support

Resolution	Link Rate Support	High Definition
4096x2304	5.4 (HBR2)	UHD (4K)
3840x2160	5.4 (HBR2)	UHD (4K)
3200x2000	5.4 (HBR2)	QHD+
3200x1800	5.4 (HBR2)	QHD+
2880x1800	2.7 (HBR)	QHD
2880x1620	2.7 (HBR)	QHD
2560x1600	2.7 (HBR)	QHD
2560x1440	2.7 (HBR)	QHD
1920x1080	1.62 (RBR)	FHD

2.3.10 Display Bit Per Pixel (BPP) Support

Table 2-27. Display Bit Per Pixel (BPP) Support

Technology	Bit Per Pixel (bpp)
eDP*	24,30,36
DisplayPort*	24,30,36
HDMI*	24,36

2.3.11 Display Resolution per Link Width

Table 2-28. Supported Resolutions[1] for HBR (2.7 Gbps) by Link Width (Sheet 1 of 2)

Link Width	Max Link Bandwidth [Gbps]	Max Pixel Clock (theoretical) [MHz]	U/Y-Processor Lines
4 lanes	10.8	360	2880x1800 @ 60 Hz, 24bpp
2 lanes	5.4	180	2048x1280 @ 60 Hz, 24bpp

Table 2-28. Supported Resolutions[1] for HBR (2.7 Gbps) by Link Width (Sheet 2 of 2)

Link Width	Max Link Bandwidth [Gbps]	Max Pixel Clock (theoretical) [MHz]	U/Y-Processor Lines
1 lane	2.7	90	1280x960 @ 60 Hz, 24bpp
Notes: 1. The examples assumed 60 Hz refresh rate and 24 bpp.			

Table 2-29. Supported Resolutions[1] for HBR2 (5.4 Gbps) by Link Width

Link Width	Max Link Bandwidth [Gbps]	Max Pixel Clock (theoretical) [MHz]	U/Y-Processor Lines
4 lanes	21.6	720	See “Maximum Display Resolutions” table
2 lanes	10.8	360	2880x1800 @ 60 Hz, 24bpp
1 lane	5.4	180	2048x1280 @ 60 Hz, 24bpp
Notes: 1. The examples assumed 60 Hz refresh rate and 24 bpp. 2.			

2.4 Platform Environmental Control Interface (PECI)

PECI is an Intel proprietary interface that provides a communication channel between Intel processors and external components like Super IO (SIO) and Embedded Controllers (EC) to provide processor temperature, Turbo, Configurable TDP, and memory throttling control mechanisms and many other services. PECI is used for platform thermal management and real time control and configuration of processor features and performance.

2.4.1 PECI Bus Architecture

The PECI architecture is based on a wired OR bus that the clients (as processor PECI) can pull up (with strong drive).

The idle state on the bus is near zero.

The following figures demonstrates PECI design and connectivity:

- PECI Host-Clients Connection: While the host/originator can be third party PECI host and one of the PECI client is a processor PECI device.
- PECI EC Connection.

Figure 2-8. Example for PECI Host-Clients Connection

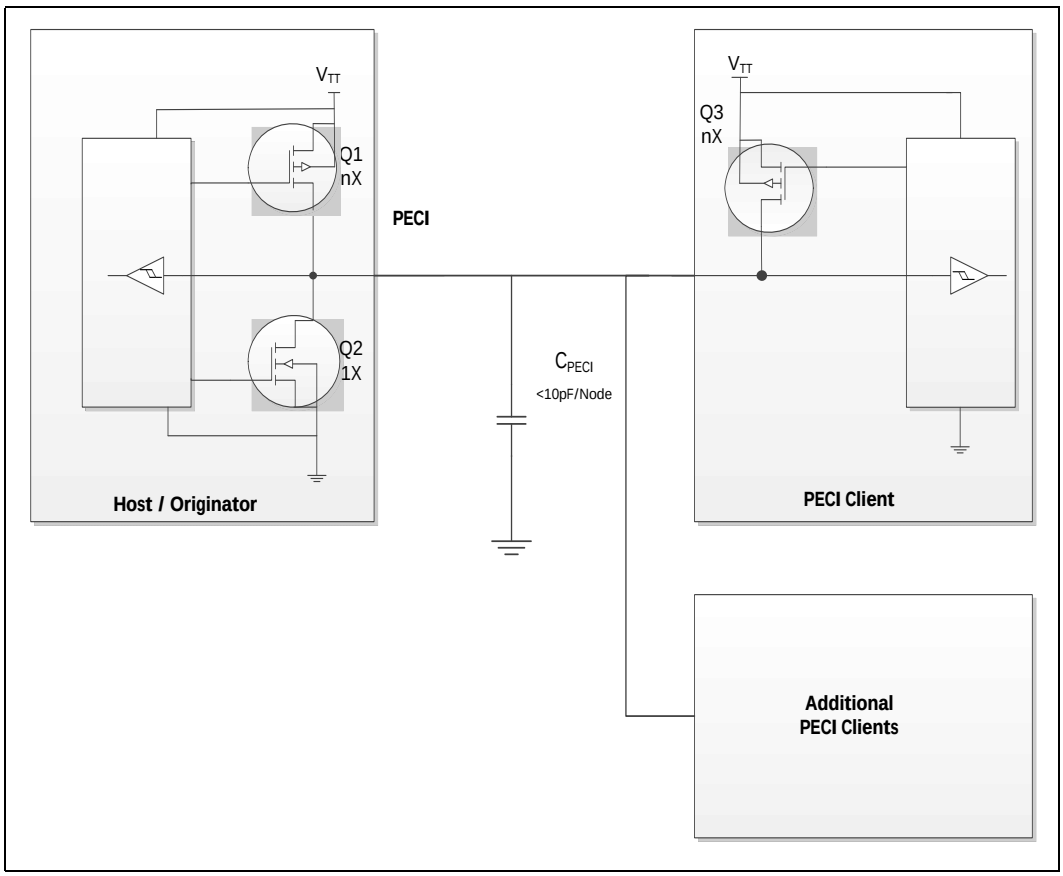
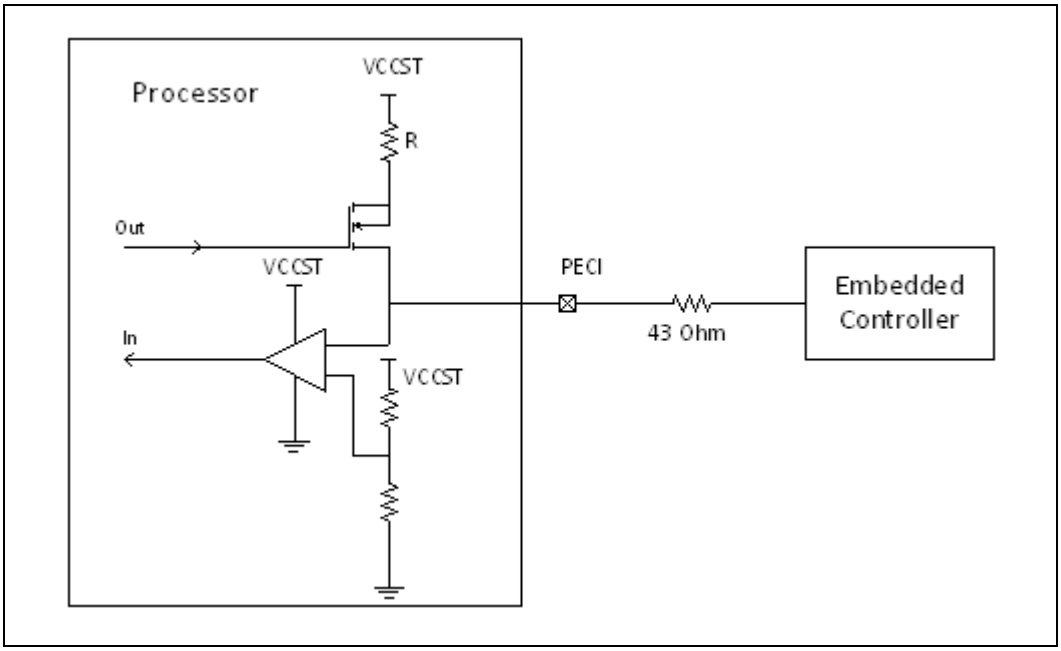


Figure 2-9. Example for PECI EC Connection



3 Technologies

This chapter provides a high-level description of Intel technologies implemented in the processor.

The implementation of the features may vary between the processor SKUs.

Details on the different technologies of Intel processors and other relevant external notes are located at the Intel technology web site: http://www.intel.com/technology/

3.1 Intel® Virtualization Technology (Intel® VT)

Intel® Virtualization Technology (Intel® VT) makes a single system appear as multiple independent systems to software. This allows multiple, independent operating systems to run simultaneously on a single system. Intel VT comprises technology components to support virtualization of platforms based on Intel architecture microprocessors and chipsets.

Intel Virtualization Technology (Intel VT) for IA-32, Intel 64 and Intel Architecture (Intel VT-x) added hardware support in the processor to improve the virtualization performance and robustness. Intel Virtualization Technology for Directed I/O (Intel VT-d) extends Intel VT-x by adding hardware assisted support to improve I/O device virtualization performance.

Intel VT-x specifications and functional descriptions are included in the *Intel 64 and IA-32 Architectures Software Developer's Manual, Volume 3*. Available at:

http://www.intel.com/products/processor/manuals/index.htm

The Intel VT-d specification and other VT documents can be referenced at:

http://www.intel.com/technology/virtualization/index.htm

https://sharedspaces.intel.com/sites/PCDC/SitePages/Ingredients/ingredient.aspx?ing=VT

3.1.1 Intel® Virtualization Technology (Intel® VT) for IA-32, Intel® 64 and Intel® Architecture (Intel® VT-X)

Intel® VT-x Objectives

Intel VT-x provides hardware acceleration for virtualization of IA platforms. Virtual Machine Monitor (VMM) can use Intel VT-x features to provide an improved reliable virtualized platform. By using Intel VT-x, a VMM is:

- **Robust:** VMMs no longer need to use para-virtualization or binary translation. This means that VMMs will be able to run off-the-shelf operating systems and applications without any special steps.
- **Enhanced:** Intel VT enables VMMs to run 64-bit guest operating systems on IA x86 processors.
- **More reliable:** Due to the hardware support, VMMs can now be smaller, less complex, and more efficient. This improves reliability and availability and reduces the potential for software conflicts.

- **More secure:** The use of hardware transitions in the VMM strengthens the isolation of VMs and further prevents corruption of one VM from affecting others on the same system.

Intel® VT-x Key Features

The processor supports the following added new Intel VT-x features:

- Extended Page Table (EPT) Accessed and Dirty Bits
  - EPT A/D bits enabled VMMs to efficiently implement memory management and page classification algorithms to optimize VM memory operations, such as de-fragmentation, paging, live migration, and check-pointing. Without hardware support for EPT A/D bits, VMMs may need to emulate A/D bits by marking EPT paging-structures as not-present or read-only, and incur the overhead of EPT page-fault VM exits and associated software processing.
- EPTP (EPT pointer) switching
  - EPTP switching is a specific VM function. EPTP switching allows guest software (in VMX non-root operation, supported by EPT) to request a different EPT paging-structure hierarchy. This is a feature by which software in VMX non-root operation can request a change of EPTP without a VM exit. Software will be able to choose among a set of potential EPTP values determined in advance by software in VMX root operation.
- Pause loop exiting
  - Support VMM schedulers seeking to determine when a virtual processor of a multiprocessor virtual machine is not performing useful work. This situation may occur when not all virtual processors of the virtual machine are currently scheduled and when the virtual processor in question is in a loop involving the PAUSE instruction. The new feature allows detection of such loops and is thus called PAUSE-loop exiting.

The processor IA core supports the following Intel VT-x features:

- **Mode based (XU/XS) EPT execute control - New Feature for this processor**
  - A new mode of EPT operation which enables different controls for executability of GPA based on Guest specified mode (User/Supervisor) of linear address translating to the GPA. When the mode is enabled, the executability of a GPA is defined by two bits in EPT entry. One bit for accesses to user pages and other one for accesses to supervisor pages.
  - The new mode requires changes in VMCS, and EPT entries. VMCS includes a bit “mode based EPT execute control” which is used to enable/disable the mode. An additional bit in EPT entry is defined as “supervisor-execute access”; the original execute control bit is considered as “user-execute access”. If the “mode based EPT execute control” is disabled the additional bit is ignored and the system works with one bit execute control for both user pages and supervisor pages.
  - Behavioral changes - Behavioral changes are across three areas:
    - **Access to GPA-** If the “mode-based EPT execute control” VM-execution control is 1, treatment of guest-physical accesses by instruction fetches depends on the linear address from which an instruction is being fetched
      1. If the translation of the linear address specifies user mode (the U/S bit was set in every paging structure entry used to translate the linear address), the resulting guest-physical address is executable under EPT only if the XU bit (at position 2) is set in every EPT paging-structure entry used to translate the guest-physical address.
      2. If the translation of the linear address specifies supervisor mode (the U/S bit was clear in at least one of the paging-structure entries used

to translate the linear address), the resulting guest-physical address is executable under EPT only if the XS bit is set in every EPT paging-structure entry used to translate the guest-physical address

—The XU and XS bits are used only when translating linear addresses for guest code fetches. They do not apply to guest page walks, data accesses, or A/D-bit updates

- **VMEntry -** If the **"**activate secondary controls" and "mode-based EPT execute control" VM-execution controls are both 1, VM entries ensure that the "enable EPT" VM-execution control is 1. VM entry fails if this check fails. When such a failure occurs, control is passed to the next instruction,
- **VMExit -** The exit qualification due to EPT violation reports clearly whether the violation was due to User mode access or supervisor mode access.

— Capability Querying: IA32_VMX_PROCBASED_CTLS2 has bit to indicate the capability, RDMSR can be used to read and query whether the processor supports the capability or not.

- Extended Page Tables (EPT)
  - — EPT is hardware assisted page table virtualization
  - — It eliminates VM exits from guest OS to the VMM for shadow page-table maintenance
- Virtual Processor IDs (VPID)
  - — Ability to assign a VM ID to tag processor IA core hardware structures (such as TLBs)
  - — This avoids flushes on VM transitions to give a lower-cost VM transition time and an overall reduction in virtualization overhead.
- Guest Preemption Timer
  - — Mechanism for a VMM to preempt the execution of a guest OS after an amount of time specified by the VMM. The VMM sets a timer value before entering a guest
  - — The feature aids VMM developers in flexibility and Quality of Service (QoS) guarantees
- Descriptor-Table Exiting
  - — Descriptor-table exiting allows a VMM to protect a guest OS from internal (malicious software based) attack by preventing relocation of key system data structures like IDT (interrupt descriptor table), GDT (global descriptor table), LDT (local descriptor table), and TSS (task segment selector).
  - — A VMM using this feature can intercept (by a VM exit) attempts to relocate these data structures and prevent them from being tampered by malicious software.

3.1.2 Intel® Virtualization Technology (Intel® VT) for Directed I/O (Intel® VT-d)

Intel® VT-d Objectives

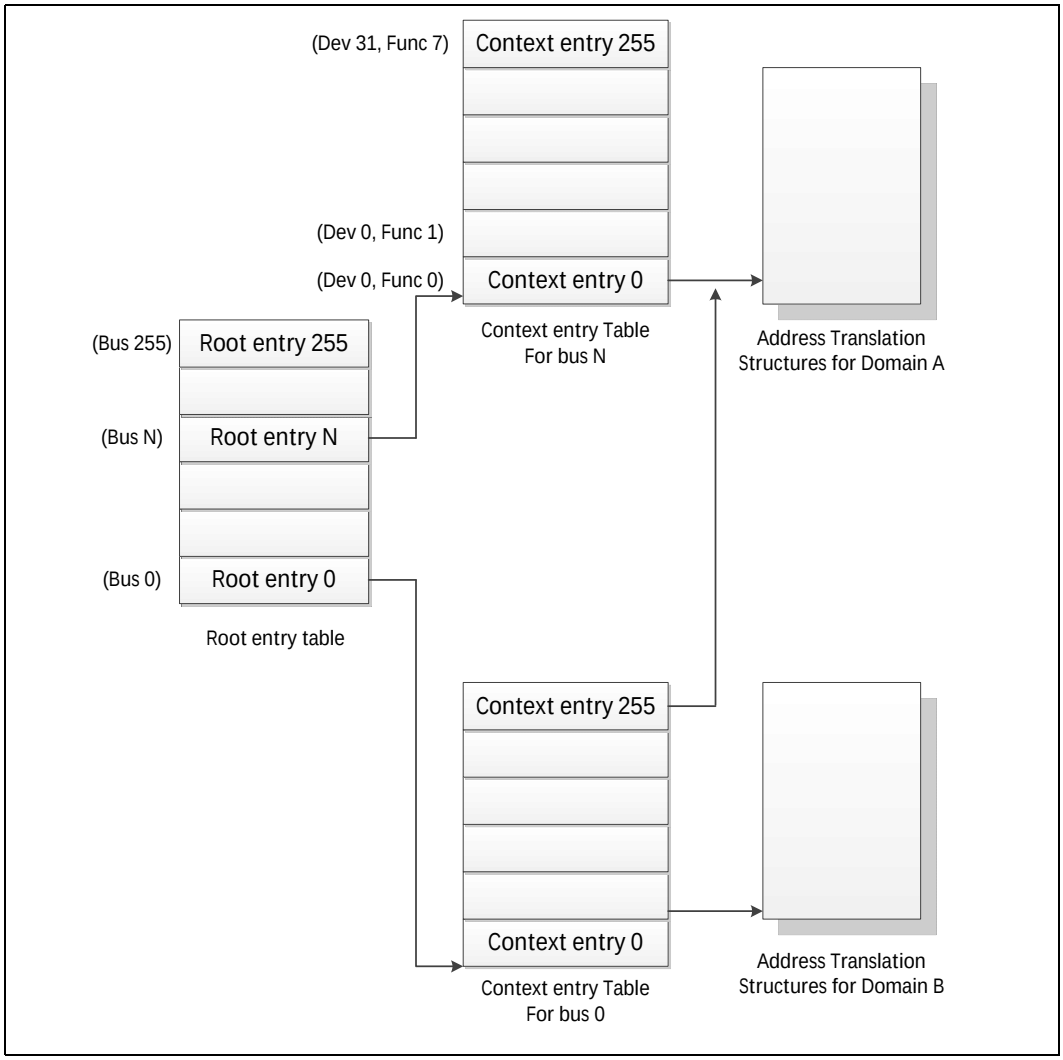
The key Intel VT-d objectives are domain-based isolation and hardware-based virtualization. A domain can be abstractly defined as an isolated environment in a platform to which a subset of host physical memory is allocated. Intel VT-d provides accelerated I/O performance for a virtualized platform and provides software with the following capabilities:

- I/O device assignment and security: for flexibly assigning I/O devices to VMs and extending the protection and isolation properties of VMs for I/O operations.

- DMA remapping: for supporting independent address translations for Direct Memory Accesses (DMA) from devices.
- Interrupt remapping: for supporting isolation and routing of interrupts from devices and external interrupt controllers to appropriate VMs.
- Reliability: for recording and reporting to system software DMA and interrupt errors that may otherwise corrupt memory or impact VM isolation.

Intel VT-d accomplishes address translation by associating transaction from a given I/O device to a translation table associated with the Guest to which the device is assigned. It does this by means of the data structure in the following illustration. This table creates an association between the device's PCI Express* Bus/Device/Function (B/D/F) number and the base address of a translation table. This data structure is populated by a VMM to map devices to translation tables in accordance with the device assignment restrictions above, and to include a multi-level translation table (VT-d Table) that contains Guest specific address translations.

Figure 3-1. Device to Domain Mapping Structures



Intel VT-d functionality, often referred to as an Intel VT-d Engine, has typically been implemented at or near a PCI Express* host bridge component of a computer system. This might be in a chipset component or in the PCI Express functionality of a processor with integrated I/O. When one such VT-d engine receives a PCI Express transaction from a PCI Express bus, it uses the B/D/F number associated with the transaction to search for an Intel VT-d translation table. In doing so, it uses the B/D/F number to traverse the data structure shown in the above figure. If it finds a valid Intel VT-d table in this data structure, it uses that table to translate the address provided on the PCI Express bus. If it does not find a valid translation table for a given translation, this results in an Intel VT-d fault. If Intel VT-d translation is required, the Intel VT-d engine performs an N-level table walk.

For more information, refer to *Intel Virtualization Technology for Directed I/O Architecture Specification* http://www.intel.com/content/dam/www/public/us/en/documents/product-specifications/vt-directed-io-spec.pdf

Intel® VT-d Key Features

The processor supports the following Intel VT-d features:

- Memory controller and processor graphics comply with the Intel VT-d 2.1 Specification.
- Two Intel VT-d DMA remap engines.
  - — iGFX DMA remap engine
  - — Default DMA remap engine (covers all devices except iGFX)
- Support for root entry, context entry, and default context
- 39-bit guest physical address and host physical address widths
- Support for 4K page sizes only
- Support for register-based fault recording only (for single entry only) and support for MSI interrupts for faults
- Support for both leaf and non-leaf caching
- Support for boot protection of default page table
- Support for non-caching of invalid page table entries
- Support for hardware based flushing of translated but pending writes and pending reads, on IOTLB invalidation
- Support for Global, Domain specific and Page specific IOTLB invalidation
- MSI cycles (MemWr to address FEEx_xxxxh) not translated
  - — Translation faults result in cycle forwarding to VBIOS region (byte enables masked for writes). Returned data may be bogus for internal agents, PEG/DMI interfaces return unsupported request status
- Interrupt Remapping is supported
- Queued invalidation is supported
- Intel VT-d translation bypass address range is supported (Pass Through)

The processor supports the following added new Intel VT-d features:

- 4-level Intel VT-d Page walk – both default Intel VT-d engine as well as the IGD VT-d engine are upgraded to support 4-level Intel VT-d tables (adjusted guest address width of 48 bits)

- Intel VT-d superpage – support of Intel VT-d superpage (2 MB, 1 GB) for default Intel VT-d engine (that covers all devices except IGD)
  IGD Intel VT-d engine does not support superpage and BIOS should disable superpage in default Intel VT-d engine when iGfx is enabled.

Note: Intel VT-d Technology may not be available on all SKUs.

3.2 Security Technologies

3.2.1 Intel® Trusted Execution Technology (Intel® TXT)

Intel® Trusted Execution Technology (Intel® TXT) defines platform-level enhancements that provide the building blocks for creating trusted platforms.

The Intel TXT platform helps to provide the authenticity of the controlling environment such that those wishing to rely on the platform can make an appropriate trust decision. The Intel TXT platform determines the identity of the controlling environment by accurately measuring and verifying the controlling software.

Another aspect of the trust decision is the ability of the platform to resist attempts to change the controlling environment. The Intel TXT platform will resist attempts by software processes to change the controlling environment or bypass the bounds set by the controlling environment.

Intel TXT is a set of extensions designed to provide a measured and controlled launch of system software that will then establish a protected environment for itself and any additional software that it may execute.

These extensions enhance two areas:

- The launching of the Measured Launched Environment (MLE).
- The protection of the MLE from potential corruption.

The enhanced platform provides these launch and control interfaces using Safer Mode Extensions (SMX).

The SMX interface includes the following functions:

- Measured/Verified launch of the MLE.
- Mechanisms to ensure the above measurement is protected and stored in a secure location.
- Protection mechanisms that allow the MLE to control attempts to modify itself.

The processor also offers additional enhancements to System Management Mode (SMM) architecture for enhanced security and performance. The processor provides new MSRs to:

- Enable a second SMM range
- Enable SMM code execution range checking
- Select whether SMM Save State is to be written to legacy SMRAM or to MSRs
- Determine if a thread is going to be delayed entering SMM
- Determine if a thread is blocked from entering SMM
- Targeted SMI, enable/disable threads from responding to SMIs, both VLWs and IPI

For the above features, BIOS should test the associated capability bit before attempting to access any of the above registers.

For more information, refer to the *Intel® Trusted Execution Technology Measured Launched Environment Programming Guide*

Note: Intel TXT Technology may not be available on all SKUs.

3.2.2 Intel® Advanced Encryption Standard New Instructions (Intel® AES-NI)

The processor supports Intel Advanced Encryption Standard New Instructions (Intel AES-NI) that are a set of Single Instruction Multiple Data (SIMD) instructions that enable fast and secure data encryption and decryption based on the Advanced Encryption Standard (AES). Intel AES-NI are valuable for a wide range of cryptographic applications, such as applications that perform bulk encryption/decryption, authentication, random number generation, and authenticated encryption. AES is broadly accepted as the standard for both government and industry applications, and is widely deployed in various protocols.

Intel AES-NI consists of six Intel SSE instructions. Four instructions, AESENC, AESENCLAST, AESDEC, and AESDELAST facilitate high performance AES encryption and decryption. The other two, AESIMC and AESKEYGENASSIST, support the AES key expansion procedure. Together, these instructions provide full hardware for supporting AES; offering security, high performance, and a great deal of flexibility.

Note: Intel AES-NI Technology may not be available on all SKUs.

3.2.3 PCLMULQDQ (Perform Carry-Less Multiplication Quad word) Instruction

The processor supports the carry-less multiplication instruction, PCLMULQDQ. PCLMULQDQ is a Single Instruction Multiple Data (SIMD) instruction that computes the 128-bit carry-less multiplication of two 64-bit operands without generating and propagating carries. Carry-less multiplication is an essential processing component of several cryptographic systems and standards. Hence, accelerating carry-less multiplication can significantly contribute to achieving high speed secure computing and communication.

3.2.4 Intel® Secure Key

The processor supports Intel Secure Key (formerly known as Digital Random Number Generator (DRNG)), a software visible random number generation mechanism supported by a high quality entropy source. This capability is available to programmers through the RDRAND instruction. The resultant random number generation capability is designed to comply with existing industry standards in this regard (ANSI X9.82 and NIST SP 800-90).

Some possible usages of the RDRAND instruction include cryptographic key generation as used in a variety of applications, including communication, digital signatures, secure storage, and so on.

3.2.5 Execute Disable Bit

The Execute Disable Bit allows memory to be marked as non executable when combined with a supporting operating system. If code attempts to run in non-executable memory, the processor raises an error to the operating system. This feature can prevent some classes of viruses or worms that exploit buffer overrun vulnerabilities and can, thus, help improve the overall security of the system.

See the *Intel 64 and IA-32 Architectures Software Developer's Manuals* for more detailed information.

3.2.6 Boot Guard Technology

Boot Guard technology is a part of boot integrity protection technology. Boot Guard can help protect the platform boot integrity by preventing execution of unauthorized boot blocks. With Boot Guard, platform manufacturers can create boot policies such that invocation of an unauthorized (or untrusted) boot block will trigger the platform protection per the manufacturer's defined policy.

With verification based in the hardware, Boot Guard extends the trust boundary of the platform boot process down to the hardware level.

Boot Guard accomplishes this by:

- Providing of hardware-based Static Root of Trust for Measurement (S-RTM) and the Root of Trust for Verification (RTV) using Intel architectural components.
- Providing of architectural definition for platform manufacturer Boot Policy.
- Enforcing of manufacture provided Boot Policy using Intel architectural components.

Benefits of this protection is that Boot Guard can help maintain platform integrity by preventing re-purposing of the manufacturer's hardware to run an unauthorized software stack.

3.2.7 Intel® Supervisor Mode Execution Protection (SMEP)

Intel® Supervisor Mode Execution Protection (SMEP) is a mechanism that provides the next level of system protection by blocking malicious software attacks from user mode code when the system is running in the highest privilege level. This technology helps to protect from virus attacks and unwanted code from harming the system. For more information, refer to *Intel® 64 and IA-32 Architectures Software Developer's Manual, Volume 3A* at: http://www.intel.com/Assets/PDF/manual/253668.pdf

3.2.8 Intel® Supervisor Mode Access Protection (SMAP)

Intel® Supervisor Mode Access Protection (SMAP) is a mechanism that provides next level of system protection by blocking a malicious user from tricking the operating system into branching off user data. This technology shuts down very popular attack vectors against operating systems.

For more information, refer to the *Intel ® 64 and IA-32 Architectures Software Developer's Manual, Volume 3A*: http://www.intel.com/Assets/PDF/manual/253668.pdf

3.2.9 Intel® Memory Protection Extensions (Intel® MPX)

Intel® MPX provides hardware accelerated mechanism for memory testing (heap and stack) buffer boundaries in order to identify buffer overflow attacks.

An Intel MPX enabled compiler inserts new instructions that tests memory boundaries prior to a buffer access. Other Intel MPX commands are used to modify a database of memory regions used by the boundary checker instructions.

The Intel MPX ISA is designed for backward compatibility and will be treated as no-operation instructions (NOPs) on older processors.

Intel MPX can be used for:

- Efficient runtime memory boundary checks for security-sensitive portions of the application.
- As part of a memory checker tool for finding difficult memory access errors. Intel MPX is significantly of magnitude faster than software implementations.

Intel MPX emulation (without hardware acceleration) is available with the Intel C++ Compiler 13.0 or newer.

For more information, refer to the Intel MPX documentation.

3.2.10 Intel® Software Guard Extensions (Intel® SGX)

Software Guard Extensions (SGX) is a processor enhancement designed to help protect application integrity and confidentiality of secrets and withstands software and certain hardware attacks.

Software Guard Extensions (SGX) creates and operates in protected regions of memory named Enclaves.

Enclave code can be accessed using new special ISA commands that jump into per Enclave predefined addresses. Data within an Enclave can only be accessed from that same Enclave code.

The latter security statements hold under all privilege levels including supervisor mode (ring-0), System Management Mode (SMM) and other Enclaves.

Software Guard Extensions (SGX) features a memory encryption engine that both encrypt Enclave memory as well as protect it from corruption and replay attacks.

Software Guard Extensions (SGX) benefits over alternative Trusted Execution Environments (TEEs) are:

- Enclaves are written using C/C++ using industry standard build tools.
- High processing power as they run on the processor.
- Large amount of memory are available as well as non-volatile storage (such as disk drives).
- Simple to maintain and debug using standard IDEs (Integrated Development Environment)
- Scalable to a larger number of applications and vendors running concurrently

For more information, refer to the Intel® SGX Website.

3.2.11 Intel® Virtualization Technology (Intel® VT) for Directed I/O (Intel® VT-d)

Refer to Section 3.1.2, "Intel® Virtualization Technology (Intel® VT) for Directed I/O (Intel® VT-d)" Intel VT-d for detail.

3.3 Power and Performance Technologies

3.3.1 Intel® Hyper-Threading Technology (Intel® HT Technology)

The processor supports Intel® Hyper-Threading Technology (Intel® HT Technology) that allows an execution processor IA core to function as two logical processors. While some execution resources such as caches, execution units, and buses are shared, each logical processor has its own architectural state with its own set of general-purpose registers and control registers. This feature should be enabled using the BIOS and requires operating system support.

Note: Intel HT Technology may not be available on all SKUs.

3.3.2 Intel® Turbo Boost Technology 2.0

The Intel® Turbo Boost Technology 2.0 allows the processor IA core / processor graphics core to opportunistically and automatically run faster than the processor IA core base frequency / processor graphics base frequency if it is operating below power, temperature, and current limits. The Intel Turbo Boost Technology 2.0 feature is designed to increase performance of both multi-threaded and single-threaded workloads.

Compared with previous generation products, Intel Turbo Boost Technology 2.0 will increase the ratio of application power towards TDP and also allows to increase power above TDP as high as PL2 for short periods of time. Thus, thermal solutions and platform cooling that are designed to less than thermal design guidance might experience thermal and performance issues since more applications will tend to run at the maximum power limit for significant periods of time.

Note: Intel Turbo Boost Technology 2.0 may not be available on all SKUs.

3.3.2.1 Intel® Turbo Boost Technology 2.0 Frequency

To determine the highest performance frequency amongst active processor IA cores, the processor takes the following into consideration:

- The number of processor IA cores operating in the C0 state.
- The estimated processor IA core current consumption and I_{CCMax} register settings.
- The estimated package prior and present power consumption and turbo power limits.
- The package temperature.
- Sustained turbo residencies at high voltages and temperature.

Any of these factors can affect the maximum frequency for a given workload. If the power, current, Voltage or thermal limit is reached, the processor will automatically reduce the frequency to stay within the PL1 value. Turbo processor frequencies are only active if the operating system is requesting the P0 state. If turbo frequencies are limited the cause is logged in IA_PERF_LIMIT_REASONS register. For more information on P-states and C-states, see Chapter 4, “Power Management”.

3.3.3 Intel® Advanced Vector Extensions 2 (Intel® AVX2)

Intel® Advanced Vector Extensions 2.0 (Intel® AVX2) is the latest expansion of the Intel instruction set. Intel AVX2 extends the Intel Advanced Vector Extensions (Intel AVX) with 256-bit integer instructions, floating-point fused multiply add (FMA) instructions, and gather operations. The 256-bit integer vectors benefit math, codec, image, and digital signal processing software. FMA improves performance in face detection, professional imaging, and high performance computing. Gather operations increase vectorization opportunities for many applications. In addition to the vector extensions, this generation of Intel processors adds new bit manipulation instructions useful in compression, encryption, and general purpose software.
For more information on Intel AVX, see http://www.intel.com/software/avx

Intel Advanced Vector Extensions (Intel AVX) are designed to achieve higher throughput to certain integer and floating point operation. Due to varying processor power characteristics, utilizing AVX instructions may cause a) parts to operate below the base frequency b) some parts with Intel Turbo Boost Technology 2.0 to not achieve any or maximum turbo frequencies. Performance varies depending on hardware, software and system configuration and you should consult your system manufacturer for more information. Intel Advanced Vector Extensions refers to Intel AVX, Intel AVX2 or Intel AVX-512.
For more information on Intel AVX, see http://www-ssl.intel.com/content/www/us/en/architecture-and-technology/turbo-boost/turbo-boost-technology.html

Note: Intel AVX2 Technology may not be available on all SKUs.

3.3.4 Intel® 64 Architecture x2APIC

The x2APIC architecture extends the xAPIC architecture that provides key mechanisms for interrupt delivery. This extension is primarily intended to increase processor addressability.

Specifically, x2APIC:

- Retains all key elements of compatibility to the xAPIC architecture:
  - — Delivery modes
  - — Interrupt and processor priorities
  - — Interrupt sources
  - — Interrupt destination types
- Provides extensions to scale processor addressability for both the logical and physical destination modes
- Adds new features to enhance performance of interrupt delivery
- Reduces complexity of logical destination mode interrupt delivery on link based architectures

The key enhancements provided by the x2APIC architecture over xAPIC are the following:

- Support for two modes of operation to provide backward compatibility and extensibility for future platform innovations:
  - In xAPIC compatibility mode, APIC registers are accessed through memory mapped interface to a 4K-Byte page, identical to the xAPIC architecture.
  - In x2APIC mode, APIC registers are accessed through Model Specific Register (MSR) interfaces. In this mode, the x2APIC architecture provides significantly increased processor addressability and some enhancements on interrupt delivery.
- Increased range of processor addressability in x2APIC mode:
  - Physical xAPIC ID field increases from 8 bits to 32 bits, allowing for interrupt processor addressability up to 4G-1 processors in physical destination mode. A processor implementation of x2APIC architecture can support fewer than 32-bits in a software transparent fashion.
  - Logical xAPIC ID field increases from 8 bits to 32 bits. The 32-bit logical x2APIC ID is partitioned into two sub-fields – a 16-bit cluster ID and a 16-bit logical ID within the cluster. Consequently, ((2^20) - 16) processors can be addressed in logical destination mode. Processor implementations can support fewer than 16 bits in the cluster ID sub-field and logical ID sub-field in a software agnostic fashion.
- More efficient MSR interface to access APIC registers:
  - To enhance inter-processor and self-directed interrupt delivery as well as the ability to virtualize the local APIC, the APIC register set can be accessed only through MSR-based interfaces in x2APIC mode. The Memory Mapped IO (MMIO) interface used by xAPIC is not supported in x2APIC mode.
- The semantics for accessing APIC registers have been revised to simplify the programming of frequently-used APIC registers by system software. Specifically, the software semantics for using the Interrupt Command Register (ICR) and End Of Interrupt (EOI) registers have been modified to allow for more efficient delivery and dispatching of interrupts.
- The x2APIC extensions are made available to system software by enabling the local x2APIC unit in the “x2APIC” mode. To benefit from x2APIC capabilities, a new operating system and a new BIOS are both needed, with special support for x2APIC mode.
- The x2APIC architecture provides backward compatibility to the xAPIC architecture and forward extendible for future Intel platform innovations.

Note: Intel x2APIC Technology may not be available on all SKUs.

For more information, see the Intel® *64 Architecture x2APIC Specification* at http://www.intel.com/products/processor/manuals/.

3.3.5 Power Aware Interrupt Routing (PAIR)

The processor includes enhanced power-performance technology that routes interrupts to threads or processor IA cores based on their sleep states. As an example, for energy savings, it routes the interrupt to the active processor IA cores without waking the deep idle processor IA cores. For performance, it routes the interrupt to the idle (C1) processor IA cores without interrupting the already heavily loaded processor IA cores. This enhancement is mostly beneficial for high-interrupt scenarios like Gigabit LAN, WLAN peripherals, and so on.

3.3.6 Intel® Transactional Synchronization Extensions (Intel® TSX-NI)

Intel® Transactional Synchronization Extensions (Intel® TSX-NI) provides a set of instruction set extensions that allow programmers to specify regions of code for transactional synchronization. Programmers can use these extensions to achieve the performance of fine-grain locking while actually programming using coarse-grain locks. Details on Intel TSX-NI may be found in *Intel® Architecture Instruction Set Extensions Programming Reference.*Intel TSX-NI may not be available on all SKUs.Intel® Image Signal Processor (Intel® ISP)

Platform Imaging Infrastructure

Note: Intel TSX-NI may not be available on all SKUs.

The imaging infrastructure is based on a number of hardware components as shown in Figure 3-3, "Platform Imaging Infrastructure". The three major components of the system are:

- **Camera SubSystem:** Located in the lid of the system and contains CMOS sensor, flash, LED, I/O interface (MIPI* CSI-2 and I^2C*), Focus control and other components.
- **Camera I/O controller:** The I/O controller is located in the PCH and contains a MIPI-CSI2 Host controller. The host controller is a PCI device (independent of the ISP device). The CSI-2 HCI brings imaging data from an external imager into the system and provides a command and control channel for the imager using I^2C.
- **Intel ISP (Image Signal Processor):** The ISP processes the images captured by Bayer sensors to be used by still or video applications (such as, JPEG, H.264, and so on).

Figure 3-2. Processor Camera System

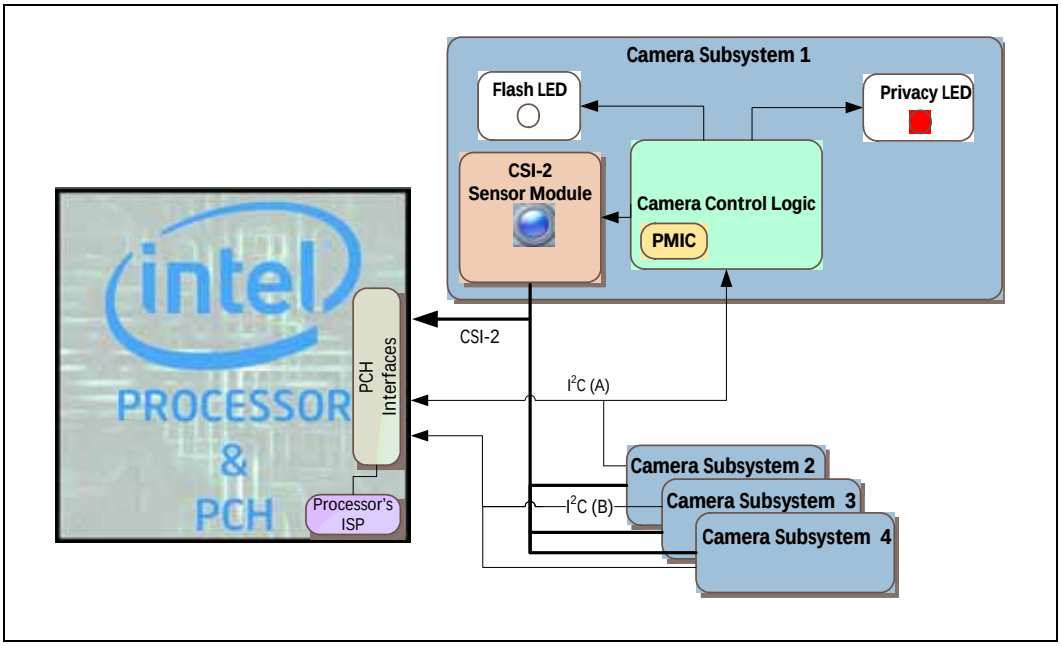
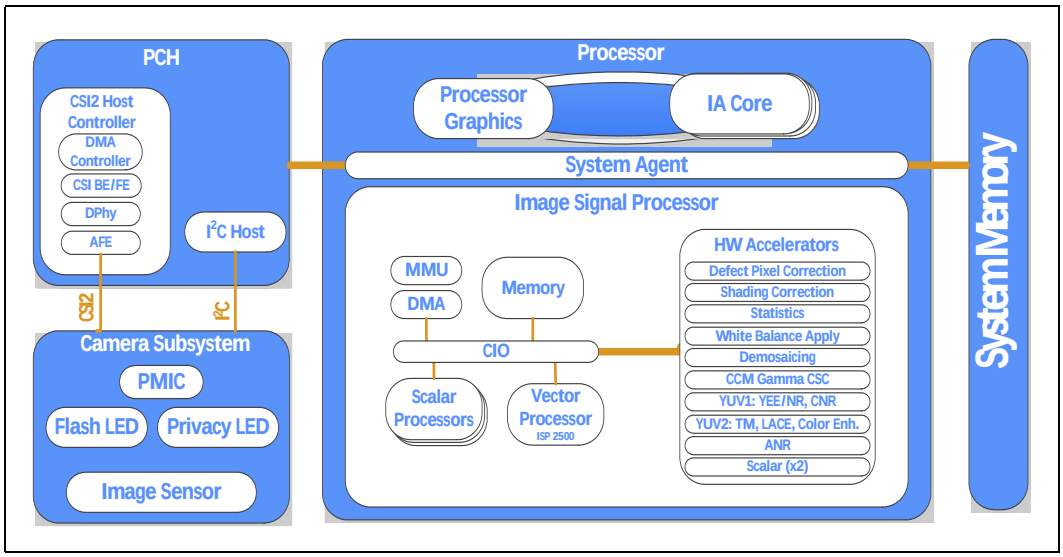


Figure 3-3. Platform Imaging Infrastructure



3.3.7 Intel® Image Signal Processor (Intel® ISP)

The Intel ISP is an embedded camera subsystem hardware component on the processor, it processes video and still images at high quality with a low-power cost by leveraging a programmable VLIW (very-long-instruction-word) SIMD vector processor, a hardware fixed function pipe (accelerators), two scalar processor, and more. The mix of hardware accelerators and compute capabilities allows the flexibility and patchability that are required for late changes and allowing the unit to support future sensor technologies while remaining in an optimized power performance point.

3.4 Debug Technologies

3.4.1 Intel® Processor Trace

Intel® Processor Trace (Intel® PT) is a new tracing capability added to Intel Architecture, for use in software debug and profiling. Intel PT provides the capability for more precise software control flow and timing information, with limited impact to software execution. This provides enhanced ability to debug software crashes, hangs, or other anomalies, as well as responsiveness and short-duration performance issues.

Intel VTune™ Amplifier for Systems and the Intel System Debugger are part of Intel System Studio 2015, which includes updates for new debug and trace features on this latest platform, including Intel PT and Intel Trace Hub.

4 Power Management

This chapter provides information on the following power management topics:

- Advanced Configuration and Power Interface (ACPI) States
- Processor IA Core Power Management
- Integrated Memory Controller (IMC) Power Management
- Processor Graphics Power Management

Figure 4-1. Processor Power States

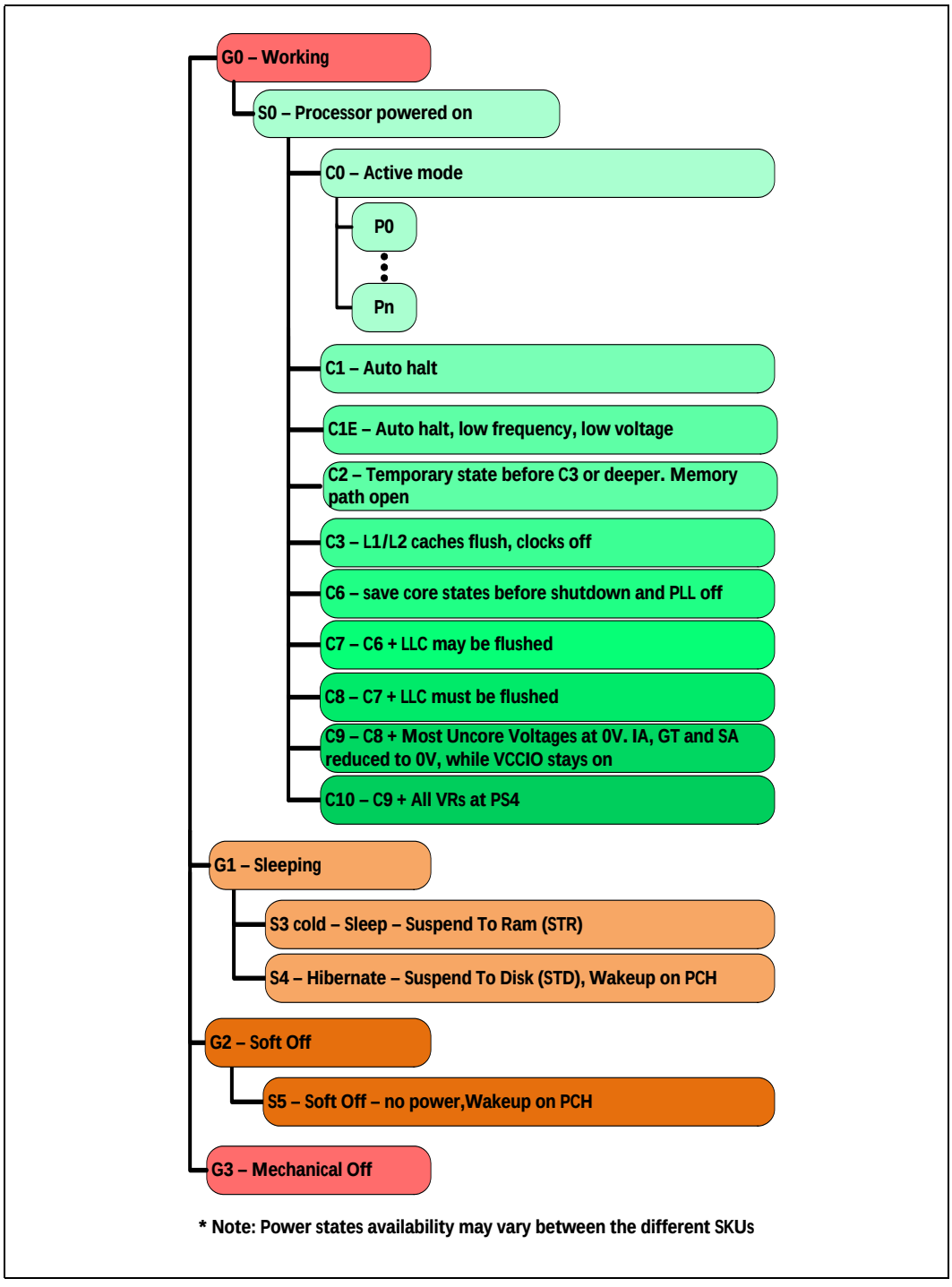
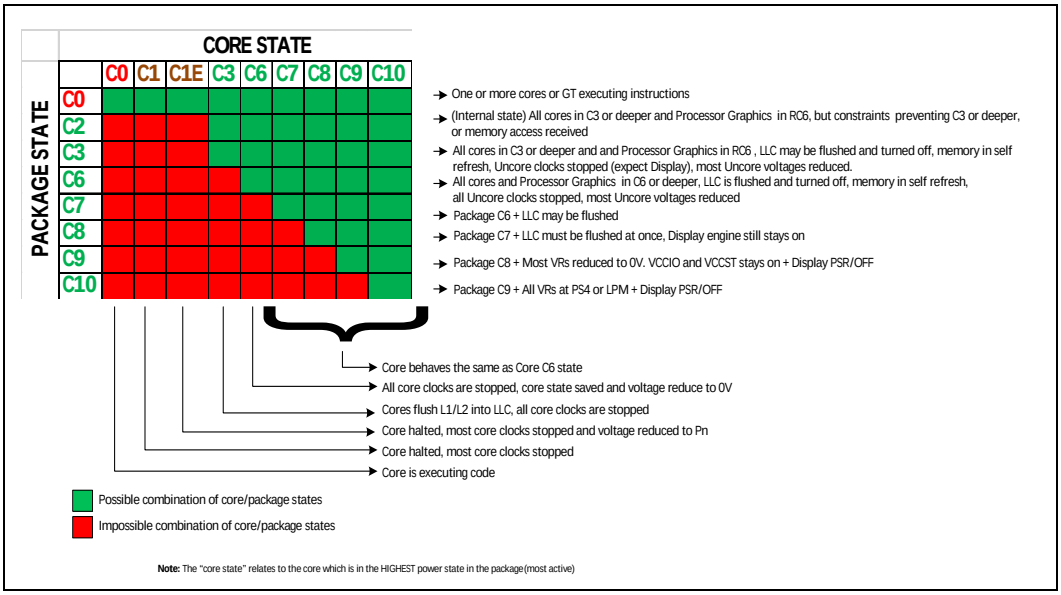


Figure 4-2. Processor Package and IA Core C-States



Note: If the Platform does not support Modern Standby (Previously known as Connected Standby) and does not support PS4, it is recommended to limit the package state to package C9 (Better power).

4.1 Advanced Configuration and Power Interface (ACPI) States Supported

This section describes the ACPI states supported by the processor.

Table 4-1. System States

State	Description
G0/S0	Full On
G1/S3-Cold	Suspend-to-RAM (STR). Context saved to memory (S3-Hot is not supported by the processor).
G1/S4	Suspend-to-Disk (STD). All power lost (except wake-up on PCH).
G2/S5	Soft off. All power lost (except wake-up on PCH). Total reboot.
G3	Mechanical off. All power removed from system.

Table 4-2. Processor IA Core / Package State Support

State	Description
C0	Active mode, processor executing code.
C1	AutoHALT processor IA core state (package C0 state).
C1E	AutoHALT processor IA core state with lowest frequency and voltage operating point (package C0 state).
C2	All processor IA cores in C3 or deeper. Memory path open. Temporary state before Package C3 or deeper.
C3	Processor IA execution cores in C3 or deeper, flush their L1 instruction cache, L1 data cache, and L2 cache to the LLC shared cache. LLC may be flushed. Clocks are shut off to each core.
C6	Processor IA execution cores in this state save their architectural state before removing core voltage. BCLK is off.
C7	Processor IA execution cores in this state behave similarly to the C6 state. If all execution cores request C7, LLC ways may be flushed until it is cleared. If the entire LLC is flushed, voltage will be removed from the LLC.
C8	C7 plus LLC should be flushed.
C9	C8 plus most Uncore voltages at 0V. IA, GT and SA reduced to 0V, while Vcc_{IO} stays on.
C10	C9 plus all VRs at PS4 or LPM. 24 MHz clock off

Table 4-3. Integrated Memory Controller (IMC) States

State	Description
Power up	CKE asserted. Active mode.
Pre-charge Power down	CKE de-asserted (not self-refresh) with all banks closed.
Active Power down	CKE de-asserted (not self-refresh) with minimum one bank active.
Self-Refresh	CKE de-asserted using device self-refresh.

Table 4-4. PCI Express* Link States

State	Description
L0	Full on – Active transfer state.
L1	Lowest Active Power Management – Longer exit latency
L3	Lowest power state (power-off) – Longest exit latency

Table 4-5. Direct Media Interface (DMI) States

State	Description
L0	Full on – Active transfer state
L1	Lowest Active Power Management – Longer exit latency
L3	Lowest power state (power-off) – Longest exit latency

Table 4-6. G, S, and C Interface State Combinations

Global (G) State	Sleep (S) State	Processor Package (C) State	Processor State	System Clocks	Description
G0	S0	C0	Full On	On	Full On
G0	S0	C1/C1E	Auto-Halt	On	Auto-Halt
G0	S0	C3	Deep Sleep	On	Deep Sleep
G0	S0	C6/C7	Deep Power Down	On	Deep Power Down
G0	S0	C8/C9/C10	Off	On	Deeper Power Down
G1	S3	Power off	Off	Off, except RTC	Suspend to RAM
G1	S4	Power off	Off	Off, except RTC	Suspend to Disk
G2	S5	Power off	Off	Off, except RTC	Soft Off
G3	N/A	Power off	Off	Power off	Hard off

4.2 Processor IA Core Power Management

While executing code, Enhanced Intel SpeedStep Technology and Intel Speed Shift® Technology optimizes the processor's IA core frequency and voltage based on workload. Each frequency and voltage operating point is defined by ACPI as a P-state. When the processor is not executing code, it is idle. A low-power idle state is defined by ACPI as a C-state. In general, deeper power C-states have longer entry and exit latencies.

4.2.1 OS/HW controlled P-states

4.2.1.1 Enhanced Intel® SpeedStep® Technology

Enhanced Intel® SpeedStep® Technology enables OS to control and select P-state. The following are the key features of Enhanced Intel SpeedStep Technology:

- Multiple frequency and voltage points for optimal performance and power efficiency. These operating points are known as P-states.
- Frequency selection is software controlled by writing to processor MSRs. The voltage is optimized based on the selected frequency and the number of active processor IA cores.
  - Once the voltage is established, the PLL locks on to the target frequency.
  - All active processor IA cores share the same frequency and voltage. In a multi-core processor, the highest frequency P-state requested among all active IA cores is selected.
  - Software-requested transitions are accepted at any time. If a previous transition is in progress, the new transition is deferred until the previous transition is completed.
- The processor controls voltage ramp rates internally to ensure glitch-free transitions.
- Because there is low transition latency between P-states, a significant number of transitions per-second are possible.

4.2.1.2 Intel® Speed Shift Technology

Intel Speed Shift Technology is an energy efficient method of frequency control by the hardware rather than relying on OS control. OS is aware of available hardware P-states and request a desired P-state or it can let Hardware determine the P-state. The OS request is based on its workload requirements and awareness of processor capabilities. Processor decision is based on the different system constraints for example: Workload demand, thermal limits while taking into consideration the minimum and maximum levels and activity window of performance requested by the operating system.

For more details, refer to the following document (see related documents section):

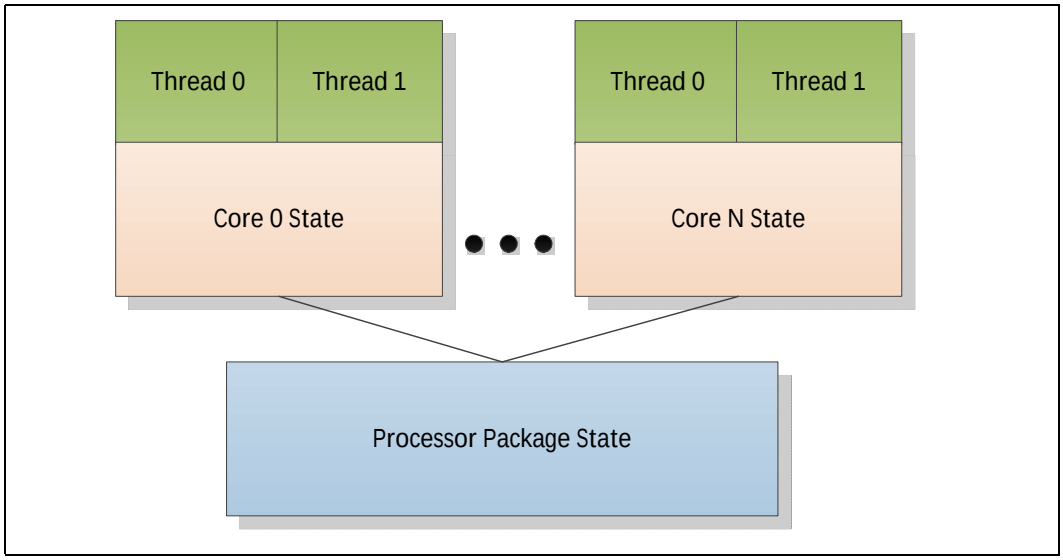
- Intel® 64 and IA-32 Architectures Software Developer's Manual (SDM), volume 3B.

4.2.2 Low-Power Idle States

When the processor is idle, low-power idle states (C-states) are used to save power. More power savings actions are taken for numerically higher C-states. However, deeper C-states have longer exit and entry latencies. Resolution of C-states occur at the thread, processor IA core, and processor package level. Thread-level C-states are available if Intel Hyper-Threading Technology is enabled.

Caution: Long term reliability cannot be assured unless all the Low-Power Idle States are enabled.

Figure 4-3. Idle Power Management Breakdown of the Processor IA Cores



While individual threads can request low-power C-states, power saving actions only take place once the processor IA core C-state is resolved. processor IA core C-states are automatically resolved by the processor. For thread and processor IA core C-states, a transition to and from C0 state is required before entering any other C-state.

4.2.3 Requesting Low-Power Idle States

The primary software interfaces for requesting low-power idle states are through the MWAIT instruction with sub-state hints and the HLT instruction (for C1 and C1E). However, software may make C-state requests using the legacy method of I/O reads from the ACPI-defined processor clock control registers, referred to as P_LVLx. This method of requesting C-states provides legacy support for operating systems that initiate C-state transitions using I/O reads.

For legacy operating systems, P_LVLx I/O reads are converted within the processor to the equivalent MWAIT C-state request. Therefore, P_LVLx reads do not directly result in I/O reads to the system. The feature, known as I/O MWAIT redirection, should be enabled in the BIOS.

The BIOS can write to the C-state range field of the PMG_IO_CAPTURE MSR to restrict the range of I/O addresses that are trapped and emulate MWAIT like functionality. Any P_LVLx reads outside of this range do not cause an I/O redirection to MWAIT(Cx) like request. They fall through like a normal I/O instruction.

When P_LVLx I/O instructions are used, MWAIT sub-states cannot be defined. The MWAIT sub-state is always zero if I/O MWAIT redirection is used. By default, P_LVLx I/O redirections enable the MWAIT 'break on EFLAGS.IF' feature that triggers a wake up on an interrupt, even if interrupts are masked by EFLAGS.IF.

4.2.4 Processor IA Core C-State Rules

The following are general rules for all processor IA core C-states, unless specified otherwise:

- A processor IA core C-State is determined by the lowest numerical thread state (such as Thread 0 requests C1E while Thread 1 requests C3 state, resulting in a processor IA core C1E state). See the *G, S, and C Interface State Combinations* table.
- A processor IA core transitions to C0 state when:
  - An interrupt occurs
  - There is an access to the monitored address if the state was entered using an MWAIT/Timed MWAIT instruction
  - The deadline corresponding to the Timed MWAIT instruction expires
- An interrupt directed toward a single thread wakes up only that thread.
- If any thread in a processor IA core is active (in C0 state), the core's C-state will resolve to C0.
- Any interrupt coming into the processor package may wake any processor IA core.
- A system reset re-initializes all processor IA cores.

processor IA core C0 State

The normal operating state of a processor IA core where code is being executed.

processor IA core C1/C1E State

C1/C1E is a low-power state entered when all threads within a processor IA core execute a HLT or MWAIT(C1/C1E) instruction.

A System Management Interrupt (SMI) handler returns execution to either Normal state or the C1/C1E state. See the *Intel 64 and IA-32 Architectures Software Developer's Manual* for more information.

While a processor IA core is in C1/C1E state, it processes bus snoops and snoops from other threads. For more information on C1E, see Section 4.2.5, "Package C-States".

processor IA core C3 State

Individual threads of a processor IA core can enter the C3 state by initiating a P_LVL2 I/O read to the P_BLK or an MWAIT(C3) instruction. A processor IA core in C3 state flushes the contents of its L1 instruction cache, L1 data cache, and L2 cache to the shared LLC, while maintaining its architectural state. All processor IA core clocks are stopped at this point. Because the processor IA core's caches are flushed, the processor does not wake any processor IA core that is in the C3 state when either a snoop is detected or when another processor IA core accesses cacheable memory.

processor IA core C6 State

Individual threads of a processor IA core can enter the C6 state by initiating a P_LVL3 I/O read or an MWAIT(C6) instruction. Before entering processor IA core C6 state, the processor IA core will save its architectural state to a dedicated SRAM. Once complete, a processor IA core will have its voltage reduced to zero volts. During exit, the processor IA core is powered on and its architectural state is restored.

processor IA core C7-C10 States

Individual threads of a processor IA core can enter the C7, C8, C9, or C10 state by initiating a P_LVL4, P_LVL5, P_LVL6, P_LVL7 I/O read (respectively) to the P_BLK or by an MWAIT(C7/C8/C9/C10) instruction. The processor IA core C7-C10 state exhibits the same behavior as the processor IA core C6 state.

C-State Auto-Demotion

In general, deeper C-states, such as C6 or C7, have long latencies and have higher energy entry/exit costs. The resulting performance and energy penalties become significant when the entry/exit frequency of a deeper C-state is high. Therefore, incorrect or inefficient usage of deeper C-states have a negative impact on battery life and idle power. To increase residency and improve battery life and idle power in deeper C-states, the processor supports C-state auto-demotion.

There are two C-State auto-demotion options:

- C7/C6 to C3
- C7/C6/C3 To C1

The decision to demote a processor IA core from C6/C7 to C3 or C3/C6/C7 to C1 is based on each processor IA core's immediate residency history. Upon each processor IA core C6/C7 request, the processor IA core C-state is demoted to C3 or C1 until a sufficient amount of residency has been established. At that point, a processor IA core is allowed to go into C3/C6 or C7. Each option can be run concurrently or individually. If the interrupt rate experienced on a processor IA core is high and the processor IA core is rarely in a deep C-state between such interrupts, the processor IA core can be demoted to a C3 or C1 state. A higher interrupt pattern is required to demote a processor IA core to C1 as compared to C3.

This feature is disabled by default. BIOS should enable it in the PMG_CST_CONFIG_CONTROL register. The auto-demotion policy is also configured by this register.

4.2.5 Package C-States

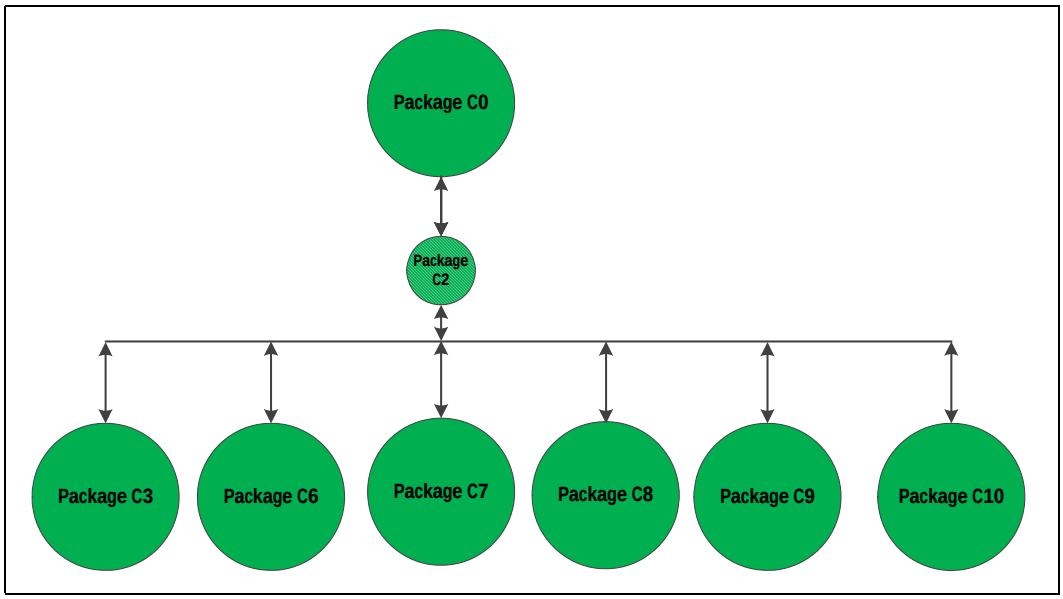
The processor supports C0, C2, C3, C6, C7, C8, C9, and C10 package states. The following is a summary of the general rules for package C-state entry. These apply to all package C-states, unless specified otherwise:

- A package C-state request is determined by the lowest numerical processor IA core C-state amongst all processor IA cores.
- A package C-state is automatically resolved by the processor depending on the processor IA core idle power states and the status of the platform components.
  - Each processor IA core can be at a lower idle power state than the package if the platform does not grant the processor permission to enter a requested package C-state.
  - The platform may allow additional power savings to be realized in the processor.
  - For package C-states, the processor is not required to enter C0 before entering any other C-state.
  - Entry into a package C-state may be subject to auto-demotion – that is, the processor may keep the package in a deeper package C-state then requested by the operating system if the processor determines, using heuristics, that the deeper C-state results in better power/performance.

The processor exits a package C-state when a break event is detected. Depending on the type of break event, the processor does the following:

- If a processor IA core break event is received, the target processor IA core is activated and the break event message is forwarded to the target processor IA core.
  - If the break event is not masked, the target processor IA core enters the processor IA core C0 state and the processor enters package C0.
  - If the break event is masked, the processor attempts to re-enter its previous package state.
- If the break event was due to a memory access or snoop request,
  - But the platform did not request to keep the processor in a higher package C-state, the package returns to its previous C-state.
  - And the platform requests a higher power C-state, the memory access or snoop request is serviced and the package remains in the higher power C-state.

Figure 4-4. Package C-State Entry and Exit



Package C0

This is the normal operating state for the processor. The processor remains in the normal state when at least one of its processor IA cores is in the C0 or C1 state or when the platform has not granted permission to the processor to go into a low-power state. Individual processor IA cores may be in deeper power idle states while the package is in C0 state.

Package C2 State

Package C2 state is an internal processor state that cannot be explicitly requested by software. A processor enters Package C2 state when either:

- All processor IA cores have requested a C3 or deeper power state and all graphics processor IA cores requested are in RC6, but constraints (LTR, programmed timer events in the near future, and so forth) prevent entry to any state deeper than C2 state.
- Or, all processor IA cores have requested a C3 or deeper power state and all graphics processor IA cores requested are in RC6 and a memory access request is received. Upon completion of all outstanding memory requests, the processor transitions back into a deeper package C-state.

Package C3 State

A processor enters the package C3 low-power state when:

- At least one processor IA core is in the C3 state.
- The other processor IA cores are in a C3 or deeper power state, and the processor has been granted permission by the platform.
- The platform has not granted a request to a package C6/C7 state or deeper state but has allowed a package C3 state.

In package C3-state, the LLC shared cache is valid.

Package C6 State

A processor enters the package C6 low-power state when:

- At least one processor IA core is in the C6 state.
- The other processor IA cores are in a C6 or deeper power state, and the processor has been granted permission by the platform.
- The platform has not granted a package C7 or deeper request but has allowed a C6 package state.

In package C6 state, all processor IA cores have saved their architectural state and have had their voltages reduced to zero volts. It is possible the LLC shared cache is flushed and turned off in package C6 state.

Package C7 State

The processor enters the package C7 low-power state when all processor IA cores are in the C7 or deeper state and the operating system may request that the LLC will be flushed.

processor IA core break events are handled the same way as in package C3 or C6.

Upon exit of the package C7 state, the LLC will be partially enabled once a processor IA core wakes up if it was fully flushed, and will be fully enabled once the processor has stayed out of C7 for a preset amount of time. Power is saved since this prevents the LLC from being re-populated only to be immediately flushed again. Some VRs are reduce to 0V.

Package C8 State

The processor enters C8 states when the processor IA cores lower numerical state is C8.

The C8 state is similar to C7 state, but in addition, the LLC is flushed in a single step, Vcc and Vcc_{GT} are reduced to 0V. The display engine stays on.

Package C9 State

The processor enters C9 states when the processor IA cores lower numerical state is C9.

Package C9 state is similar to C8 state; the VRs are off, Vcc, Vcc_{GT} and Vcc_{SA} at 0V, Vcc_{IO} and Vcc_{ST} stays on.

Package C10 State

The processor enters C10 states when the processor IA cores lower numerical state is C10.

Package C10 state is similar to the package C9 state, but in addition the IMVP8 VR is in PS4 low-power state, which is near to shut off of the IMVP8 VR. The Vcc_{IO} is in low-power mode as well.

InstantGo

InstantGo is a platform state. On display time out the OS requests the processor to enter package C10 and platform devices at RTD3 (or disabled) in order to attain low power in idle.

Dynamic LLC Sizing

When all processor IA cores request C7 or deeper C-state, internal heuristics dynamically flushes the LLC. Once the processor IA cores enter a deep C-state, depending on their MWAIT sub-state request, the LLC is either gradually flushed N-ways at a time or flushed all at once. Upon the processor IA cores exiting to C0 state, the LLC is gradually expanded based on internal heuristics.

4.2.6 Package C-States and Display Resolutions

The integrated graphics engine has the frame buffer located in system memory. When the display is updated, the graphics engine fetches display data from system memory. Different screen resolutions and refresh rates have different memory latency requirements. These requirements may limit the deepest Package C-state the processor can enter. Other elements that may affect the deepest Package C-state available are the following:

- Display is on or off
- Single or multiple displays
- Native or non-native resolution
- Panel Self Refresh (PSR) technology

Note: Display resolution is not the only factor influencing the deepest Package C-state the processor can get into. Device latencies, interrupt response latencies, and core C-states are among other factors that influence the final package C-state the processor can enter.

The following table lists display resolutions and deepest available package C-State.The display resolutions are examples using common values for blanking and pixel rate. Actual results will vary. The table shows the deepest possible Package C-state.System workload, system idle, and AC or DC power also affect the deepest possible Package C-state.

Table 4-7. Deepest Package C-State Available (Sheet 1 of 2)

		Y/U Processor Line[1,2]	
Resolution	Number of Displays	PSR Enabled	PSR Disabled
800x600 60Hz	Single	PC10	PC8
1024x768 60Hz	Single	PC10	PC8
1280x1024 60Hz	Single	PC10	PC8
1920x1080 60Hz	Single	PC10	PC8
1920x1200 60Hz	Single	PC10	PC8
1920x1440 60Hz	Single	PC10	PC8
2048x1536 60Hz	Single	PC10	PC8
2560x1600 60Hz	Single	PC10	PC8

Table 4-7. Deepest Package C-State Available (Sheet 2 of 2)

		Y/U Processor Line[1,2]	
Resolution	Number of Displays	PSR Enabled	PSR Disabled
2560x1920 60Hz	Single	PC10	PC8
2880x1620 60Hz	Single	PC10	PC8
2880x1800 60Hz	Single	PC10	PC8
3200x1800 60Hz	Single	PC10	PC8
3200*2000 60Hz	Single	PC10	PC8
3840x2160 60Hz	Single	PC10	PC8
4096x2160 60Hz	Single	PC10	PC8

Notes:
1. All Deep states are with Display ON.
2. The deepest C-state has variance, dependent on various parameters, such software and Platform devices.
3. N/A

4.3 Integrated Memory Controller (IMC) Power Management

The main memory is power managed during normal operation and in low-power ACPI C-states.

4.3.1 Disabling Unused System Memory Outputs

Any system memory (SM) interface signal that goes to a memory in which it is not connected to any actual memory devices (such as SODIMM connector is unpopulated, or is single-sided) is tri-stated. The benefits of disabling unused SM signals are:

- Reduced power consumption.
- Reduced possible overshoot/undershoot signal quality issues seen by the processor I/O buffer receivers caused by reflections from potentially un-terminated transmission lines.

When a given rank is not populated, the corresponding control signals (CLK_P/CLK_N/CKE/ODT/CS) are not driven.

At reset, all rows should be assumed to be populated, until it can be proven that they are not populated. This is due to the fact that when CKE is tri-stated with a DRAMs present, the DRAMs are not ensured to maintain data integrity. CKE tri-state should be enabled by BIOS where appropriate, since at reset all rows should be assumed to be populated.

4.3.2 DRAM Power Management and Initialization

The processor implements extensive support for power management on the memory interface.Each channel drives 4 CKE pins, one per rank.

The CKE is one of the power-saving means. When CKE is off, the internal DDR clock is disabled and the DDR power is reduced. The power-saving differs according to the selected mode and the DDR type used. For more information, refer to the IDD table in the DDR specification.

The processor supports four different types of power-down modes in package C0 state. The different power-down modes can be enabled through configuring PM PDWN configuration register. The type of CKE power-down can be configured through PDWN_mode (bits 15:12) and the idle timer can be configured through PDWN_idle_counter (bits 11:0). The different power-down modes supported are:

- **No power-down** (CKE disable)
- **Active power-down (APD):** This mode is entered if there are open pages when de-asserting CKE. In this mode the open pages are retained. Power-saving in this mode is the lowest. Power consumption of DDR is defined by IDD3P. Exiting this mode is fined by tXP – small number of cycles. For this mode, DRAM DLL should be on.
- **PPD/DLL-off:** In this mode the data-in DLLs on DDR are off. Power-saving in this mode is the best among all power modes. Power consumption is defined by IDD2P. Exiting this mode is defined by tXP, but also tXPDLL (10–20 according to DDR type) cycles until first data transfer is allowed. For this mode, DRAM DLL should be off.
- **Precharged power-down (PPD):** This mode is entered if all banks in DDR are precharged when de-asserting CKE. Power-saving in this mode is intermediate – better than APD, but less than DLL-off. Power consumption is defined by IDD2P. Exiting this mode is defined by tXP. The difference from APD mode is that when waking-up, all page-buffers are empty.) The LPDDR does not have a DLL. As a result, the power savings are as good as PPD/DDL-off but will have lower exit latency and higher performance.

The CKE is determined per rank, whenever it is inactive. Each rank has an idle counter. The idle-counter starts counting as soon as the rank has no accesses, and if it expires, the rank may enter power-down while no new transactions to the rank arrives to queues. The idle-counter begins counting at the last incoming transaction arrival.

It is important to understand that since the power-down decision is per rank, the IMC can find many opportunities to power down ranks, even while running memory intensive applications; the savings are significant (may be few Watts, according to DDR specification). This is significant when each channel is populated with more ranks.

Selection of power modes should be according to power-performance or thermal trade-off of a given system:

- When trying to achieve maximum performance and power or thermal consideration is not an issue: use no power-down
- In a system which tries to minimize power-consumption, try using the deepest power-down mode possible – PPD/DLL-off with a low idle timer value
- In high-performance systems with dense packaging (that is, tricky thermal design) the power-down mode should be considered in order to reduce the heating and avoid DDR throttling caused by the heating.

The default value that BIOS configures in PM PDWN configuration register is 6080 – that is, PPD/DLL-off mode with idle timer of 0x80, or 128 DCLKs. This is a balanced setting with deep power-down mode and moderate idle timer value.

The idle timer expiration count defines the # of DCLKs that a rank is idle that causes entry to the selected power mode. As this timer is set to a shorter time the IMC will have more opportunities to put the DDR in power-down. There is no BIOS hook to set

this register. Customers choosing to change the value of this register can do it by changing it in the BIOS. For experiments, this register can be modified in real time if BIOS does not lock the IMC registers.

4.3.2.1 Initialization Role of CKE

During power-up, CKE is the only input to the SDRAM that has its level recognized (other than the reset pin) once power is applied. It should be driven LOW by the DDR controller to make sure the SDRAM components float DQ and DQS during power-up. CKE signals remain LOW (while any reset is active) until the BIOS writes to a configuration register. Using this method, CKE is ensured to remain inactive for much longer than the specified 200 micro-seconds after power and clocks to SDRAM devices are stable.

4.3.2.2 Conditional Self-Refresh

During S0 idle state, system memory may be conditionally placed into self-refresh state when the processor is in package C3 or deeper power state. Refer to Section 4.4.1.1, "Intel® Rapid Memory Power Management (Intel® RMPM)" for more details on conditional self-refresh with Intel HD Graphics enabled.

When entering the S3 – Suspend-to-RAM (STR) state or S0 conditional self-refresh, the processor IA core flushes pending cycles and then enters SDRAM ranks that are not used by the processor graphics into self-refresh. The CKE signals remain LOW so the SDRAM devices perform self-refresh.

The target behavior is to enter self-refresh for package C3 or deeper power states as long as there are no memory requests to service.

Table 4-8. Targeted Memory State Conditions

State	Memory State with Processor Graphics	Memory State with External Graphics
C0, C1, C1E	Dynamic memory rank power-down based on idle conditions.	Dynamic memory rank power-down based on idle conditions.
C3, C6, C7 or deeper	If the processor graphics engine is idle and there are no pending display requests, then enter self-refresh. Otherwise use dynamic memory rank power-down based on idle conditions.	If there are no memory requests, then enter self-refresh. Otherwise use dynamic memory rank power-down based on idle conditions.
S3	Self-Refresh Mode	Self-Refresh Mode
S4	Memory power-down (contents lost)	Memory power-down (contents lost)

4.3.2.3 Dynamic Power-Down

Dynamic power-down of memory is employed during normal operation. Based on idle conditions, a given memory rank may be powered down. The IMC implements aggressive CKE control to dynamically put the DRAM devices in a power-down state. The processor IA core controller can be configured to put the devices in active power-down (CKE de-assertion with open pages) or precharge power-down (CKE de-assertion with all pages closed). Precharge power-down provides greater power savings but has a bigger performance impact, since all pages will first be closed before putting the devices in power-down mode.

If dynamic power-down is enabled, all ranks are powered up before doing a refresh cycle and all ranks are powered down at the end of refresh.

4.3.2.4 DRAM I/O Power Management

Unused signals should be disabled to save power and reduce electromagnetic interference. This includes all signals associated with an unused memory channel. Clocks, CKE, ODT and CS signals are controlled per DIMM rank and will be powered down for unused ranks.

The I/O buffer for an unused signal should be tri-stated (output driver disabled), the input receiver (differential sense-amp) should be disabled, and any DLL circuitry related ONLY to unused signals should be disabled. The input path should be gated to prevent spurious results due to noise on the unused signals (typically handled automatically when input receiver is disabled).

4.3.3 DDR Electrical Power Gating (EPG)

The DDR I/O of the processor supports Electrical Power Gating (DDR-EPG) while the processor is at C3 or deeper power state.

In C3 or deeper power state, the processor internally gates VDDQ for the majority of the logic to reduce idle power while keeping all critical DDR pins such as CKE and VREF in the appropriate state.

In C7 or deeper power state, the processor internally gates V_{CCIO} for all non-critical state to reduce idle power.

In S3 or C-state transitions, the DDR does not go through training mode and will restore the previous training information.

4.3.4 Power Training

BIOS MRC performing Power Training steps to reduce DDR I/O power while keeping reasonable operational margins, still ensuring platform operation. The algorithms attempt to weaken ODT, driver strength and the related buffers parameters both on the MC and the DRAM side and find the best possible trade-off between the total I/O power and the operational margins using advanced mathematical models.

Note:

Note:

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4.4 Processor Graphics Power Management

4.4.1 Memory Power Savings Technologies

4.4.1.1 Intel® Rapid Memory Power Management (Intel® RMPM)

Intel® Rapid Memory Power Management (Intel® RMPM) conditionally places memory into self-refresh when the processor is in package C3 or deeper power state to allow the system to remain in the deeper power states longer for memory not reserved for graphics memory. Intel RMPM functionality depends on graphics/display state (relevant only when processor graphics is being used), as well as memory traffic patterns generated by other connected I/O devices.

4.4.1.2 Intel® Smart 2D Display Technology (Intel® S2DDT)

Intel S2DDT reduces display refresh memory traffic by reducing memory reads required for display refresh. Power consumption is reduced by less accesses to the IMC. Intel S2DDT is only enabled in single pipe mode.

Intel S2DDT is most effective with:

- Display images well suited to compression, such as text windows, slide shows, and so on. Poor examples are 3D games.
- Static screens such as screens with significant portions of the background showing 2D applications, processor benchmarks, and so on, or conditions when the processor is idle. Poor examples are full-screen 3D games and benchmarks that flip the display image at or near display refresh rates.

4.4.2 Display Power Savings Technologies

4.4.2.1 Intel® (Seamless & Static) Display Refresh Rate Switching (DRRS) with eDP* Port

Intel DRRS provides a mechanism where the monitor is placed in a slower refresh rate (the rate at which the display is updated). The system is smart enough to know that the user is not displaying either 3D or media like a movie where specific refresh rates are required. The technology is very useful in an environment such as a plane where the user is in battery mode doing E-mail, or other standard office applications. It is also useful where the user may be viewing web pages or social media sites while in battery mode.

4.4.2.2 Intel® Automatic Display Brightness

Intel Automatic Display Brightness feature dynamically adjusts the backlight brightness based upon the current ambient light environment. This feature requires an additional sensor to be on the panel front. The sensor receives the changing ambient light conditions and sends the interrupts to the Intel Graphics driver. As per the change in Lux, (current ambient light illuminance), the new backlight setting can be adjusted through BLC. The converse applies for a brightly lit environment. Intel Automatic Display Brightness increases the backlight setting.

4.4.2.3 Smooth Brightness

The Smooth Brightness feature is the ability to make fine grained changes to the screen brightness. All Windows* 10 system that support brightness control are required to support Smooth Brightness control and it should be supporting 101 levels of brightness control. Apart from the Graphics driver changes, there may be few System BIOS changes required to make this feature functional.

4.4.2.4 Intel® Display Power Saving Technology (Intel® DPST) 6.0

The Intel DPST technique achieves backlight power savings while maintaining a good visual experience. This is accomplished by adaptively enhancing the displayed image while decreasing the backlight brightness simultaneously. The goal of this technique is to provide equivalent end-user-perceived image quality at a decreased backlight power level.

1. The original (input) image produced by the operating system or application is analyzed by the Intel DPST subsystem. An interrupt to Intel DPST software is

generated whenever a meaningful change in the image attributes is detected. (A meaningful change is when the Intel DPST software algorithm determines that enough brightness, contrast, or color change has occurred to the displaying images that the image enhancement and backlight control needs to be altered.)

2. Intel DPST subsystem applies an image-specific enhancement to increase image contrast, brightness, and other attributes.
3. A corresponding decrease to the backlight brightness is applied simultaneously to produce an image with similar user-perceived quality (such as brightness) as the original image.

Intel DPST 6.0 has improved the software algorithms and has minor hardware changes to better handle backlight phase-in and ensures the documented and validated method to interrupt hardware phase-in.

4.4.2.5 Panel Self-Refresh 2 (PSR 2)

Panel Self-Refresh feature allows the Processor Graphics core to enter low-power state when the frame buffer content is not changing constantly. This feature is available on panels capable of supporting Panel Self-Refresh. Apart from being able to support, the eDP* panel should be eDP 1.4 compliant. PSR 2 adds partial frame updates and requires an eDP 1.4 compliant panel.
PSR2 is limited to 3200x2000@60 Maximum display resolution.

4.4.2.6 Low-Power Single Pipe (LPSP)

Low-power single pipe is a power conservation feature that helps save power by keeping the inactive pipes powered OFF. This feature is enabled only in a single display configuration without any scaling functionalities. This feature is supported from 4th Generation Intel® Core™ processor family onwards. LPSP is achieved by keeping a single pipe enabled during eDP* only with minimal display pipeline support. This feature is panel independent and works with any eDP panel (port A) in single display mode.

4.4.3 Processor Graphics Core Power Savings Technologies

4.4.3.1 Intel® Graphics Dynamic Frequency

Intel Turbo Boost Technology 2.0 is the ability of the processor IA cores and graphics (Graphics Dynamic Frequency) cores to opportunistically increase frequency and/or voltage above the guaranteed processor and graphics frequency for the given part. Intel Graphics Dynamic Frequency is a performance feature that makes use of unused package power and thermals to increase application performance. The increase in frequency is determined by how much power and thermal budget is available in the package, and the application demand for additional processor or graphics performance. The processor IA core control is maintained by an embedded controller. The graphics driver dynamically adjusts between P-States to maintain optimal performance, power, and thermals. The graphics driver will always place the graphics engine in its lowest possible P-State. Intel Graphics Dynamic Frequency requires BIOS support. Additional power and thermal budget should be available.

4.4.3.2 Intel® Graphics Render Standby Technology (Intel® GRST)

The final power savings technology from Intel happens while the system is asleep. This is another technology where the voltage is adjusted down. For RC6 the voltage is adjusted very low, or very close to zero, what may reduced power by over 1000.

4.4.3.3 Dynamic FPS (DFPS)

Dynamic FPS (DFPS) or dynamic frame-rate control is a runtime feature for improving power-efficiency for 3D workloads. Its purpose is to limit the frame-rate of full screen 3D applications without compromising on user experience. By limiting the frame rate, the load on the graphics engine is reduced, giving an opportunity to run the Processor Graphics at lower speeds, resulting in power savings. This feature works in both AC/DC modes.

4.5 System Agent Enhanced Intel® Speedstep® Technology

System Agent Enhanced Intel Speedstep Technology, a new feature for this processor, is dynamic voltage frequency scaling of the System Agent clock based on memory utilization. Unlike processor core and package Enhanced Intel Speedstep Technology, System Agent Enhanced Intel Speedstep Technology has only two valid operating points.

When workload is low and SA Enhanced Speedstep Technology is enabled, the DDR data rate may drop temporally as follows:

- DDR3L/LPDDR3 – 1066 MT/s
- DDR4 – 1333 MT/s

Before changing the DDR data rate, the processor sets DDR to self-refresh and changes needed parameters. The DDR voltage remains stable and unchanged.

BIOS/MRC DDR training at high and low frequencies sets I/O and timing parameters.

4.6 Voltage Optimization

Voltage Optimization opportunistically provides reduction in power consumption, that is, a boost in performance at a given PL1. Over time the benefit is reduced. There is no change to base frequency or turbo frequency. During system validation and tuning, this feature should be disabled to reflect processor power and performance that is expected over time.

5 Thermal Management

5.1 Processor Thermal Management

The thermal solution provides both component-level and system-level thermal management. To allow optimal operation and long-term reliability of Intel processor-based systems, the system/processor thermal solution should be designed so that the processor:

- Bare Die Parts: Remains below the maximum junction temperature (Tj_{MAX}) specification at the maximum thermal design power (TDP).
- Lidded Parts: Remains below the maximum case temperature (Tcmax) specification at the maximum thermal design power.
- Conforms to system constraints, such as system acoustics, system skin-temperatures, and exhaust-temperature requirements.

Caution: Thermal specifications given in this chapter are on the component and package level and apply specifically to the processor. Operating the processor outside the specified limits may result in permanent damage to the processor and potentially other components in the system.

5.1.1 Thermal Considerations

The processor TDP is the maximum sustained power that should be used for design of the processor thermal solution. TDP is a power dissipation and component temperature operating condition limit, specified in this document, that is validated during manufacturing for the base configuration when executing a near worst case commercially available workload as specified by Intel for the SKU segment. TDP may be exceeded for short periods of time or if running a very high power workload.

To allow the optimal operation and long-term reliability of Intel processor-based systems, the processor must remain within the minimum and maximum component temperature specifications. For lidded parts, the appropriate case temperature (T_{CASE}) specifications is defined by the applicable thermal profile. For bare die parts, the component temperature specification is the applicable Tj_{MAX}.

Thermal solutions not designed to provide this level of thermal capability may affect the long-term reliability of the processor and system.

The processor integrates multiple processing IA cores, graphics cores and a PCH, or a PCH and EDRAM, on a single package. This may result in power distribution differences across the package and should be considered when designing the thermal solution.

Intel Turbo Boost Technology 2.0 allows processor IA cores to run faster than the base frequency. It is invoked opportunistically and automatically as long as the processor is conforming to its temperature, voltage, power delivery and current control limits. When Intel Turbo Boost Technology 2.0 is enabled:

- Applications are expected to run closer to TDP more often as the processor will attempt to maximize performance by taking advantage of estimated available energy budget in the processor package.

- The processor may exceed the TDP for short durations to utilize any available thermal capacitance within the thermal solution. The duration and time of such operation can be limited by platform runtime configurable registers within the processor.
- Graphics peak frequency operation is based on the assumption of only one of the graphics domains (GT/GTx) being active. This definition is similar to the IA core Turbo concept, where peak turbo frequency can be achieved when only one IA core is active. Depending on the workload being applied and the distribution across the graphics domains the user may not observe peak graphics frequency for a given workload or benchmark.
- Thermal solutions and platform cooling that are designed to less than thermal design guidance may experience thermal and performance issues.

Note: Intel Turbo Boost Technology 2.0 availability may vary between the different SKUs.

5.1.2 Intel® Turbo Boost Technology 2.0 Power Monitoring

When operating in turbo mode, the processor monitors its own power and adjusts the processor and graphics frequencies to maintain the average power within limits over a thermally significant time period. The processor estimates the package power for all components on package. In the event that a workload causes the temperature to exceed program temperature limits, the processor will protect itself using the Adaptive Thermal Monitor.

5.1.3 Intel® Turbo Boost Technology 2.0 Power Control

Illustration of Intel® Turbo Boost Technology 2.0 power control is shown in the following sections and figures. Multiple controls operate simultaneously allowing customization for multiple system thermal and power limitations. These controls allow for turbo optimizations within system constraints and are accessible using MSR, MMIO, or PECI interfaces (see the appropriate processor Turbo Implementation Guide for more information).

5.1.3.1 Package Power Control

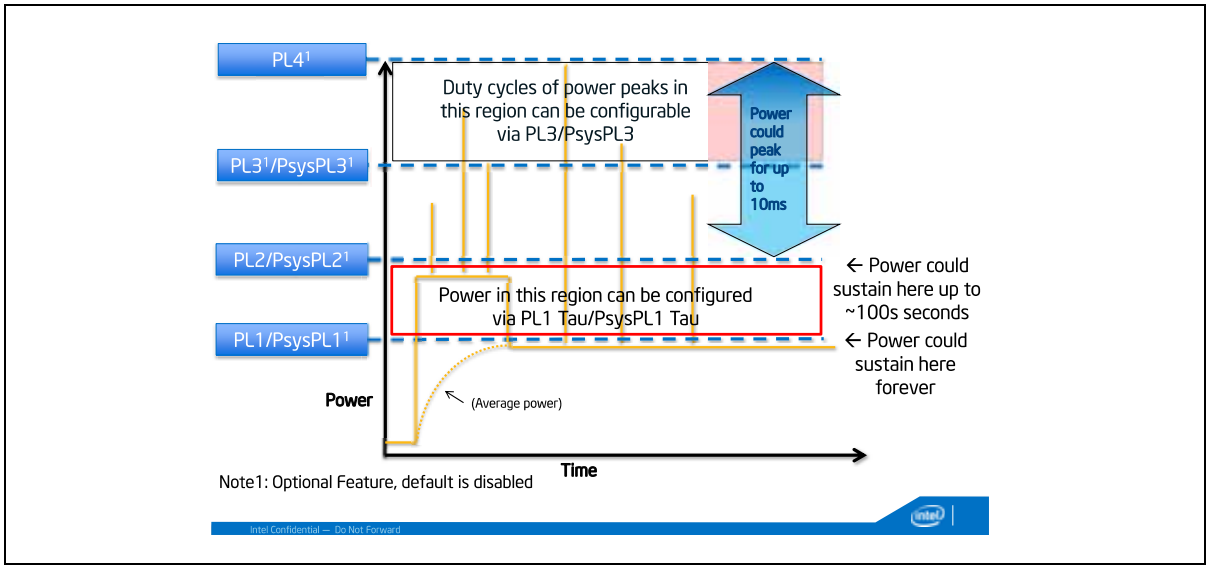
The package power control settings of PL1, PL2, PL3, PL4 and Tau allow the designer to configure Intel Turbo Boost Technology 2.0 to match the platform power delivery and package thermal solution limitations.

- Power Limit 1 (PL1): A threshold for average power that will not exceed - recommend to set to equal TDP power. PL1 should not be set higher than thermal solution cooling limits.
- Power Limit 2 (PL2): A threshold that if exceeded, the PL2 rapid power limiting algorithms will attempt to limit the spike above PL2.
- Power Limit 3 (PL3): A threshold that if exceeded, the PL3 rapid power limiting algorithms will attempt to limit the duty cycle of spikes above PL3 by reactively limiting frequency. This is an optional setting
- Power Limit 4 (PL4): A limit that will not be exceeded, the PL4 power limiting algorithms will preemptively limit frequency to prevent spikes above PL4.
- Turbo Time Parameter (Tau): An averaging constant used for PL1 exponential weighted moving average (EWMA) power calculation.

Note: Implementation of Intel Turbo Boost Technology 2.0 only requires configuring PL1, PL1 Tau, and PL2.

Note: PL3 and PL4 are disabled by default.

Figure 5-1. Package Power Control



5.1.3.2 Platform Power Control

The processor supports Psys (Platform Power) to enhance processor power management. The Psys signal needs to be sourced from a compatible charger circuit and routed to the IMVP8 (voltage regulator). This signal will provide the total thermally relevant platform power consumption (processor and rest of platform) via SVID to the processor.

When the Psys signal is properly implemented, the system designer can utilize the package power control settings of PsysPL1/Tau, PsysPL2 and PsysPL3 for additional manageability to match the platform power delivery and platform thermal solution limitations for Intel Turbo Boost Technology 2.0. The operation of the PsysPL1/tau, PsysPL2 and PsysPL3 is analogous to the processor power limits described in Section 5.1.3.1, “Package Power Control”.

- Platform Power Limit 1 (PsysPL1): A threshold for average platform power that will not be exceeded - recommend to set to equal platform thermal capability.
- Platform Power Limit 2 (PsysPL2): A threshold that if exceeded, the PsysPL2 rapid power limiting algorithms will attempt to limit the spikes above PsysPL2.
- Platform Power Limit 3 (PsysPL3): A threshold that if exceeded, the PsysPL3 rapid power limiting algorithms will attempt to limit the duty cycle of spikes above PsysPL3 by reactively limiting frequency.
- PsysPL1 Tau: An averaging constant used for PsysPL1 exponential weighted moving average (EWMA) power calculation.
- The Psys signal and associated power limits / Tau are optional for the system designer and disabled by default.
- The Psys data will not include power consumption for charging.

5.1.3.3 Turbo Time Parameter (Tau)

Turbo Time Parameter (Tau) is a mathematical parameter (units of seconds) that controls the Intel Turbo Boost Technology 2.0 algorithm. During a maximum power turbo event, the processor could sustain PL2 for a duration longer than the Turbo Time Parameter. If the power value and/or Turbo Time Parameter is changed during runtime, it may take some time based on the new Turbo Time Parameter level for the algorithm to settle at the new control limits. The time varies depending on the magnitude of the change, power limits, and other factors. There is an individual Turbo Time Parameter associated with Package Power Control and Platform Power Control.

5.1.4 Configurable TDP (cTDP) and Low-Power Mode

Configurable TDP (cTDP) and Low-Power Mode (LPM) form a design option where the processor's behavior and package TDP are dynamically adjusted to a desired system performance and power envelope. Configurable TDP and Low-Power Mode technologies offer opportunities to differentiate system design while running active workloads on select processor SKUs through scalability, configuration and adaptability. The scenarios or methods by which each technology is used are customizable but typically involve changes to PL1 and associated frequencies for the scenario with a resultant change in performance depending on system's usage. Either technology can be triggered by (but are not limited to) changes in OS power policies or hardware events such as docking a system, flipping a switch or pressing a button. cTDP and LPM are designed to be configured dynamically and do not require an operating system reboot.

Note: Configurable TDP and Low-Power Mode technologies are not battery life improvement technologies.

5.1.4.1 Configurable TDP

Note: Configurable TDP availability may vary between the different SKUs.

With cTDP, the processor is now capable of altering the maximum sustained power with an alternate processor IA core base frequency. Configurable TDP allows operation in situations where extra cooling is available or situations where a cooler and quieter mode of operation is desired. Configurable TDP can be enabled using Intel's DPTF driver or through HW/EC firmware. Enabling cTDP using the DPTF driver is recommended as Intel does not provide specific application or EC source code.

cTDP consists of three modes as shown in the following table.

Table 5-1. Configurable TDP Modes (Sheet 1 of 2)

Mode	Description
Base	The average power dissipation and junction temperature operating condition limit, specified in Table 5-2, Table 5-3 and Table 5-5 for the SKU Segment and Configuration, for which the processor is validated during manufacturing when executing an associated Intel-specified high-complexity workload at the processor IA core frequency corresponding to the configuration and SKU.
TDP-Up	The SKU-specific processor IA core frequency where manufacturing confirms logical functionality within the set of operating condition limits specified for the SKU segment and Configurable TDP-Up configuration in Table 5-2, Table 5-3 and Table 5-5. The Configurable TDP-Up Frequency and corresponding TDP is higher than the processor IA core Base Frequency and SKU Segment Base TDP.

Table 5-1. Configurable TDP Modes (Sheet 2 of 2)

Mode	Description
TDP-Down	The processor IA core frequency where manufacturing confirms logical functionality within the set of operating condition limits specified for the SKU segment and Configurable TDP-Down configuration in Table 5-2, Table 5-3 and Table 5-5. The Configurable TDP-Down Frequency and corresponding TDP is lower than the processor IA core Base Frequency and SKU Segment Base TDP.

In each mode, the Intel Turbo Boost Technology 2.0 power limits are reprogrammed along with a new OS controlled frequency range. The DPTF driver assists in all these operations. The cTDP mode does not change the max per-processor IA core turbo frequency.

5.1.4.2 Low-Power Mode

Low-Power Mode (LPM) can provide cooler and quieter system operation. By combining several active power limiting techniques, the processor can consume less power while running at equivalent low frequencies. Active power is defined as processor power consumed while a workload is running and does not refer to the power consumed during idle modes of operation. LPM is only available using the Intel DPTF driver.

5.1.5 Thermal Management Features

Occasionally the processor may operate in conditions that are near to its maximum operating temperature. This can be due to internal overheating or overheating within the platform. In order to protect the processor and the platform from thermal failure, several thermal management features exist to reduce package power consumption and thereby temperature in order to remain within normal operating limits. Furthermore, the processor supports several methods to reduce memory power.

5.1.5.1 Adaptive Thermal Monitor

The purpose of the Adaptive Thermal Monitor is to reduce processor IA core power consumption and temperature until it operates below its maximum operating temperature. Processor IA core power reduction is achieved by:

- Adjusting the operating frequency (using the processor IA core ratio multiplier) and voltage.
- Modulating (starting and stopping) the internal processor IA core clocks (duty cycle).

The Adaptive Thermal Monitor can be activated when the package temperature, monitored by any digital thermal sensor (DTS), meets its maximum operating temperature. The maximum operating temperature implies maximum junction temperature Tj_{MAX}.

Reaching the maximum operating temperature activates the Thermal Control Circuit (TCC). When activated the TCC causes both the processor IA core and graphics core to reduce frequency and voltage adaptively. The Adaptive Thermal Monitor will remain active as long as the package temperature remains at its specified limit. Therefore, the Adaptive Thermal Monitor will continue to reduce the package frequency and voltage until the TCC is de-activated.

Tj_{MAX} is factory calibrated and is not user configurable. The default value is software visible in the TEMPERATURE_TARGET (0x1A2) MSR, bits [23:16].

The Adaptive Thermal Monitor does not require any additional hardware, software drivers, or interrupt handling routines. It is not intended as a mechanism to maintain processor thermal control to PL1 = TDP. The system design should provide a thermal solution that can maintain normal operation when PL1 = TDP within the intended usage range.

Adaptive Thermal Monitor protection is always enabled.

5.1.5.1.1 TCC Activation Offset

TCC Activation Offset can be set as an offset from the maximum allowed component temperature to lower the onset of TCC and Adaptive Thermal Monitor. In addition, the processor has added an optional time window (Tau) to manage processor performance at the TCC Activation offset value via an EWMA (Exponential Weighted Moving Average) of temperature.

TCC Activation Offset with Tau=0

An offset (degrees Celsius) can be written to the TEMPERATURE_TARGET (0x1A2) MSR, bits [29:24], the offset value will be subtracted from the value found in bits [23:16]. When the time window (Tau) is set to zero, there will be no averaging, the offset, will be subtracted from the Tj_{MAX} value and used as a new max temperature set point for Adaptive Thermal Monitoring. This will have the same behavior as in prior products to have TCC activation and Adaptive Thermal Monitor to occur at this lower target silicon temperature.

If enabled, the offset should be set lower than any other passive protection such as ACPI _PSV trip points

TCC Activation Offset with Tau

To manage the processor with the EWMA (Exponential Weighted Moving Average) of temperature, an offset (degrees Celsius) is written to the TEMPERATURE_TARGET (0x1A2) MSR, bits [29:24], and the time window (Tau) is written to the TEMPERATURE_TARGET (0x1A2) MSR [6:0]. The Offset value will be subtracted from the value found in bits [23:16] and be the temperature.

The processor will manage to this average temperature by adjusting the frequency of the various domains. The instantaneous Tj can briefly exceed the average temperature. The magnitude and duration of the overshoot is managed by the time window value (Tau).

This averaged temperature thermal management mechanism is in addition, and not instead of Tj_{MAX} thermal management. That is, whether the TCC activation offset is 0 or not, TCC Activation will occur at Tj_{MAX}.

5.1.5.1.2 Frequency / Voltage Control

Upon Adaptive Thermal Monitor activation, the processor attempts to dynamically reduce processor temperature by lowering the frequency and voltage operating point. The operating points are automatically calculated by the processor IA core itself and do not require the BIOS to program them as with previous generations of Intel processors. The processor IA core will scale the operating points such that:

- The voltage will be optimized according to the temperature, the processor IA core bus ratio and number of processor IA cores in deep C-states.

- The processor IA core power and temperature are reduced while minimizing performance degradation.

Once the temperature has dropped below the trigger temperature, the operating frequency and voltage will transition back to the normal system operating point.

Once a target frequency/bus ratio is resolved, the processor IA core will transition to the new target automatically.

- On an upward operating point transition the voltage transition precedes the frequency transition.
- On a downward transition the frequency transition precedes the voltage transition.
- The processor continues to execute instructions. However, the processor will halt instruction execution for frequency transitions.

If a processor load-based Enhanced Intel SpeedStep Technology/P-state transition (through MSR write) is initiated while the Adaptive Thermal Monitor is active, there are two possible outcomes:

- If the P-state target frequency is higher than the processor IA core optimized target frequency, the P-state transition will be deferred until the thermal event has been completed.
- If the P-state target frequency is lower than the processor IA core optimized target frequency, the processor will transition to the P-state operating point.

5.1.5.1.3 Clock Modulation

If the frequency/voltage changes are unable to end an Adaptive Thermal Monitor event, the Adaptive Thermal Monitor will utilize clock modulation. Clock modulation is done by alternately turning the clocks off and on at a duty cycle (ratio between clock “on” time and total time) specific to the processor. The duty cycle is factory configured to 25% on and 75% off and cannot be modified. The period of the duty cycle is configured to 32 microseconds when the Adaptive Thermal Monitor is active. Cycle times are independent of processor frequency. A small amount of hysteresis has been included to prevent excessive clock modulation when the processor temperature is near its maximum operating temperature. Once the temperature has dropped below the maximum operating temperature, and the hysteresis timer has expired, the Adaptive Thermal Monitor goes inactive and clock modulation ceases. Clock modulation is automatically engaged as part of the Adaptive Thermal Monitor activation when the frequency/voltage targets are at their minimum settings. Processor performance will be decreased when clock modulation is active. Snooping and interrupt processing are performed in the normal manner while the Adaptive Thermal Monitor is active.

Clock modulation will not be activated by the Package average temperature control mechanism.

5.1.5.2 Digital Thermal Sensor

Each processor has multiple on-die Digital Thermal Sensor (DTS) that detects the processor IA, GT and other areas of interest instantaneous temperature.

Temperature values from the DTS can be retrieved through:

- A software interface using processor Model Specific Register (MSR).
- A processor hardware interface as described in Section 2.4, “Platform Environmental Control Interface (PECI)”.

When temperature is retrieved by the processor MSR, it is the instantaneous temperature of the given DTS. When temperature is retrieved using PECI, it is the average of the highest DTS temperature in the package over a 256 ms time window. Intel recommends using the PECI reported temperature for platform thermal control that benefits from averaging, such as fan speed control. The average DTS temperature may not be a good indicator of package Adaptive Thermal Monitor activation or rapid increases in temperature that triggers the Out of Specification status bit within the PACKAGE_THERM_STATUS MSR 1B1h and IA32_THERM_STATUS MSR 19Ch.

Code execution is halted in C1 or deeper C- states. Package temperature can still be monitored through PECI in lower C-states.

Unlike traditional thermal devices, the DTS outputs a temperature relative to the maximum supported operating temperature of the processor (Tj_{MAX}), regardless of TCC activation offset. It is the responsibility of software to convert the relative temperature to an absolute temperature. The absolute reference temperature is readable in the TEMPERATURE_TARGET MSR 1A2h. The temperature returned by the DTS is an implied negative integer indicating the relative offset from Tj_{MAX}. The DTS does not report temperatures greater than Tj_{MAX}. The DTS-relative temperature readout directly impacts the Adaptive Thermal Monitor trigger point. When a package DTS indicates that it has reached the TCC activation (a reading of 0x0, except when the TCC activation offset is changed), the TCC will activate and indicate an Adaptive Thermal Monitor event. A TCC activation will lower both processor IA core and graphics core frequency, voltage, or both. Changes to the temperature can be detected using two programmable thresholds located in the processor thermal MSRs. These thresholds have the capability of generating interrupts using the processor IA core's local APIC. Refer to the *Intel 64 and IA-32 Architectures Software Developer's Manual* for specific register and programming details.

5.1.5.2.1 Digital Thermal Sensor Accuracy (Taccuracy)

The error associated with DTS measurements will not exceed ±5 °C within the entire operating range.

5.1.5.2.2 Fan Speed Control with Digital Thermal Sensor

Digital Thermal Sensor based fan speed control (T_{FAN}) is a recommended feature to achieve optimal thermal performance. At the T_{FAN} temperature, Intel recommends full cooling capability before the DTS reading reaches Tj_{MAX}.

5.1.5.3 PROCHOT# Signal

PROCHOT# (processor hot) is asserted by the processor when the TCC is active. Only a single PROCHOT# pin exists at a package level. When any DTS temperature reaches the TCC activation temperature, the PROCHOT# signal will be asserted. PROCHOT# assertion policies are independent of Adaptive Thermal Monitor enabling.

5.1.5.4 Bi-Directional PROCHOT#

By default, the PROCHOT# signal is set to input only. When configured as an input or bi-directional signal, PROCHOT# can be used for thermally protecting other platform components should they overheat as well. When PROCHOT# is driven by an external device:

- The package will immediately transition to the lowest P-State (Pn) supported by the processor IA cores and graphics cores. This is contrary to the internally-generated Adaptive Thermal Monitor response.
- Clock modulation is not activated.

The processor package will remain at the lowest supported P-state until the system de-asserts PROCHOT#. The processor can be configured to generate an interrupt upon assertion and de-assertion of the PROCHOT# signal.

When PROCHOT# is configured as a bi-directional signal and PROCHOT# is asserted by the processor, it is impossible for the processor to detect a system assertion of PROCHOT#. The system assertion will have to wait until the processor de-asserts PROCHOT# before PROCHOT# action can occur due to the system assertion. While the processor is hot and asserting PROCHOT#, the power is reduced but the reduction rate is slower than the system PROCHOT# response of < 100 us. The processor thermal control is staged in smaller increments over many milliseconds. This may cause several milliseconds of delay to a system assertion of PROCHOT# while the output function is asserted.

5.1.5.5 Voltage Regulator Protection using PROCHOT#

PROCHOT# may be used for thermal protection of voltage regulators (VR). System designers can create a circuit to monitor the VR temperature and assert PROCHOT# and, if enabled, activate the TCC when the temperature limit of the VR is reached. When PROCHOT# is configured as a bi-directional or input only signal, if the system assertion of PROCHOT# is recognized by the processor, it will result in an immediate transition to the lowest P-State (Pn) supported by the processor IA cores and graphics cores. Systems should still provide proper cooling for the VR and rely on bi-directional PROCHOT# only as a backup in case of system cooling failure. Overall, the system thermal design should allow the power delivery circuitry to operate within its temperature specification even while the processor is operating at its TDP.

5.1.5.6 Thermal Solution Design and PROCHOT# Behavior

With a properly designed and characterized thermal solution, it is anticipated that PROCHOT# will only be asserted for very short periods of time when running the most power intensive applications. The processor performance impact due to these brief periods of TCC activation is expected to be so minor that it would be immeasurable. However, an under-designed thermal solution that is not able to prevent excessive assertion of PROCHOT# in the anticipated ambient environment may:

- Cause a noticeable performance loss.
- Result in prolonged operation at or above the specified maximum junction temperature and affect the long-term reliability of the processor.
- May be incapable of cooling the processor even when the TCC is active continuously (in extreme situations).

5.1.5.7 Low-Power States and PROCHOT# Behavior

Depending on package power levels during package C-states, outbound PROCHOT# may de-assert while the processor is idle as power is removed from the signal. Upon wake up, if the processor is still hot, the PROCHOT# will re-assert. Although, typically package idle state residency should resolve any thermal issues. The PECI interface is fully operational during all C-states and it is expected that the platform continues to manage processor IA core and package thermals even during idle states by regularly polling for thermal data over PECI.

5.1.5.8 THERMTRIP# Signal

Regardless of enabling the automatic or on-demand modes, in the event of a catastrophic cooling failure, the package will automatically shut down when the silicon has reached an elevated temperature that risks physical damage to the product. At this point, the THERMTRIP# signal will go active.

5.1.5.9 Critical Temperature Detection

Critical Temperature detection is performed by monitoring the package temperature. This feature is intended for graceful shutdown before the THERMTRIP# is activated. However, the processor execution is not guaranteed between critical temperature and THERMTRIP#. If the Adaptive Thermal Monitor is triggered and the temperature remains high, a critical temperature status and sticky bit are latched in the PACKAGE_THERM_STATUS MSR 1B1h and the condition also generates a thermal interrupt, if enabled. For more details on the interrupt mechanism, refer to the *Intel® 64 and IA-32 Architectures Software Developer's Manual* (Related Documents section).

5.1.5.10 On-Demand Mode

The processor provides an auxiliary mechanism that allows system software to force the processor to reduce its power consumption using clock modulation. This mechanism is referred to as "On-Demand" mode and is distinct from Adaptive Thermal Monitor and bi-directional PROCHOT#. The processor platforms should not rely on software usage of this mechanism to limit the processor temperature. On-Demand Mode can be accomplished using processor MSR or chipset I/O emulation. On-Demand Mode may be used in conjunction with the Adaptive Thermal Monitor. However, if the system software tries to enable On-Demand mode at the same time the TCC is engaged, the factory configured duty cycle of the TCC will override the duty cycle selected by the On-Demand mode. If the I/O based and MSR-based On-Demand modes are in conflict, the duty cycle selected by the I/O emulation-based On-Demand mode will take precedence over the MSR-based On-Demand Mode.

5.1.5.11 MSR Based On-Demand Mode

If Bit 4 of the IA32_CLOCK_MODULATION MSR is set to 1, the processor will immediately reduce its power consumption using modulation of the internal processor IA core clock, independent of the processor temperature. The duty cycle of the clock modulation is programmable using bits [3:1] of the same IA32_CLOCK_MODULATION MSR. In this mode, the duty cycle can be programmed in either 12.5% or 6.25% increments (discoverable using CPUID). Thermal throttling using this method will modulate each processor IA core's clock independently.

5.1.5.12 I/O Emulation-Based On-Demand Mode

I/O emulation-based clock modulation provides legacy support for operating system software that initiates clock modulation through I/O writes to ACPI defined processor clock control registers on the chipset (PROC_CNT). Thermal throttling using this method will modulate all processor IA cores simultaneously.

5.1.6 Intel® Memory Thermal Management

The processor provides thermal protection for system memory by throttling memory traffic when using either DIMM modules or a memory down implementation. Two levels of throttling are supported by the processor, either a warm threshold or hot threshold that is customizable through memory mapped I/O registers. Throttling based on the warm threshold should be an intermediate level of throttling. Throttling based on the hot threshold should be the most severe. The amount of throttling is dynamically controlled by the processor.

The on Die Thermal Sensor (ODTS) uses a physical thermal sensor on DRAM dies. ODTS is available for DDR4 and LPDDR3. It is used to set refresh rate according to DRAM temperature.

The memory controller reads LPDDR3 MR4 or DDR4 MR3 and configures the DDR refresh rate accordingly.

When using ODTS, the memory controller gets a Warm/Hot/Cold indication from DRAMs On-Die TS and throttles DDR accordingly. This is a method of Closed Loop Thermal Management (CLTM). Refer to document 604677 for more details on closed loop thermal management.

Memory temperature may be acquired through an on-board thermal sensor (TS-on-Board), retrieved by an embedded controller and reported to the processor through the PECI 3.1 interface. This methodology is known as PECI injected temperature. This is a method of Closed Loop Thermal Management (CLTM).

5.1.7 Scenario Design Power (SDP)

SDP requires that the POWER_LIMIT_1 (PL1) to be set to the cooling level capability (SDP level, or higher). While the SDP specification is characterized at Tj of 80 °C, the functional limit for the product remains at Tj_{MAX}. Customers may choose to program the TCC Offset to have TCC Activation at 80 °C, but it is not required.

The processors that have SDP specified can still exceed SDP under certain workloads, such as TDP workloads. TDP power dissipation is still possible with the intended usage models, and protection mechanisms to handle levels beyond cooling capabilities are recommended. Intel recommends using such thermal control mechanisms to manage situations where power may exceed the thermal design capability.

Note: cTDP-Down mode is required for Intel Core products in order to achieve SDP.

Note: Although SDP is defined at 80 °C, the TCC activation temperature is Tj_{MAX}.

5.2 Thermal and Power Specifications

The following notes apply only to Table 5.2 and Table 5-7.

Note	Definition
1	The TDP and Configurable TDP values are the average power dissipation in junction temperature operating condition limit, for the SKU Segment and Configuration, for which the processor is validated during manufacturing when executing an associated Intel-specified high-complexity workload at the processor IA core frequency corresponding to the configuration and SKU.
2	TDP workload may consist of a combination of processor IA core intensive and graphics core intensive applications.
3	Can be modified at runtime by MSR writes, with MMIO and with PECI commands.
4	'Turbo Time Parameter' is a mathematical parameter (units of seconds) that controls the processor turbo algorithm using a moving average of energy usage. Do not set the Turbo Time Parameter to a value less than 0.1 seconds. refer to Section 5.1.3.2, "Platform Power Control" for further information.
5	Shown limit is a time averaged power, based upon the Turbo Time Parameter. Absolute product power may exceed the set limits for short durations or under virus or uncharacterized workloads.
6	Processor will be controlled to specified power limit as described in Section 5.1.2, "Intel® Turbo Boost Technology 2.0 Power Monitoring". If the power value and/or 'Turbo Time Parameter' is changed during runtime, it may take a short period of time (approximately 3 to 5 times the 'Turbo Time Parameter') for the algorithm to settle at the new control limits.
7	This is a hardware default setting and not a behavioral characteristic of the part. The reference BIOS code may override the hardware default power limit values to optimize performance
8	For controllable turbo workloads, the PL2 limit may be exceeded for up to 10 ms.
9	Refer to Table 5-1, "Configurable TDP Modes" for the definitions of 'base'base, 'TDP-Up' and 'TDP-Down'.
10	LPM power level is an opportunistic power and is not a guaranteed value as usages and implementations may vary.
11	Power limits may vary depending on if the product supports the 'TDP-up' and/or 'TDP-down' modes. Default power limits can be found in the PKG_PWR_SKU MSR (614h).
12	The processor die and OPCM die do not reach maximum sustained power simultaneously since the sum of the 2 dies estimated power budget is controlled to be equal to or less than the package TDP (PL1) limit.
13	cTDP down power is based on GT2 equivalent graphics configuration. cTDP down does not decrease the number of active Processor Graphics EUs, but relies on Power Budget Management (PL1) to achieve the specified power level.
14	May vary based on SKU.
16	Sustained residencies at high voltages and temperatures may temporarily limit turbo frequency.
17	The formula of PL2=PL1*1.25 is the hardware default but may not represent the optimum value for processor performance. By including the benefits available from power and thermal management features the recommended value for PL2 found in the Power Map can be higher.

5.2.1 KBL U/Y Processor Line Thermal and Power Specifications

Table 5-2. TDP Specifications (KBL U/Y/AML-Y22 Processor Line)

Segment and Package	Processor IA Cores, Graphics Configuration and TDP	Configuration	Processor IA Core Frequency	Graphics core Frequency	Thermal Design Power (TDP) [w]	Scenario Design Power (SDP) [w]	Notes
U-Processor Line BGA	2 Core GT2 15W	Configurable TDP-Up	2.7 GHz to 2.9 GHz	900 MHz to 1.1 GHz	25	N/A	1,9,10, 11,16
		Base	2.4 GHz to 2.7 GHz		15		
		Configurable TDP-Down / LFM	800 MHz		7.5		
		LPM	400 MHz	300 MHz	~7		
Y-Processor Line BGA	2 Core GT2 4.5W	Configurable TDP-Up	1.6 GHz	300 MHz to 1.05 GHz	7	3.0	1,9,10, 11,16,17
		Base	1.0 GHz to 1.3 GHz		4.5		
		Configurable TDP-Down	600 MHz		3.75		
		LFM	400 MHz	100 MHz	~3.75		
Y-Processor Line BGA	2 Core GT2 6W	Base	1.3 GHz to 1.5 GHz	300 MHz to 850 MHz	6	N/A	1,9,10, 11,16,17
		Configurable TDP-Down	600 MHz		4.5		
		LFM	400 MHz	100 MHz	~3.75		
AML-Y Processor Line BGA	2 Core GT2 5W	Configurable TDP-Up	1.6 GHz	900 MHz to 1.05GHz	7	N/A	1,9,10, 11,16,17
		Base	1.1 GHz to 1.5 GHz		5		
		Configurable TDP-Down	600 MHz		3.5		
		LFM	400 MHz	300 MHz	~3.5		

Note: The ~ sign stands for approximation.

Table 5-3. Package Turbo Specifications (KBL U/Y and AML-Y22 Processor Line) (Sheet 1 of 2)

Segment and Package	Processor IA Cores, Graphics Configuration and TDP	Parameter	Min.	Hardware Default	Max	Units	Notes
U-Processor Line BGA	2-Core GT3 28W with OPC	Power Limit 1 Time (PL1 Tau) Power Limit 1 (PL1) Power Limit 2 (PL2)	0.01 N/A N/A	1 28 1.25*28	448 N/A N/A	s W W	3,4,5,6,7, 8,14,17
U-Processor Line BGA	2- Core GT3 15W with OPC	Power Limit 1 Time (PL1 Tau) Power Limit 1 (PL1) Power Limit 2 (PL2)	0.01 N/A N/A	1 15 1.25*15	448 N/A N/A	s W W	3,4,5,6,7, 8,14,17

Table 5-3. Package Turbo Specifications (KBL U/Y and AML-Y22 Processor Line) (Sheet 2 of 2)

Segment and Package	Processor IA Cores, Graphics Configuration and TDP	Parameter	Min.	Hardware Default	Max	Units	Notes
U-Processor Line BGA	2-Core GT2 15W	Power Limit 1 Time (PL1 Tau) Power Limit 1 (PL1) Power Limit 2 (PL2)	0.01 N/A N/A	1 15 1.25*15	448 N/A N/A	s W W	3,4,5,6,7, 8,14,17
Y-Processor Line BGA	2-Core GT2 ~4.5W	Power Limit 1 Time (PL1 Tau) Power Limit 1 (PL1) Power Limit 2 (PL2)	0.01 N/A N/A	1 4.5 1.25*4.5	448 N/A N/A	s W W	3,4,5,6,7, 8,14,17
AML-Y Processor Line BGA	2-Core GT2 5W)	Power Limit 1 Time (PL1 Tau) Power Limit 1 (PL1) Power Limit 2 (PL2)	0.01 N/A N/A	1 5 1.25*5	448 N/A N/A	s W W	3,4,5,6,7, 8,14,17
Note: No Specifications for Min/Max PL1/PL2 values, refer PAG (Power Arch Guide) for PL1/PL2 recommendation.							

Table 5-4. Junction Temperature Specifications (KBL U/Y and AML-Y22 Processor Line)

Segment	Symbol	Package Turbo Parameter	Temperature Range		TDP Specification Temperature Range		Units	Notes
			Min	Max	Min	Max		
U/U- 4 Core Processor Line BGA	T_j	Junction temperature limit	0	100	35	100	ºC	1, 2
U-Processor Line + OPC BGA	T_j	Junction temperature limit	0	100	35	100	ºC	1, 2
Y-Processor Line BGA	T_j	Junction temperature limit	0	100	N/A	90	ºC	1, 2, 3
AML-Y22 Processor Line BGA	T_j	Junction temperature limit	0	100	N/A	90	ºC	1, 2, 3

Notes:
1. The thermal solution needs to ensure that the processor temperature does not exceed the TDP Specification Temperature.
2. The processor junction temperature is monitored by Digital Temperature Sensors (DTS). For DTS accuracy, refer to Section 5.1.5.2.1, "Digital Thermal Sensor Accuracy (Taccuracy)".
3. For this SKU to be specification compliance to the 90 ºC TDP specification temperature, TCC Offset = 10 and Tau value should be programed into MSR 1A2h. The recommended TCC_Offset averaging Tau value is 5s. Refer to the Volume 2 for additional details.

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5.3.1 KBL U/Y Processor Line Thermal and Power Specifications

Note: The ~ sign stands for approximation.

Table 5-6. Package Turbo Specifications (U/Y and AML-Y22 Processor Line)

Segment and Package	Processor IA Cores, Graphics Configuration and TDP	Parameter	Min.	Hardware Default	Max	Units	Notes
U-Processor Line BGA	2-Core GT3 28W with OPC	Power Limit 1 Time (PL1 Tau) Power Limit 1 (PL1) Power Limit 2 (PL2)	0.01 N/A N/A	1 28 1.25*28	448 N/A N/A	s W W	3,4,5,6,7, 8,14,17
U-Processor Line BGA	2- Core GT3 15W with OPC	Power Limit 1 Time (PL1 Tau) Power Limit 1 (PL1) Power Limit 2 (PL2)	0.01 N/A N/A	1 15 1.25*15	448 N/A N/A	s W W	3,4,5,6,7, 8,14,17
U-Processor Line BGA	2-Core GT2 15W	Power Limit 1 Time (PL1 Tau) Power Limit 1 (PL1) Power Limit 2 (PL2)	0.01 N/A N/A	1 15 1.25*15	448 N/A N/A	s W W	3,4,5,6,7, 8,14,17
Y-Processor Line BGA	2-Core GT2 ~4.5W	Power Limit 1 Time (PL1 Tau) Power Limit 1 (PL1) Power Limit 2 (PL2)	0.01 N/A N/A	1 4.5 1.25*4.5	448 N/A N/A	s W W	3,4,5,6,7, 8,14,17
H-Y Processor Line BGA	Quad-Core GT2 5W)	Power Limit 1 Time (PL1 Tau) Power Limit 1 (PL1) Power Limit 2 (PL2)	0.01 N/A N/A	1 5 1.25*5	448 N/A N/A	s W W	3,4,5,6,7, 8,14,17
Note: No Specifications for Min/Max PL1/PL2 values, refer PAG (Power Arch Guide) for PL1/PL2 recommendation.							

Table 5-7. Junction Temperature Specifications (KBL U/Y and AML-Y22 Processor Line)

Segment	Symbol	Package Turbo Parameter	Temperature Range		TDP Specification Temperature Range		Units	Notes
			Min	Max	Min	Max		
U/U- 4 Core Processor Line BGA	T_j	Junction temperature limit	0	100	35	100	ºC	1, 2
U-Processor Line + OPC BGA	T_j	Junction temperature limit	0	100	35	100	ºC	1, 2
Y-Processor Line BGA	T_j	Junction temperature limit	0	100	N/A	90	ºC	1, 2, 3
AML-Y22 Processor Line BGA	T_j	Junction temperature limit	0	100	N/A	90	ºC	1, 2, 3

Notes:
1. The thermal solution needs to ensure that the processor temperature does not exceed the TDP Specification Temperature.
2. The processor junction temperature is monitored by Digital Temperature Sensors (DTS). For DTS accuracy, refer to Section 5.1.5.2.1, "Digital Thermal Sensor Accuracy (Taccuracy)".
3. For this SKU to be specification compliance to the 90 ºC TDP specification temperature, TCC Offset = 10 and Tau value should be programed into MSR 1A2h. The recommended TCC_Offset averaging Tau value is 5s. Refer to the Volume 2 for additional details.

6 Signal Description

This chapter describes the processor signals. They are arranged in functional groups according to their associated interface or category. The notations in the following table are used to describe the signal type.

The signal description also includes the type of buffer used for the particular signal (see the following table).

Table 6-1. Signal Tables Terminology

Notation	Signal Type
I	Input pin
O	Output pin
I/O	Bi-directional Input/Output pin
SE	Single Ended Link
Diff	Differential Link
CMOS	CMOS buffers. 1.05V- tolerant
OD	Open Drain buffer
DDR3L/-RS	DDR3L/DDR3L-RS buffers: 1.35V-tolerant
DDR3L/-RS	DDR3L/DDR3L-RS buffers: 1.35V-tolerant
LPDDR3	LPDDR3 buffers: 1.2V- tolerant
DDR4	DDR4 buffers: 1.2V-tolerant
A	Analog reference or output. May be used as a threshold voltage or for buffer compensation
GTL	Gunning Transceiver Logic signaling technology
Ref	Voltage reference signal
Availability	Signal Availability condition - based on segment, SKU, platform type or any other factor
Asynchronous [1]	Signal has no timing relationship with any reference clock.

Note:
1. Qualifier for a buffer type.

6.1 System Memory Interface

Table 6-2. DDR3L/-RS Memory Interface (Sheet 1 of 2)

Signal Name	Description	Dir.	Buffer Type	Link Type	Availability
DDR0_DQ[63:0] DDR1_DQ[63:0]	**Data Buses:** Data signals interface to the SDRAM data buses.	I/O	DDR3L	SE	All Processor Lines
DDR0_DQSP[7:0] DDR0_DQSN[7:0] DDR1_DQSP[7:0] DDR1_DQSN[7:0]	**Data Strobes:** Differential data strobe pairs. The data is captured at the crossing point of DQS during read and write transactions.	I/O	DDR3L	Diff	All Processor Lines

Table 6-2. DDR3L/-RS Memory Interface (Sheet 2 of 2)

Signal Name	Description	Dir.	Buffer Type	Link Type	Availability
DDR0_CKN[1:0] DDR0_CKP[1:0] DDR1_CKN[1:0] DDR1_CKP[1:0]	**SDRAM Differential Clock:** Differential clocks signal pairs, pair per rank. The crossing of the positive edge of DDR0_CKP/DDR1_CKP and the negative edge of their complement DDR0_CKN / DDR1_CKN are used to sample the command and control signals on the SDRAM.	O	DDR3L	Diff	[1:0] applicable for all Processor Lines.
DDR0_CKE[1:0] DDR1_CKE[1:0]	**Clock Enable:** (1 per rank). These signals are used to: • Initialize the SDRAMs during power-up. • Power-down SDRAM ranks. • Place all SDRAM ranks into and out of self-refresh during STR (Suspend to RAM).	O	DDR3L	SE	[1:0] applicable for all Processor Lines.
DDR0_CS#[1:0] DDR1_CS#[1:0]	**Chip Select:** (1 per rank). These signals are used to select particular SDRAM components during the active state. There is one Chip Select for each SDRAM rank.	O	DDR3L	SE	[1:0] applicable for all Processor Lines.
DDR0_ODT[1:0] DDR1_ODT[1:0]	**On Die Termination: (1 per rank).** Active SDRAM Termination Control**.**	O	DDR3L	SE	[0] applicable for all Processor Lines. [1:0] applicable for U/U-4 Core Processor Lines.
DDR0_MA[15:0] DDR1_MA[15:0]	**Memory Address:** These signals are used to provide the multiplexed row and column address to the SDRAM. • A10 is sampled during Read/Write commands to determine whether Autoprecharge should be performed to the accessed bank after the Read/Write operation. HIGH: Autoprecharge; LOW: no Autoprecharge. • A10 is sampled during a Precharge command to determine whether the Precharge applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by bank addresses. • A12 is sampled during Read and Write commands to determine if burst chop (on-the-fly) will be performed. HIGH: no burst chop; LOW: burst chopped.	O	DDR3L	SE	All Processor Lines
DDR0_BA[2:0] DDR1_BA[2:0]	**Bank Select:** These signals define which banks are selected within each SDRAM rank.	O	DDR3L	SE	All Processor Lines
DDR0_CAS# DDR1_CAS#	**CAS Control Signal:** Column Address Select command signal	O	DDR3L	SE	All Processor Lines
DDR0_RAS# DDR1_RAS#	**RAS Control Signal:** Row Address Select command signal	O	DDR3L	SE	All Processor Lines
DDR0_WE# DDR1_WE#	**WE Control Signal:** Write Enable command signal	O	DDR3L	SE	All Processor Lines
DDR0_VREF_DQ DDR1_VREF_DQ	**Memory Reference Voltage for DQ:**	O	A	SE	All Processor Lines
DDR_VREF_CA	**Memory Reference Voltage for Command & Address:**	O	A	SE	All Processor Lines

Table 6-3. LPDDR3 Memory Interface

Signal Name	Description	Dir.	Buffer Type	Link Type	Availability
DDR0_DQ[63:0] DDR1_DQ[63:0]	**Data Buses:** Data signals interface to the SDRAM data buses.	I/O	LPDDR3	SE	All Processor Lines
DDR0_DQSP[7:0] DDR0_DQSN[7:0] DDR1_DQSP[7:0] DDR1_DQSN[7:0]	**Data Strobes:** Differential data strobe pairs. The data is captured at the crossing point of DQS during read and write transactions.	I/O	LPDDR3	Diff	All Processor Lines
DDR0_CKN[1:0] DDR0_CKP[1:0] DDR1_CKN[1:0] DDR1_CKP[1:0]	**SDRAM Differential Clock:** Differential clocks signal pairs, pair per rank. The crossing of the positive edge of DDR0_CKP/DDR1_CKP and the negative edge of their complement DDR0_CKN / DDR1_CKN are used to sample the command and control signals on the SDRAM.	O	LPDDR3	Diff	All Processor Lines
DDR0_CKE[3:0] DDR1_CKE[3:0]	**Clock Enable:** (1 per rank) These signals are used to: • Initialize the SDRAMs during power-up. • Power-down SDRAM ranks. • Place all SDRAM ranks into and out of self-refresh during STR.	O	LPDDR3	SE	All Processor Lines.
DDR0_CS#[1:0] DDR1_CS#[1:0]	**Chip Select:** (1 per rank). These signals are used to select particular SDRAM components during the active state. There is one Chip Select for each SDRAM rank.	O	LPDDR3	SE	All Processor Lines
DDR0_ODT[3:0] DDR1_ODT[3:0]	**On Die Termination:** Active Termination Control.	O	LPDDR3	SE	For LPDDR3 only ODT[0] is in use. [0] applicable for Y-Processor Lines. [1:0] applicable for U Processor Line.
DDR0_CAA[9:0] DDR1_CAA[9:0]	**Command Address:** These signals are used to provide the multiplexed command and address to the SDRAM.	O	LPDDR3	SE	All Processor Lines
DDR0_CAB[9:0] DDR1_CAB[9:0]	**Command Address:** These signals are used to provide the multiplexed command and address to the SDRAM.	O	LPDDR3	SE	All Processor Lines
DDR0_VREF_DQ DDR1_VREF_DQ	**Memory Reference Voltage for DQ:**	O	A	SE	All Processor Lines
DDR_VREF_CA	**Memory Reference Voltage for Command & Address:**	O	A	SE	All Processor Lines

Table 6-4. DDR4 Memory Interface (Sheet 1 of 3)

Signal Name	Description	Dir.	Buffer Type	Link Type	Availability
DDR0_DQ[63:0] DDR1_DQ[63:0]	**Data Buses:** Data signals interface to the SDRAM data buses.	I/O	DDR4	SE	All Processor Lines
DDR0_DQSP[7:0] DDR0_DQSN[7:0] DDR1_DQSP[7:0] DDR1_DQSN[7:0]	**Data Strobes:** Differential data strobe pairs. The data is captured at the crossing point of DQS during read and write transactions.	I/O	DDR4	Diff	All Processor Lines

Table 6-4. DDR4 Memory Interface (Sheet 2 of 3)

Signal Name	Description	Dir.	Buffer Type	Link Type	Availability
DDR0_CKN[1:0] DDR0_CKP[1:0] DDR1_CKN[1:0] DDR1_CKP[1:0]	**SDRAM Differential Clock:** Differential clocks signal pairs, pair per rank. The crossing of the positive edge of DDR0_CKP/DDR1_CKP and the negative edge of their complement DDR0_CKN / DDR1_CKN are used to sample the command and control signals on the SDRAM.	O	DDR4	Diff	[1:0] applicable for All Processor Lines.
DDR0_CKE[1:0] DDR1_CKE[1:0]	**Clock Enable:** (1 per rank). These signals are used to: • Initialize the SDRAMs during power-up. • Power-down SDRAM ranks. • Place all SDRAM ranks into and out of self-refresh during STR (Suspend to RAM).	O	DDR4	SE	[1:0] applicable for All Processor Lines.
DDR0_CS#[1:0] DDR1_CS#[1:0]	**Chip Select:** (1 per rank). These signals are used to select particular SDRAM components during the active state. There is one Chip Select for each SDRAM rank.	O	DDR4	SE	[1:0] applicable for All Processor Lines.
DDR0_ODT[1:0] DDR1_ODT[1:0]	**On Die Termination:** (1 per rank). Active SDRAM Termination Control.	O	DDR4	SE	[0] applicable for Y-Processor Lines. [1:0] applicable for U and U- 4 Core Line processors
DDR0_MA[16:0] DDR1_MA[16:0]	**Address:** These signals are used to provide the multiplexed row and column address to the SDRAM. • A[16:14] use also as command signals, see ACT# signal description. • A10 is sampled during Read/Write commands to determine whether Autoprecharge should be performed to the accessed bank after the Read/Write operation. HIGH: Autoprecharge; LOW: no Autoprecharge). • A10 is sampled during a Precharge command to determine whether the Precharge applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by bank addresses. • A12 is sampled during Read and Write commands to determine if burst chop (on-the-fly) will be performed. HIGH, no burst chop; LOW: burst chopped).	O	DDR4	SE	All Processor Lines
DDR0_ACT# DDR1_ACT#	**Activation Command:** ACT# HIGH along with CS# determines that the signals addresses below have command functionality. A16 use as RAS# signal A15 use as CAS# signal A14 use as WE# signal	O	DDR4	SE	All Processor Lines
DDR0_BG[1:0] DDR1_BG[1:0]	**Bank Group:** BG[0:1] define to which bank group an Active, Read, Write or Precharge command is being applied. BG0 also determines which mode register is to be accessed during a MRS cycle.	O	DDR4	SE	All processor lines SO-DIMM, x8 DRAMs, x16 DDP DRAMs devices use BG[1:0]. x16 SDP DRAMs devices use BG[0]
DDR0_BA[1:0] DDR1_BA[1:0]	**Bank Address:** BA[1:0] define to which bank an Active, Read, Write or Precharge command is being applied. Bank address also determines which mode register is to be accessed during a MRS cycle.	O	DDR4	SE	All Processor Lines

Table 6-4. DDR4 Memory Interface (Sheet 3 of 3)

Signal Name	Description	Dir.	Buffer Type	Link Type	Availability
DDR0_ALERT# DDR1_ALERT#	**Alert:** This signal is used at command training only. It is getting the Command and Address Parity error flag during training. CRC feature is not supported.	I	DDR4	SE	All Processor Lines
DDR0_PAR DDR1_PAR	**Command and Address Parity:** These signals are used for parity check.	O	DDR4	SE	All Processor Lines
DDR_VREF_CA	**Memory Reference Voltage for Command & Address:**	O	A	SE	All Processor Lines

Table 6-5. System Memory Reference and Compensation Signals

Signal Name	Description	Dir.	Buffer Type	Link Type	Availability
DDR_RCOMP[2:0]	**System Memory Resistance Compensation:**	N/A	A	SE	All Processor Lines
OPC_RCOMP	**On-Package Cache resistance Compensation from processor:** Unconnected for Processors without OPC.	N/A	A	SE	Processors w/ on-package cache
OPCE_RCOMP	**On-Package Cache resistance Compensation from OPC:** Unconnected for Processors without OPC.	N/A	A	SE	Processors w/ on-package cache
DDR_VTT_CNTL	**System Memory Power Gate Control:** When signal is high – platform memory VTT regulator is enable, output high. When signal is low - Disables the platform memory VTT regulator in C8 and deeper and S3.	O	CMOS	SE	All Processor Lines

6.2 Reset and Miscellaneous Signals

Table 6-6. Reset and Miscellaneous Signals (Sheet 1 of 2)

Signal Name	Description	Dir.	Buffer Type	Link Type	Availability
CFG[19:0]	**Configuration Signals:** The CFG signals have a default value of '1' if not terminated on the board. Intel recommends placing test points on the board for CFG pins. • **CFG[0]**: Stall reset sequence after PCU PLL lock until de-asserted: — 1 = (Default) Normal Operation; No stall. — 0 = Stall. • **CFG[1]**: Reserved configuration lane. • **CFG[2]**: Reserved • **CFG[3]:** Reserved configuration lane. • **CFG[4]:** eDP enable: — 1 = Disabled. — 0 = Enabled. • **CFG[6:5]:** Reserved • **CFG[7]**: Reserved • **CFG[19:8]:** Reserved configuration lanes.	I	GTL	SE	All Processor Lines. .
CFG_RCOMP	**Configuration Resistance Compensation**	N/A	N/A	SE	All Processor Lines
PROC_POPIRCOMP	**POPIO Resistance Compensation**	N/A	N/A	SE	Y and U/U- 4 Core Processor Line

Table 6-6. Reset and Miscellaneous Signals (Sheet 2 of 2)

Signal Name	Description	Dir.	Buffer Type	Link Type	Availability
PROC_SELECT#	**Processor Select:** This pin is for compatibility with future platforms. It should be unconnected for this processor.			N/A	All Processor Lines

6.3 embedded DisplayPort* (eDP*) Signals

Table 6-7. embedded DisplayPort* Signals

Signal Name	Description	Dir.	Buffer Type	Link Type	Availability
eDP_TXP[3:0] eDP_TXN[3:0]	**embedded DisplayPort Transmit:** differential pair	O	eDP	Diff	All Processor Lines
eDP_AUXP eDP_AUXN	**embedded DisplayPort Auxiliary:** Half-duplex, bidirectional channel consist of one differential pair.	O	eDP	Diff	All Processor Lines
eDP_DISP_UTIL	**embedded DisplayPort Utility:** Output control signal used for brightness correction of embedded LCD displays with backlight modulation. This pin will co-exist with functionality similar to existing BKLTCTL pin on PCH	O	Async CMOS	SE	All Processor Lines
eDP_RCOMP	**DDI IO Compensation resistor, supporting DP*, eDP* and HDMI* channels.**	N/A	A	SE	All Processor Lines

6.4 Display Interface Signals

Table 6-8. Display Interface Signals

Signal Name	Description	Dir.	Buffer Type	Link Type	Availability[2]
DDI1_TXP[3:0] DDI1_TXN[3:0] DDI2_TXP[3:0] DDI2_TXN[3:0]	**Digital Display Interface Transmit:** Differential Pairs	O	DP/ HDMI*	Diff	All Processor Lines.
DDI1_AUXP DDI1_AUXN DDI2_AUXP DDI2_AUXN	**Digital Display Interface Display Port Auxiliary:** Half-duplex, bidirectional channel consist of one differential pair for each channel.	O	DP/ HDMI*	Diff	

Note:
1. For DDC signals, refer to the PCH UY Datasheet or PCH H Datasheet (See Related Documents section).
2. DDI3_AUXN and DDI3_AUXP are valid in U/U- 4 Core Processor Line but should be considered as reserved pins.

6.5 Testability Signals

Table 6-9. Testability Signals (Sheet 1 of 2)

Signal Name	Description	Dir.	Buffer Type	Link Type	Availability
BPM#[3:0]	**Breakpoint and Performance Monitor Signals:** Outputs from the processor that indicate the status of breakpoints and programmable counters used for monitoring processor performance.	I/O	GTL	SE	All Processor Lines

Table 6-9. Testability Signals (Sheet 2 of 2)

Signal Name	Description	Dir.	Buffer Type	Link Type	Availability
PROC_PRDY#	**Probe Mode Ready:** PROC_PRDY# is a processor output used by debug tools to determine processor debug readiness.	O	OD	SE	All Processor Lines
PROC_PREQ#	**Probe Mode Request:** PROC_PREQ# is used by debug tools to request debug operation of the processor.	I	GTL	SE	All Processor Lines
PROC_TCK	**Test Clock:** This signal provides the clock input for the processor Test Bus (also known as the Test Access Port). This signal should be driven low or allowed to float during power on Reset.	I	GTL	SE	All Processor Lines
PROC_TDI	**Test Data In:** This signal transfers serial test data into the processor. This signal provides the serial input needed for JTAG specification support.	I	GTL	SE	All Processor Lines
PROC_TDO	**Test Data Out:** This signal transfers serial test data out of the processor. This signal provides the serial output needed for JTAG specification support.	O	OD	SE	All Processor Lines
PROC_TMS	**Test Mode Select:** A JTAG specification support signal used by debug tools.	I	GTL	SE	All Processor Lines
PROC_TRST#	**Test Reset:** Resets the Test Access Port (TAP) logic. This signal should be driven low during power on Reset.	I	GTL	SE	All Processor Lines

6.6 Error and Thermal Protection Signals

Table 6-10. Error and Thermal Protection Signals

Signal Name	Description	Dir.	Buffer Type	Link Type	Availability
CATERR#	**Catastrophic Error:** This signal indicates that the system has experienced a catastrophic error and cannot continue to operate. The processor will set this signal for non-recoverable machine check errors or other unrecoverable internal errors. CATERR# is used for signaling the following types of errors: Legacy MCERRs, CATERR# is asserted for 16 BCLKs. Legacy IERRs, CATERR# remains asserted until warm or cold reset.	O	OD	SE	All Processor Lines
PECI	**Platform Environment Control Interface:** A serial sideband interface to the processor. It is used primarily for thermal, power, and error management. Details regarding the PECI electrical specifications, protocols and functions can be found in the RS-Platform Environment Control Interface (PECI) Specification, Revision 3.0.	I/O	PECI, Async	SE	All Processor Lines
PROCHOT#	**Processor Hot:** PROCHOT# goes active when the processor temperature monitoring sensor(s) detects that the processor has reached its maximum safe operating temperature. This indicates that the processor Thermal Control Circuit (TCC) has been activated, if enabled. This signal can also be driven to the processor to activate the TCC.	I/O	GTL I OD O	SE	All Processor Lines
THERMTRIP#	**Thermal Trip:** The processor protects itself from catastrophic overheating by use of an internal thermal sensor. This sensor is set well above the normal operating temperature to ensure that there are no false trips. The processor will stop all executions when the junction temperature exceeds approximately 130 °C. This is signaled to the system by the THERMTRIP# pin.	O	OD	SE	All Processor Lines

6.7 Power Sequencing Signals

Table 6-11. Power Sequencing Signals

Signal Name	Description	Dir.	Buffer Type	Link Type	Availability
PROCPWRGD	**Processor Power Good:** The processor requires this input signal to be a clean indication that the V_{CC} and V_{DDQ} power supplies are stable and within specifications. This requirement applies regardless of the S-state of the processor. 'Clean' implies that the signal will remain low (capable of sinking leakage current), without glitches, from the time that the power supplies are turned on until they come within specification. The signal should then transition monotonically to a high state.	I	CMOS	SE	All Processor Lines
VCCST_PWRGD	**VCCST Power Good:** The processor requires this input signal to be a clean indication that the VCCST and VDDQ power supplies are stable and within specifications. This signal should have a valid level during both S0 and S3 power states. 'Clean' implies that the signal will remain low (capable of sinking leakage current), without glitches, from the time that the power supplies are turned on until they come within specification. The signal should then transition monotonically to a high state.	I	CMOS	SE	All Processor Lines
PROC_DETECT# /SKTOCC#	**Processor Detect / Socket Occupied:** Pulled down directly (0 Ohms) on the processor package to the ground. There is no connection to the processor silicon for this signal. System board designers may use this signal to determine if the processor is present.	N/A	N/A	SE	All Processor Lines
VIDSOUT VIDSCK VIDALERT#	**VIDSOUT**, **VIDSCK, VIDALERT#:** These signals comprise a three-signal serial synchronous interface used to transfer power management information between the processor and the voltage regulator controllers.	I/O O I	I:GTL/O:OD OD CMOS	SE	All Processor Lines
MSM#	**Minimum Speed Mode:** Control signal to VccEOPIO VR (connected only in 2 VR solution for OPC).	O	CMOS	SE	Processors w/ on-package cache
ZVM#	**Zero Voltage Mode:** Control Signal to OPC VR, when low OPC VR output is 0V.	O	CMOS	SE	Processors w/ on-package cache

6.8 Processor Power Rails

Table 6-12. Processor Power Rails Signals

Signal Name	Description	Dir.	Buffer Type	Link Type	Availability
Vcc	Processor IA cores power rail	I	Power	—	All Processor Lines
$V_{CCG0/1}$	Processor IA cores gated power rail, connects to board capacitors for filtering.	I	Power	—	Y-Processor Line AML-Y22 Processor Line
Vcc_{GT}	Processor Graphics power rail	I	Power	—	All Processor Lines
Vcc_{GTX}	Processor Graphics power rail (extension)	I	Power	-	Processors w/ GT3
V_{DDQ}	System Memory power rail	I	Power	—	All Processor Lines
V_{DDQC}	System Memory clock power rail, feeds from VDDQ through LP filter.	I	Power	—	U/Y-Processor Lines AML-Y22 Processor Line
Vcc_{SA}	Processor System Agent power rail	I	Power	—	All Processor Lines
Vcc_{IO}	Processor I/O power rail. Consists of V_{CCIO} and Vcc_{IO_DDR}. V_{CCIO} and V_{CCIO_DDR} should be isolated from each other.	I	Power	—	All Processor Lines
Vcc_{ST}	Sustain voltage for processor standby modes	I	Power	—	All Processor Lines
Vcc_{STG}	Gated sustain voltage for processor standby modes	I	Power	—	KBL U/Y-Processor Lines AML-Y22 Processor Line
Vcc_{PLL}	Processor PLLs power rails	I	Power	—	All Processor Lines
Vcc_{PLL_OC}	Processor PLLs power rails	I	Power	—	All Processor Lines
Vcc_{OPC}	Processor OPC power rails	I	Power	-	Processors w/ on-package cache
Vcc_{OPC_1p8}	Processor OPC power rails	I	Power	-	Processors w/ on-package cache
Vcc_{EOPIO}	Processor OPC power rails	I	Power	-	Processors w/ on-package cache
Vcc_SENSE Vss_SENSE	Isolated, low impedance voltage sense pins. They can be used to sense or measure voltage near the silicon.	N/A	Power	—	All Processor Lines
Vcc_{GT}_SENSE Vss_{GT}_SENSE	Isolated, low impedance voltage sense pins. They can be used to sense or measure voltage near the silicon.	N/A	Power	—	All Processor Lines
Vcc_{GTx}_SENSE Vss_{GTx}_SENSE	Isolated, low impedance voltage sense pins. They can be used to sense or measure voltage near the silicon.	N/A	Power	-	Processors w/ GT3
Vcc_{IO}_SENSE Vss_{IO}_SENSE	Isolated, low impedance voltage sense pins. They can be used to sense or measure voltage near the silicon.	N/A	Power	—	All Processor Lines
Vcc_{SA}_SENSE Vss_{SA}_SENSE	Isolated, low impedance voltage sense pins. They can be used to sense or measure voltage near the silicon.	N/A	Power	—	All Processor Lines
Vcc_{OPC}_SENSE Vss_{OPC}_SENSE	Isolated, low impedance voltage sense pins. They can be used to sense or measure voltage near the silicon.	N/A	Power	-	Processors w/ on-package cache
Vcc_{EOPIO}_SENSE Vss_{EOPIO}_SENSE	Isolated, low impedance voltage sense pins. They can be used to sense or measure voltage near the silicon.	N/A	Power	-	Processors w/ on-package cache

6.9 Ground, Reserved and Non-Critical to Function (NCTF) Signals

The following are the general types of reserved (RSVD) signals and connection guidelines:

- RSVD – these signals should not be connected
- RSVD_TP – these signals should be routed to a test point
- RSVD_NCTF – these signals are non-critical to function and may be left un-connected

Arbitrary connection of these signals to VCC, VDDQ, VSS, or to any other signal (including each other) may result in component malfunction or incompatibility with future processors. See Table 6-13, “GND, RSVD, and NCTF Signals”.

For reliable operation, always connect unused inputs or bi-directional signals to an appropriate signal level. Unused active high inputs should be connected through a resistor to ground (V_{SS}). Unused outputs may be left unconnected however, this may interfere with some Test Access Port (TAP) functions, complicate debug probing and prevent boundary scan testing. A resistor should be used when tying bi-directional signals to power or ground. When tying any signal to power or ground, the resistor can also be used for system testability.

Table 6-13. GND, RSVD, and NCTF Signals

Signal Name	Description
Vss	Processor ground node
Vss_NCTF	**Non-Critical To Function:** These signals are for package mechanical reliability.
RSVD	**Reserved**: All signals that are RSVD should not be connected on the board.
RSVD_NCTF	**RSVD_NCTF**: RSVD_NCTF should not be connected on the board.
RSVD_TP	**RSVD_TP**: Intel recommends to route each RSVD_TP to an accessible test point. Intel may require these test points for platform specific debug. Leaving these test points inaccessible could delay debug by Intel.

6.10 Processor Internal Pull-Up / Pull-Down Terminations

Table 6-14. Processor Internal Pull-Up / Pull-Down Terminations

Signal Name	Pull Up/Pull Down	Rail	Value
BPM[3:0]	Pull Up / Pull Down	Vcc_{IO}	16-60 ohms
PREQ#	Pull Up	Vcc_{ST}	3 kohms
PROC_TDI	Pull Up	Vcc_{STG}	3 kohms
PROC_TMS	Pull Up	Vcc_{STG}	3 kohms
PROC_TRSN#	Pull Down	-	3 kohms
CFG[19:0]	Pull Up	Vcc_{IO}	3 kohms

7 Electrical Specifications

7.1 Processor Power Rails

Table 7-1. Processor Power Rails

Power Rail	Description	Control	Availability
V_{CC}	Processor IA Cores Power Rail	SVID	All Processor Lines
Vcc_{GT}	Processor Graphics Power Rails	SVID	All Processor Lines
Vcc_{GTX} Note 2,6	Processor Graphics Extended Power Rail	SVID	Processors w/ GT3
Vcc_{SA}	System Agent Power Rail	SVID/Fixed (SKU dependent)	All Processor Lines
Vcc_{IO}	IO Power Rail	Fixed	All Processor Lines
Vcc_{ST}	Sustain Power Rail	Fixed	All Processor Lines
Vcc_{STG} 5	Sustain Gated Power Rail	Fixed	U/Y-Processor Lines AML-Y22 Processor Line
Vcc_{PLL}	Processor PLLs power Rail	Fixed	All Processor Lines
Vcc_{PLL_OC} 4	Processor PLLs OC power Rail	Fixed	All Processor Lines
V_{DDQ}	Integrated Memory Controller Power Rail	Fixed (Memory technology dependent)	All Processor Lines
Vcc_{OPC} 3	Processor OPC power Rail	Fixed	Processors w/OPC
Vcc_{OPC_1P8} 3	Processor OPC power Rail	Fixed	Processors w/OPC
Vcc_{EOPIO} 3	Processor EOPIO power Rail	Fixed	Processors w/OPC

Notes:
1. N/A
2. Rail is unconnected for Processors without GT3.
3. Rail is unconnected for Processors without OPC.
4. Vcc_{PLL_OC} power rail should be sourced from the VDDQ VR. The connection can be direct or through a load switch, depending desired power optimization. In case of direct connection (Vcc_{PLL_OC} is shorted to V_{DDQ}, no load switch), platform should ensure that Vcc_{ST} is ON (high) while Vcc_{PLL_OC} is ON (high).
5. Vcc_{STG} power rail should be sourced from the VR as V_{CCST}. The connection can be direct or through a load switch, depending desired power optimization.
6. Intel has added the option of merging the GT/GTx power rails for the U-Processor Line GT3 product family.

7.1.1 Power and Ground Pins

All power pins should be connected to their respective processor power planes, while all VSS pins should be connected to the system ground plane. Use of multiple power and ground planes is recommended to reduce I*R drop.

7.1.2 V_{CC} Voltage Identification (VID)

Intel processors/chipsets are individually calibrated in the factory to operate on a specific voltage/frequency and operating-condition curve specified for that individual processor. In normal operation, the processor autonomously issues voltage control requests according to this calibrated curve using the serial voltage-identifier (SVID) interface. Altering the voltage applied at the processor/chipset causing operation outside of this calibrated curve is considered out-of-specification operation.

The SVID bus consists of three open-drain signals: clock, data, and alert# to both set voltage-levels and gather telemetry data from the voltage regulators. Voltages are controlled per an 8-bit integer value, called a VID, that maps to an analog voltage level. An offset field also exists that allows altering the VID table. Alert can be used to inform the processor that a voltage-change request has been completed or to interrupt the processor with a fault notification.

7.2 DC Specifications

The processor DC specifications in this section are defined at the processor signal pins, unless noted otherwise.

- The DC specifications for the DDR3L/-RS/LPDDR3/DDR4 signals are listed in the *Voltage and Current Specifications* section.
- The *Voltage and Current Specifications* section lists the DC specifications for the processor and are valid only while meeting specifications for junction temperature, clock frequency, and input voltages. Read all notes associated with each parameter.
- AC tolerances for all DC rails include dynamic load currents at switching frequencies up to 1 MHz.

7.2.1 Processor Power Rails DC Specifications

7.2.1.1 Vcc DC Specifications

Table 7-2. Processor IA core (Vcc) Active and Idle Mode DC Voltage and Current Specifications (Sheet 1 of 3)

Symbol	Parameter	Segment	Min	Typ	Max	Unit	Note[1]
Operating Voltage	Voltage Range for Processor Operating Modes	All		—	1.52	V	1, 2, 3, 7, 12
Icc_{MAX} (U/Y-Processors)	Maximum Processor IA Core I_{CC}	Y-Processor Line (4.5W)	—	—	24	A	4, 6, 7, 11
		Y-Processor Line (6W) Pentium/Celeron	—	—	24		
		AML-Y22 Processor Line (5W)	—	—	28		
		U-Processor Line (15W) - 2 Core GT2,GT1	—	—	32		
		U-Processor Line (15W) - 2 Core GT1 Pentium/Celeron	—	—	29		
		U-Processor Line (15W) - 4 Core GT2 (U- 4 Core)	—	—	64		
		U-Processor Line (15W) - 2 Core GT3+OPC	—	—	32		
		U-Processor Line (28W) - 2 Core GT3+OPC	—	—	32		

Table 7-2. Processor IA core (Vcc) Active and Idle Mode DC Voltage and Current Specifications (Sheet 2 of 3)

Symbol	Parameter	Segment	Min	Typ	Max			Unit	Note[1]
TOB_{VCC}	Voltage Tolerance	PS0, PS1	—	—	±20			mV	3, 6, 8
		PS2, PS3	—	—	±20				
Ripple	Ripple Tolerance				$I_L <= 0.5$	$0.5 < I_L < Icc_{TDC}$	$Icc_{TDC} < I_L < Icc_{MAX}$	mV	3, 6, 8
		PS0	—	—	+30/-10	±10	±15		
		PS1	—	—	+30/-10	±15	±15		
		PS2	—	—	+30/-10	+30/-10	+30/-10		
		PS3	—	—	+30/-10	+30/-10	+30/-10		
DC_LL (U/Y-Processors)	Loadline slope within the VR regulation loop capability	Y-Processor Line	—	—	5.9			mΩ	10, 13, 14
		AML-Y22 Processor Line (5W)	—	—	4				
		U-Processor Line - 2 Core GT2,GT1	—	—	2.4				
		U-Processor Line (U-4 Core) - 4-Core			2.4				
		U-Processor Line - 2 Core GT3 with OPC			2.4				
AC_LL (Y/U-Processors)	AC Loadline	U-Processor Lines	—	—	Same as Max DC_LL (up to 1MHz)			mΩ	10,13, 14
AC_LL (Y-Processors)	AC Loadline	AML-Y22-Processor Line	—	—	• 1MHz – 2MHz: Increasing linearly with log (frequency) from 4 to 6 • 2MHz – 20MHz: 6 • 20MHz – 30MHz: Increasing linearly with log (frequency) from 6 to 15.5 • 30MHz – 40MHz: 15.5			mΩ	10, 13, 14,15
AC_LL (Y-Processors)	AC Loadline	Y-Processor Line	—	—	• 1MHz – 2MHz: 5.9 • 2MHz – 4MHz:Increasing linearly with log (frequency) from 5.9 to 11.7 • 4MHz – 20MHz: 11.7 • 20MHz – 30MHz: Increasing linearly with log (frequency) from 11.7 to 18.3 • 30MHz – 40MHz: 18.3			mΩ	10, 13, 14,15
T_OVS_TDP_MAX	Max Overshoot time **TDP/virus mode**	—	—	—	10/30			µs	
V_OVS TDP_MAX/ virus_MAX	Max Overshoot at **TDP/virus mode**	—	—	—	70/200			mV	

Table 7-2. Processor IA core (Vcc) Active and Idle Mode DC Voltage and Current Specifications (Sheet 3 of 3)

Symbol	Parameter	Segment	Min	Typ	Max	Unit	Note[1]

Notes:

1. Unless otherwise noted, all specifications in this table are based on estimates and simulations or empirical data. These specifications will be updated with characterized data from silicon measurements at a later date.
2. Each processor is programmed with a maximum valid voltage identification value (VID) that is set at manufacturing and cannot be altered. Individual maximum VID values are calibrated during manufacturing such that two processors at the same frequency may have different settings within the VID range. Note that this differs from the VID employed by the processor during a power management event (Adaptive Thermal Monitor, Enhanced Intel SpeedStep Technology, or low-power states).
3. The voltage specification requirements are measured across Vcc_SENSE and Vss_SENSE as near as possible to the processor with an oscilloscope set to 100-MHz bandwidth, 1.5 pF maximum probe capacitance, and 1 MΩ minimum impedance. The maximum length of ground wire on the probe should be less than 5 mm. Ensure external noise from the system is not coupled into the oscilloscope probe.
4. Processor IA core VR to be designed to electrically support this current.
5. Processor IA core VR to be designed to thermally support this current indefinitely.
6. Long term reliability cannot be assured if tolerance, ripple, and core noise parameters are violated.
7. Long term reliability cannot be assured in conditions above or below Max/Min functional limits.
8. PSx refers to the voltage regulator power state as set by the SVID protocol.
9. N/A
10. LL measured at sense points.
11. Typ column represents Icc_{MAX} for commercial application it is NOT a specification - it is a characterization of limited samples using limited set of benchmarks that can be exceeded.
12. Operating voltage range in steady state.
13. LL specification values should not be exceeded. If exceeded, power, performance and reliability penalty are expected.
14. Load Line (AC/DC) should be measured by the VRTT tool and programmed accordingly using the BIOS Load Line override setup options. AC/DC Load Line BIOS programming directly affects operating voltages (AC) and power measurements (DC). A superior board design with a shallower AC Load Line can improve on power, performance, and thermals compared to boards designed for POR impedance.
15. For more details on AML-Y22 loadline target, refer to Power Integrity Model Set Doc ID# 597383.

7.2.1.2 Vcc_{GT} and Vcc_{GTX} DC Specifications

Table 7-3. Processor Graphics ($Vcc_{GT}$and Vcc_{GTX}) Supply DC Voltage and Current Specifications (Sheet 1 of 2)

Symbol	Parameter	Segment	Min	Typ	Max	Unit	Note[1]
Operating voltage	Active voltage Range for Vcc_{GT}	All	0	—	1.52	V	2,3,6, 8
Icc_{MAX_GT}/ Icc_{MAX_GTx} (U/Y-Processors)	Max. Current for Processor Graphics Rail	Y-Processor Line (4.5W)	—	—	24	A	6
		AML-Y22- Processor Line (5W)	—	—	24		
		Y-Processor Line (6W) Pentium/Celeron	—	—			
		U-Processor Line (15W) - 2 Core GT2,GT1	—	—	31		
		U-Processor Line (15W) - 4 Core GT2 (U-4 Core)	—	—	31		
		U-Processor Line (15W) - 2 Core GT1 Pentium/Celeron	—	—	31		
		U-Processor Line (15,28W)- 2 Core GT3 with OPC	—	—	Merged: 64(GT+GTx) Separate: GT-57/GTx-19		6,11, 12
TOB_{GT}	Vcc_{GT} Tolerance	PS0,PS1	—	—	±20	mV	3, 4
		PS2,PS3	—	—	±20	mV	3, 4

Table 7-3. Processor Graphics (Vcc_{GT} and Vcc_{GTX}) Supply DC Voltage and Current Specifications (Sheet 2 of 2)

Symbol	Parameter	Segment	Min	Typ	Max			Unit	Note[1]
Ripple	Ripple Tolerance	—			$I_L <= 0.5$	$0.5 < I_L < Icc_{TDC}$	$Icc_{TDC} < I_L < Icc_{MAX}$	mV	3,4
		PS0	—	—	+30/-10	±10	±15		
		PS1	—	—	+30/-10	±15	±15		
		PS2	—	—	+30/-10	+30/-10	+30/-10		
		PS3	—	—	+30/-10	+30/-10	+30/-10		
DC_LL (UY-Processor)	Vcc_{GT} Loadline slope	Y/AML-Y22 -Processor Line	—	4.2	5.7			mΩ	7, 9, 10
		U- 2 Core GT2, GT1	—	—	3.1				
		U- 4 Core GT2 (U- 4 Core)	—	—	3.1				
		U- 2 Core GT3+OPC	—	—	2/6.0(GTx)				
AC_LL (Y/U-Processors)	AC Loadline	U-Processor Line	—	—	Same as Max DC_LL (up to 1MHz)			mΩ	7,9, 10,13
AC_LL (Y-Processors)	AC Loadline	Y/AML-Y22 -Processor Line	—	—	• 1MHz – 3MHz: 5.7 • 3MHz – 10MHz: Increasing linearly with log (frequency) from 5.7 to 12.1 • 10MHz – 40MHz: 12.1			mΩ	7,9, 10,13
T_OVS_MAX	Max Overshoot time	—	—	—	10			µs	
V_OVS_MAX	Max Overshoot	—	—	—	70			mV	

Notes:

1. Unless otherwise noted, all specifications in this table are based on estimates and simulations or empirical data. These specifications will be updated with characterized data from silicon measurements at a later date.
2. Each processor is programmed with a maximum valid voltage identification value (VID), which is set at manufacturing and cannot be altered. Individual maximum VID values are calibrated during manufacturing such that two processors at the same frequency may have different settings within the VID range. This differs from the VID employed by the processor during a power or thermal management event (Intel Adaptive Thermal Monitor, Enhanced Intel SpeedStep Technology, or low-power states).
3. The voltage specification requirements are measured across Vcc_{GT_SENSE} and Vss_{GT_SENSE} as near as possible to the processor with an oscilloscope set to 100-MHz bandwidth, 1.5 pF maximum probe capacitance, and 1 MΩ minimum impedance. The maximum length of ground wire on the probe should be less than 5 mm. Ensure external noise from the system is not coupled into the oscilloscope probe.
4. PSx refers to the voltage regulator power state as set by the SVID protocol.
5. Each processor is programmed with a maximum valid voltage identification value (VID), which is set at manufacturing and cannot be altered. Individual maximum VID values are calibrated during manufacturing such that two processors at the same frequency may have different settings within the VID range. This differs from the VID employed by the processor during a power or thermal management event (Intel Adaptive Thermal Monitor, Enhanced Intel SpeedStep Technology, or low-power states).
6. N/A
7. LL measured at sense points.
8. Operating voltage range in steady state.
9. LL specification values should not be exceeded. If exceeded, power, performance and reliability penalty are expected.
10. Load Line (AC/DC) should be measured by the VRTT tool and programmed accordingly using the BIOS Load Line override setup options. AC/DC Load Line BIOS programming directly affects operating voltages (AC) and power measurements (DC). A superior board design with a shallower AC Load Line can improve on power, performance, and thermals compared to boards designed for POR impedance.
11. N/A
12. For merged GT/GTx rails the sense point need to be taken from Vcc_{GT}_SENSE/VSSGT_SENSE, the Vcc_{GTx_SENSE}/Vss_{GTx_SENSE} should be unconnected (not connected).For more details on AML-Y22 loadline target, refer to Power Integrity Model Set Doc ID# 597383..

7.2.1.3 V_{DDQ} DC Specifications

Table 7-4. Memory Controller (V_{DDQ}) Supply DC Voltage and Current Specifications

Symbol	Parameter	Segment	Min	Typ	Max	Unit	Note[1]
$V_{DDQ\ (DDR3L/-RS)}$	Processor I/O supply voltage for DDR3L/-RS	All	Typ-5%	1.35	Typ+5%	V	3,4,5
$V_{DDQ\ (LPDDR3)}$	Processor I/O supply voltage for LPDDR3	All	Typ-5%	1.20	Typ+5%	V	3, 4, 5
$V_{DDQ\ (DDR4)}$	Processor I/O supply voltage for DDR4	All	Typ-5%	1.20	Typ+5%	V	3, 4, 5
TOB_{VDDQ}	VDDQ Tolerance	All	AC+DC:± 5			%	3, 4, 6
Icc_{MAX_VDDQ} (DDR3L/-RS)	Max Current for V_{DDQ} Rail (DDR3L/-RS)	U	—	—	2	A	2
		—	—	—	—		
Icc_{MAX_VDDQ} (LPDDR3)	Max Current for V_{DDQ} Rail (LPDDR3)	Y/AML-Y22	—	—	2	A	2
		U	—	—	2		
		—	—	—			
Icc_{MAX_VDDQ} (DDR4)	Max Current for V_{DDQ} Rail (DDR4)	U	—	—	2.8	A	2

Notes:
1. Unless otherwise noted, all specifications in this table are based on estimates and simulations or empirical data. These specifications will be updated with characterized data from silicon measurements at a later date.
2. The current supplied to the DIMM modules is not included in this specification.
3. Includes AC and DC error, where the AC noise is bandwidth limited to under 100 MHz, measured on package pins.
4. No requirement on the breakdown of AC versus DC noise.
5. The voltage specification requirements are measured as near as possible to the processor with an oscilloscope set to 100-MHz bandwidth, 1.5 pF maximum probe capacitance, and 1 MΩ minimum impedance. The maximum length of ground wire on the probe should be less than 5 mm. Ensure external noise from the system is not coupled into the oscilloscope probe.For Voltage less than 1v, TOB will be 50 mv.

7.2.1.4 Vcc_{SA} DC Specifications

Table 7-5. System Agent (Vcc_{SA}) Supply DC Voltage and Current Specifications (Sheet 1 of 2)

Symbol	Parameter	Segment	Min	Typ	Max	Unit	Note[1,2]
Vcc_{SA} (U/Y-Processors)	Voltage for the System Agent	Y/AML-Y22 -Processor Line	0	—	1.52	V	3, 5
		U-Processor Line	0	—	1.52		
TOB_{VCCSA}	Vcc_{SA} Tolerance	U/Y/AML-Y22 -Processor Lines	0	—	±20	mV	3
		-	0	—	-	%	3, 11
I_{CCMAX_VCCSA}	Max Current for V_{CCSA} Rail	Y/AML-Y22 -Processor Line	—	—	4.1	A	
		U- 2 Core GT2	—	—	4.5		9
		U- 2 Core GT3+OPC	—	—	5.1		10
			—	—	6		
DC_LL	Vcc_{SA} Loadline	Y/AML-Y22-Processor Line	—	14	18	mΩ	6, 7, 8
		U/U- 4 Core Processor Line	—	—	10.3		
AC_LL	AC Loadline	U/-Processor Line	—	—	Same as Max DC_LL (up to 1MHz)	mΩ	6, 7, 8,12
AC_LL	AC Loadline	Y/AML-Y22 -Processor Line	—	—	• 1MHz – 2MHz: Increasing linearly with log (frequency) from 18 to 42.6 • 2MHz – 40MHz: 42.6	mΩ	6, 7, 8,12

Table 7-5. System Agent (Vcc_{SA}) Supply DC Voltage and Current Specifications (Sheet 2 of 2)

Symbol	Parameter	Segment	Min	Typ	Max			Unit	Note[1,2]
Ripple	Ripple Tolerance	U/Y-Processor Lines			$I_L <= 0.5$	$0.5 < I_L < Icc_{TDC}$	$I_{CCTDC} < I_L < Icc_{MAX}$	mV	3, 4
		PS0	—	—	+30/-10	±10	±15		
		PS1	—	—	+30/-10	±15	±15		
		PS2	—	—	+30/-10	+30/-10	+30/-10		
		PS3	—	—	+30/-10	+30/-10	+30/-10		
T_OVS_MAX	Max Overshoot time	—	—	—	10			µs	
V_OVS_MAX	Max Overshoot	—	—	—	70			mV	

Notes:

1. Unless otherwise noted, all specifications in this table are based on estimates and simulations or empirical data. These specifications will be updated with characterized data from silicon measurements at a later date.
2. Long term reliability cannot be assured in conditions above or below Max/Min functional limits.
3. The voltage specification requirements are measured across Vcc_{SA_SENSE} and Vss_{SA_SENSE} as near as possible to the processor with an oscilloscope set to 100-MHz bandwidth, 1.5 pF maximum probe capacitance, and 1 MΩ minimum impedance. The maximum length of ground wire on the probe should be less than 5 mm. Ensure external noise from the system is not coupled into the oscilloscope probe.
4. PSx refers to the voltage regulator power state as set by the SVID protocol.
5. Vcc_{SA} voltage during boot (Vboot)1.05V for a duration of 2 seconds.
6. LL measured at sense points.
7. LL specification values should not be exceeded. If exceeded, power, performance and reliability penalty are expected.
8. Load Line (AC/DC) should be measured by the VRTT tool and programmed accordingly using the BIOS Load Line override setup options. AC/DC Load Line BIOS programming directly affects operating voltages (AC) and power measurements (DC). A superior board design with a shallower AC Load Line can improve on power, performance, and thermals compared to boards designed for POR impedance.
9. IPU designs with U-Processor Line Pentium/Celeron require additional 0.5A, SA Icc_{MAX}=5A.
10. U-Processor Line GT2+OPC 28W IPU designs will require additional 2A, SA Icc_{MAX} when using IPU=7.1AFor Voltage less than 1V, TOB will be 50 mV.
11. For more details on AML-Y22 loadline target, refer to Power Integrity Model Set Doc ID# 597383.

7.2.1.5 Vcc_{IO} DC Specifications

Table 7-6. Processor I/O (Vcc_{IO}) Supply DC Voltage and Current Specifications

Symbol	Parameter	Segment	Min	Typ	Max	Unit	Note[1,2]
Vcc_{IO}	Voltage for the memory controller and shared cache	Y/AML-Y22	—	0.85/0.95	—	V	3, 4, 5, 6
		U	—	0.95	—		
		—	—	—	—		
TOB_{VCCIO}	Vcc_{IO} Tolerance	All	+/-5 (AC + DC + Ripple) Up to 1 MHz			%	3, 8
Icc_{MAX_VCCIO}	Max Current for V_{CCIO} Rail	Y/AML-Y22	—	—	3	A	
		U	—	—	3.1		
T_OVS_MAX	Max Overshoot time	All	—	—	100	µS	7
V_OVS_MAX	Max Overshoot at TDP	All	—	—	20	mV	7

Notes:
1. Unless otherwise noted, all specifications in this table are based on estimates and simulations or empirical data. These specifications will be updated with characterized data from silicon measurements at a later date.
2. Long term reliability cannot be assured in conditions above or below Max/Min functional limits.
3. The voltage specification requirements are measured across Vcc_{IO_SENSE} and Vss_{IO_SENSE} as near as possible to the processor with an oscilloscope set to 100-MHz bandwidth, 1.5 pF maximum probe capacitance, and 1 MΩ minimum impedance. The maximum length of ground wire on the probe should be less than 5 mm. Ensure external noise from the system is not coupled into the oscilloscope probe.
4. For low BW bus connection between processor and PCH -> Vcc_{IO}=0.85V.
5. For high BW bus connection between processor and PCH -> Vcc_{IO}=0.95V.
6. For KBL-Y and AML Y-Processor Line, Setting Vcc_{IO} to 0.95V may lead to a power penalty up to 250mW.
7. OS occurs during power on only, **not** during normal operation.For Voltage less than 1v, TOB will be +/-50mV (AC + DC + Ripple) up to 1 MHz

7.2.1.6 Vcc_{OPC} DC Specifications

OPC VR output voltage is fixed to 1V, the processor can drive VR to LPM (Low Power Mode) which sets VR output to 0V using ZVM# signal as shown in the following table.

Table 7-7. VCC_{OPC} Voltage levels

ZVM# State	VCC_{OPC}	Units
0	0	V
1	1.0	V

Table 7-8. Processor OPC (Vcc_{OPC}) Supply DC Voltage and Current Specifications (Sheet 1 of 2)

Symbol	Parameter	Segment	Min	Typ	Max	Unit	Note[1,2]
Vcc_{OPC}	Voltage for the on-package cache	Processor Line w/OPC	—	1.0	—	V	3
TOB_{VCCOPC}	Vcc_{OPC} Tolerance	Processor Line w/OPC	AC+DC:± 5			%	3, 5
Icc_{MAX_VCCOPC}	Max Current for V_{CCOPC} Rail	Processor Line w/OPC	—	—	3.2	A	
T_OVS_MAX	Max Overshoot time	All	—	—	100	µS	4
V_OVS_MAX	Max Overshoot at TDP	All	—	—	20	mV	4

Table 7-8. Processor OPC (Vcc_{OPC}) Supply DC Voltage and Current Specifications (Sheet 2 of 2)

Symbol	Parameter	Segment	Min	Typ	Max	Unit	Note[1,2]

Notes:
1. Unless otherwise noted, all specifications in this table are based on estimates and simulations or empirical data. These specifications will be updated with characterized data from silicon measurements at a later date.
2. Long term reliability cannot be assured in conditions above or below Max/Min functional limits.
3. The voltage specification requirements are measured across Vcc_{OPC_SENSE} and Vss_{OPC_SENSE} as near as possible to the processor with an oscilloscope set to 100-MHz bandwidth, 1.5 pF maximum probe capacitance, and 1 MΩ minimum impedance. The maximum length of ground wire on the probe should be less than 5 mm. Ensure external noise from the system is not coupled into the oscilloscope probe.
4. OS occurs during power on only, **not** during normal operation.
5. For Voltage less than 1V, TOB will be 50 mV.

7.2.1.7 Vcc_{EOPIO} DC Specifications

Vcc_{EOPIO} may be connected to OPC VR. The processor can drive VR to LPM (Low Power Mode) which sets VR output to 0V using ZVM# signal (as shown in Table 7-9, "VCC_{EOPIO} Voltage levels (separate VR)").

Table 7-9. VCC_{EOPIO} Voltage levels (separate VR)

ZVM# state	MSM# state	VCC_{EOPIO}	Units
0	X	0	V
1	1	1.0	V

Table 7-10. Processor EOPIO (Vcc_{EOPIO}) Supply DC Voltage and Current Specifications

Symbol	Parameter	Segment	Min	Typ	Max	Unit	Note[1,2]
Vcc_{EOPIO}	Voltage for the EOPIO interface	U-Processor Line GT3 with OPC	—	1.0	—	V	3
$TOB_{VCCEOPIO}$	Vcc_{EOPIO} Tolerance		AC+DC: ± 5			%	3, 5
$Icc_{MAX\_VCCEOPIO}$	Max Current for $V_{CCEOPIO}$ Rail		—	—	2	A	
T_OVS_MAX	Max Overshoot time		—	—	100	µS	4
V_OVS_MAX	Max Overshoot at TDP		—	—	20	mV	4

Notes:
1. Unless otherwise noted, all specifications in this table are based on estimates and simulations or empirical data. These specifications will be updated with characterized data from silicon measurements at a later date.
2. Long term reliability cannot be assured in conditions above or below Max/Min functional limits.
3. The voltage specification requirements are measured across Vcc_{EOPIO_SENSE} and Vss_{EOPIO_SENSE} as near as possible to the processor with an oscilloscope set to 100-MHz bandwidth, 1.5 pF maximum probe capacitance, and 1 MΩ minimum impedance. The maximum length of ground wire on the probe should be less than 5 mm. Ensure external noise from the system is not coupled into the oscilloscope probe.
4. OS occurs during power on only, **not** during normal operation.
5. For Voltage less than 1V, TOB will be 50 mV.

7.2.1.8 Vcc_{OPC_1p8} DC Specifications

Table 7-11. Processor OPC (Vcc_{OPC_1p8}) Supply DC Voltage and Current Specifications

Symbol	Parameter	Segment	Min	Typ	Max	Unit	Note[1,2]
Vcc_{OPC_1p8}	Voltage for the on-package cache	U-Processor Line GT3 with OPC	—	1.8	—	V	3
$TOB_{VCC\_OPC\_1p8}$	Vcc_{OPC_1p8} Tolerance		AC+DC: ± 5			%	3, 4
$Icc_{MAX\_VCC\_OPC\_1p8}$	Max Current for $V_{CC\_OPC\_1p8}$ Rail		—	—	50	mA	

Table 7-11. Processor OPC (Vcc_{OPC_1p8}) Supply DC Voltage and Current Specifications

Symbol	Parameter	Segment	Min	Typ	Max	Unit	Note[1,2]
Notes: 1. Unless otherwise noted, all specifications in this table are based on estimates and simulations or empirical data. These specifications will be updated with characterized data from silicon measurements at a later date. 2. Long term reliability cannot be assured in conditions above or below Max/Min functional limits. 3. The voltage specification requirements are measured as near as possible to the processor with an oscilloscope set to 100-MHz bandwidth, 1.5 pF maximum probe capacitance, and 1 MΩ minimum impedance. The maximum length of ground wire on the probe should be less than 5 mm. Ensure external noise from the system is not coupled into the oscilloscope probe. 4. For Voltage less than 1V, TOB will be 50 mV.							

7.2.1.9 Vcc_{ST} DC Specifications

Table 7-12. Vcc Sustain (Vcc_{ST}) Supply DC Voltage and Current Specifications

Symbol	Parameter	Segment	Min	Typ	Max	Units	Notes [1,2]
Vcc_{ST}	Processor Vcc Sustain supply voltage	All	—	1.0	—	V	3
TOB_{ST}	Vcc_{ST} Tolerance	All	AC+DC: ± 5			%	3, 4
Icc_{MAX_ST}	Max Current for Vcc_{ST}	Y/AML-Y22-Processor Line	—	—	60	mA	
		U-Processor Line	—	—			
			—	—			
Notes: 1. Unless otherwise noted, all specifications in this table are based on estimates and simulations or empirical data. These specifications will be updated with characterized data from silicon measurements at a later date. 2. Long term reliability cannot be assured in conditions above or below Max/Min functional limits. 3. The voltage specification requirements are measured on package pins as near as possible to the processor with an oscilloscope set to 100-MHz bandwidth, 1.5 pF maximum probe capacitance, and 1 MΩ minimum impedance. The maximum length of ground wire on the probe should be less than 5 mm. Ensure external noise from the system is not coupled into the oscilloscope probe.For Voltage less than 1V, TOB will be 50 mV.							

Table 7-13. Vcc Sustain Gated (Vcc_{STG}) Supply DC Voltage and Current Specifications

Symbol	Parameter	Segment	Min	Typ	Max	Units	Notes [1,2]
Vcc_{STG}	Processor Vcc Sustain supply voltage	All	—	1.0	—	V	3
TOB_{STG}	Vcc_{STG} Tolerance	All	AC+DC: ± 5			%	3, 4
Icc_{MAX_STG}	Max Current for Vcc_{STG}	Y/AML-Y22 -Processor Line	—	—	20	mA	
		U-Processor Line	—	—			
			—	—			
Notes: 1. Unless otherwise noted, all specifications in this table are based on estimates and simulations or empirical data. These specifications will be updated with characterized data from silicon measurements at a later date. 2. Long term reliability cannot be assured in conditions above or below Max/Min functional limits. 3. The voltage specification requirements are measured on package pins as near as possible to the processor with an oscilloscope set to 100-MHz bandwidth, 1.5 pF maximum probe capacitance, and 1 MΩ minimum impedance. The maximum length of ground wire on the probe should be less than 5 mm. Ensure external noise from the system is not coupled into the oscilloscope probe.For Voltage less than 1V, TOB will be 50 mV.							

7.2.1.10 Vcc_{PLL} DC Specifications

Table 7-14. Processor PLL (Vcc_{PLL}) Supply DC Voltage and Current Specifications

Symbol	Parameter	Segment	Min	Typ	Max	Unit	Notes[1,2]
Vcc_{PLL}	PLL supply voltage (DC + AC specification)	All	—	1.0	—	V	3,7
TOB_{VCCPLL}	Vcc_{PLL} Tolerance	All	VCC_{PLLmax} > AC+DC > VCC_{PLLmin}			V	3,4,5,6,7
LPF	Noise Filtering for Vcc_{PLL}	All	A low pass filter or behavior like is required, the low pass filter requirements are 150KHz cut-off frequency and -20dB/Decade attenuation for higher frequencies.				5,6
Icc_{MAX_VCCPLL}	Max Current for Vcc_{PLL} Rail	Y/AML-Y22 -Processor Line	—	—	100	mA	
		U-Processor Line	—	—	130		
		4	—	—	130		

Notes:
1. Unless otherwise noted, all specifications in this table are based on estimates and simulations or empirical data. These specifications will be updated with characterized data from silicon measurements at a later date.
2. Long term reliability cannot be assured in conditions above or below Max/Min functional limits.
3. The voltage specification requirements are measured on package pins as near as possible to the processor with an oscilloscope set to 100-MHz bandwidth, 1.5 pF maximum probe capacitance, and 1 MΩ minimum impedance. The maximum length of ground wire on the probe should be less than 5 mm. Ensure external noise from the system is not coupled into the oscilloscope probe.For Voltage less than 1v, TOB will be 50 mv.Vcc_{PLL} max noise freq 0.5 MHz.
4. LPF should implement after making sure VCCPLL AC+DC are inside TOB_{VCCPLL} limits
5. Should be measured and verified prior to LPF assembly

Table 7-15. Processor PLL_OC (Vcc_{PLL_OC}) Supply DC Voltage and Current Specifications

Symbol	Parameter	Segment	Min	Typ	Max	Unit	Notes[1,2]
Vcc_{PLL_OC}	PLL_OC supply voltage (DC + AC specification)	All	—	V_{DDQ}	—	V	3
TOB_{CCPLL_OC}	Vcc_{PLL_OC} Tolerance	All	AC+DC: ± 5			%	3,4
$Icc_{MAX\_VCCPLL\_OC}$	Max Current for Vcc_{PLL_OC} Rail	Y/AML-Y22 -Processor Line	—	—	100	mA	
		U-Processor Line - 2 Core GT2	—	—	100		
			—	—			
		U-Processor Line - 2 Core GT3+OPC	—	—	120		

Notes:
1. Unless otherwise noted, all specifications in this table are based on estimates and simulations or empirical data. These specifications will be updated with characterized data from silicon measurements at a later date.
2. Long term reliability cannot be assured in conditions above or below Max/Min functional limits.
3. The voltage specification requirements are measured on package pins as near as possible to the processor with an oscilloscope set to 100-MHz bandwidth, 1.5 pF maximum probe capacitance, and 1 MΩ minimum impedance. The maximum length of ground wire on the probe should be less than 5 mm. Ensure external noise from the system is not coupled into the oscilloscope probe.For Voltage less than 1V, TOB will be 50 mV.

7.2.2 Processor Interfaces DC Specifications

7.2.2.1 DDR3L/-RS DC Specifications

Table 7-16. DDR3L/-RS Signal Group DC Specifications

Symbol	Parameter	Y and U-Processor Line			Units	Notes[1]
		Min	Typ	Max		
V_{IL}	Input Low Voltage	—	—	0.43* V_{DDQ}	V	2, 4, 8, 9
V_{IH}	Input High Voltage	0.57* V_{DDQ}	—	—	V	3, 4, 8, 9
$R_{ON\_UP/DN(DQ)}$	DDR3L/-RS Data Buffer pull-up/down Resistance	Trainable			Ω	10
$R_{ODT(DQ)}$	DDR3L/-RS On-die termination equivalent resistance for data signals	Trainable			Ω	10
$V_{ODT(DC)}$	DDR3L/-RS On-die termination DC working point (driver set to receive mode)	0.45* V_{DDQ}	0.5* V_{DDQ}	0.55* V_{DDQ}	V	10
$R_{ON\_UP/DN(CK)}$	DDR3L/-RS Clock Buffer pull-up/down Resistance	0.8*Typ	26	1.2*Typ	Ω	5, 10
$R_{ON\_UP/DN(CMD)}$	DDR3L/-RS Command Buffer pull-up/down Resistance	0.8*Typ	20	1.2*Typ	Ω	10
$R_{ON\_UP/DN(CTL)}$	DDR3L/-RS Control Buffer pull-up/down Resistance	0.8*Typ	20	1.2*Typ	Ω	5, 10
$R_{ON\_UP/DN}$ (DDR_VTT_CNTL)	System Memory Power Gate Control Buffer Pull-Up/ down Resistance	40	—	140	Ω	
I_{LI}	Input Leakage Current (DQ, CK) 0 V 0.2*V_{DDQ} 0.8*V_{DDQ}	—	—	1	mA	
DDR0_Vref_DQ DDR1_Vref_DQ DDR_Vref_CA	VREF output voltage	Trainable	$V_{DDQ}/2$	Trainable	V	9,11
DDR_RCOMP[0]	ODT resistance compensation	RCOMP values are memory topology dependent.			Ω	6
DDR_RCOMP[1]	Data resistance compensation				Ω	6
DDR_RCOMP[2]	Command resistance compensation				Ω	6

Notes:
1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. V_{IL} is defined as the maximum voltage level at a receiving agent that will be interpreted as a logical low value.
3. V_{IH} is defined as the minimum voltage level at a receiving agent that will be interpreted as a logical high value.
4. V_{IH} and V_{IL} may experience excursions above V_{DDQ}. However, input signal drivers should comply with the signal quality specifications.
5. This is the pull up/down driver resistance after compensation. Note that BIOS power training may change these values significantly based on margin/power trade-off.
6. For U/Y Processors DDR_RCOMP resistance should be provided on the system board with ±1% resistors. DDR_RCOMP resistors are connected to V_{SS}.
7. DDR_VREF is defined as $V_{DDQ}/2$ for DDR3L/-RS
8. R_{ON} tolerance is preliminary and might be subject to change.
9. Processor may be damaged if V_{IH} exceeds the maximum voltage for extended periods.
10. Final value determined by BIOS power training, values might vary between bytes and/or units.
11. The value will be set during the MRC boot training within the specified range.
12. DDR0_Vref_DQ - Not in use in DDR4, DDR1_Vref_DQ = DDR4_CA_ch1, DDR_Vref_CA = DD4_CA_ch0.

7.2.2.2 LPDDR3 DC Specifications

Table 7-17. LPDDR3 Signal Group DC Specifications

Symbol	Parameter	U/U- 4 Core and AML Y-Processor Line			Unit	Note
		Min	Typ	Max		
V_{IL}	Input Low Voltage	—	—	0.43*V_{DDQ}	V	2, 4, 8, 9
V_{IH}	Input High Voltage	0.57*V_{DDQ}	—	—	V	3, 4, 8, 9
$R_{ON\_UP/DN(DQ)}$	LPDDR3 Data Buffer pull-up/ down Resistance	Trainable			Ω	11
$R_{ODT(DQ)}$	LPDDR3 On-die termination equivalent resistance for data signals	Trainable			Ω	11
$V_{ODT(DC)}$	LPDDR3 On-die termination DC working point (driver set to receive mode)	0.45*V_{DDQ}	0.5*V_{DDQ}	0.55*V_{DDQ}	V	9
$R_{ON\_UP/DN(CK)}$	LPDDR3 Clock Buffer pull-up/ down Resistance	0.8*Typ	40	1.2*Typ	Ω	5, 11
$R_{ON\_UP/DN(CMD)}$	LPDDR3 Command Buffer pull-up/ down Resistance	0.8*Typ	40	1.2*Typ	Ω	11
$R_{ON\_UP/DN(CTL)}$	LPDDR3 Control Buffer pull-up/ down Resistance	0.8*Typ	23	1.2*typ	Ω	5, 11
$R_{ON\_UP/DN}$ (DDR_VTT_CNTL)	System Memory Power Gate Control Buffer Pull-Up Resistance	40	—	140	Ω	-
I_{LI}	Input Leakage Current (DQ, CK) 0V 0.2* V_{DDQ} 0.8*V_{DDQ}	—	—	0.75	mA	-
I_{LI}	Input Leakage Current (CMD,CTL) 0V 0.2*V_{DDQ} 0.8*V_{DDQ}	—	—	0.9	mA	-
DDR0_VREF_DQ DDR1_VREF_DQ DDR_VREF_CA	VREF output voltage	Trainable	V_{DDQ}/2	Trainable	V	12,13
DDR_RCOMP[0]	ODT resistance compensation	RCOMP values are memory topology dependent.			Ω	6
DDR_RCOMP[1]	Data resistance compensation				Ω	6
DDR_RCOMP[2]	Command resistance compensation				Ω	6

Notes:
1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. V_{IL} is defined as the maximum voltage level at a receiving agent that will be interpreted as a logical low value.
3. V_{IH} is defined as the minimum voltage level at a receiving agent that will be interpreted as a logical high value.
4. V_{IH} and V_{IL} may experience excursions above V_{DDQ}. However, input signal drivers should comply with the signal quality specifications.
5. This is the pull up/down driver resistance after compensation. Note that BIOS power training may change these values significantly based on margin/power trade-off.
6. DDR_RCOMP resistance should be provided on the system board with ±1% resistors. DDR_RCOMP resistors are to V_{SS}.
7. DDR_VREF is defined as V_{DDQ}/2 for LPDDR3
8. R_{ON} tolerance is preliminary and might be subject to change.
9. The value will be set during the MRC boot training within the specified range.
10. Processor may be damaged if V_{IH} exceeds the maximum voltage for extended periods.
11. Final value determined by BIOS power training, values might vary between bytes and/or units.
12. VREF values determined by BIOS training, values might vary between units.
13. DDR0_Vref_DQ - Not in use in DDR4, DDR1_Vref_DQ = DDR4_CA_ch1, DDR_Vref_CA = DD4_CA_ch0.

7.2.2.3 DDR4 DC Specifications

Table 7-18. DDR4 Signal Group DC Specifications

Symbol	Parameter	U/U- 4 Core-Processor Line			Units	Notes[1]
		Min	Typ	Max		
V_{IL}	Input Low Voltage	—	—	VREF(INT) - 0.07*VDDQ	V	2, 4, 8, 9, 13
V_{IH}	Input High Voltage	VREF(INT) + 0.07*VDDQ	—	—	V	3, 4, 8, 9, 13
$R_{ON\_UP/DN(DQ)}$	DDR4 Data Buffer pull-up/ down Resistance	Trainable			Ω	11
$R_{ODT(DQ)}$	DDR4 On-die termination equivalent resistance for data signals	Trainable			Ω	11
$V_{ODT(DC)}$	DDR4 On-die termination DC working point (driver set to receive mode)	$0.45*V_{DDQ}$	$0.5*V_{DDQ}$	$0.55*V_{DDQ}$	V	9
$R_{ON\_UP/DN(CK)}$	DDR4 Clock Buffer pull-up/ down Resistance	0.8*Typ	26	1.2*Typ	Ω	5, 11
$R_{ON\_UP/DN(CMD)}$	DDR4 Command Buffer pull-up/ down Resistance	0.8*Typ	20	1.2*Typ	Ω	11
$R_{ON\_UP/DN(CTL)}$	DDR4 Control Buffer pull-up/ down Resistance	0.8*Typ	20	1.2*Typ	Ω	5, 11
$R_{ON\_UP/DN}$ (DDR_VTT_CNTL)	System Memory Power Gate Control Buffer Pull-Up/ down Resistance	40	—	140	Ω	-
I_{LI}	Input Leakage Current (DQ, CK) 0 V $0.2*V_{DDQ}$ $0.8*V_{DDQ}$	—	—	1	mA	-
DDR0_VREF_DQ DDR1_VREF_DQ DDR_VREF_CA	VREF output voltage	Trainable	$V_{DDQ}/2$	Trainable	V	12, 14
DDR_RCOMP[0]	ODT resistance compensation	RCOMP values are memory topology dependent.			Ω	6
DDR_RCOMP[1]	Data resistance compensation				Ω	6
DDR_RCOMP[2]	Command resistance compensation				Ω	6

Notes:
1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. V_{IL} is defined as the maximum voltage level at a receiving agent that will be interpreted as a logical low value.
3. V_{IH} is defined as the minimum voltage level at a receiving agent that will be interpreted as a logical high value.
4. V_{IH} and V_{IL} may experience excursions above V_{DDQ}. However, input signal drivers should comply with the signal quality specifications.
5. This is the pull up/down driver resistance after compensation. Note that BIOS power training may change these values significantly based on margin/power trade-off. See processor I/O Buffer Models for I/V characteristics.
6. DDR_RCOMP resistance should be provided on the system board with ±1% resistors. DDR_RCOMP resistors are to V_{SS}.
7. DDR_VREF is defined as $V_{DDQ}/2$ for DDR4
8. R_{ON} tolerance is preliminary and might be subject to change.
9. The value will be set during the MRC boot training within the specified range.
10. Processor may be damaged if V_{IH} exceeds the maximum voltage for extended periods.
11. Final value determined by BIOS power training, values might vary between bytes and/or units.
12. VREF values determined by BIOS training, values might vary between units.
13. VREF(INT) is a trainable parameter whose value is determined by BIOS for margin optimization.
14. DDR0_Vref_DQ - Not in use in DDR4, DDR1_Vref_DQ = DDR4_CA_ch1, DDR_Vref_CA = DD4_CA_ch0

7.2.2.4 Digital Display Interface (DDI) DC Specifications

Table 7-19. Digital Display Interface Group DC Specifications (DP/HDMI)

Symbol	Parameter	Min	Typ	Max	Units	Notes[1]
V_{OL}	DDIB_TXC[3:0] Output Low Voltage DDIC_TXC[3:0] Output Low Voltage DDID_TXC[3:0] Output Low Voltage	—	—	$0.25*V_{CCIO}$	V	1,2
V_{OH}	DDIB_TXC[3:0] Output High Voltage DDIC_TXC[3:0] Output High Voltage DDID_TXC[3:0] Output High Voltage	$0.75*V_{CCIO}$	—	—	V	1,2
$Z_{TX-DIFF-DC}$	DC Differential Tx Impedance	80	100	120	Ω	
Notes: 1. Vcc_{IO} depends on segment. 2. V_{OL} and V_{OH} levels depends on the level chosen by the Platform.						

7.2.2.5 embedded DisplayPort* (eDP*) DC Specification

Table 7-20. embedded DisplayPort* (eDP*) Group DC Specifications

Symbol	Parameter	Min	Typ	Max	Units
V_{OL}	eDP_DISP_UTIL Output Low Voltage	—	—	$0.1*V_{CCIO}$	V
V_{OH}	eDP_DISP_UTIL Output High Voltage	$0.9*Vcc_{IO}$	—	—	V
R_{UP}	eDP_DISP_UTIL Internal pull-up	100	—	—	Ω
R_{DOWN}	eDP_DISP_UTIL Internal pull-down	100	—	—	Ω
eDP_RCOMP	eDP resistance compensation	24.75	25	25.25	Ω
$Z_{TX-DIFF-DC}$	DC Differential Tx Impedance	80	100	120	Ω
Notes: 1. COMP resistance is to VCOMP_OUT. 2. eDP_RCOMP resistor should be provided on the system board.					

7.2.2.6 CMOS DC Specifications

Table 7-21. CMOS Signal Group DC Specifications

Symbol	Parameter	Min	Max	Units	Notes[1]
V_{IL}	Input Low Voltage	—	Vcc * 0.3	V	2, 5
V_{IH}	Input High Voltage	Vcc * 0.7	—	V	2, 4, 5
V_{OL}	Output Low Voltage	—	Vcc * 0.1	V	2
V_{OH}	Output High Voltage	Vcc * 0.9	—	V	2, 4
R_{ON}	Buffer on Resistance	23	73	Ω	-
I_{LI}	Input Leakage Current	—	±150	µA	3
Notes: 1. Unless otherwise noted, all specifications in this table apply to all processor frequencies. 2. The Vcc referred to in these specifications refers to instantaneous Vcc levels. 3. For VIN between “0” V and Vcc Measured when the driver is tri-stated. 4. V_{IH} and V_{OH} may experience excursions above Vcc. However, input signal drivers should comply with the signal quality specifications. 5. N/A					

7.2.2.7 GTL and OD DC Specifications

Table 7-22. GTL Signal Group and Open Drain Signal Group DC Specifications

Symbol	Parameter	Min	Max	Units	Notes[1]
V_{IL}	Input Low Voltage (TAP, except PROC_TCK, PROC_TRST#)	—	Vcc * 0.6	V	2, 5, 6
V_{IH}	Input High Voltage (TAP, except PROC_TCK, PROC_TRST#)	Vcc * 0.72	—	V	2, 4, 5, 6
V_{IL}	Input Low Voltage (PROC_TCK,PROC_TRST#)	—	Vcc * 0.3	V	2, 5, 6
V_{IH}	Input High Voltage (PROC_TCK,PROC_TRST#)	Vcc * 0.3	—	V	2, 4, 5, 6
$V_{HYSTERESIS}$	Hysteresis Voltage	Vcc * 0.2	—	V	-
R_{ON}	Buffer on Resistance (TDO)	7	17	Ω	-
V_{IL}	Input Low Voltage (other GTL)	—	Vcc * 0.6	V	2, 5, 6
V_{IH}	Input High Voltage (other GTL)	Vcc * 0.72	—	V	2, 4, 5, 6
R_{ON}	Buffer on Resistance (CFG/BPM)	16	24	Ω	-
R_{ON}	Buffer on Resistance (other GTL)	12	28	Ω	-
I_{LI}	Input Leakage Current	—	±150	µA	3

Notes:
1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. The Vcc_{ST} referred to in these specifications refers to instantaneous $Vcc_{ST/IO}$.
3. For V_{IN} between 0 V and Vcc_{ST}. Measured when the driver is tri-stated.
4. V_{IH} and V_{OH} may experience excursions above Vcc_{ST}. However, input signal drivers should comply with the signal quality specifications.
5. N/A
6. Those V_{IL}/V_{IH} values are based on ODT disabled (ODT Pull-up not exist).

7.2.2.8 PECI DC Characteristics

The PECI interface operates at a nominal voltage set by Vcc_{ST}. The set of DC electrical specifications shown in the following table is used with devices normally operating from a Vcc_{ST} interface supply.

Vcc_{ST} nominal levels will vary between processor families. All PECI devices will operate at the Vcc_{ST} level determined by the processor installed in the system.

Table 7-23. PECI DC Electrical Limits (Sheet 1 of 2)

Symbol	Definition and Conditions	Min	Max	Units	Notes[1]
R_{up}	Internal pull up resistance	15	45	Ω	3
V_{IN}	Input Voltage Range	-0.15	Vcc_{ST} + 0.15	V	-
$V_{Hysteresis}$	Hysteresis	0.15 * Vcc_{ST}	—	V	-
V_{IL}	Input Voltage Low- Edge Threshold Voltage	—	0.3 * Vcc_{ST}	V	-
V_{IH}	Input Voltage High-Edge Threshold Voltage	0.7 * Vcc_{ST}	—	V	-
C_{bus}	Bus Capacitance per Node	N/A	10	pF	-
C_{pad}	Pad Capacitance	0.7	1.8	pF	-
Ileak000	leakage current @ 0V	—	0.6	mA	-
Ileak025	leakage current @ 0.25* Vcc_{ST}	—	0.4	mA	-
Ileak050	leakage current @ 0.50* Vcc_{ST}	—	0.2	mA	-

Table 7-23. PECI DC Electrical Limits (Sheet 2 of 2)

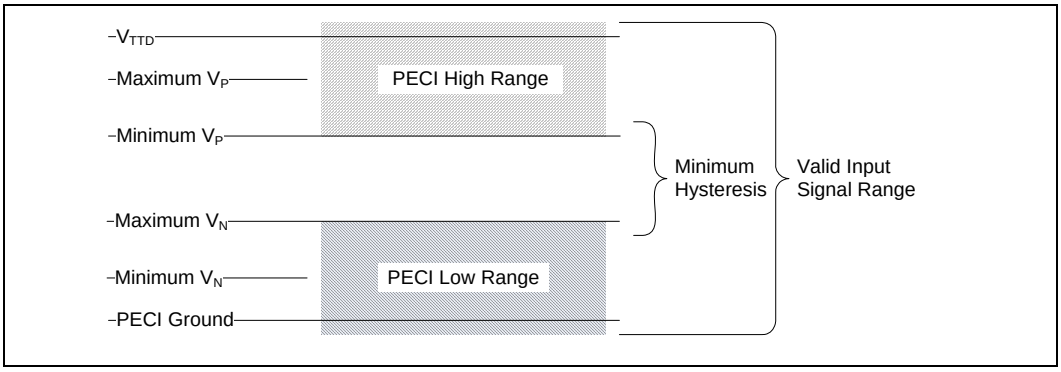
Symbol	Definition and Conditions	Min	Max	Units	Notes[1]
Ileak075	leakage current @ 0.75* Vcc_{ST}	—	0.13	mA	-
Ileak100	leakage current @ Vcc_{ST}	—	0.10	mA	-

Notes:
1. Vcc_{ST} supplies the PECI interface. PECI behavior does not affect Vcc_{ST} min/max specifications.
2. The leakage specification applies to powered devices on the PECI bus.
3. The PECI buffer internal pull up resistance measured at 0.75* Vcc_{ST}.

Input Device Hysteresis

The input buffers in both client and host models should use a Schmitt-triggered input design for improved noise immunity. Use the following figure as a guide for input buffer design.

Figure 7-1. Input Device Hysteresis



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8 Package Mechanical Specifications

8.1 Package Mechanical Attributes

The U/U-4 Core/YProcessors use a Flip Chip technology available in a Ball Grid Array (BGA) package. The following table provides an overview of the mechanical attributes of the package.

Table 8-1. Package Mechanical Attributes

Package	Parameter	Y-Processor Line	U- Processor Line		U-Quad Core Processor Line
		Dual Core GT2	Dual Core GT3+OPC	Dual Core GT2	Quad Core GT2
Package Technology	Package Type	Flip Chip Ball Grid Array	Flip Chip Ball Grid Array		Flip Chip Ball Grid Array
	Interconnect	Ball Grid Array (BGA)	Ball Grid Array (BGA)		Ball Grid Array (BGA)
	Lead Free	Yes	Yes		Yes
	Halogenated Flame Retardant Free	Yes	Yes		Yes
Package Configuration	Solder Ball Composition	SAC1205	SAC405		SAC405
	Ball/Pin Count	1515	1356		1356
	Grid Array Pattern	Balls Anywhere	Balls Anywhere		Balls Anywhere
	Land Side Capacitors	No	Yes		Yes
	Die Side Capacitors	No	No		No
	Die Configuration	2 Dice Multi-Chip Package (MCP)	3 Dice MCP	2 Dice MCP	2 Dice MCP
Package Dimensions	Nominal Package Size	20.5x16.5 mm	42x24 mm		42x24 mm
	Min Ball/Pin pitch	0.4 mm	0.65 mm		0.65 mm

8.2 Package Loading Specifications

Table 8-2. Package Loading Specifications

Maximum Static Normal Load	Limit	Minimum PCB Thickness Assumptions	Notes
Y/ AML-Y22 Processor Lines	44.5 N (10 lbf)	0.7 mm	1, 2, 3
U/U- 4 Core Processor Line	67 N (15 lbf)	0.8 mm	1, 2, 3

Table 8-2. Package Loading Specifications

Maximum Static Normal Load	Limit	Minimum PCB Thickness Assumptions	Notes
Notes: 1. The thermal solution attach mechanism should not induce continuous stress to the package. It may only apply a uniform load to the die to maintain a thermal interface. 2. This specification applies to the uniform compressive load in the direction perpendicular to the dies' top surface. Load should be centered on processor die center. 3. This specification is based on limited testing for design characterization. 4. This load limit assumes the use of a backing plate.			

8.3 Package Storage Specifications

Table 8-3. Package Storage Specifications

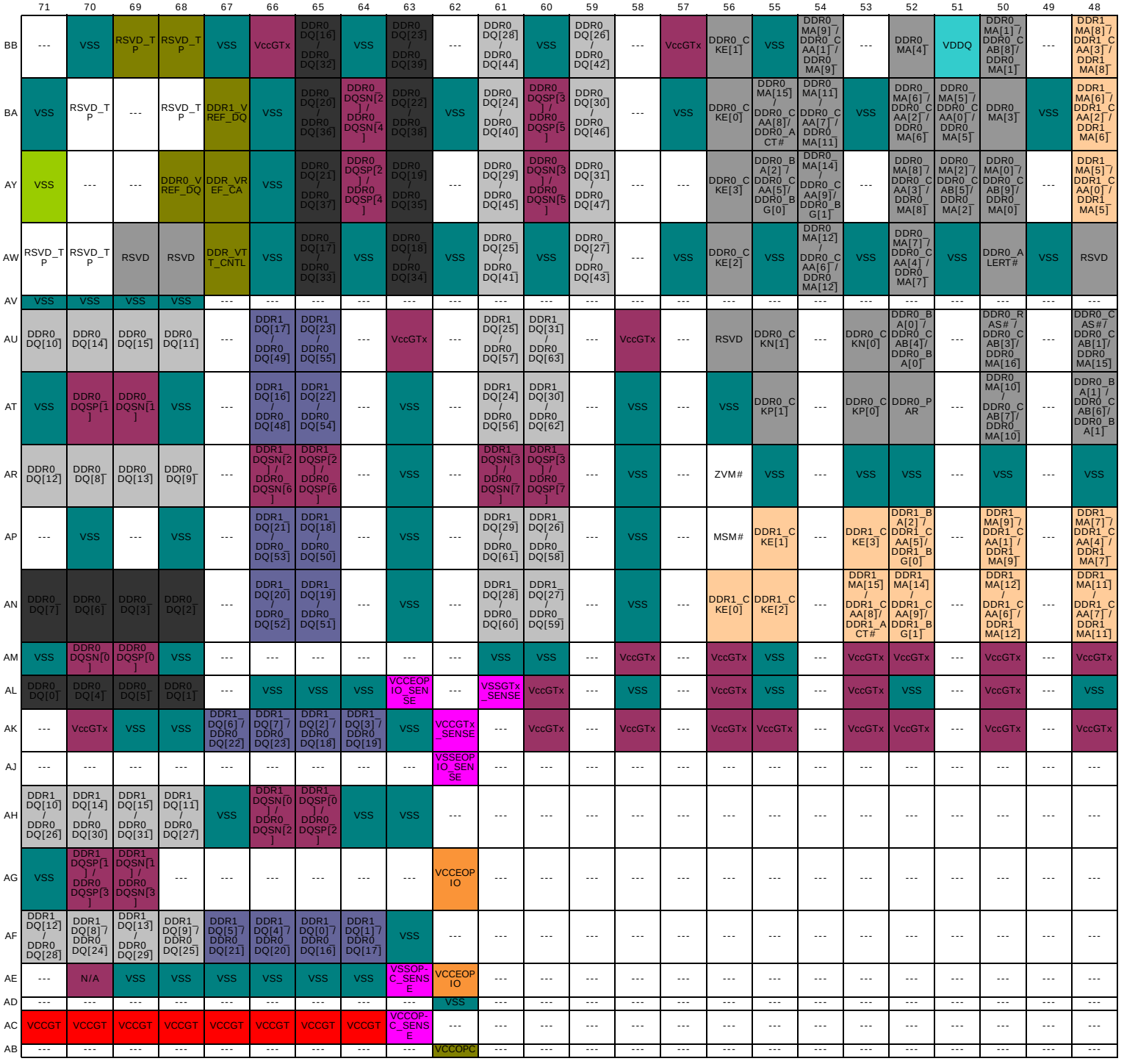
Parameter	Description	Min	Max	Notes
$T_{ABSOLUTE\ STORAGE}$	The non-operating device storage temperature. Damage (latent or otherwise) may occur when subjected to this temperature for any length of time in Intel Original sealed moisture barrier bagand / or box.	-25 °C	125 °C	1, 2, 3
$T_{SUSTAINED\ STORAGE}$	The ambient storage temperature limit (in shipping media) for the sustained period of time as specified below in Intel Original sealed moisture barrier bagand / or box.	-5 °C	40 °C	1, 2, 3
$RH_{SUSTAINED\ STORAGE}$	The maximum device storage relative humidity for the sustained period of time as specified below in Intel Original sealed moisture barrier bagand / or box	60% @ 24 °C		1, 2, 3
$TIME_{SUSTAINED\ STORAGE}$	**Maximum time: associated with customer shelf life in Intel Original sealed moisture barrier bag and / or box**	NA	Moisture Sensitive Devices: 60 months from bag seal date; Non-moisture sensitive devices: 60 months from lot date	1, 2, 3
Notes: 1. applies to the un-assembled component only and does not apply to the shipping media, moisture barrier bags or desiccant. Refers to a component device that is not assembled in a board or socket that is not to be electrically connected to a voltage reference or I/O signals. 2. Specified temperatures are based on data collected. Exceptions for surface mount re-flow are specified by applicable JEDEC J-STD-020 and MAS documents. The JEDEC, J-STD-020 moisture level rating and associated handling practices apply to all moisture sensitive de-vices removed from the moisture barrier bag. 3. Post board attach storage temperature limits are not specifiedfor non-Intel branded boards. Consult your board manufacturer for storage specifications.				

9 U/U-Quad Core/Y Processor Ball Information

9.1 U-Processor and U-Quad Core Processor Ball Information

The U-Processors and U-Quad Core Processors are available in the BGA package (BGA1356), Figure 9-1 through Figure 9-6 provide a top view of the Ball map. Table 9-1 provides the Ball list.

Figure 9-1. U/U-Quad Core Processor Ball Map (Upper Left, Columns 71-48)



	71	70	69	68	67	66	65	64	63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48
BB	---	VSS	RSVD_TP	RSVD_TP	VSS	VccGTx	DDR0_DQ[16] / DDR0_DQ[32]	VSS	DDR0_DQ[23] / DDR0_DQ[39]	---	DDR0_DQ[28] / DDR0_DQ[44]	VSS	DDR0_DQ[26] / DDR0_DQ[42]	---	VccGTx	DDR0_CKE[1]	VSS	DDR0_MA[9] / DDR0_CAA[1] / DDR0_MA[9]	---	DDR0_MA[4]	VDDQ	DDR0_MA[1] / DDR0_CAB[8] / DDR0_MA[1]	---	DDR1_MA[8] / DDR1_CAA[3] / DDR1_MA[8]
BA	VSS	RSVD_TP	---	RSVD_TP	DDR1_VREF_DQ	VSS	DDR0_DQ[20] / DDR0_DQ[36]	DDR0_DQSN[2] / DDR0_DQSN[4]	DDR0_DQ[22] / DDR0_DQ[38]	VSS	DDR0_DQ[24] / DDR0_DQ[40]	DDR0_DQSP[3] / DDR0_DQSP[5]	DDR0_DQ[30] / DDR0_DQ[46]	---	VSS	DDR0_CKE[0]	DDR0_MA[15] / DDR0_CAA[8] / DDR0_ACT#	DDR0_MA[11] / DDR0_CAA[7] / DDR0_MA[11]	VSS	DDR0_MA[6] / DDR0_CAA[2] / DDR0_MA[6]	DDR0_MA[5] / DDR0_CAA[0] / DDR0_MA[5]	DDR0_MA[3]	VSS	DDR1_MA[6] / DDR1_CAA[2] / DDR1_MA[6]
AY	VSS	---	---	DDR0_VREF_DQ	DDR_VREF_CA	VSS	DDR0_DQ[21] / DDR0_DQ[37]	DDR0_DQSP[2] / DDR0_DQSP[4]	DDR0_DQ[19] / DDR0_DQ[35]	---	DDR0_DQ[29] / DDR0_DQ[45]	DDR0_DQSN[3] / DDR0_DQSN[5]	DDR0_DQ[31] / DDR0_DQ[47]	---	---	DDR0_CKE[3]	DDR0_BA[2] / DDR0_CAA[5] / DDR0_BG[0]	DDR0_MA[14] / DDR0_CAA[9] / DDR0_BG[1]	---	DDR0_MA[8] / DDR0_CAA[3] / DDR0_MA[8]	DDR0_MA[2] / DDR0_CAB[5] / DDR0_MA[2]	DDR0_MA[0] / DDR0_CAB[9] / DDR0_MA[0]	---	DDR1_MA[5] / DDR1_CAA[0] / DDR1_MA[5]
AW	RSVD_TP	RSVD_TP	RSVD	RSVD	DDR_VTT_CNTL	VSS	DDR0_DQ[17] / DDR0_DQ[33]	VSS	DDR0_DQ[18] / DDR0_DQ[34]	VSS	DDR0_DQ[25] / DDR0_DQ[41]	VSS	DDR0_DQ[27] / DDR0_DQ[43]	---	VSS	DDR0_CKE[2]	VSS	DDR0_MA[12] / DDR0_CAA[6] / DDR0_MA[12]	VSS	DDR0_MA[7] / DDR0_CAA[4] / DDR0_MA[7]	VSS	DDR0_ALERT#	VSS	RSVD
AV	VSS	VSS	VSS	VSS	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---
AU	DDR0_DQ[10]	DDR0_DQ[14]	DDR0_DQ[15]	DDR0_DQ[11]	---	DDR1_DQ[17] / DDR0_DQ[49]	DDR1_DQ[23] / DDR0_DQ[55]	---	VccGTx	---	DDR1_DQ[25] / DDR0_DQ[57]	DDR1_DQ[31] / DDR0_DQ[63]	---	VccGTx	---	RSVD	DDR0_CKN[1]	---	DDR0_CKN[0]	DDR0_BA[0] / DDR0_CAB[4] / DDR0_BA[0]	---	DDR0_RAS# / DDR0_CAB[3] / DDR0_MA[16]	---	DDR0_CAS#/ DDR0_CAB[1]/ DDR0_MA[15]
AT	VSS	DDR0_DQSP[1]	DDR0_DQSN[1]	VSS	---	DDR1_DQ[16] / DDR0_DQ[48]	DDR1_DQ[22] / DDR0_DQ[54]	---	VSS	---	DDR1_DQ[24] / DDR0_DQ[56]	DDR1_DQ[30] / DDR0_DQ[62]	---	VSS	---	VSS	DDR0_CKP[1]	---	DDR0_CKP[0]	DDR0_PAR	---	DDR0_MA[10] / DDR0_CAB[7]/ DDR0_MA[10]	---	DDR0_BA[1] / DDR0_CAB[6]/ DDR0_BA[1]
AR	DDR0_DQ[12]	DDR0_DQ[8]	DDR0_DQ[13]	DDR0_DQ[9]	---	DDR1_DQSN[2] / DDR0_DQSN[6]	DDR1_DQSP[2] / DDR0_DQSP[6]	---	VSS	---	DDR1_DQSN[3] / DDR0_DQSN[7]	DDR1_DQSP[3] / DDR0_DQSP[7]	---	VSS	---	ZVM#	VSS	---	VSS	VSS	---	VSS	---	VSS
AP	---	VSS	---	VSS	---	DDR1_DQ[21] / DDR0_DQ[53]	DDR1_DQ[18] / DDR0_DQ[50]	---	VSS	---	DDR1_DQ[29] / DDR0_DQ[61]	DDR1_DQ[26] / DDR0_DQ[58]	---	VSS	---	MSM#	DDR1_CKE[1]	---	DDR1_CKE[3]	DDR1_BA[2] / DDR1_CAA[5]/ DDR1_BG[0]	---	DDR1_MA[9] / DDR1_CAA[1] / DDR1_MA[9]	---	DDR1_MA[7] / DDR1_CAA[4] / DDR1_MA[7]
AN	DDR0_DQ[7]	DDR0_DQ[6]	DDR0_DQ[3]	DDR0_DQ[2]	---	DDR1_DQ[20] / DDR0_DQ[52]	DDR1_DQ[19] / DDR0_DQ[51]	---	VSS	---	DDR1_DQ[28] / DDR0_DQ[60]	DDR1_DQ[27] / DDR0_DQ[59]	---	VSS	---	DDR1_CKE[0]	DDR1_CKE[2]	---	DDR1_MA[15] / DDR1_CAA[8]/ DDR1_ACT#	DDR1_MA[14] / DDR1_CAA[9]/ DDR1_BG[1]	---	DDR1_MA[12] / DDR1_CAA[6] / DDR1_MA[12]	---	DDR1_MA[11] / DDR1_CAA[7] / DDR1_MA[11]
AM	VSS	DDR0_DQSN[0]	DDR0_DQSP[0]	VSS	---	---	---	---	---	---	VSS	VSS	---	VccGTx	---	VccGTx	VSS	---	VccGTx	VccGTx	---	VccGTx	---	VccGTx
AL	DDR0_DQ[0]	DDR0_DQ[4]	DDR0_DQ[5]	DDR0_DQ[1]	---	VSS	VSS	VSS	VCCEOPIO_SENSE	---	VSSGTx_SENSE	VccGTx	---	VSS	---	VccGTx	VSS	---	VccGTx	VSS	---	VccGTx	---	VSS
AK	---	VccGTx	VSS	VSS	DDR1_DQ[6] / DDR0_DQ[22]	DDR1_DQ[7] / DDR0_DQ[23]	DDR1_DQ[2] / DDR0_DQ[18]	DDR1_DQ[3] / DDR0_DQ[19]	VSS	VCCGTx_SENSE	---	VccGTx	---	VccGTx	---	VccGTx	VccGTx	---	VccGTx	VccGTx	---	VccGTx	---	VccGTx
AJ	---	---	---	---	---	---	---	---	---	VSSEOPIO_SENSE	---	---	---	---	---	---	---	---	---	---	---	---	---	---
AH	DDR1_DQ[10] / DDR0_DQ[26]	DDR1_DQ[14] / DDR0_DQ[30]	DDR1_DQ[15] / DDR0_DQ[31]	DDR1_DQ[11] / DDR0_DQ[27]	VSS	DDR1_DQSN[0] / DDR0_DQSN[2]	DDR1_DQSP[0] / DDR0_DQSP[2]	VSS	VSS	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---
AG	VSS	DDR1_DQSP[1] / DDR0_DQSP[3]	DDR1_DQSN[1] / DDR0_DQSN[3]	---	---	---	---	---	---	VCCEOPIO	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---
AF	DDR1_DQ[12] / DDR0_DQ[28]	DDR1_DQ[8] / DDR0_DQ[24]	DDR1_DQ[13] / DDR0_DQ[29]	DDR1_DQ[9] / DDR0_DQ[25]	DDR1_DQ[5] / DDR0_DQ[21]	DDR1_DQ[4] / DDR0_DQ[20]	DDR1_DQ[0] / DDR0_DQ[16]	DDR1_DQ[1] / DDR0_DQ[17]	VSS	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---
AE	---	N/A	VSS	VSS	VSS	VSS	VSS	VSS	VSSOP-C_SENSE	VCCEOPIO	---	---	---	---	---	---	---	---	---	---	---	---	---	---
AD	---	---	---	---	---	---	---	---	---	VSS	---	---	---	---	---	---	---	---	---	---	---	---	---	---
AC	VCCGT	VCCGT	VCCGT	VCCGT	VCCGT	VCCGT	VCCGT	VCCGT	VCCOP-C_SENSE	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---
AB	---	---	---	---	---	---	---	---	---	VCCOPC	---	---	---	---	---	---	---	---	---	---	---	---	---	---

Figure 9-2. U/U-Quad Core Processor Ball Map (Upper Middle, Columns 47-24)

	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32	31	30	29	28	27	26	25	24
BB	VDDQ	DDR1_MA[3]	---	DDR1_BA[0] / DDR1_CAB[4] / DDR1_BA[0]	VSS	DDR1_CS#[0]	VDDQ	---	DDR0_DQ[36] / DDR1_DQ[4]	VSS	DDR0_DQ[39] / DDR1_DQ[7]	---	DDR0_DQ[44] / DDR1_DQ[12]	VSS	DDR0_DQ[47] / DDR1_DQ[15]	VDDQ	DDR0_DQ[52] / DDR1_DQ[36]	VSS	DDR0_DQ[55] / DDR1_DQ[39]	---	DDR0_DQ[60] / DDR1_DQ[44]	VSS	DDR0_DQ[63] / DDR1_DQ[47]	---
BA	DDR1_MA[4]	DDR1_MA[0] / DDR1_CAB[9] / DDR1_MA[0]	VSS	DDR1_BA[1] / DDR1_CAB[6] / DDR1_BA[1]	DDR1_MA[13] / DDR1_CAB[0] / DDR1_MA[13]	DDR1_ODT[0]	VSS	---	DDR0_DQ[37] / DDR1_DQ[5]	DDR0_DQSN[4] / DDR1_DQSN[0]	DDR0_DQ[38] / DDR1_DQ[6]	VSS	DDR0_DQ[45] / DDR1_DQ[13]	DDR0_DQSP[5] / DDR1_DQSP[1]	DDR0_DQ[46] / DDR1_DQ[14]	VSS	DDR0_DQ[53] / DDR1_DQ[37]	DDR0_DQSN[6] / DDR1_DQSN[4]	DDR0_DQ[54] / DDR1_DQ[38]	VSS	DDR0_DQ[61] / DDR1_DQ[45]	DDR0_DQSP[7] / DDR1_DQSP[5]	DDR0_DQ[62] / DDR1_DQ[46]	---
AY	DDR1_MA[2] / DDR1_CAB[5] / DDR1_MA[2]	DDR1_MA[1] / DDR1_CAB[8] / DDR1_MA[1]	---	DDR1_WE#/ DDR1_CAB[2] / DDR1_MA[14]	DDR1_CAS#/ DDR1_CAB[1] / DDR1_MA[15]	DDR1_CS#[1]	---	---	DDR0_DQ[32] / DDR1_DQ[0]	DDR0_DQSP[4] / DDR1_DQSP[0]	DDR0_DQ[34] / DDR1_DQ[2]	---	DDR0_DQ[40] / DDR1_DQ[8]	DDR0_DQSN[5] / DDR1_DQSN[1]	DDR0_DQ[42] / DDR1_DQ[10]	---	DDR0_DQ[48] / DDR1_DQ[32]	DDR0_DQSP[6] / DDR1_DQSP[4]	DDR0_DQ[50] / DDR1_DQ[34]	---	DDR0_DQ[56] / DDR1_DQ[40]	DDR0_DQSN[7] / DDR1_DQSN[5]	DDR0_DQ[58] / DDR1_DQ[42]	---
AW	VSS	DDR1_MA[10] / DDR1_CAB[7] / DDR1_MA[10]	VSS	DDR1_RAS#/ DDR1_CAB[3] / DDR1_MA[16]	VSS	DDR1_ODT[1]	VSS	---	DDR0_DQ[33] / DDR1_DQ[1]	VSS	DDR0_DQ[35] / DDR1_DQ[3]	VSS	DDR0_DQ[41] / DDR1_DQ[9]	VSS	DDR0_DQ[43] / DDR1_DQ[11]	VSS	DDR0_DQ[49] / DDR1_DQ[33]	VSS	DDR0_DQ[51] / DDR1_DQ[35]	VSS	DDR0_DQ[57] / DDR1_DQ[41]	VSS	DDR0_DQ[59] / DDR1_DQ[43]	---
AV	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---
AU	---	DDR0_MA[13] / DDR0_CAB[0] / DDR0_MA[13]	DDR0_CS#[0]	---	DDR0_CS#[1]	VDDQ	---	DDR1_DQ[32] / DDR1_DQ[16]	---	VSS	DDR1_DQ[35] / DDR1_DQ[19]	---	VDDQ	---	DDR1_DQ[41] / DDR1_DQ[25]	VSS	---	DDR1_DQ[42] / DDR1_DQ[26]	---	VDDQ	DDR1_DQ[48]	---	DDR1_DQ[51]	---
AT	---	DDR0_WE#/ DDR0_CAB[2] / DDR0_MA[14]	DDR0_ODT[0]	---	DDR0_ODT[1]	VSS	---	DDR1_DQ[33] / DDR1_DQ[17]	---	DDR1_DQSN[4] / DDR1_DQSN[2]	DDR1_DQ[34] / DDR1_DQ[18]	---	VSS	---	DDR1_DQ[40] / DDR1_DQ[24]	DDR1_DQSN[5] / DDR1_DQSN[3]	---	DDR1_DQ[43] / DDR1_DQ[27]	---	VSS	DDR1_DQ[49]	---	DDR1_DQ[50]	---
AR	---	VSS	VSS	---	VSS	VSS	---	DDR1_DQ[36] / DDR1_DQ[20]	---	DDR1_DQSP[4] / DDR1_DQSP[2]	DDR1_DQ[39] / DDR1_DQ[23]	---	VSS	---	DDR1_DQ[44] / DDR1_DQ[28]	DDR1_DQSP[5] / DDR1_DQSP[3]	---	DDR1_DQ[46] / DDR1_DQ[30]	---	VSS	DDR1_DQSP[6]	---	DDR1_DQSN[6]	---
AP	---	DDR1_CKP[1]	DDR1_CKP[0]	---	DDR1_PAR	VSS	---	DDR1_DQ[37] / DDR1_DQ[21]	---	VSS	DDR1_DQ[38] / DDR1_DQ[22]	---	VSS	---	DDR1_DQ[45] / DDR1_DQ[29]	VSS	---	DDR1_DQ[47] / DDR1_DQ[31]	---	VSS	DDR1_DQ[52]	---	DDR1_DQ[55]	---
AN	---	DDR1_CKN[1]	DDR1_CKN[0]	---	DDR1_ALERT#	VSS	---	VSS	---	VSS	VSS	---	VSS	---	VSS	VSS	---	VSS	---	VSS	DDR1_DQ[53]	---	DDR1_DQ[54]	---
AM	---	VSS	VSS	---	VSS	VCCIO	---	VDDQC	---	VCC	VCC	---	VCC	---	VCC	VCC	---	VCCIO	---	VCCIO	VSS	---	VSS	---
AL	---	VccGTx	VSS	---	VccGTx	VCCIO	---	VCC	---	VSS	VCC	---	VSS	---	VCC	VSS	---	VCCIO	---	VSS	RSVD	---	RSVD	---
AK	---	VccGTx	VccGTx	---	VccGTx	VccGTx	---	VCC	---	VCC	VCC	---	VCC	---	VCC	RSVD	---	VCCIO	---	VCCIO	VSS	---	VCCSA	---
AJ	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---
AH	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---
AG	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---
AF	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---
AE	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---
AD	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---
AC	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---
AB	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---

Figure 9-3. U/U-Quad Core Processor Ball Map (Upper Right, Columns 23-1)

	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
BB	VDDQ	HDA_SDO / I2S0_TXD	---	DSW_PWROK	---	VSS	GPD9 / SLP_WLAN#	---	WAKE#	VCCRTC	GPP_A3 / LAD2 / ESPI_IO2	---	GPP_A7 / PIRQA#	DCPRTC	GPP_A16 / SD_1P8_SEL	---	GPP_A20 / ISH_GP2	VSS	TP4	RSVD	TP2	RSVD	---
BA	VSS	HDA_SYNC / I2S0_SFRM	HDA_SDI0 / I2S0_RXD	PCH_PWROK	---	VSS	GPD8 / SUSCLK	GPD5 / SLP_S4#	GPD3 / PWRBTN#	VSS	GPP_A2 / LAD1 / ESPI_IO1	GPP_A5 / LFRAME# / ESPI_CS#	GPP_A14 / SUS_STAT# / ESPI_RESET#	VSS	GPP_A17 / SD_PWR_EN# / ISH_GP7	GPP_A19 / ISH_GP1	GPP_A21 / ISH_GP3	VSS	GPP_B3 / CPU_GP2	RSVD	RSVD	VSS	VSS
AY	---	HDA_BLK / I2S0_SCLK	HDA_SDI1 / I2S1_RXD	I2S1_SFRM	---	---	RSMRST#	GPD10 / SLP_S5#	GPD1 / ACPRESENT	---	GPP_A1 / LAD0 / ESPI_IO0	GPP_A4 / LAD3 / ESPI_IO3	GPP_A6 / SERIRQ	---	GPP_A10 / CLKOUT_LPC1	GPP_A18 / ISH_GP0	GPP_A22 / ISH_GP4	---	GPP_B4 / CPU_GP3	TP1	RSVD	RSVD	RSVD
AW	VSS	HDA_RST# / I2S1_SCLK	VSS	I2S1_TXD	---	VSS	GPD11 / LANPHYPC	VSS	SLP_LAN#	VSS	GPP_A0 / RCIN#	VSS	GPP_A8 / CLKRUN#	VSS	GPP_A9 / CLKOUT_LPC0 / ESPI_CLK	VSS	GPP_A23 / ISH_GP5	VSS	GPP_B14 / SPKR	N/A	SPI0_MISO	SPI0_IO2	RSVD
AV	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	SPI0_MOSI	SPI0_CLK	VSS
AU	VDDQ	DDR1_DQ[57]	DDR1_DQ[58]	VSS	---	DDR_RCOMP[2]	---	PCH_OPIRCOMP	VSS	---	GPD0 / BATLOW#	---	GPP_A11 /PME#	VSS	---	GPP_B9 / SRCCLKREQ4#	GPP_B10 / SRCCLKREQ5#	---	TP5	SPI0_IO3	SPI0_CS0#	SPI0_CS1#	SPI0_CS2#
AT	VSS	DDR1_DQ[56]	DDR1_DQ[59]	VSS	---	DDR_RCOMP[1]	---	PROC_POPIRCOMP	GPD7 / RSVD	---	DRAM_RESET#	---	GPP_B12 / SLP_S0#	GPP_B8 / SRCCLKREQ3#	---	GPP_B7 / SRCCLKREQ2#	GPP_B6 / SRCCLKREQ1#	---	TP6	VSS	---	VSS	EMMC_RCOMP
AR	VSS	DDR1_DQSN[7]	DDR1_DQSP[7]	VSS	---	DDR_RCOMP[0]	---	VSS	VSS	---	GPP_A13 / SUSWARN# / SUSPWRDNACK	---	VSS	GPP_B5 / SRCCLKREQ0#	---	VSS	GPP_B18 / GSPI0_MOSI	---	VSS	---	---	---	---
AP	VSS	DDR1_DQ[61]	DDR1_DQ[62]	VSS	---	VSS	---	INTRUDER#	GPD4 / SLP_S3#	---	Sx_EXIT_HOLDOFF# / GPP_A12 / BM_BUSY# / ISH_GP6	---	GPP_A15 / SUSACK#	VSS	---	GPP_B17 / GSPI0_MISO	GPP_B16 / GSPI0_CLK	---	GPP_B21 / GSPI1_MISO	GPP_F27 / EMMC_CMD	GPP_F15 / EMMC_DATA2	GPP_F13 / EMMC_DATA0	GPP_F14 / EMMC_DATA1
AN	VSS	DDR1_DQ[60]	DDR1_DQ[63]	VSS	---	SRTCRST#	---	GPD6 / SLP_A#	SLP_SUS#	---	GPP_B1 / CORE_VID1	---	GPP_B0 / CORE_VID0	GPP_B13 / PLTRST#	---	GPP_B15 / GSPI0_CS#	GPP_B20 / GSPI1_CLK	---	GPP_B22 / GSPI1_MOSI	---	GPP_F16 / EMMC_DATA3	GPP_F18 / EMMC_DATA5	GPP_F17 / EMMC_DATA4
AM	VCCIO_SENSE	VSSIO_SENSE	VSS	RTCX2	---	RTCX1	---	RTCRST#	GPD2 / LAN_WAKE#	---	VSS	---	GPP_B2 / VRALERT#	GPP_B11 / EXT_PWR_GATE#	---	VSS	GPP_B23 / SML1ALERT# / PCHHOT#	---	GPP_B19 / GSPI1_CS#	GPP_F19 / EMMC_DATA6	GPP_F22 / EMMC_CLK	GPP_F21 / EMMC_RCLK	GPP_F20 / EMMC_DATA7
AL	VCCPLL_OC	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	VSS	---	VSS	DCPDSW_1p0
AK	VCCSA	VSS	VSS	VCCPRIM_1p0	VCCRTC	VSS	VCCRTCPRIM_3p3	VSS	VCCPGPPA	---	RSVD_TP	RSVD_TP	VSS	GPP_F3 / I2S2_RXD	GPP_F2 / I2S2_TXD	VSS	GPP_F1 / I2S2_SFRM	GPP_F0 / I2S2_SCLK	---	---	---	---	---
AJ	---	---	VCCPRIM_3p3	VSS	VCCHDA	VSS	VCCDSW_3p3	VCCSPI	VSS	---	---	---	---	---	---	---	---	---	---	VSS	USB2P_3	USB2P_5	USB2N_5
AH	---	---	---	---	---	---	---	---	---	---	VSS	GPP_F7 / I2C3_SCL	GPP_F6 / I2C3_SDA	GPP_F5 / I2C2_SCL	GPP_F4 / I2C2_SDA	USB2P_10	USB2N_10	VSS	---	---	USB2N_3	USB2P_7	USB2N_7
AG	---	---	VSS	VSS	VSS	VSS	VSS	VSS	VCCPGPPB	---	---	---	---	---	---	---	---	---	---	USB2_VBUSSENSE	USB2_ID	USB2P_9	USB2N_9
AF	---	---	VCCSRAM_1P0	VCCSRAM_1P0	VCCPRIM_CORE	VCCPRIM_CORE	VSS	VCCPGPPF	VSS	---	GPP_F23	GPP_F9 / I2C4_SCL	GPP_F8 / I2C4_SDA	VSS	USB2P_8	USB2N_8	USB2P_6	USB2N_6	---	VSS	---	VSS	VSS
AE	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---
AD	---	---	VSS	VSS	VSS	VCCDSW_3p3	VCCDSW_3p3	VSS	VCCPGPPG	---	VSS	GPP_F11 / I2C5_SCL / ISH_I2C2_SCL	GPP_F10 / I2C5_SDA / ISH_I2C2_SDA	USB2P_4	USB2N_4	VSS	USB2P_2	USB2N_2	---	GPP_C23 / UART2_CTS#	GPP_C22 / UART2_RTS#	GPP_C21 / UART2_TXD	GPP_C20 / UART2_RXD
AC	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	GPP_C14 / UART1_RTS# / ISH_UART1_RTS#	GPP_C13 / UART1_TXD / ISH_UART1_TXD	GPP_C12 / UART1_RXD / ISH_UART1_RXD
AB	---	---	VSS	VCCPRIM_1P0	VCCPRIM_1P0	VSS	VCCPRIM_1p0	VSS	VSS	---	GPP_G1 / SD_DATA0	GPP_G2 / SD_DATA1	GPP_G0 / SD_CMD	USB2P_1	USB2N_1	VSS	SD_RCOMP	USB2_COMP	---	GPP_C15 / UART1_CTS# / ISH_UART1_CTS#	GPP_C11 / UART0_CTS#	GPP_C9 / UART0_TXD	GPP_C8 / UART0_RXD

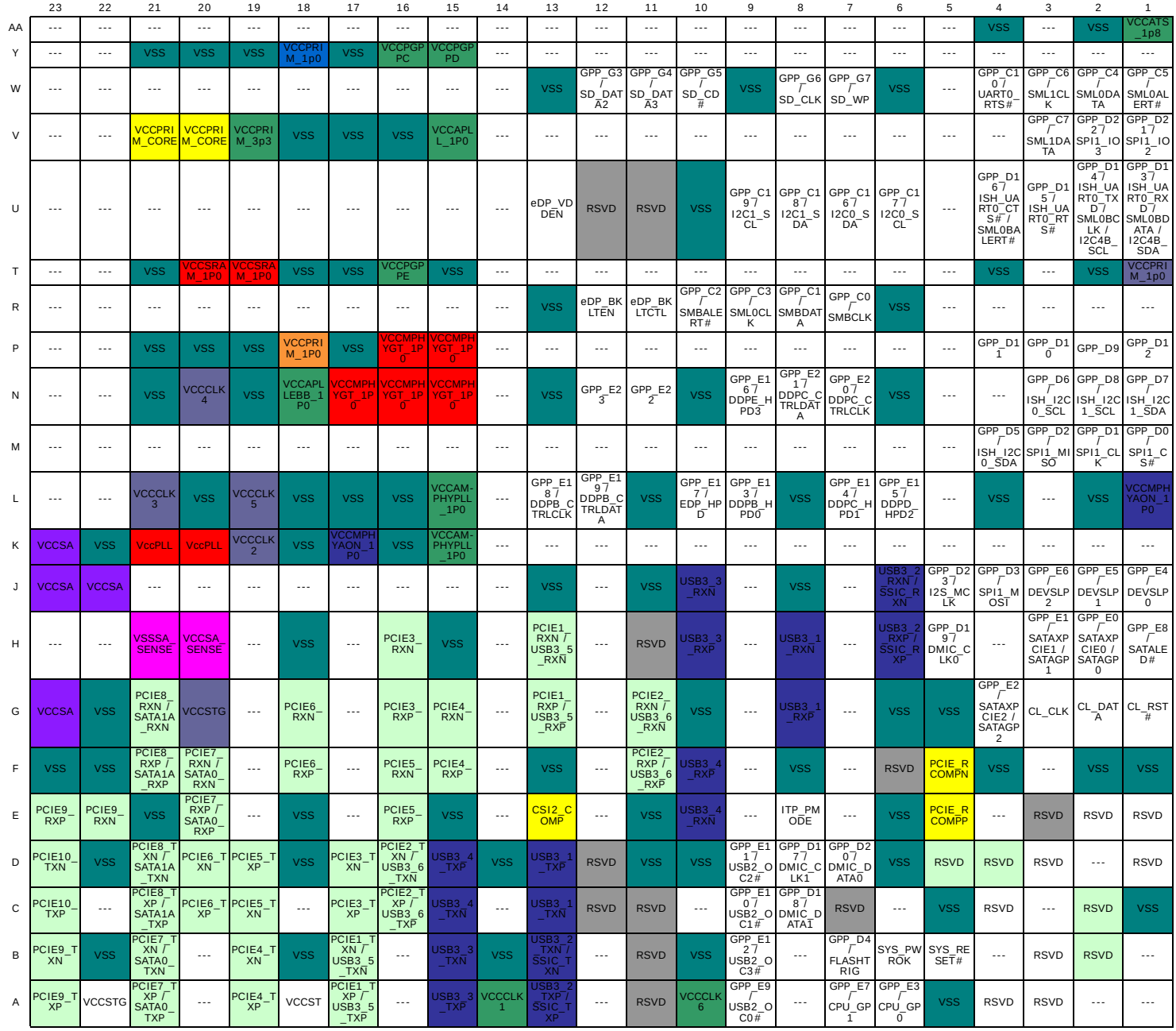
Figure 9-4. U/U-Quad Core Processor Ball Map (Lower Left, Columns 71-48)

	71	70	69	68	67	66	65	64	63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48
AA	VCCGT	VCCGT	VCCGT	VSS	VCCGT	VCCGT	VSS	VCCGT	VCCGT	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---
Y	---	---	---	---	---	---	---	---	---	VCCGT	---	---	---	---	---	---	---	---	---	---	---	---	---	---
W	VCCGT	VCCGT	VCCGT	VCCGT	VCCGT	VCCGT	VCCGT	VCCGT	VCCGT	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---
V	---	---	---	---	---	---	---	---	---	VCCOPC	---	---	---	---	---	---	---	---	---	---	---	---	---	---
U	VCCGT	VSS	VSS	VCCGT	VSS	VSS	VCCGT	VSS	VSS	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---
T	---	---	---	---	---	---	---	---	---	VCCGT	---	---	---	---	---	---	---	---	---	---	---	---	---	---
R	VCCGT	VCCGT	VCCGT	VCCGT	VCCGT	VCCGT	VCCGT	VCCGT	VCCGT	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---
P	---	---	---	---	---	---	---	---	---	VCCOPC	---	---	---	---	---	---	---	---	---	---	---	---	---	---
N	VCCGT	VCCGT	VCCGT	VSS	VCCGT	VCCGT	VSS	VCCGT	VCCGT	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---
M	---	---	---	---	---	---	---	---	---	VCCGT	---	---	---	---	---	---	---	---	---	---	---	---	---	---
L	VCCGT	VCCGT	VCCGT	VCCGT	VCCGT	VCCGT	VCCGT	VCCGT	VCCGT	VCCGT	---	---	---	---	---	---	---	---	---	---	---	---	---	---
K	VSS	VSS	---	VSS	VSS	VSS	VSS	VSS	VSS	---	VSS	VCCGT	---	VCCGT	---	VCCGT	VCCGT	---	VCCGT	VCCGT	---	VCCGT	---	VCCGT
J	RSVD	VCCGT_SENSE	VSSGT_SENSE	RSVD	---	---	---	---	---	---	---	VCCGT	---	VCCGT	---	VCCGT	VCCGT	---	VCCGT	VCCGT	---	VCCGT	---	VCCGT
H	VSS	CFG[12]	CFG[14]	---	---	OPCE_RCOMP	OPC_RCOMP	---	VCC_OPC_1P8	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---
G	CFG[13]	CFG[15]	CFG[9]	CFG[11]	---	VSS	VSS	---	VSS	---	VCC_OPC_1P8	VSS	---	VSS	---	DDI1_TXP[3]	VSS	---	DDI1_TXP[2]	VSS	---	DDI1_AUXN	---	VSS
F	CFG[8]	CFG[10]	---	VSS	---	CFG[19]	VSS	---	CFG[17]	---	RSVD	RSVD	---	DDI1_TXP[1]	---	DDI1_TXN[3]	DDI1_TXP[0]	---	DDI1_TXN[2]	RSVD	---	DDI1_AUXP	---	DDI2_AUXP
E	VSS	CFG[4]	---	CFG[0]	---	CFG[18]	VSS	---	CFG[16]	---	RSVD	CFG_RCOMP	---	DDI1_TXN[1]	---	VSS	DDI1_TXN[0]	---	VSS	eDP_RCOMP	---	VSS	---	DDI2_AUXN
D	RSVD	---	VSS	CFG[6]	CFG[3]	VSS	CFG[2]	VIDSOUT	CATERR#	VSS	PROC_PREQ#	PROC_TDI	PCH_JTAG_TDI	VSS	---	PROC_PRDY#	BPM#[1]	RSVD	VSS	DDI2_TXP[1]	DDI2_TXN[3]	DDI2_TXP[0]	---	VSS
C	RSVD	RSVD	---	CFG[5]	CFG[7]	---	PROCHOT#	PROC_SELECT#	THERMTRIP#	---	PCH_TRST#	PROC_TMS	PCH_JTAG_TMS	---	---	BPM#[3]	BPM#[0]	RSVD	---	DDI2_TXN[1]	DDI2_TXP[3]	DDI2_TXN[0]	---	---
B	VSS	RSVD	RSVD	---	CFG[1]	VSS	VCCST_PWRGD	---	VIDALERT#	VSS	PROC_TCK	---	PROC_TRST#	VSS	---	PCH_JTAG_TCK	---	BPM#[2]	VSS	EDP_DISP_UTIL	---	DDI2_TXP[2]	---	VSS
A	---	VSS	RSVD	PROCPWRGD	VSS	VCCGT	SKTOCC#	---	VIDSCK	VCCGT	PROC_TDO	---	JTAGX	VCCGT	---	PCH_JTAG_TDO	---	PECI	VCCGT	RSVD	---	DDI2_TXN[2]	---	VCCGT

Figure 9-5. U/U-Quad Core Processor Ball Map (Lower Middle, Columns 47-24)

	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32	31	30	29	28	27	26	25	24
AA	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---
Y	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---
W	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---
V	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---
U	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---
T	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---
R	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---
P	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---
N	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---
M	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---
L	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---
K	---	RSVD	RSVD	---	VCC	VCC	---	VCC	---	VCC	VCC	---	VCC	---	VCC	RSVD	---	VCCSA	---	VCCSA	VCCSA	---	VCCSA	---
J	---	VCCGT	VCCGT	---	VCCGT	VSS	---	VCC	---	VSS	VCC	---	VSS	---	VCC	VSS	---	VCC	---	VSS	VCCSA	---	VSS	---
H	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---
G	---	RSVD	VSS	---	VSS	VCC	---	VCC	---	VCC	VCC	---	VCC	---	VCC	VCC	---	VCC	---	VCCSA	VCCSA	---	VCCSA	---
F	---	RSVD	EDP_AUXP	---	CLKOUT_ITPXDP_N	VSS	---	VSS	---	VSS	VSS	---	VSS	---	VSS	VSS	---	PCIE12_RXP / SATA2_RXP	---	VSS	VSS	---	PCIE10_RXN	---
E	---	VSS	EDP_AUXN	---	CLKOUT_ITPXDP_P	XCLK_BIASREF	---	CLKOUT_PCIE_N5	---	CLKOUT_PCIE_P5	XTAL24_IN	---	XTAL24_OUT	---	VSS_SENSE	VCC_SENSE	---	PCIE12_RXN / SATA2_RXN	---	PCIE11_RXN / SATA1B_RXN	PCIE11_RXP / SATA1B_RXP	---	PCIE10_RXP	---
D	VSS	EDP_TXN[1]	VSS	VSS	---	CLKOUT_PCIE_N0	CLKOUT_PCIE_N2	CLKOUT_PCIE_N3	VSS	CSI2_DP1	CSI2_CLKP0	CSI2_DP2	---	VSS	CSI2_DP5	CSI2_CLKP1	CSI2_DP4	VSS	CSI2_CLKP2	CSI2_DP9	CSI2_DP11	VSS	VSS	PCIE11_TXN / SATA1B_TXN
C	EDP_TXN[0]	EDP_TXP[0]	EDP_TXP[1]	---	---	CLKOUT_PCIE_P0	CLKOUT_PCIE_P2	CLKOUT_PCIE_P3	---	CSI2_DN1	CSI2_CLKN0	CSI2_DN2	---	---	CSI2_DN5	CSI2_CLKN1	CSI2_DN4	---	CSI2_CLKN2	CSI2_DN9	CSI2_DN11	---	VSS	PCIE11_TXP / SATA1B_TXP
B	EDP_TXP[3]	---	EDP_TXP[2]	VSS	---	CLKOUT_PCIE_N1	---	CLKOUT_PCIE_N4	VSS	CSI2_DP3	---	CSI2_DP0	---	VSS	CSI2_DP7	---	CSI2_DP6	VSS	CSI2_DP8	---	CSI2_DP10	CSI2_CLKN3	PCIE12_TXP / SATA2_TXP	---
A	EDP_TXN[3]	---	EDP_TXN[2]	VCC	---	CLKOUT_PCIE_P1	---	CLKOUT_PCIE_P4	VCC	CSI2_DN3	---	CSI2_DN0	---	VCC	CSI2_DN7	---	CSI2_DN6	VCC	CSI2_DN8	---	CSI2_DN10	CSI2_CLKP3	PCIE12_TXN / SATA2_TXN	---

Figure 9-6. U/U-Quad Core Processor Ball Map (Lower Right, Columns 23-1)



	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
AA	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	VSS	---	VSS	VCCATS_1p8
Y	---	---	VSS	VSS	VSS	VCCPRIM_1p0	VSS	VCCPGPPC	VCCPGPPD	---	---	---	---	---	---	---	---	---	---	---	---	---	---
W	---	---	---	---	---	---	---	---	---	---	VSS	GPP_G3/SD_DATA2	GPP_G4/SD_DATA3	GPP_G5/SD_CD#	VSS	GPP_G6/SD_CLK	GPP_G7/SD_WP	VSS	---	GPP_C10/UART0_RTS#	GPP_C6/SML1CLK	GPP_C4/SML0DATA	GPP_C5/SML0ALERT#
V	---	---	VCCPRIM_CORE	VCCPRIM_CORE	VCCPRIM_3p3	VSS	VSS	VSS	VCCAPLL_1P0	---	---	---	---	---	---	---	---	---	---	---	GPP_C7/SML1DATA	GPP_D22/SPI1_IO3	GPP_D21/SPI1_IO2
U	---	---	---	---	---	---	---	---	---	---	eDP_VDDEN	RSVD	RSVD	VSS	GPP_C19/I2C1_SCL	GPP_C18/I2C1_SDA	GPP_C16/I2C0_SDA	GPP_C17/I2C0_SCL	---	GPP_D16/ISH_UART0_CTS#/SML0BALERT#	GPP_D15/ISH_UART0_RTS#	GPP_D14/ISH_UART0_TXD/SML0BCLK/I2C4B_SCL	GPP_D13/ISH_UART0_RXD/SML0BDATA/I2C4B_SDA
T	---	---	VSS	VCCSRAM_1P0	VCCSRAM_1P0	VSS	VSS	VCCPGPPE	VSS	---	---	---	---	---	---	---	---	---	---	VSS	---	VSS	VCCPRIM_1p0
R	---	---	---	---	---	---	---	---	---	---	VSS	eDP_BKLTEN	eDP_BKLTCTL	GPP_C2/SMBALERT#	GPP_C3/SML0CLK	GPP_C1/SMBDATA	GPP_C0/SMBCLK	VSS	---	---	---	---	---
P	---	---	VSS	VSS	VSS	VCCPRIM_1P0	VSS	VCCMPHYGT_1P0	VCCMPHYGT_1P0	---	---	---	---	---	---	---	---	---	---	GPP_D11	GPP_D10	GPP_D9	GPP_D12
N	---	---	VSS	VCCCLK4	VSS	VCCAPLLEBB_1P0	VCCMPHYGT_1P0	VCCMPHYGT_1P0	VCCMPHYGT_1P0	---	VSS	GPP_E23	GPP_E22	VSS	GPP_E16/DDPE_HPD3	GPP_E21/DDPC_CTRLDATA	GPP_E20/DDPC_CTRLCLK	VSS	---	---	GPP_D6/ISH_I2C0_SCL	GPP_D8/ISH_I2C1_SCL	GPP_D7/ISH_I2C1_SDA
M	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	GPP_D5/ISH_I2C0_SDA	GPP_D2/SPI1_MISO	GPP_D1/SPI1_CLK	GPP_D0/SPI1_CS#
L	---	---	VCCCLK3	VSS	VCCCLK5	VSS	VSS	VSS	VCCAM-PHYPLL_1P0	---	GPP_E18/DDPB_CTRLCLK	GPP_E19/DDPB_CTRLDATA	VSS	GPP_E17/EDP_HPD	GPP_E13/DDPB_HPD0	VSS	GPP_E14/DDPC_HPD1	GPP_E15/DDPD_HPD2	---	VSS	---	VSS	VCCMPHYAON_1P0
K	VCCSA	VSS	VccPLL	VccPLL	VCCCLK2	VSS	VCCMPHYAON_1P0	VSS	VCCAM-PHYPLL_1P0	---	---	---	---	---	---	---	---	---	---	---	---	---	---
J	VCCSA	VCCSA	---	---	---	---	---	---	---	---	VSS	---	VSS	USB3_3_RXN	---	VSS	---	USB3_2_RXN/SSIC_RXN	GPP_D23/I2S_MCLK	GPP_D3/SPI1_MOSI	GPP_E6/DEVSLP2	GPP_E5/DEVSLP1	GPP_E4/DEVSLP0
H	---	---	VSSSA_SENSE	VCCSA_SENSE	---	VSS	---	PCIE3_RXN	VSS	---	PCIE1_RXN/USB3_5_RXN	---	RSVD	USB3_3_RXP	---	USB3_1_RXN	---	USB3_2_RXP/SSIC_RXP	GPP_D19/DMIC_CLK0	---	GPP_E1/SATAXPCIE1/SATAGP1	GPP_E0/SATAXPCIE0/SATAGP0	GPP_E8/SATALED#
G	VCCSA	VSS	PCIE8_RXN/SATA1A_RXN	VCCSTG	---	PCIE6_RXN	---	PCIE3_RXP	PCIE4_RXN	---	PCIE1_RXP/USB3_5_RXP	---	PCIE2_RXN/USB3_6_RXN	VSS	---	USB3_1_RXP	---	VSS	VSS	GPP_E2/SATAXPCIE2/SATAGP2	CL_CLK	CL_DATA	CL_RST#
F	VSS	VSS	PCIE8_RXP/SATA1A_RXP	PCIE7_RXN/SATA0_RXN	---	PCIE6_RXP	---	PCIE5_RXN	PCIE4_RXP	---	VSS	---	PCIE2_RXP/USB3_6_RXP	USB3_4_RXP	---	VSS	---	RSVD	PCIE_RCOMPN	VSS	---	VSS	VSS
E	PCIE9_RXP	PCIE9_RXN	VSS	PCIE7_RXP/SATA0_RXP	---	VSS	---	PCIE5_RXP	VSS	---	CSI2_COMP	---	VSS	USB3_4_RXN	---	ITP_PMODE	---	VSS	PCIE_RCOMPP	---	RSVD	RSVD	RSVD
D	PCIE10_TXN	VSS	PCIE8_TXN/SATA1A_TXN	PCIE6_TXN	PCIE5_TXP	VSS	PCIE3_TXN	PCIE2_TXN/USB3_6_TXN	USB3_4_TXP	VSS	USB3_1_TXP	RSVD	VSS	VSS	GPP_E11/USB2_OC2#	GPP_D17/DMIC_CLK1	GPP_D20/DMIC_DATA0	VSS	RSVD	RSVD	RSVD	---	RSVD
C	PCIE10_TXP	---	PCIE8_TXP/SATA1A_TXP	PCIE6_TXP	PCIE5_TXN	---	PCIE3_TXP	PCIE2_TXP/USB3_6_TXP	USB3_4_TXN	---	USB3_1_TXN	RSVD	RSVD	---	GPP_E10/USB2_OC1#	GPP_D18/DMIC_DATA1	RSVD	---	VSS	RSVD	---	RSVD	VSS
B	PCIE9_TXN	VSS	PCIE7_TXN/SATA0_TXN	---	PCIE4_TXN	VSS	PCIE1_TXN/USB3_5_TXN	---	USB3_3_TXN	VSS	USB3_2_TXN/SSIC_TXN	---	RSVD	VSS	GPP_E12/USB2_OC3#	---	GPP_D4/FLASHTRIG	SYS_PWROK	SYS_RESET#	---	RSVD	RSVD	---
A	PCIE9_TXP	VCCSTG	PCIE7_TXP/SATA0_TXP	---	PCIE4_TXP	VCCST	PCIE1_TXP/USB3_5_TXP	---	USB3_3_TXP	VCCCLK1	USB3_2_TXP/SSIC_TXP	---	RSVD	VCCCLK6	GPP_E9/USB2_OC0#	---	GPP_E7/CPU_GP1	GPP_E3/CPU_GP0	VSS	RSVD	RSVD	---	---

Table 9-1. U/U-Quad Core Processor Ball List (Sheet 1 of 39)

Ball #	Ball Name	DDR3L	LPDDR3	DDR4	Interleaved (IL)	Non-Interleaved (NIL)	X[um]	Y[um]
A10	VCCCLK6						14988.794	-10989.056
A11	RSVD						14313.154	-11314.176
A13	USB3_2_TXP / SSIC_TXP						13186.41	-11314.176
A14	VCCCLK1						12510.77	-10989.056
A15	USB3_3_TXP						11835.13	-11314.176
A17	PCIE1_TXP / USB3_5_TXP						10708.386	-11314.176
A18	VCCST						10032.746	-10989.056
A19	PCIE4_TXP						9357.106	-11314.176
A21	PCIE7_TXP / SATA0_TXP						8230.362	-11314.176
A22	VCCSTG						7554.722	-10989.056
A23	PCIE9_TXP						6879.082	-11314.176
A25	PCIE12_TXN / SATA2_TXN						5752.338	-11314.176
A26	CSI2_CLKP3						5076.698	-10989.056
A27	CSI2_DN10						4401.058	-11314.176
A29	CSI2_DN8						3274.314	-11314.176
A3	RSVD						19348.958	-11314.176
A30	VCC						2598.674	-10989.056
A31	CSI2_DN6						1923.034	-11314.176
A33	CSI2_DN7						796.29	-11314.176
A34	VCC						120.65	-10989.056
A36	CSI2_DN0						-554.99	-11314.176
A38	CSI2_DN3						-1681.734	-11314.176
A39	VCC						-2357.374	-10989.056
A4	RSVD						18698.718	-11314.176
A40	CLKOUT_PCIE_P4						-3033.014	-11314.176
A42	CLKOUT_PCIE_P1						-4159.758	-11314.176
A44	VCC						-4835.398	-10989.056
A45	EDP_TXN[2]						-5511.038	-11314.176
A47	EDP_TXN[3]						-6637.782	-11314.176
A48	VCCGT						-7313.422	-10989.056
A5	VSS						18048.478	-11314.176
A50	DDI2_TXN[2]						-7989.062	-11314.176
A52	RSVD						-9115.806	-11314.176
A53	VCCGT						-9791.446	-10989.056
A54	PECI						-10467.086	-11314.176
A56	PCH_JTAG_TDO						-11593.83	-11314.176
A58	VCCGT						-12269.47	-10989.056

Table 9-1. U/U-Quad Core Processor Ball List (Sheet 2 of 39)

Ball #	Ball Name	DDR3L	LPDDR3	DDR4	Interleaved (IL)	Non-Interleaved (NIL)	X[um]	Y[um]
A59	JTAGX						-12945.11	-11314.176
A6	GPP_E3 / CPU_GP0						17466.818	-10989.056
A61	PROC_TDO						-14071.854	-11314.176
A62	VCCGT						-14747.494	-10989.056
A63	VIDSCK						-15423.134	-11314.176
A65	SKTOCC#						-16549.878	-11314.176
A66	VCCGT						-17225.518	-10989.056
A67	VSS						-17901.158	-11314.176
A68	PROCPWRGD						-18551.652	-11314.176
A69	RSVD						-19201.892	-11314.176
A7	GPP_E7 / CPU_GP1						16791.178	-11314.176
A70	VSS						-19852.132	-11314.176
A9	GPP_E9 / USB2_OC0#						15664.434	-11314.176
AA1	VCCATS_1p8						19989.038	-510.54
AA2	VSS						19338.798	-510.54
AA4	VSS						18363.438	-510.54
AA63	VCCGT						-15112.492	-595.63
AA64	VCCGT						-15762.732	-595.63
AA65	VSS						-16412.972	-595.63
AA66	VCCGT						-17063.212	-595.63
AA67	VCCGT						-17713.452	-595.63
AA68	VSS						-18363.692	-595.63
AA69	VCCGT						-19013.932	-595.63
AA70	VCCGT						-19664.172	-595.63
AA71	VCCGT						-20314.412	-595.63
AB1	GPP_C8 / UART0_RXD						20314.158	152.4
AB10	USB2P_1						14984.476	-133.096
AB11	GPP_G0 / SD_CMD						14334.236	-133.096
AB12	GPP_G2 / SD_DATA1						13683.996	-133.096
AB13	GPP_G1 / SD_DATA0						13033.756	-133.096
AB15	VSS						12188.19	-8.89
AB16	VSS						11537.95	-8.89
AB17	VCCPRIM_1p0						10887.71	-8.89
AB18	VSS						10237.47	-8.89
AB19	VCCPRIM_1P0						9587.23	-8.89
AB2	GPP_C9 / UART0_TXD						19663.918	152.4
AB20	VCCPRIM_1P0						8936.99	-8.89
AB21	VSS						8286.75	-8.89

Table 9-1. U/U-Quad Core Processor Ball List (Sheet 3 of 39)

Ball #	Ball Name	DDR3L	LPDDR3	DDR4	Interleaved (IL)	Non-Interleaved (NIL)	X[um]	Y[um]
AB3	GPP_C11 / UART0_CTS#						19013.678	152.4
AB4	GPP_C15 / UART1_CTS# / ISH_UART1_CTS#						18363.438	152.4
AB6	USB2_COMP						17585.436	-133.096
AB62	VCCOPC						-14643.862	-138.43
AB7	SD_RCOMP						16935.196	-133.096
AB8	VSS						16284.956	-133.096
AB9	USB2N_1						15634.716	-133.096
AC1	GPP_C12 / UART1_RXD / ISH_UART1_RXD						19989.038	815.34
AC2	GPP_C13 / UART1_TXD / ISH_UART1_TXD						19338.798	815.34
AC3	GPP_C14 / UART1_RTS# / ISH_UART1_RTS#						18688.558	815.34
AC63	VCCOPC_SENSE						-15112.492	318.77
AC64	VCCGT						-15762.732	318.77
AC65	VCCGT						-16412.972	318.77
AC66	VCCGT						-17063.212	318.77
AC67	VCCGT						-17713.452	318.77
AC68	VCCGT						-18363.692	318.77
AC69	VCCGT						-19013.932	318.77
AC70	VCCGT						-19664.172	318.77
AC71	VCCGT						-20314.412	318.77
AD1	GPP_C20 / UART2_RXD						20314.158	1478.28
AD10	USB2P_4						14984.476	933.704
AD11	GPP_F10 / I2C5_SDA / ISH_I2C2_SDA						14334.236	933.704
AD12	GPP_F11/ I2C5_SCL / ISH_I2C2_SCL						13683.996	933.704
AD13	VSS						13033.756	933.704
AD15	VCCPGPPG						12188.19	829.31
AD16	VSS						11537.95	829.31
AD17	VCCDSW_3p3						10887.71	829.31
AD18	VCCDSW_3p3						10237.47	829.31
AD19	VSS						9587.23	829.31
AD2	GPP_C21 / UART2_TXD						19663.918	1478.28
AD20	VSS						8936.99	829.31
AD21	VSS						8286.75	829.31
AD3	GPP_C22 / UART2_RTS#						19013.678	1478.28
AD4	GPP_C23 / UART2_CTS#						18363.438	1478.28
AD6	USB2N_2						17585.436	933.704
AD62	VSS						-14643.862	775.97

Table 9-1. U/U-Quad Core Processor Ball List (Sheet 4 of 39)

Ball #	Ball Name	DDR3L	LPDDR3	DDR4	Interleaved (IL)	Non-Interleaved (NIL)	X[um]	Y[um]
AD7	USB2P_2						16935.196	933.704
AD8	VSS						16284.956	933.704
AD9	USB2N_4						15634.716	933.704
AE62	VCCEOPIO						-14643.862	1690.37
AE63	VSSOPC_SENSE						-15112.492	1233.17
AE64	VSS						-15762.732	1233.17
AE65	VSS						-16412.972	1233.17
AE66	VSS						-17063.212	1233.17
AE67	VSS						-17713.452	1233.17
AE68	VSS						-18363.692	1233.17
AE69	VSS						-19013.932	1233.17
AF1	VSS						19989.038	2141.22
AF10	VSS						14984.476	2000.504
AF11	GPP_F8 / I2C4_SDA						14334.236	2000.504
AF12	GPP_F9 / I2C4_SCL						13683.996	2000.504
AF13	GPP_F23						13033.756	2000.504
AF15	VSS						12188.19	1667.51
AF16	VCCPGPPF						11537.95	1667.51
AF17	VSS						10887.71	1667.51
AF18	VCCPRIM_CORE						10237.47	1667.51
AF19	VCCPRIM_CORE						9587.23	1667.51
AF2	VSS						19338.798	2141.22
AF20	VCCSRAM_1P0						8936.99	1667.51
AF21	VCCSRAM_1P0						8286.75	1667.51
AF4	VSS						18363.438	2141.22
AF6	USB2N_6						17585.436	2000.504
AF63	VSS						-15112.492	2147.57
AF64	DDR1_DQ[1] / DDR0_DQ[17]				DDR1_DQ[1]	DDR0_DQ[17]	-15762.732	2147.57
AF65	DDR1_DQ[0] / DDR0_DQ[16]				DDR1_DQ[0]	DDR0_DQ[16]	-16412.972	2147.57
AF66	DDR1_DQ[4] / DDR0_DQ[20]				DDR1_DQ[4]	DDR0_DQ[20]	-17063.212	2147.57
AF67	DDR1_DQ[5] / DDR0_DQ[21]				DDR1_DQ[5]	DDR0_DQ[21]	-17713.452	2147.57
AF68	DDR1_DQ[9] / DDR0_DQ[25]				DDR1_DQ[9]	DDR0_DQ[25]	-18363.692	1939.036
AF69	DDR1_DQ[13] / DDR0_DQ[29]				DDR1_DQ[13]	DDR0_DQ[29]	-19013.932	1939.036
AF7	USB2P_6						16935.196	2000.504
AF70	DDR1_DQ[8] / DDR0_DQ[24]				DDR1_DQ[8]	DDR0_DQ[24]	-19664.172	1839.976

Table 9-1. U/U-Quad Core Processor Ball List (Sheet 5 of 39)

Ball #	Ball Name	DDR3L	LPDDR3	DDR4	Interleaved (IL)	Non-Interleaved (NIL)	X[um]	Y[um]
AF71	DDR1_DQ[12] / DDR0_DQ[28]				DDR1_DQ[12]	DDR0_DQ[28]	-20314.412	1839.976
AF8	USB2N_8						16284.956	2000.504
AF9	USB2P_8						15634.716	2000.504
AG1	USB2N_9						20314.158	2804.16
AG15	VCCPGPPB						12188.19	2505.71
AG16	VSS						11537.95	2505.71
AG17	VSS						10887.71	2505.71
AG18	VSS						10237.47	2505.71
AG19	VSS						9587.23	2505.71
AG2	USB2P_9						19663.918	2804.16
AG20	VSS						8936.99	2505.71
AG21	VSS						8286.75	2505.71
AG3	USB2_ID						19013.678	2804.16
AG4	USB2_VBUSSENSE						18363.438	2804.16
AG62	VCCEOPIO						-14643.862	2604.77
AG69	DDR1_DQSN[1] / DDR0_DQSN[3]				DDR1_DQSN[1]	DDR0_DQSN[3]	-18688.812	2601.976
AG70	DDR1_DQSP[1] / DDR0_DQSP[3]				DDR1_DQSP[1]	DDR0_DQSP[3]	-19339.052	2502.916
AG71	VSS						-19989.292	2502.916
AH1	USB2N_7						19989.038	3467.1
AH10	GPP_F5 / I2C2_SCL						14984.476	3067.304
AH11	GPP_F6 / I2C3_SDA						14334.236	3067.304
AH12	GPP_F7 / I2C3_SCL						13683.996	3067.304
AH13	VSS						13033.756	3067.304
AH2	USB2P_7						19338.798	3467.1
AH3	USB2N_3						18688.558	3467.1
AH6	VSS						17585.436	3067.304
AH63	VSS						-15112.492	3061.97
AH64	VSS						-15762.732	3061.97
AH65	DDR1_DQSP[0] / DDR0_DQSP[2]				DDR1_DQSP[0]	DDR0_DQSP[2]	-16412.972	3061.97
AH66	DDR1_DQSN[0] / DDR0_DQSN[2]				DDR1_DQSN[0]	DDR0_DQSN[2]	-17063.212	3061.97
AH67	VSS						-17713.452	3061.97
AH68	DDR1_DQ[11] / DDR0_DQ[27]				DDR1_DQ[11]	DDR0_DQ[27]	-18363.692	3165.856
AH69	DDR1_DQ[15] / DDR0_DQ[31]				DDR1_DQ[15]	DDR0_DQ[31]	-19013.932	3165.856
AH7	USB2N_10						16935.196	3067.304
AH70	DDR1_DQ[14] / DDR0_DQ[30]				DDR1_DQ[14]	DDR0_DQ[30]	-19664.172	3165.856

Table 9-1. U/U-Quad Core Processor Ball List (Sheet 6 of 39)

Ball #	Ball Name	DDR3L	LPDDR3	DDR4	Interleaved (IL)	Non-Interleaved (NIL)	X[um]	Y[um]
AH71	DDR1_DQ[10] / DDR0_DQ[26]				DDR1_DQ[10]	DDR0_DQ[26]	-20314.412	3165.856
AH8	USB2P_10						16284.956	3067.304
AH9	GPP_F4 / I2C2_SDA						15634.716	3067.304
AJ1	USB2N_5						20314.158	4130.04
AJ15	VSS						12188.19	3343.91
AJ16	VCCSPI						11537.95	3343.91
AJ17	VCCDSW_3p3						10887.71	3343.91
AJ18	VSS						10237.47	3343.91
AJ19	VCCHDA						9587.23	3343.91
AJ2	USB2P_5						19663.918	4130.04
AJ20	VSS						8936.99	3343.91
AJ21	VCCPRIM_3p3						8286.75	3343.91
AJ3	USB2P_3						19013.678	4130.04
AJ4	VSS						18363.438	4130.04
AJ62	VSSEOPIO_SENSE						-14643.862	3519.17
AK10	GPP_F3 / I2S2_RXD						14984.476	4007.104
AK11	VSS						14334.236	4007.104
AK12	RSVD_TP						13683.996	4007.104
AK13	RSVD_TP						13033.756	4007.104
AK15	VCCPGPPA						12188.19	4182.11
AK16	VSS						11537.95	4182.11
AK17	VCCRTCPRIM_3p3						10887.71	4182.11
AK18	VSS						10237.47	4182.11
AK19	VCCRTC						9587.23	4182.11
AK20	VCCPRIM_1p0						8936.99	4182.11
AK21	VSS						8286.75	4182.11
AK22	VSS						7595.616	4009.136
AK23	VCCSA						6681.216	4009.136
AK25	VCCSA						5766.816	4009.136
AK27	VSS						4852.416	4009.136
AK28	VCCIO						3938.016	4009.136
AK30	VCCIO						3023.616	4009.136
AK32	RSVD						2109.216	4009.136
AK33	VCC						1194.816	4009.136
AK35	VCC						280.416	4009.136
AK37	VCC						-633.984	4009.136
AK38	VCC						-1548.384	4009.136
AK40	VCC						-2462.784	4009.136

Table 9-1. U/U-Quad Core Processor Ball List (Sheet 7 of 39)

Ball #	Ball Name	DDR3L	LPDDR3	DDR4	Interleaved (IL)	Non-Interleaved (NIL)	X[um]	Y[um]
AK42	VccGTx						-3377.184	4009.136
AK43	VccGTx						-4291.584	4009.136
AK45	VccGTx						-5205.984	4009.136
AK46	VccGTx						-6120.384	4009.136
AK48	VccGTx						-7034.784	4009.136
AK50	VccGTx						-7949.184	4009.136
AK52	VccGTx						-8863.584	4009.136
AK53	VccGTx						-9777.984	4009.136
AK55	VccGTx						-10692.384	4009.136
AK56	VccGTx						-11606.784	4009.136
AK58	VccGTx						-12521.184	4009.136
AK6	GPP_F0 / I2S2_SCLK						17585.436	4007.104
AK60	VccGTx						-13435.584	4009.136
AK62	VCCGTx_SENSE						-14459.712	4143.756
AK63	VSS						-15112.492	3976.37
AK64	DDR1_DQ[3] / DDR0_DQ[19]				DDR1_DQ[3]	DDR0_DQ[19]	-15762.732	3976.37
AK65	DDR1_DQ[2] / DDR0_DQ[18]				DDR1_DQ[2]	DDR0_DQ[18]	-16412.972	3976.37
AK66	DDR1_DQ[7] / DDR0_DQ[23]				DDR1_DQ[7]	DDR0_DQ[23]	-17063.212	3976.37
AK67	DDR1_DQ[6] / DDR0_DQ[22]				DDR1_DQ[6]	DDR0_DQ[22]	-17713.452	3976.37
AK68	VSS						-18363.692	3828.796
AK69	VSS						-19339.052	3828.796
AK7	GPP_F1 / I2S2_SFRM						16935.196	4007.104
AK70	VccGTx						-19989.292	3828.796
AK8	VSS						16284.956	4007.104
AK9	GPP_F2 / I2S2_TXD						15634.716	4007.104
AL1	DCPDSW_1p0						19989.038	4792.98
AL2	VSS						19338.798	4792.98
AL23	VCCPLL_OC						7138.416	4473.956
AL25	RSVD						6224.016	4473.956
AL27	RSVD						5309.616	4473.956
AL28	VSS						4395.216	4473.956
AL30	VCCIO						3480.816	4473.956
AL32	VSS						2566.416	4473.956
AL33	VCC						1652.016	4473.956
AL35	VSS						737.616	4473.956
AL37	VCC						-176.784	4473.956
AL38	VSS						-1091.184	4473.956

Table 9-1. U/U-Quad Core Processor Ball List (Sheet 8 of 39)

Ball #	Ball Name	DDR3L	LPDDR3	DDR4	Interleaved (IL)	Non-Interleaved (NIL)	X[um]	Y[um]
AL4	VSS						18363.438	4792.98
AL40	VCC						-2005.584	4473.956
AL42	VCCIO						-2919.984	4473.956
AL43	VccGTx						-3834.384	4473.956
AL45	VSS						-4748.784	4473.956
AL46	VccGTx						-5663.184	4473.956
AL48	VSS						-6577.584	4473.956
AL50	VccGTx						-7491.984	4473.956
AL52	VSS						-8406.384	4473.956
AL53	VccGTx						-9320.784	4473.956
AL55	VSS						-10235.184	4473.956
AL56	VccGTx						-11149.584	4473.956
AL58	VSS						-12063.984	4473.956
AL60	VccGTx						-12978.384	4473.956
AL61	VSSGTx_SENSE						-13892.784	4473.956
AL63	VCCEOPIO_SENSE						-15112.492	4845.05
AL64	VSS						-15762.732	4845.05
AL65	VSS						-16412.972	4845.05
AL66	VSS						-17063.212	4845.05
AL68	DDR0_DQ[1]						-18363.692	4491.736
AL69	DDR0_DQ[5]						-19013.932	4491.736
AL70	DDR0_DQ[4]						-19664.172	4491.736
AL71	DDR0_DQ[0]						-20314.412	4491.736
AM1	GPP_F20 / EMMC_DATA7						20314.158	5455.92
AM10	GPP_B11 / EXT_PWR_GATE#						14910.816	4946.396
AM11	GPP_B2 / VRALERT#						13996.416	4946.396
AM13	VSS						13082.016	4946.396
AM15	GPD2 / LAN_WAKE#						12167.616	4946.396
AM16	RTCRST#						11253.216	4946.396
AM18	RTCX1						10338.816	4946.396
AM2	GPP_F21 / EMMC_RCLK						19663.918	5455.92
AM20	RTCX2						9424.416	4946.396
AM21	VSS						8510.016	4946.396
AM22	VSSIO_SENSE						7595.616	4946.396
AM23	VCCIO_SENSE						6681.216	4946.396
AM25	VSS						5766.816	4946.396
AM27	VSS						4852.416	4946.396
AM28	VCCIO						3938.016	4946.396

Table 9-1. U/U-Quad Core Processor Ball List (Sheet 9 of 39)

Ball #	Ball Name	DDR3L	LPDDR3	DDR4	Interleaved (IL)	Non-Interleaved (NIL)	X[um]	Y[um]
AM3	GPP_F22 / EMMC_CLK						19013.678	5455.92
AM30	VCCIO						3023.616	4946.396
AM32	VCC						2109.216	4946.396
AM33	VCC						1194.816	4946.396
AM35	VCC						280.416	4946.396
AM37	VCC						-633.984	4946.396
AM38	VCC						-1548.384	4946.396
AM4	GPP_F19 / EMMC_DATA6						18363.438	5455.92
AM40	VDDQC						-2462.784	4946.396
AM42	VCCIO						-3377.184	4946.396
AM43	VSS						-4291.584	4946.396
AM45	VSS						-5205.984	4946.396
AM46	VSS						-6120.384	4946.396
AM48	VccGTx						-7034.784	4946.396
AM5	GPP_B19 / GSPI1_CS#						17654.016	4946.396
AM50	VccGTx						-7949.184	4946.396
AM52	VccGTx						-8863.584	4946.396
AM53	VccGTx						-9777.984	4946.396
AM55	VSS						-10692.384	4946.396
AM56	VccGTx						-11606.784	4946.396
AM58	VccGTx						-12521.184	4946.396
AM60	VSS						-13435.584	4946.396
AM61	VSS						-14349.984	4946.396
AM68	VSS						-18038.572	5055.616
AM69	DDR0_DQSP[0]						-18688.812	5055.616
AM7	GPP_B23 / SML1ALERT# / PCHHOT#						16739.616	4946.396
AM70	DDR0_DQSN[0]						-19339.052	5154.676
AM71	VSS						-19989.292	5154.676
AM8	VSS						15825.216	4946.396
AN1	GPP_F17 / EMMC_DATA4						19989.038	6118.86
AN10	GPP_B13 / PLTRST#						14910.816	5596.636
AN11	GPP_B0 / CORE_VID0						13996.416	5596.636
AN13	GPP_B1 / CORE_VID1						13082.016	5596.636
AN15	SLP_SUS#						12167.616	5596.636
AN16	GPD6 / SLP_A#						11253.216	5596.636
AN18	SRTCRST#						10338.816	5596.636
AN2	GPP_F18 / EMMC_DATA5						19338.798	6118.86
AN20	VSS						9424.416	5596.636

Table 9-1. U/U-Quad Core Processor Ball List (Sheet 10 of 39)

Ball #	Ball Name	DDR3L	LPDDR3	DDR4	Interleaved (IL)	Non-Interleaved (NIL)	X[um]	Y[um]
AN21	DDR1_DQ[63]						8510.016	5596.636
AN22	DDR1_DQ[60]						7595.616	5596.636
AN23	VSS						6681.216	5596.636
AN25	DDR1_DQ[54]						5766.816	5596.636
AN27	DDR1_DQ[53]						4852.416	5596.636
AN28	VSS						3938.016	5596.636
AN3	GPP_F16 / EMMC_DATA3						18688.558	6118.86
AN30	VSS						3023.616	5596.636
AN32	VSS						2109.216	5596.636
AN33	VSS						1194.816	5596.636
AN35	VSS						280.416	5596.636
AN37	VSS						-633.984	5596.636
AN38	VSS						-1548.384	5596.636
AN40	VSS						-2462.784	5596.636
AN42	VSS						-3377.184	5596.636
AN43	DDR1_ALERT#						-4291.584	5596.636
AN45	DDR1_CKN[0]						-5205.984	5596.636
AN46	DDR1_CKN[1]						-6120.384	5596.636
AN48	DDR1_MA[11] / DDR1_CAA[7] / DDR1_MA[11]	DDR1_MA[11]	DDR1_CAA[7]	DDR1_MA[11]			-7034.784	5596.636
AN5	GPP_B22 / GSPI1_MOSI						17654.016	5596.636
AN50	DDR1_MA[12] / DDR1_CAA[6] / DDR1_MA[12]	DDR1_MA[12]	DDR1_CAA[6]	DDR1_MA[12]			-7949.184	5596.636
AN52	DDR1_MA[14] / DDR1_CAA[9]/ DDR1_BG[1]	DDR1_MA[14]	DDR1_CAA[9]	DDR1_BG[1]			-8863.584	5596.636
AN53	DDR1_MA[15] / DDR1_CAA[8]/ DDR1_ACT#	DDR1_MA[15]	DDR1_CAA[8]	DDR1_ACT#			-9777.984	5596.636
AN55	DDR1_CKE[2]						-10692.384	5596.636
AN56	DDR1_CKE[0]						-11606.784	5596.636
AN58	VSS						-12521.184	5596.636
AN60	DDR1_DQ[27] / DDR0_DQ[59]				DDR1_DQ[27]	DDR0_DQ[59]	-13435.584	5596.636
AN61	DDR1_DQ[28] / DDR0_DQ[60]				DDR1_DQ[28]	DDR0_DQ[60]	-14349.984	5596.636
AN63	VSS						-15264.384	5596.636
AN65	DDR1_DQ[19] / DDR0_DQ[51]				DDR1_DQ[19]	DDR0_DQ[51]	-16178.784	5596.636
AN66	DDR1_DQ[20] / DDR0_DQ[52]				DDR1_DQ[20]	DDR0_DQ[52]	-17093.184	5596.636
AN68	DDR0_DQ[2]						-18363.692	5718.556

Table 9-1. U/U-Quad Core Processor Ball List (Sheet 11 of 39)

Ball #	Ball Name	DDR3L	LPDDR3	DDR4	Interleaved (IL)	Non-Interleaved (NIL)	X[um]	Y[um]
AN69	DDR0_DQ[3]						-19013.932	5718.556
AN7	GPP_B20 / GSPI1_CLK						16739.616	5596.636
AN70	DDR0_DQ[6]						-19664.172	5817.616
AN71	DDR0_DQ[7]						-20314.412	5817.616
AN8	GPP_B15 / GSPI0_CS#						15825.216	5596.636
AP1	GPP_F14 / EMMC_DATA1						20314.158	6781.8
AP10	VSS						14910.816	6246.876
AP11	GPP_A15 / SUSACK#						13996.416	6246.876
AP13	Sx_EXIT_HOLDOFF# / GPP_A12 / BM_BUSY# / ISH_GP6						13082.016	6246.876
AP15	GPD4 / SLP_S3#						12167.616	6246.876
AP16	INTRUDER#						11253.216	6246.876
AP18	VSS						10338.816	6246.876
AP2	GPP_F13 / EMMC_DATA0						19663.918	6781.8
AP20	VSS						9424.416	6246.876
AP21	DDR1_DQ[62]						8510.016	6246.876
AP22	DDR1_DQ[61]						7595.616	6246.876
AP23	VSS						6681.216	6246.876
AP25	DDR1_DQ[55]						5766.816	6246.876
AP27	DDR1_DQ[52]						4852.416	6246.876
AP28	VSS						3938.016	6246.876
AP3	GPP_F15 / EMMC_DATA2						19013.678	6781.8
AP30	DDR1_DQ[47] / DDR1_DQ[31]				DDR1_DQ[47]	DDR1_DQ[31]	3023.616	6246.876
AP32	VSS						2109.216	6246.876
AP33	DDR1_DQ[45] / DDR1_DQ[29]				DDR1_DQ[45]	DDR1_DQ[29]	1194.816	6246.876
AP35	VSS						280.416	6246.876
AP37	DDR1_DQ[38] / DDR1_DQ[22]				DDR1_DQ[38]	DDR1_DQ[22]	-633.984	6246.876
AP38	VSS						-1548.384	6246.876
AP4	GPP_F12 / EMMC_CMD						18363.438	6781.8
AP40	DDR1_DQ[37] / DDR1_DQ[21]				DDR1_DQ[37]	DDR1_DQ[21]	-2462.784	6246.876
AP42	VSS						-3377.184	6246.876
AP43	DDR1_PAR						-4291.584	6246.876
AP45	DDR1_CKP[0]						-5205.984	6246.876
AP46	DDR1_CKP[1]						-6120.384	6246.876
AP48	DDR1_MA[7] / DDR1_CAA[4] / DDR1_MA[7]	DDR1_MA[7]	DDR1_CAA[4]	DDR1_MA[7]			-7034.784	6246.876

Table 9-1. U/U-Quad Core Processor Ball List (Sheet 12 of 39)

Ball #	Ball Name	DDR3L	LPDDR3	DDR4	Interleaved (IL)	Non-Interleaved (NIL)	X[um]	Y[um]
AP5	GPP_B21 / GSPI1_MISO						17654.016	6246.876
AP50	DDR1_MA[9] / DDR1_CAA[1] / DDR1_MA[9]	DDR1_MA[9]	DDR1_CAA[1]	DDR1_MA[9]			-7949.184	6246.876
AP52	DDR1_BA[2] / DDR1_CAA[5]/ DDR1_BG[0]	DDR1_BA[2]	DDR1_CAA[5]	DDR1_BG[0]			-8863.584	6246.876
AP53	DDR1_CKE[3]						-9777.984	6246.876
AP55	DDR1_CKE[1]						-10692.384	6246.876
AP56	MSM#						-11606.784	6246.876
AP58	VSS						-12521.184	6246.876
AP60	DDR1_DQ[26] / DDR0_DQ[58]				DDR1_DQ[26]	DDR0_DQ[58]	-13435.584	6246.876
AP61	DDR1_DQ[29] / DDR0_DQ[61]				DDR1_DQ[29]	DDR0_DQ[61]	-14349.984	6246.876
AP63	VSS						-15264.384	6246.876
AP65	DDR1_DQ[18] / DDR0_DQ[50]				DDR1_DQ[18]	DDR0_DQ[50]	-16178.784	6246.876
AP66	DDR1_DQ[21] / DDR0_DQ[53]				DDR1_DQ[21]	DDR0_DQ[53]	-17093.184	6246.876
AP68	VSS						-18038.572	6331.966
AP7	GPP_B16 / GSPI0_CLK						16739.616	6246.876
AP70	VSS						-19257.772	6331.966
AP8	GPP_B17 / GSPI0_MISO						15825.216	6246.876
AR10	GPP_B5 / SRCCLKREQ0#						14910.816	6897.116
AR11	VSS						13996.416	6897.116
AR13	GPP_A13 / SUSWARN# / SUSPWRDNACK						13082.016	6897.116
AR15	VSS						12167.616	6897.116
AR16	VSS						11253.216	6897.116
AR18	DDR_RCOMP[0]						10338.816	6897.116
AR20	VSS						9424.416	6897.116
AR21	DDR1_DQSP[7]						8510.016	6897.116
AR22	DDR1_DQSN[7]						7595.616	6897.116
AR23	VSS						6681.216	6897.116
AR25	DDR1_DQSN[6]						5766.816	6897.116
AR27	DDR1_DQSP[6]						4852.416	6897.116
AR28	VSS						3938.016	6897.116
AR30	DDR1_DQ[46] / DDR1_DQ[30]				DDR1_DQ[46]	DDR1_DQ[30]	3023.616	6897.116
AR32	DDR1_DQSP[5] / DDR1_DQSP[3]				DDR1_DQSP[5]	DDR1_DQSP[3]	2109.216	6897.116
AR33	DDR1_DQ[44] / DDR1_DQ[28]				DDR1_DQ[44]	DDR1_DQ[28]	1194.816	6897.116

Table 9-1. U/U-Quad Core Processor Ball List (Sheet 13 of 39)

Ball #	Ball Name	DDR3L	LPDDR3	DDR4	Interleaved (IL)	Non-Interleaved (NIL)	X[um]	Y[um]
AR35	VSS						280.416	6897.116
AR37	DDR1_DQ[39] / DDR1_DQ[23]				DDR1_DQ[39]	DDR1_DQ[23]	-633.984	6897.116
AR38	DDR1_DQSP[4] / DDR1_DQSP[2]				DDR1_DQSP[4]	DDR1_DQSP[2]	-1548.384	6897.116
AR40	DDR1_DQ[36] / DDR1_DQ[20]				DDR1_DQ[36]	DDR1_DQ[20]	-2462.784	6897.116
AR42	VSS						-3377.184	6897.116
AR43	VSS						-4291.584	6897.116
AR45	VSS						-5205.984	6897.116
AR46	VSS						-6120.384	6897.116
AR48	VSS						-7034.784	6897.116
AR5	VSS						17654.016	6897.116
AR50	VSS						-7949.184	6897.116
AR52	VSS						-8863.584	6897.116
AR53	VSS						-9777.984	6897.116
AR55	VSS						-10692.384	6897.116
AR56	ZVM#						-11606.784	6897.116
AR58	VSS						-12521.184	6897.116
AR60	DDR1_DQSP[3] / DDR0_DQSP[7]				DDR1_DQSP[3]	DDR0_DQSP[7]	-13435.584	6897.116
AR61	DDR1_DQSN[3] / DDR0_DQSN[7]				DDR1_DQSN[3]	DDR0_DQSN[7]	-14349.984	6897.116
AR63	VSS						-15264.384	6897.116
AR65	DDR1_DQSP[2] / DDR0_DQSP[6]				DDR1_DQSP[2]	DDR0_DQSP[6]	-16178.784	6897.116
AR66	DDR1_DQSN[2] / DDR0_DQSN[6]				DDR1_DQSN[2]	DDR0_DQSN[6]	-17093.184	6897.116
AR68	DDR0_DQ[9]						-18363.692	6945.376
AR69	DDR0_DQ[13]						-19013.932	6945.376
AR7	GPP_B18 / GSPI0_MOSI						16739.616	6897.116
AR70	DDR0_DQ[8]						-19664.172	6846.316
AR71	DDR0_DQ[12]						-20314.412	6846.316
AR8	VSS						15825.216	6897.116
AT1	EMMC_RCOMP						19989.038	7444.74
AT10	GPP_B8 / SRCCLKREQ3#						14910.816	7547.356
AT11	GPP_B12 / SLP_S0#						13996.416	7547.356
AT13	DRAM_RESET#						13082.016	7547.356
AT15	GPD7 / RSVD						12167.616	7547.356
AT16	PROC_POPIRCOMP						11253.216	7547.356
AT18	DDR_RCOMP[1]						10338.816	7547.356
AT2	VSS						19338.798	7444.74

Table 9-1. U/U-Quad Core Processor Ball List (Sheet 14 of 39)

Ball #	Ball Name	DDR3L	LPDDR3	DDR4	Interleaved (IL)	Non-Interleaved (NIL)	X[um]	Y[um]
AT20	VSS						9424.416	7547.356
AT21	DDR1_DQ[59]						8510.016	7547.356
AT22	DDR1_DQ[56]						7595.616	7547.356
AT23	VSS						6681.216	7547.356
AT25	DDR1_DQ[50]						5766.816	7547.356
AT27	DDR1_DQ[49]						4852.416	7547.356
AT28	VSS						3938.016	7547.356
AT30	DDR1_DQ[43] / DDR1_DQ[27]				DDR1_DQ[43]	DDR1_DQ[27]	3023.616	7547.356
AT32	DDR1_DQSN[5] / DDR1_DQSN[3]				DDR1_DQSN[5]	DDR1_DQSN[3]	2109.216	7547.356
AT33	DDR1_DQ[40] / DDR1_DQ[24]				DDR1_DQ[40]	DDR1_DQ[24]	1194.816	7547.356
AT35	VSS						280.416	7547.356
AT37	DDR1_DQ[34] / DDR1_DQ[18]				DDR1_DQ[34]	DDR1_DQ[18]	-633.984	7547.356
AT38	DDR1_DQSN[4] / DDR1_DQSN[2]				DDR1_DQSN[4]	DDR1_DQSN[2]	-1548.384	7547.356
AT4	VSS						18363.438	7444.74
AT40	DDR1_DQ[33] / DDR1_DQ[17]				DDR1_DQ[33]	DDR1_DQ[17]	-2462.784	7547.356
AT42	VSS						-3377.184	7547.356
AT43	DDR0_ODT[1]						-4291.584	7547.356
AT45	DDR0_ODT[0]						-5205.984	7547.356
AT46	DDR0_WE#/ DDR0_CAB[2]/ DDR0_MA[14]	DDR0_WE#	DDR0_CAB[2]	DDR0_MA[14]			-6120.384	7547.356
AT48	DDR0_BA[1] / DDR0_CAB[6]/ DDR0_BA[1]	DDR0_BA[1]	DDR0_CAB[6]	DDR0_BA[1]			-7034.784	7547.356
AT5	TP6						17654.016	7547.356
AT50	DDR0_MA[10] / DDR0_CAB[7]/ DDR0_MA[10]	DDR0_MA[10]	DDR0_CAB[7]	DDR0_MA[10]			-7949.184	7547.356
AT52	DDR0_PAR						-8863.584	7547.356
AT53	DDR0_CKP[0]						-9777.984	7547.356
AT55	DDR0_CKP[1]						-10692.384	7547.356
AT56	VSS						-11606.784	7547.356
AT58	VSS						-12521.184	7547.356
AT60	DDR1_DQ[30] / DDR0_DQ[62]				DDR1_DQ[30]	DDR0_DQ[62]	-13435.584	7547.356
AT61	DDR1_DQ[24] / DDR0_DQ[56]				DDR1_DQ[24]	DDR0_DQ[56]	-14349.984	7547.356
AT63	VSS						-15264.384	7547.356
AT65	DDR1_DQ[22] / DDR0_DQ[54]				DDR1_DQ[22]	DDR0_DQ[54]	-16178.784	7547.356

Table 9-1. U/U-Quad Core Processor Ball List (Sheet 15 of 39)

Ball #	Ball Name	DDR3L	LPDDR3	DDR4	Interleaved (IL)	Non-Interleaved (NIL)	X[um]	Y[um]
AT66	DDR1_DQ[16] / DDR0_DQ[48]				DDR1_DQ[16]	DDR0_DQ[48]	-17093.184	7547.356
AT68	VSS						-18038.572	7509.256
AT69	DDR0_DQSN[1]						-18688.812	7509.256
AT7	GPP_B6 / SRCCLKREQ1#						16739.616	7547.356
AT70	DDR0_DQSP[1]						-19339.052	7509.256
AT71	VSS						-19989.292	7509.256
AT8	GPP_B7 / SRCCLKREQ2#						15825.216	7547.356
AU1	SPI0_CS2#						20314.158	8107.68
AU10	VSS						14910.816	8197.596
AU11	GPP_A11 /PME#						13996.416	8197.596
AU13	GPD0 / BATLOW#						13082.016	8197.596
AU15	VSS						12167.616	8197.596
AU16	PCH_OPIRCOMP						11253.216	8197.596
AU18	DDR_RCOMP[2]						10338.816	8197.596
AU2	SPI0_CS1#						19663.918	8107.68
AU20	VSS						9424.416	8197.596
AU21	DDR1_DQ[58]						8510.016	8197.596
AU22	DDR1_DQ[57]						7595.616	8197.596
AU23	VDDQ						6681.216	8197.596
AU25	DDR1_DQ[51]						5766.816	8197.596
AU27	DDR1_DQ[48]						4852.416	8197.596
AU28	VDDQ						3938.016	8197.596
AU3	SPI0_CS0#						19013.678	8107.68
AU30	DDR1_DQ[42] / DDR1_DQ[26]				DDR1_DQ[42]	DDR1_DQ[26]	3023.616	8197.596
AU32	VSS						2109.216	8197.596
AU33	DDR1_DQ[41] / DDR1_DQ[25]				DDR1_DQ[41]	DDR1_DQ[25]	1194.816	8197.596
AU35	VDDQ						280.416	8197.596
AU37	DDR1_DQ[35] / DDR1_DQ[19]				DDR1_DQ[35]	DDR1_DQ[19]	-633.984	8197.596
AU38	VSS						-1548.384	8197.596
AU4	SPI0_IO3						18363.438	8107.68
AU40	DDR1_DQ[32] / DDR1_DQ[16]				DDR1_DQ[32]	DDR1_DQ[16]	-2462.784	8197.596
AU42	VDDQ						-3377.184	8197.596
AU43	DDR0_CS#[1]						-4291.584	8197.596
AU45	DDR0_CS#[0]						-5205.984	8197.596

Table 9-1. U/U-Quad Core Processor Ball List (Sheet 16 of 39)

Ball #	Ball Name	DDR3L	LPDDR3	DDR4	Interleaved (IL)	Non-Interleaved (NIL)	X[um]	Y[um]
AU46	DDR0_MA[13] / DDR0_CAB[0] / DDR0_MA[13]	DDR0_MA[13]	DDR0_CAB[0]	DDR0_MA[13]			-6120.384	8197.596
AU48	DDR0_CAS#/ DDR0_CAB[1]/ DDR0_MA[15]	DDR0_CAS#	DDR0_CAB[1]	DDR0_MA[15]			-7034.784	8197.596
AU5	TP5						17654.016	8197.596
AU50	DDR0_RAS# / DDR0_CAB[3]/ DDR0_MA[16]	DDR0_RAS#	DDR0_CAB[3]	DDR0_MA[16]			-7949.184	8197.596
AU52	DDR0_BA[0] / DDR0_CAB[4]/ DDR0_BA[0]	DDR0_BA[0]	DDR0_CAB[4]	DDR0_BA[0]			-8863.584	8197.596
AU53	DDR0_CKN[0]						-9777.984	8197.596
AU55	DDR0_CKN[1]						-10692.384	8197.596
AU56	RSVD						-11606.784	8197.596
AU58	VccGTx						-12521.184	8197.596
AU60	DDR1_DQ[31] / DDR0_DQ[63]				DDR1_DQ[31]	DDR0_DQ[63]	-13435.584	8197.596
AU61	DDR1_DQ[25] / DDR0_DQ[57]				DDR1_DQ[25]	DDR0_DQ[57]	-14349.984	8197.596
AU63	VccGTx						-15264.384	8197.596
AU65	DDR1_DQ[23] / DDR0_DQ[55]				DDR1_DQ[23]	DDR0_DQ[55]	-16178.784	8197.596
AU66	DDR1_DQ[17] / DDR0_DQ[49]				DDR1_DQ[17]	DDR0_DQ[49]	-17093.184	8197.596
AU68	DDR0_DQ[11]						-18363.692	8146.796
AU69	DDR0_DQ[15]						-19013.932	8172.196
AU7	GPP_B10 / SRCCLKREQ5#						16739.616	8197.596
AU70	DDR0_DQ[14]						-19664.172	8172.196
AU71	DDR0_DQ[10]						-20314.412	8172.196
AU8	GPP_B9 / SRCCLKREQ4#						15825.216	8197.596
AV1	VSS						20314.158	8827.516
AV2	SPI0_CLK						19364.198	8798.56
AV3	SPI0_MOSI						18688.558	8798.56
AV68	VSS						-18028.92	8711.438
AV69	VSS						-19013.932	8901.176
AV70	VSS						-19664.172	8901.176
AV71	VSS						-20314.412	8901.176
AW1	RSVD						20314.158	9551.416
AW10	VSS						14752.828	9038.336
AW11	GPP_A8 / CLKRUN#						14143.228	9363.456
AW12	VSS						13565.124	9038.336
AW13	GPP_A0 / RCIN#						12995.148	9363.456

Table 9-1. U/U-Quad Core Processor Ball List (Sheet 17 of 39)

Ball #	Ball Name	DDR3L	LPDDR3	DDR4	Interleaved (IL)	Non-Interleaved (NIL)	X[um]	Y[um]
AW14	VSS						12332.208	9038.336
AW15	SLP_LAN#						11722.608	9363.456
AW16	VSS						11144.504	9038.336
AW17	GPD11 / LANPHYPC						10574.528	9363.456
AW18	VSS						9911.588	9038.336
AW2	SPI0_IO2						19689.318	9362.44
AW20	I2S1_TXD						9301.988	9363.456
AW21	VSS						8723.884	9038.336
AW22	HDA_RST# / I2S1_SCLK						8153.908	9363.456
AW23	VSS						7465.568	9038.336
AW25	DDR0_DQ[59] / DDR1_DQ[43]				DDR0_DQ[59]	DDR1_DQ[43]	6828.028	9363.456
AW26	VSS						6264.148	9038.336
AW27	DDR0_DQ[57] / DDR1_DQ[41]				DDR0_DQ[57]	DDR1_DQ[41]	5601.208	9363.456
AW28	VSS						4987.798	9038.336
AW29	DDR0_DQ[51] / DDR1_DQ[35]				DDR0_DQ[51]	DDR1_DQ[35]	4374.388	9363.456
AW3	SPI0_MISO						19039.078	9362.44
AW30	VSS						3711.448	9038.336
AW31	DDR0_DQ[49] / DDR1_DQ[33]				DDR0_DQ[49]	DDR1_DQ[33]	3147.568	9363.456
AW32	VSS						2484.628	9038.336
AW33	DDR0_DQ[43] / DDR1_DQ[11]				DDR0_DQ[43]	DDR1_DQ[11]	1847.088	9363.456
AW34	VSS						1283.208	9038.336
AW35	DDR0_DQ[41] / DDR1_DQ[9]				DDR0_DQ[41]	DDR1_DQ[9]	620.268	9363.456
AW36	VSS						6.858	9038.336
AW37	DDR0_DQ[35] / DDR1_DQ[3]				DDR0_DQ[35]	DDR1_DQ[3]	-606.552	9363.456
AW38	VSS						-1269.492	9038.336
AW39	DDR0_DQ[33] / DDR1_DQ[1]				DDR0_DQ[33]	DDR1_DQ[1]	-1833.372	9363.456
AW41	VSS						-2470.912	9038.336
AW42	DDR1_ODT[1]						-3108.452	9363.456
AW43	VSS						-3672.332	9038.336
AW44	DDR1_RAS# / DDR1_CAB[3]/ DDR1_MA[16]	DDR1_RAS#	DDR1_CAB[3]	DDR1_MA[16]			-4335.272	9363.456
AW45	VSS						-4948.682	9038.336
AW46	DDR1_MA[10] / DDR1_CAB[7]/ DDR1_MA[10]	DDR1_MA[10]	DDR1_CAB[7]	DDR1_MA[10]			-5562.092	9363.456
AW47	VSS						-6162.802	9038.336

Table 9-1. U/U-Quad Core Processor Ball List (Sheet 18 of 39)

Ball #	Ball Name	DDR3L	LPDDR3	DDR4	Interleaved (IL)	Non-Interleaved (NIL)	X[um]	Y[um]
AW48	RSVD						-6726.682	9363.456
AW49	VSS						-7355.332	9038.336
AW5	GPP_B14 / SPKR						17780.508	8911.336
AW50	DDR0_ALERT#						-7983.982	9363.456
AW51	VSS						-8547.862	9038.336
AW52	DDR0_MA[7] / DDR0_CAA[4] / DDR0_MA[7]	DDR0_MA[7]	DDR0_CAA[4]	DDR0_MA[7]			-9148.572	9363.456
AW53	VSS						-9761.982	9038.336
AW54	DDR0_MA[12] / DDR0_CAA[6] / DDR0_MA[12]	DDR0_MA[12]	DDR0_CAA[6]	DDR0_MA[12]			-10375.392	9363.456
AW55	VSS						-11038.332	9038.336
AW56	DDR0_CKE[2]						-11602.212	9363.456
AW57	VSS						-12239.752	9038.336
AW59	DDR0_DQ[27] / DDR0_DQ[43]				DDR0_DQ[27]	DDR0_DQ[43]	-12877.292	9363.456
AW6	VSS						17130.268	9038.336
AW60	VSS						-13441.172	9038.336
AW61	DDR0_DQ[25] / DDR0_DQ[41]				DDR0_DQ[25]	DDR0_DQ[41]	-14104.112	9363.456
AW62	VSS						-14717.522	9038.336
AW63	DDR0_DQ[18] / DDR0_DQ[34]				DDR0_DQ[18]	DDR0_DQ[34]	-15330.932	9363.456
AW64	VSS						-15993.872	9038.336
AW65	DDR0_DQ[17] / DDR0_DQ[33]				DDR0_DQ[17]	DDR0_DQ[33]	-16557.752	9363.456
AW66	VSS						-17093.184	8900.414
AW67	DDR_VTT_CNTL						-18017.744	9370.568
AW68	RSVD						-18621.756	9622.028
AW69	RSVD						-19266.916	9535.668
AW7	GPP_A23 / ISH_GP5						16563.848	9363.456
AW70	RSVD_TP						-19684.746	10034.778
AW71	RSVD_TP						-20314.412	9551.416
AW8	VSS						15985.744	9038.336
AW9	GPP_A9 / CLKOUT_LPC0 / ESPI_CLK						15415.768	9363.456
AY1	RSVD						20314.158	10201.656
AY11	GPP_A6 / SERIRQ						14130.528	10013.696
AY12	GPP_A4 / LAD3 / ESPI_IO3						13565.124	9688.576
AY13	GPP_A1 / LAD0 / ESPI_IO0						12995.148	10013.696
AY15	GPD1 / ACPRESENT						11709.908	10013.696

Table 9-1. U/U-Quad Core Processor Ball List (Sheet 19 of 39)

Ball #	Ball Name	DDR3L	LPDDR3	DDR4	Interleaved (IL)	Non-Interleaved (NIL)	X[um]	Y[um]
AY16	GPD10 / SLP_S5#						11144.504	9688.576
AY17	RSMRST#						10574.528	10013.696
AY2	RSVD						19685	10034.27
AY20	I2S1_SFRM						9289.288	10013.696
AY21	HDA_SDI1 / I2S1_RXD						8723.884	9688.576
AY22	HDA_BLK / I2S0_SCLK						8153.908	10013.696
AY25	DDR0_DQ[58] / DDR1_DQ[42]				DDR0_DQ[58]	DDR1_DQ[42]	6828.028	10013.696
AY26	DDR0_DQSN[7] / DDR1_DQSN[5]				DDR0_DQSN[7]	DDR1_DQSN[5]	6264.148	9688.576
AY27	DDR0_DQ[56] / DDR1_DQ[40]				DDR0_DQ[56]	DDR1_DQ[40]	5601.208	10013.696
AY29	DDR0_DQ[50] / DDR1_DQ[34]				DDR0_DQ[50]	DDR1_DQ[34]	4374.388	10013.696
AY3	RSVD						19028.41	10027.92
AY30	DDR0_DQSP[6] / DDR1_DQSP[4]				DDR0_DQSP[6]	DDR1_DQSP[4]	3711.448	9688.576
AY31	DDR0_DQ[48] / DDR1_DQ[32]				DDR0_DQ[48]	DDR1_DQ[32]	3147.568	10013.696
AY33	DDR0_DQ[42] / DDR1_DQ[10]				DDR0_DQ[42]	DDR1_DQ[10]	1847.088	10013.696
AY34	DDR0_DQSN[5] / DDR1_DQSN[1]				DDR0_DQSN[5]	DDR1_DQSN[1]	1283.208	9688.576
AY35	DDR0_DQ[40] / DDR1_DQ[8]				DDR0_DQ[40]	DDR1_DQ[8]	620.268	10013.696
AY37	DDR0_DQ[34] / DDR1_DQ[2]				DDR0_DQ[34]	DDR1_DQ[2]	-606.552	10013.696
AY38	DDR0_DQSP[4] / DDR1_DQSP[0]				DDR0_DQSP[4]	DDR1_DQSP[0]	-1269.492	9688.576
AY39	DDR0_DQ[32] / DDR1_DQ[0]				DDR0_DQ[32]	DDR1_DQ[0]	-1833.372	10013.696
AY4	TP1						18274.284	10043.16
AY42	DDR1_CS#[1]						-3108.452	10013.696
AY43	DDR1_CAS#/ DDR1_CAB[1]/ DDR1_MA[15]	DDR1_CAS#	DDR1_CAB[1]	DDR1_MA[15]			-3672.332	9688.576
AY44	DDR1_WE#/ DDR1_CAB[2]/ DDR1_MA[14]	DDR1_WE#	DDR1_CAB[2]	DDR1_MA[14]			-4335.272	10013.696
AY46	DDR1_MA[1] / DDR1_CAB[8]/ DDR1_MA[1]	DDR1_MA[1]	DDR1_CAB[8]	DDR1_MA[1]			-5562.092	10013.696
AY47	DDR1_MA[2] / DDR1_CAB[5]/ DDR1_MA[2]	DDR1_MA[2]	DDR1_CAB[5]	DDR1_MA[2]			-6162.802	9688.576
AY48	DDR1_MA[5] / DDR1_CAA[0] / DDR1_MA[5]	DDR1_MA[5]	DDR1_CAA[0]	DDR1_MA[5]			-6788.912	10013.696
AY5	GPP_B4 / CPU_GP3						17664.684	9688.576

Table 9-1. U/U-Quad Core Processor Ball List (Sheet 20 of 39)

Ball #	Ball Name	DDR3L	LPDDR3	DDR4	Interleaved (IL)	Non-Interleaved (NIL)	X[um]	Y[um]
AY50	DDR0_MA[0] / DDR0_CAB[9]/ DDR0_MA[0]	DDR0_MA[0]	DDR0_CAB[9]	DDR0_MA[0]			-7921.752	10013.696
AY51	DDR0_MA[2] / DDR0_CAB[5]/ DDR0_MA[2]	DDR0_MA[2]	DDR0_CAB[5]	DDR0_MA[2]			-8547.862	9688.576
AY52	DDR0_MA[8] / DDR0_CAA[3] / DDR0_MA[8]	DDR0_MA[8]	DDR0_CAA[3]	DDR0_MA[8]			-9148.572	10013.696
AY54	DDR0_MA[14] / DDR0_CAA[9]/ DDR0_BG[1]	DDR0_MA[14]	DDR0_CAA[9]	DDR0_BG[1]			-10375.392	10013.696
AY55	DDR0_BA[2] / DDR0_CAA[5]/ DDR0_BG[0]	DDR0_BA[2]	DDR0_CAA[5]	DDR0_BG[0]			-11038.332	9688.576
AY56	DDR0_CKE[3]						-11602.212	10013.696
AY59	DDR0_DQ[31] / DDR0_DQ[47]				DDR0_DQ[31]	DDR0_DQ[47]	-12877.292	10013.696
AY60	DDR0_DQSN[3] / DDR0_DQSN[5]				DDR0_DQSN[3]	DDR0_DQSN[5]	-13441.172	9688.576
AY61	DDR0_DQ[29] / DDR0_DQ[45]				DDR0_DQ[29]	DDR0_DQ[45]	-14104.112	10013.696
AY63	DDR0_DQ[19] / DDR0_DQ[35]				DDR0_DQ[19]	DDR0_DQ[35]	-15330.932	10013.696
AY64	DDR0_DQSP[2] / DDR0_DQSP[4]				DDR0_DQSP[2]	DDR0_DQSP[4]	-15993.872	9688.576
AY65	DDR0_DQ[21] / DDR0_DQ[37]				DDR0_DQ[21]	DDR0_DQ[37]	-16557.752	10013.696
AY66	VSS						-17220.692	9688.576
AY67	DDR_VREF_CA						-17901.412	10013.696
AY68	DDR0_VREF_DQ						-18535.396	10267.188
AY7	GPP_A22 / ISH_GP4						16551.148	10013.696
AY71	VSS						-20314.412	10201.656
AY8	GPP_A18 / ISH_GP0						15985.744	9688.576
AY9	GPP_A10 / CLKOUT_LPC1						15415.768	10013.696
B10	VSS						14988.794	-10338.816
B11	RSVD						14313.154	-10663.936
B13	USB3_2_TXN / SSIC_TXN						13186.41	-10663.936
B14	VSS						12510.77	-10338.816
B15	USB3_3_TXN						11835.13	-10663.936
B17	PCIE1_TXN / USB3_5_TXN						10708.386	-10663.936
B18	VSS						10032.746	-10338.816
B19	PCIE4_TXN						9357.106	-10663.936
B2	RSVD						19831.558	-10831.576
B21	PCIE7_TXN / SATA0_TXN						8230.362	-10663.936

Table 9-1. U/U-Quad Core Processor Ball List (Sheet 21 of 39)

Ball #	Ball Name	DDR3L	LPDDR3	DDR4	Interleaved (IL)	Non-Interleaved (NIL)	X[um]	Y[um]
B22	VSS						7554.722	-10338.816
B23	PCIE9_TXN						6879.082	-10663.936
B25	PCIE12_TXP / SATA2_TXP						5752.338	-10663.936
B26	CSI2_CLKN3						5076.698	-10338.816
B27	CSI2_DP10						4401.058	-10663.936
B29	CSI2_DP8						3274.314	-10663.936
B3	RSVD						19196.558	-10679.176
B30	VSS						2598.674	-10338.816
B31	CSI2_DP6						1923.034	-10663.936
B33	CSI2_DP7						796.29	-10663.936
B34	VSS						120.65	-10338.816
B36	CSI2_DP0						-554.99	-10663.936
B38	CSI2_DP3						-1681.734	-10663.936
B39	VSS						-2357.374	-10338.816
B40	CLKOUT_PCIE_N4						-3033.014	-10663.936
B42	CLKOUT_PCIE_N1						-4159.758	-10663.936
B44	VSS						-4835.398	-10338.816
B45	EDP_TXP[2]						-5511.038	-10663.936
B47	EDP_TXP[3]						-6637.782	-10663.936
B48	VSS						-7313.422	-10338.816
B5	SYS_RESET#						18048.478	-10663.936
B50	DDI2_TXP[2]						-7989.062	-10663.936
B52	EDP_DISP_UTIL						-9115.806	-10663.936
B53	VSS						-9791.446	-10338.816
B54	BPM#[2]						-10467.086	-10663.936
B56	PCH_JTAG_TCK						-11593.83	-10663.936
B58	VSS						-12269.47	-10338.816
B59	PROC_TRST#						-12945.11	-10663.936
B6	SYS_PWROK						17466.818	-10338.816
B61	PROC_TCK						-14071.854	-10663.936
B62	VSS						-14747.494	-10338.816
B63	VIDALERT#						-15423.134	-10663.936
B65	VCCST_PWRGD						-16549.878	-10663.936
B66	VSS						-17225.518	-10338.816
B67	CFG[1]						-17901.158	-10663.936
B69	RSVD						-19035.014	-10684.51
B7	GPP_D4 / FLASHTRIG						16791.178	-10663.936
B70	RSVD						-19685.254	-10684.51

Table 9-1. U/U-Quad Core Processor Ball List (Sheet 22 of 39)

Ball #	Ball Name	DDR3L	LPDDR3	DDR4	Interleaved (IL)	Non-Interleaved (NIL)	X[um]	Y[um]
B71	VSS						-20314.412	-10851.896
B9	GPP_E12 / USB2_OC3#						15664.434	-10663.936
BA1	VSS						20314.158	10851.896
BA10	VSS						14752.828	10257.536
BA11	GPP_A14 / SUS_STAT#/ ESPI_RESET#						14188.948	10663.936
BA12	GPP_A5 / LFRAME# / ESPI_CS#						13565.124	10338.816
BA13	GPP_A2 / LAD1 / ESPI_IO1						12995.148	10663.936
BA14	VSS						12332.208	10257.536
BA15	GPD3 / PWRBTN#						11768.328	10663.936
BA16	GPD5 / SLP_S4#						11144.504	10338.816
BA17	GPD8 / SUSCLK						10574.528	10663.936
BA18	VSS						9911.588	10257.536
BA2	VSS						19685	10684.51
BA20	PCH_PWROK						9347.708	10663.936
BA21	HDA_SDI0/ I2S0_RXD						8723.884	10338.816
BA22	HDA_SYNC / I2S0_SFRM						8153.908	10663.936
BA23	VSS						7465.568	10257.536
BA25	DDR0_DQ[62] / DDR1_DQ[46]				DDR0_DQ[62]	DDR1_DQ[46]	6828.028	10663.936
BA26	DDR0_DQSP[7] / DDR1_DQSP[5]				DDR0_DQSP[7]	DDR1_DQSP[5]	6165.088	10338.816
BA27	DDR0_DQ[61] / DDR1_DQ[45]				DDR0_DQ[61]	DDR1_DQ[45]	5502.148	10663.936
BA28	VSS						4987.798	10257.536
BA29	DDR0_DQ[54] / DDR1_DQ[38]				DDR0_DQ[54]	DDR1_DQ[38]	4473.448	10663.936
BA3	RSVD						19034.76	10684.51
BA30	DDR0_DQSN[6] / DDR1_DQSN[4]				DDR0_DQSN[6]	DDR1_DQSN[4]	3810.508	10338.816
BA31	DDR0_DQ[53] / DDR1_DQ[37]				DDR0_DQ[53]	DDR1_DQ[37]	3147.568	10663.936
BA32	VSS						2484.628	10257.536
BA33	DDR0_DQ[46] / DDR1_DQ[14]				DDR0_DQ[46]	DDR1_DQ[14]	1847.088	10663.936
BA34	DDR0_DQSP[5] / DDR1_DQSP[1]				DDR0_DQSP[5]	DDR1_DQSP[1]	1184.148	10338.816
BA35	DDR0_DQ[45] / DDR1_DQ[13]				DDR0_DQ[45]	DDR1_DQ[13]	521.208	10663.936
BA36	VSS						6.858	10257.536
BA37	DDR0_DQ[38] / DDR1_DQ[6]				DDR0_DQ[38]	DDR1_DQ[6]	-507.492	10663.936
BA38	DDR0_DQSN[4] / DDR1_DQSN[0]				DDR0_DQSN[4]	DDR1_DQSN[0]	-1170.432	10338.816

Table 9-1. U/U-Quad Core Processor Ball List (Sheet 23 of 39)

Ball #	Ball Name	DDR3L	LPDDR3	DDR4	Interleaved (IL)	Non-Interleaved (NIL)	X[um]	Y[um]
BA39	DDR0_DQ[37] / DDR1_DQ[5]				DDR0_DQ[37]	DDR1_DQ[5]	-1833.372	10663.936
BA4	RSVD						18365.724	10689.336
BA41	VSS						-2470.912	10257.536
BA42	DDR1_ODT[0]						-3108.452	10663.936
BA43	DDR1_MA[13] / DDR1_CAB[0] / DDR1_MA[13]	DDR1_MA[13]	DDR1_CAB[0]	DDR1_MA[13]			-3771.392	10338.816
BA44	DDR1_BA[1] / DDR1_CAB[6]/ DDR1_BA[1]	DDR1_BA[1]	DDR1_CAB[6]	DDR1_BA[1]			-4434.332	10663.936
BA45	VSS						-4948.682	10257.536
BA46	DDR1_MA[0] / DDR1_CAB[9]/ DDR1_MA[0]	DDR1_MA[0]	DDR1_CAB[9]	DDR1_MA[0]			-5463.032	10663.936
BA47	DDR1_MA[4]						-6125.972	10338.816
BA48	DDR1_MA[6] / DDR1_CAA[2] / DDR1_MA[6]	DDR1_MA[6]	DDR1_CAA[2]	DDR1_MA[6]			-6788.912	10663.936
BA49	VSS						-7355.332	10338.816
BA5	GPP_B3 / CPU_GP2						17715.484	10625.836
BA50	DDR0_MA[3]						-7921.752	10663.936
BA51	DDR0_MA[5] / DDR0_CAA[0] / DDR0_MA[5]	DDR0_MA[5]	DDR0_CAA[0]	DDR0_MA[5]			-8584.692	10338.816
BA52	DDR0_MA[6] / DDR0_CAA[2] / DDR0_MA[6]	DDR0_MA[6]	DDR0_CAA[2]	DDR0_MA[6]			-9247.632	10663.936
BA53	VSS						-9761.982	10257.536
BA54	DDR0_MA[11] / DDR0_CAA[7] / DDR0_MA[11]	DDR0_MA[11]	DDR0_CAA[7]	DDR0_MA[11]			-10276.332	10663.936
BA55	DDR0_MA[15] / DDR0_CAA[8]/ DDR0_ACT#	DDR0_MA[15]	DDR0_CAA[8]	DDR0_ACT#			-10939.272	10338.816
BA56	DDR0_CKE[0]						-11602.212	10663.936
BA57	VSS						-12239.752	10257.536
BA59	DDR0_DQ[30] / DDR0_DQ[46]				DDR0_DQ[30]	DDR0_DQ[46]	-12877.292	10663.936
BA6	VSS						17173.448	10257.536
BA60	DDR0_DQSP[3] / DDR0_DQSP[5]				DDR0_DQSP[3]	DDR0_DQSP[5]	-13540.232	10338.816
BA61	DDR0_DQ[24] / DDR0_DQ[40]				DDR0_DQ[24]	DDR0_DQ[40]	-14203.172	10663.936
BA62	VSS						-14717.522	10257.536
BA63	DDR0_DQ[22] / DDR0_DQ[38]				DDR0_DQ[22]	DDR0_DQ[38]	-15231.872	10663.936
BA64	DDR0_DQSN[2] / DDR0_DQSN[4]				DDR0_DQSN[2]	DDR0_DQSN[4]	-15894.812	10338.816

Table 9-1. U/U-Quad Core Processor Ball List (Sheet 24 of 39)

Ball #	Ball Name	DDR3L	LPDDR3	DDR4	Interleaved (IL)	Non-Interleaved (NIL)	X[um]	Y[um]
BA65	DDR0_DQ[20] / DDR0_DQ[36]				DDR0_DQ[20]	DDR0_DQ[36]	-16557.752	10663.936
BA66	VSS						-17220.692	10338.816
BA67	DDR1_VREF_DQ						-17901.412	10663.936
BA68	RSVD_TP						-19034.506	10685.018
BA7	GPP_A21 / ISH_GP3						16609.568	10663.936
BA70	RSVD_TP						-19684.746	10685.018
BA71	VSS						-20314.412	10851.896
BA8	GPP_A19 / ISH_GP1						15985.744	10338.816
BA9	GPP_A17 / SD_PWR_EN# / ISH_GP7						15415.768	10663.936
BB10	DCPRTC						14752.828	10989.056
BB11	GPP_A7 / PIRQA#						14188.948	11314.176
BB13	GPP_A3 / LAD2 / ESPI_IO2						12995.148	11314.176
BB14	VCCRTC						12332.208	10989.056
BB15	WAKE#						11768.328	11314.176
BB17	GPD9 / SLP_WLAN#						10574.528	11314.176
BB18	VSS						9911.588	10989.056
BB2	RSVD						19851.878	11314.176
BB20	DSW_PWROK						9347.708	11314.176
BB22	HDA_SDO / I2S0_TXD						8153.908	11314.176
BB23	VDDQ						7465.568	10907.776
BB25	DDR0_DQ[63] / DDR1_DQ[47]				DDR0_DQ[63]	DDR1_DQ[47]	6828.028	11314.176
BB26	VSS						6165.088	10989.056
BB27	DDR0_DQ[60] / DDR1_DQ[44]				DDR0_DQ[60]	DDR1_DQ[44]	5502.148	11314.176
BB29	DDR0_DQ[55] / DDR1_DQ[39]				DDR0_DQ[55]	DDR1_DQ[39]	4473.448	11314.176
BB3	TP2						19201.638	11314.176
BB30	VSS						3810.508	10989.056
BB31	DDR0_DQ[52] / DDR1_DQ[36]				DDR0_DQ[52]	DDR1_DQ[36]	3147.568	11314.176
BB32	VDDQ						2484.628	10907.776
BB33	DDR0_DQ[47] / DDR1_DQ[15]				DDR0_DQ[47]	DDR1_DQ[15]	1847.088	11314.176
BB34	VSS						1184.148	10989.056
BB35	DDR0_DQ[44] / DDR1_DQ[12]				DDR0_DQ[44]	DDR1_DQ[12]	521.208	11314.176
BB37	DDR0_DQ[39] / DDR1_DQ[7]				DDR0_DQ[39]	DDR1_DQ[7]	-507.492	11314.176
BB38	VSS						-1170.432	10989.056

Table 9-1. U/U-Quad Core Processor Ball List (Sheet 25 of 39)

Ball #	Ball Name	DDR3L	LPDDR3	DDR4	Interleaved (IL)	Non-Interleaved (NIL)	X[um]	Y[um]
BB39	DDR0_DQ[36] / DDR1_DQ[4]				DDR0_DQ[36]	DDR1_DQ[4]	-1833.372	11314.176
BB4	RSVD						18551.398	11314.176
BB41	VDDQ						-2470.912	10907.776
BB42	DDR1_CS#[0]						-3108.452	11314.176
BB43	VSS						-3771.392	10989.056
BB44	DDR1_BA[0] / DDR1_CAB[4]/ DDR1_BA[0]	DDR1_BA[0]	DDR1_CAB[4]	DDR1_BA[0]			-4434.332	11314.176
BB46	DDR1_MA[3]						-5463.032	11314.176
BB47	VDDQ						-6125.972	10989.056
BB48	DDR1_MA[8] / DDR1_CAA[3] / DDR1_MA[8]	DDR1_MA[8]	DDR1_CAA[3]	DDR1_MA[8]			-6788.912	11314.176
BB5	TP4						17785.588	11314.176
BB50	DDR0_MA[1] / DDR0_CAB[8]/ DDR0_MA[1]	DDR0_MA[1]	DDR0_CAB[8]	DDR0_MA[1]			-7921.752	11314.176
BB51	VDDQ						-8584.692	10989.056
BB52	DDR0_MA[4]						-9247.632	11314.176
BB54	DDR0_MA[9] / DDR0_CAA[1] / DDR0_MA[9]	DDR0_MA[9]	DDR0_CAA[1]	DDR0_MA[9]			-10276.332	11314.176
BB55	VSS						-10939.272	10989.056
BB56	DDR0_CKE[1]						-11602.212	11314.176
BB57	VccGTx						-12239.752	10907.776
BB59	DDR0_DQ[26] / DDR0_DQ[42]				DDR0_DQ[26]	DDR0_DQ[42]	-12877.292	11314.176
BB6	VSS						17173.448	10989.056
BB60	VSS						-13540.232	10989.056
BB61	DDR0_DQ[28] / DDR0_DQ[44]				DDR0_DQ[28]	DDR0_DQ[44]	-14203.172	11314.176
BB63	DDR0_DQ[23] / DDR0_DQ[39]				DDR0_DQ[23]	DDR0_DQ[39]	-15231.872	11314.176
BB64	VSS						-15894.812	10989.056
BB65	DDR0_DQ[16] / DDR0_DQ[32]				DDR0_DQ[16]	DDR0_DQ[32]	-16557.752	11314.176
BB66	VccGTx						-17220.692	10989.056
BB67	VSS						-17901.412	11314.176
BB68	RSVD_TP						-18551.652	11314.176
BB69	RSVD_TP						-19201.892	11314.176
BB7	GPP_A20 / ISH_GP2						16609.568	11314.176
BB70	VSS						-19852.132	11314.176
BB9	GPP_A16 / SD_1P8_SEL						15415.768	11314.176
C1	VSS						20314.158	-10348.976

Table 9-1. U/U-Quad Core Processor Ball List (Sheet 26 of 39)

Ball #	Ball Name	DDR3L	LPDDR3	DDR4	Interleaved (IL)	Non-Interleaved (NIL)	X[um]	Y[um]
C11	RSVD						14313.154	-10013.696
C12	RSVD						13749.782	-10338.816
C13	USB3_1_TXN						13186.41	-10013.696
C15	USB3_4_TXN						11835.13	-10013.696
C16	PCIE2_TXP / USB3_6_TXP						11271.758	-10338.816
C17	PCIE3_TXP						10708.386	-10013.696
C19	PCIE5_TXN						9357.106	-10013.696
C2	RSVD						19679.158	-10196.576
C20	PCIE6_TXP						8793.734	-10338.816
C21	PCIE8_TXP / SATA1A_TXP						8230.362	-10013.696
C23	PCIE10_TXP						6879.082	-10013.696
C24	PCIE11_TXP / SATA1B_TXP						6315.71	-10338.816
C25	VSS						5752.338	-10013.696
C27	CSI2_DN11						4401.058	-10013.696
C28	CSI2_DN9						3837.686	-10338.816
C29	CSI2_CLKN2						3274.314	-10013.696
C31	CSI2_DN4						1923.034	-10013.696
C32	CSI2_CLKN1						1359.662	-10338.816
C33	CSI2_DN5						796.29	-10013.696
C36	CSI2_DN2						-554.99	-10013.696
C37	CSI2_CLKN0						-1118.362	-10338.816
C38	CSI2_DN1						-1681.734	-10013.696
C4	RSVD						18614.898	-10336.276
C40	CLKOUT_PCIE_P3						-3033.014	-10013.696
C41	CLKOUT_PCIE_P2						-3596.386	-10338.816
C42	CLKOUT_PCIE_P0						-4159.758	-10013.696
C45	EDP_TXP[1]						-5511.038	-10013.696
C46	EDP_TXP[0]						-6074.41	-10338.816
C47	EDP_TXN[0]						-6637.782	-10013.696
C5	VSS						18048.478	-10013.696
C50	DDI2_TXN[0]						-7989.062	-10013.696
C51	DDI2_TXP[3]						-8552.434	-10338.816
C52	DDI2_TXN[1]						-9115.806	-10013.696
C54	RSVD						-10467.086	-10013.696
C55	BPM#[0]						-11030.458	-10338.816
C56	BPM#[3]						-11593.83	-10013.696
C59	PCH_JTAG_TMS						-12945.11	-10013.696

Table 9-1. U/U-Quad Core Processor Ball List (Sheet 27 of 39)

Ball #	Ball Name	DDR3L	LPDDR3	DDR4	Interleaved (IL)	Non-Interleaved (NIL)	X[um]	Y[um]
C60	PROC_TMS						-13508.482	-10338.816
C61	PCH_TRST#						-14071.854	-10013.696
C63	THERMTRIP#						-15423.134	-10013.696
C64	PROC_SELECT#						-15986.506	-10338.816
C65	PROCHOT#						-16549.878	-10013.696
C67	CFG[7]						-18485.104	-10299.446
C68	CFG[5]						-18622.264	-9621.52
C7	RSVD						16791.178	-10013.696
C70	RSVD						-19685.254	-10034.27
C71	RSVD						-20314.412	-10201.656
C8	GPP_D18 / DMIC_DATA1						16227.806	-10338.816
C9	GPP_E10 / USB2_OC1#						15664.434	-10013.696
D1	RSVD						20314.158	-9698.736
D10	VSS						14988.794	-9322.816
D11	VSS						14313.154	-9363.456
D12	RSVD						13749.782	-9688.576
D13	USB3_1_TXP						13186.41	-9363.456
D14	VSS						12510.77	-9322.816
D15	USB3_4_TXP						11835.13	-9363.456
D16	PCIE2_TXN / USB3_6_TXN						11271.758	-9688.576
D17	PCIE3_TXN						10708.386	-9363.456
D18	VSS						10032.746	-9322.816
D19	PCIE5_TXP						9357.106	-9363.456
D20	PCIE6_TXN						8793.734	-9688.576
D21	PCIE8_TXN / SATA1A_TXN						8230.362	-9363.456
D22	VSS						7554.722	-9322.816
D23	PCIE10_TXN						6879.082	-9363.456
D24	PCIE11_TXN / SATA1B_TXN						6315.71	-9688.576
D25	VSS						5752.338	-9363.456
D26	VSS						5076.698	-9322.816
D27	CSI2_DP11						4401.058	-9363.456
D28	CSI2_DP9						3837.686	-9688.576
D29	CSI2_CLKP2						3274.314	-9363.456
D3	RSVD						19338.798	-9608.312
D30	VSS						2598.674	-9322.816
D31	CSI2_DP4						1923.034	-9363.456
D32	CSI2_CLKP1						1359.662	-9688.576

Table 9-1. U/U-Quad Core Processor Ball List (Sheet 28 of 39)

Ball #	Ball Name	DDR3L	LPDDR3	DDR4	Interleaved (IL)	Non-Interleaved (NIL)	X[um]	Y[um]
D33	CSI2_DP5						796.29	-9363.456
D34	VSS						120.65	-9322.816
D36	CSI2_DP2						-554.99	-9363.456
D37	CSI2_CLKP0						-1118.362	-9688.576
D38	CSI2_DP1						-1681.734	-9363.456
D39	VSS						-2357.374	-9322.816
D4	RSVD						18690.59	-9668.51
D40	CLKOUT_PCIE_N3						-3033.014	-9363.456
D41	CLKOUT_PCIE_N2						-3596.386	-9688.576
D42	CLKOUT_PCIE_N0						-4159.758	-9363.456
D44	VSS						-4835.398	-9322.816
D45	VSS						-5511.038	-9363.456
D46	EDP_TXN[1]						-6074.41	-9688.576
D47	VSS						-6637.782	-9363.456
D48	VSS						-7313.422	-9322.816
D5	RSVD						18090.388	-9363.456
D50	DDI2_TXP[0]						-7989.062	-9363.456
D51	DDI2_TXN[3]						-8552.434	-9688.576
D52	DDI2_TXP[1]						-9115.806	-9363.456
D53	VSS						-9791.446	-9322.816
D54	RSVD						-10467.086	-9363.456
D55	BPM#[1]						-11030.458	-9688.576
D56	PROC_PRDY#						-11593.83	-9363.456
D58	VSS						-12269.47	-9322.816
D59	PCH_JTAG_TDI						-12945.11	-9363.456
D6	VSS						17441.418	-9322.816
D60	PROC_TDI						-13508.482	-9688.576
D61	PROC_PREQ#						-14071.854	-9363.456
D62	VSS						-14747.494	-9322.816
D63	CATERR#						-15423.134	-9363.456
D64	VIDSOUT						-15986.506	-9688.576
D65	CFG[2]						-16549.878	-9363.456
D66	VSS						-17225.518	-9322.816
D67	CFG[3]						-17898.618	-10013.696
D68	CFG[6]						-19267.424	-9535.16
D69	VSS						-18561.812	-8971.026
D7	GPP_D20 / DMIC_DATA0						16791.178	-9363.456
D71	RSVD						-20314.412	-9551.416

Table 9-1. U/U-Quad Core Processor Ball List (Sheet 29 of 39)

Ball #	Ball Name	DDR3L	LPDDR3	DDR4	Interleaved (IL)	Non-Interleaved (NIL)	X[um]	Y[um]
D8	GPP_D17 / DMIC_CLK1						16227.806	-9688.576
D9	GPP_E11 / USB2_OC2#						15664.434	-9363.456
E1	RSVD						20314.158	-9039.86
E10	USB3_4_RXN						14910.816	-8591.296
E11	VSS						13996.416	-8591.296
E13	CSI2_COMP						13082.016	-8591.296
E15	VSS						12167.616	-8591.296
E16	PCIE5_RXP						11253.216	-8591.296
E18	VSS						10338.816	-8591.296
E2	RSVD						19663.918	-9039.86
E20	PCIE7_RXP / SATA0_RXP						9424.416	-8591.296
E21	VSS						8510.016	-8591.296
E22	PCIE9_RXN						7595.616	-8591.296
E23	PCIE9_RXP						6681.216	-8591.296
E25	PCIE10_RXP						5766.816	-8591.296
E27	PCIE11_RXP / SATA1B_RXP						4852.416	-8591.296
E28	PCIE11_RXN / SATA1B_RXN						3938.016	-8591.296
E3	RSVD						19013.678	-9039.86
E30	PCIE12_RXN / SATA2_RXN						3023.616	-8591.296
E32	VCC_SENSE						2109.216	-8591.296
E33	VSS_SENSE						1194.816	-8591.296
E35	XTAL24_OUT						280.416	-8591.296
E37	XTAL24_IN						-633.984	-8591.296
E38	CLKOUT_PCIE_P5						-1548.384	-8591.296
E40	CLKOUT_PCIE_N5						-2462.784	-8591.296
E42	XCLK_BIASREF						-3377.184	-8591.296
E43	CLKOUT_ITPXDP_P						-4291.584	-8591.296
E45	EDP_AUXN						-5205.984	-8591.296
E46	VSS						-6120.384	-8591.296
E48	DDI2_AUXN						-7034.784	-8591.296
E5	PCIE_RCOMPP						17654.016	-8591.296
E50	VSS						-7949.184	-8591.296
E52	eDP_RCOMP						-8863.584	-8591.296
E53	VSS						-9777.984	-8591.296
E55	DDI1_TXN[0]						-10692.384	-8591.296
E56	VSS						-11606.784	-8591.296
E58	DDI1_TXN[1]						-12521.184	-8591.296

Table 9-1. U/U-Quad Core Processor Ball List (Sheet 30 of 39)

Ball #	Ball Name	DDR3L	LPDDR3	DDR4	Interleaved (IL)	Non-Interleaved (NIL)	X[um]	Y[um]
E6	VSS						16739.616	-8591.296
E60	CFG_RCOMP						-13435.584	-8591.296
E61	RSVD						-14349.984	-8591.296
E63	CFG[16]						-15315.184	-8654.796
E65	VSS						-16331.184	-8654.796
E66	CFG[18]						-17347.184	-8654.796
E68	CFG[0]						-17898.618	-9363.456
E70	CFG[4]						-19664.172	-9009.126
E71	VSS						-20314.412	-8901.176
E8	ITP_PMODE						15825.216	-8591.296
F1	VSS						19989.038	-8465.82
F10	USB3_4_RXP						14910.816	-7941.056
F11	PCIE2_RXP / USB3_6_RXP						13996.416	-7941.056
F13	VSS						13082.016	-7941.056
F15	PCIE4_RXP						12167.616	-7941.056
F16	PCIE5_RXN						11253.216	-7941.056
F18	PCIE6_RXP						10338.816	-7941.056
F2	VSS						19338.798	-8465.82
F20	PCIE7_RXN / SATA0_RXN						9424.416	-7941.056
F21	PCIE8_RXP / SATA1A_RXP						8510.016	-7941.056
F22	VSS						7595.616	-7941.056
F23	VSS						6681.216	-7941.056
F25	PCIE10_RXN						5766.816	-7941.056
F27	VSS						4852.416	-7941.056
F28	VSS						3938.016	-7941.056
F30	PCIE12_RXP / SATA2_RXP						3023.616	-7941.056
F32	VSS						2109.216	-7941.056
F33	VSS						1194.816	-7941.056
F35	VSS						280.416	-7941.056
F37	VSS						-633.984	-7941.056
F38	VSS						-1548.384	-7941.056
F4	VSS						18363.438	-8465.82
F40	VSS						-2462.784	-7941.056
F42	VSS						-3377.184	-7941.056
F43	CLKOUT_ITPXDP_N						-4291.584	-7941.056
F45	EDP_AUXP						-5205.984	-7941.056
F46	RSVD						-6120.384	-7941.056



Table 9-1. U/U-Quad Core Processor Ball List (Sheet 31 of 39)

Ball #	Ball Name	DDR3L	LPDDR3	DDR4	Interleaved (IL)	Non-Interleaved (NIL)	X[um]	Y[um]
F48	DDI2_AUXP						-7034.784	-7941.056
F5	PCIE_RCOMPN						17654.016	-7941.056
F50	DDI1_AUXP						-7949.184	-7941.056
F52	RSVD						-8863.584	-7941.056
F53	DDI1_TXN[2]						-9777.984	-7941.056
F55	DDI1_TXP[0]						-10692.384	-7941.056
F56	DDI1_TXN[3]						-11606.784	-7941.056
F58	DDI1_TXP[1]						-12521.184	-7941.056
F6	RSVD						16739.616	-7941.056
F60	RSVD						-13435.584	-7941.056
F61	RSVD						-14349.984	-7941.056
F63	CFG[17]						-15315.184	-8004.556
F65	VSS						-16331.184	-8004.556
F66	CFG[19]						-17347.184	-8004.556
F68	VSS						-18561.812	-8320.024
F70	CFG[10]						-19212.052	-8320.024
F71	CFG[8]						-19862.292	-8383.524
F8	VSS						15825.216	-7941.056
G1	CL_RST#						20314.158	-7802.88
G10	VSS						14910.816	-7290.816
G11	PCIE2_RXN / USB3_6_RXN						13996.416	-7290.816
G13	PCIE1_RXP / USB3_5_RXP						13082.016	-7290.816
G15	PCIE4_RXN						12167.616	-7290.816
G16	PCIE3_RXP						11253.216	-7290.816
G18	PCIE6_RXN						10338.816	-7290.816
G2	CL_DATA						19663.918	-7802.88
G20	VCCSTG						9424.416	-7290.816
G21	PCIE8_RXN / SATA1A_RXN						8510.016	-7290.816
G22	VSS						7595.616	-7290.816
G23	VCCSA						6681.216	-7290.816
G25	VCCSA						5766.816	-7290.816
G27	VCCSA						4852.416	-7290.816
G28	VCCSA						3938.016	-7290.816
G3	CL_CLK						19013.678	-7802.88
G30	VCC						3023.616	-7290.816
G32	VCC						2109.216	-7290.816
G33	VCC						1194.816	-7290.816

Table 9-1. U/U-Quad Core Processor Ball List (Sheet 32 of 39)

Ball #	Ball Name	DDR3L	LPDDR3	DDR4	Interleaved (IL)	Non-Interleaved (NIL)	X[um]	Y[um]
G35	VCC						280.416	-7290.816
G37	VCC						-633.984	-7290.816
G38	VCC						-1548.384	-7290.816
G4	GPP_E2 / SATAXPCIE2 / SATAGP2						18363.438	-7802.88
G40	VCC						-2462.784	-7290.816
G42	VCC						-3377.184	-7290.816
G43	VSS						-4291.584	-7290.816
G45	VSS						-5205.984	-7290.816
G46	RSVD						-6120.384	-7290.816
G48	VSS						-7034.784	-7290.816
G5	VSS						17654.016	-7290.816
G50	DDI1_AUXN						-7949.184	-7290.816
G52	VSS						-8863.584	-7290.816
G53	DDI1_TXP[2]						-9777.984	-7290.816
G55	VSS						-10692.384	-7290.816
G56	DDI1_TXP[3]						-11606.784	-7290.816
G58	VSS						-12521.184	-7290.816
G6	VSS						16739.616	-7290.816
G60	VSS						-13435.584	-7290.816
G61	VCC_OPC_1P8						-14349.984	-7290.816
G63	VSS						-15315.184	-7354.316
G65	VSS						-16331.184	-7354.316
G66	VSS						-17347.184	-7354.316
G68	CFG[11]						-18363.692	-7659.624
G69	CFG[9]						-19013.932	-7659.624
G70	CFG[15]						-19664.172	-7758.684
G71	CFG[13]						-20314.412	-7758.684
G8	USB3_1_RXP						15825.216	-7290.816
H1	GPP_E8 / SATALED#						19989.038	-7139.94
H10	USB3_3_RXP	?					14910.816	-6640.576
H11	RSVD						13996.416	-6640.576
H13	PCIE1_RXN / USB3_5_RXN						13082.016	-6640.576
H15	VSS						12167.616	-6640.576
H16	PCIE3_RXN						11253.216	-6640.576
H18	VSS						10338.816	-6640.576
H2	GPP_E0 / SATAXPCIE0 / SATAGP0						19338.798	-7139.94
H20	VCCSA_SENSE						9424.416	-6640.576



Table 9-1. U/U-Quad Core Processor Ball List (Sheet 33 of 39)

Ball #	Ball Name	DDR3L	LPDDR3	DDR4	Interleaved (IL)	Non-Interleaved (NIL)	X[um]	Y[um]
H21	VSSSA_SENSE						8510.016	-6640.576
H3	GPP_E1 / SATAXPCIE1 / SATAGP1						18688.558	-7139.94
H5	GPP_D19 / DMIC_CLK0						17654.016	-6640.576
H6	USB3_2_RXP / SSIC_RXP						16739.616	-6640.576
H63	VCC_OPC_1P8						-15315.184	-6704.076
H65	OPC_RCOMP						-16331.184	-6704.076
H66	OPCE_RCOMP						-17347.184	-6704.076
H69	CFG[14]						-18688.812	-7095.744
H70	CFG[12]						-19339.052	-7095.744
H71	VSS						-19989.292	-7095.744
H8	USB3_1_RXN						15825.216	-6640.576
J1	GPP_E4 / DEVSLP0						20314.158	-6477
J10	USB3_3_RXN						14910.816	-5990.336
J11	VSS						13996.416	-5990.336
J13	VSS						13082.016	-5990.336
J2	GPP_E5 / DEVSLP1						19663.918	-6477
J22	VCCSA						7138.416	-6826.504
J23	VCCSA						6224.016	-6826.504
J25	VSS						5309.616	-6826.504
J27	VCCSA						4395.216	-6826.504
J28	VSS						3480.816	-6826.504
J3	GPP_E6 / DEVSLP2						19013.678	-6477
J30	VCC						2566.416	-6826.504
J32	VSS						1652.016	-6826.504
J33	VCC						737.616	-6826.504
J35	VSS						-176.784	-6826.504
J37	VCC						-1091.184	-6826.504
J38	VSS						-2005.584	-6826.504
J4	GPP_D3 / SPI1_MOSI						18363.438	-6477
J40	VCC						-2919.984	-6826.504
J42	VSS						-3834.384	-6826.504
J43	VCCGT						-4748.784	-6826.504
J45	VCCGT						-5663.184	-6826.504
J46	VCCGT						-6577.584	-6826.504
J48	VCCGT						-7491.984	-6826.504
J5	GPP_D23 / I2S_MCLK						17654.016	-5990.336
J50	VCCGT						-8406.384	-6826.504

Table 9-1. U/U-Quad Core Processor Ball List (Sheet 34 of 39)

Ball #	Ball Name	DDR3L	LPDDR3	DDR4	Interleaved (IL)	Non-Interleaved (NIL)	X[um]	Y[um]
J52	VCCGT						-9320.784	-6826.504
J53	VCCGT						-10235.184	-6826.504
J55	VCCGT						-11149.584	-6826.504
J56	VCCGT						-12063.984	-6826.504
J58	VCCGT						-12978.384	-6826.504
J6	USB3_2_RXN / SSIC_RXN						16739.616	-5990.336
J60	VCCGT						-13892.784	-6826.504
J68	RSVD						-18361.914	-6519.926
J69	VSSGT_SENSE						-19013.932	-6432.804
J70	VCCGT_SENSE						-19664.172	-6432.804
J71	RSVD						-20314.412	-6432.804
J8	VSS						15825.216	-5990.336
K15	VCCAMPHYPLL_1P0						12188.19	-5876.29
K16	VSS						11537.95	-5876.29
K17	VCCMPHYAON_1P0						10887.71	-5876.29
K18	VSS						10237.47	-5876.29
K19	VCCCLK2						9587.23	-5876.29
K20	VccPLL						8936.99	-5876.29
K21	VccPLL						8286.75	-5876.29
K22	VSS						7595.616	-6361.684
K23	VCCSA						6681.216	-6361.684
K25	VCCSA						5766.816	-6361.684
K27	VCCSA						4852.416	-6361.684
K28	VCCSA						3938.016	-6361.684
K30	VCCSA						3023.616	-6361.684
K32	RSVD						2109.216	-6361.684
K33	VCC						1194.816	-6361.684
K35	VCC						280.416	-6361.684
K37	VCC						-633.984	-6361.684
K38	VCC						-1548.384	-6361.684
K40	VCC						-2462.784	-6361.684
K42	VCC						-3377.184	-6361.684
K43	VCC						-4291.584	-6361.684
K45	RSVD						-5205.984	-6361.684
K46	RSVD						-6120.384	-6361.684
K48	VCCGT						-7034.784	-6361.684
K50	VCCGT						-7949.184	-6361.684
K52	VCCGT						-8863.584	-6361.684

Table 9-1. U/U-Quad Core Processor Ball List (Sheet 35 of 39)

Ball #	Ball Name	DDR3L	LPDDR3	DDR4	Interleaved (IL)	Non-Interleaved (NIL)	X[um]	Y[um]
K53	VCCGT						-9777.984	-6361.684
K55	VCCGT						-10692.384	-6361.684
K56	VCCGT						-11606.784	-6361.684
K58	VCCGT						-12521.184	-6361.684
K60	VCCGT						-13435.584	-6361.684
K61	VSS						-14349.984	-6361.684
K63	VSS						-15132.812	-6054.09
K64	VSS						-15783.052	-6054.09
K65	VSS						-16433.292	-6054.09
K66	VSS						-17083.532	-6054.09
K67	VSS						-17733.772	-6054.09
K68	VSS						-18351.754	-5846.064
K70	VSS						-19339.052	-5744.464
K71	VSS						-19989.292	-5744.464
L1	VCCMPHYAON_1P0						19989.038	-5814.06
L10	GPP_E17 / EDP_HPD						14984.476	-5340.096
L11	VSS						14334.236	-5340.096
L12	GPP_E19 / DDPB_CTRLDATA						13683.996	-5340.096
L13	GPP_E18 / DDPB_CTRLCLK						13033.756	-5340.096
L15	VCCAMPHYPLL_1P0						12188.19	-5038.09
L16	VSS						11537.95	-5038.09
L17	VSS						10887.71	-5038.09
L18	VSS						10237.47	-5038.09
L19	VCCCLK5						9587.23	-5038.09
L2	VSS						19338.798	-5814.06
L20	VSS						8936.99	-5038.09
L21	VCCCLK3						8286.75	-5038.09
L4	VSS						18363.438	-5814.06
L6	GPP_E15 / DDPD_HPD2						17585.436	-5340.096
L62	VCCGT						-14643.862	-5624.83
L63	VCCGT						-15112.492	-5167.63
L64	VCCGT						-15762.732	-5167.63
L65	VCCGT						-16412.972	-5167.63
L66	VCCGT						-17063.212	-5167.63
L67	VCCGT						-17713.452	-5167.63
L68	VCCGT						-18363.692	-5167.63
L69	VCCGT						-19013.932	-5167.63

Table 9-1. U/U-Quad Core Processor Ball List (Sheet 36 of 39)

Ball #	Ball Name	DDR3L	LPDDR3	DDR4	Interleaved (IL)	Non-Interleaved (NIL)	X[um]	Y[um]
L7	GPP_E14 / DDPC_HPD1						16935.196	-5340.096
L70	VCCGT						-19664.172	-5167.63
L71	VCCGT						-20314.412	-5167.63
L8	VSS						16284.956	-5340.096
L9	GPP_E13 / DDPB_HPD0						15634.716	-5340.096
M1	GPP_D0 / SPI1_CS#						20314.158	-5151.12
M2	GPP_D1 / SPI1_CLK						19663.918	-5151.12
M3	GPP_D2 / SPI1_MISO						19013.678	-5151.12
M4	GPP_D5 / ISH_I2C0_SDA						18363.438	-5151.12
M62	VCCGT						-14643.862	-4710.43
N1	GPP_D7 / ISH_I2C1_SDA						19989.038	-4488.18
N10	VSS						14984.476	-4400.296
N11	GPP_E22						14334.236	-4400.296
N12	GPP_E23						13683.996	-4400.296
N13	VSS						13033.756	-4400.296
N15	VCCMPHYGT_1P0						12188.19	-4199.89
N16	VCCMPHYGT_1P0						11537.95	-4199.89
N17	VCCMPHYGT_1P0						10887.71	-4199.89
N18	VCCAPLLEBB_1P0						10237.47	-4199.89
N19	VSS						9587.23	-4199.89
N2	GPP_D8 / ISH_I2C1_SCL						19338.798	-4488.18
N20	VCCCLK4						8936.99	-4199.89
N21	VSS						8286.75	-4199.89
N3	GPP_D6 / ISH_I2C0_SCL						18688.558	-4488.18
N6	VSS						17585.436	-4400.296
N63	VCCGT						-15112.492	-4253.23
N64	VCCGT						-15762.732	-4253.23
N65	VSS						-16412.972	-4253.23
N66	VCCGT						-17063.212	-4253.23
N67	VCCGT						-17713.452	-4253.23
N68	VSS						-18363.692	-4253.23
N69	VCCGT						-19013.932	-4253.23
N7	GPP_E20 / DDPC_CTRLCLK						16935.196	-4400.296
N70	VCCGT						-19664.172	-4253.23
N71	VCCGT						-20314.412	-4253.23
N8	GPP_E21 / DDPC_CTRLDATA						16284.956	-4400.296
N9	GPP_E16 / DDPE_HPD3						15634.716	-4400.296

Table 9-1. U/U-Quad Core Processor Ball List (Sheet 37 of 39)

Ball #	Ball Name	DDR3L	LPDDR3	DDR4	Interleaved (IL)	Non-Interleaved (NIL)	X[um]	Y[um]
P1	GPP_D12						20314.158	-3825.24
P15	VCCMPHYGT_1P0						12188.19	-3361.69
P16	VCCMPHYGT_1P0						11537.95	-3361.69
P17	VSS						10887.71	-3361.69
P18	VCCPRIM_1P0						10237.47	-3361.69
P19	VSS						9587.23	-3361.69
P2	GPP_D9						19663.918	-3825.24
P20	VSS						8936.99	-3361.69
P21	VSS						8286.75	-3361.69
P3	GPP_D10						19013.678	-3825.24
P4	GPP_D11						18363.438	-3825.24
P62	VCCOPC						-14643.862	-3796.03
R10	GPP_C2 / SMBALERT#						14984.476	-3333.496
R11	eDP_BKLTCTL						14334.236	-3333.496
R12	eDP_BKLTEN						13683.996	-3333.496
R13	VSS						13033.756	-3333.496
R6	VSS						17585.436	-3333.496
R63	VCCGT						-15112.492	-3338.83
R64	VCCGT						-15762.732	-3338.83
R65	VCCGT						-16412.972	-3338.83
R66	VCCGT						-17063.212	-3338.83
R67	VCCGT						-17713.452	-3338.83
R68	VCCGT						-18363.692	-3338.83
R69	VCCGT						-19013.932	-3338.83
R7	GPP_C0 / SMBCLK						16935.196	-3333.496
R70	VCCGT						-19664.172	-3338.83
R71	VCCGT						-20314.412	-3338.83
R8	GPP_C1 / SMBDATA						16284.956	-3333.496
R9	GPP_C3 / SML0CLK						15634.716	-3333.496
T1	VCCPRIM_1p0						19989.038	-3162.3
T15	VSS						12188.19	-2523.49
T16	VCCPGPPE						11537.95	-2523.49
T17	VSS						10887.71	-2523.49
T18	VSS						10237.47	-2523.49
T19	VCCSRAM_1P0						9587.23	-2523.49
T2	VSS						19338.798	-3162.3
T20	VCCSRAM_1P0						8936.99	-2523.49
T21	VSS						8286.75	-2523.49

Table 9-1. U/U-Quad Core Processor Ball List (Sheet 38 of 39)

Ball #	Ball Name	DDR3L	LPDDR3	DDR4	Interleaved (IL)	Non-Interleaved (NIL)	X[um]	Y[um]
T4	VSS						18363.438	-3162.3
T62	VCCGT						-14643.862	-2881.63
U1	GPP_D13 / ISH_UART0_RXD / SML0BDATA / I2C4B_SDA						20314.158	-2499.36
U10	VSS						14984.476	-2266.696
U11	RSVD						14334.236	-2266.696
U12	RSVD						13683.996	-2266.696
U13	eDP_VDDEN						13033.756	-2266.696
U2	GPP_D14 / ISH_UART0_TXD / SML0BCLK / I2C4B_SCL						19663.918	-2499.36
U3	GPP_D15 / ISH_UART0_RTS#						19013.678	-2499.36
U4	GPP_D16 / ISH_UART0_CTS# / SML0BALERT#						18363.438	-2499.36
U6	GPP_C17 / I2C0_SCL						17585.436	-2266.696
U63	VSS						-15112.492	-2424.43
U64	VSS						-15762.732	-2424.43
U65	VCCGT						-16412.972	-2424.43
U66	VSS						-17063.212	-2424.43
U67	VSS						-17713.452	-2424.43
U68	VCCGT						-18363.692	-2424.43
U69	VSS						-19013.932	-2424.43
U7	GPP_C16 / I2C0_SDA						16935.196	-2266.696
U70	VSS						-19664.172	-2424.43
U71	VCCGT						-20314.412	-2424.43
U8	GPP_C18 / I2C1_SDA						16284.956	-2266.696
U9	GPP_C19 / I2C1_SCL						15634.716	-2266.696
V1	GPP_D21 / SPI1_IO2						19989.038	-1836.42
V15	VCCAPLL_1P0						12188.19	-1685.29
V16	VSS						11537.95	-1685.29
V17	VSS						10887.71	-1685.29
V18	VSS						10237.47	-1685.29
V19	VCCPRIM_3p3						9587.23	-1685.29
V2	GPP_D22 / SPI1_IO3						19338.798	-1836.42
V20	VCCPRIM_CORE						8936.99	-1685.29
V21	VCCPRIM_CORE						8286.75	-1685.29
V3	GPP_C7 / SML1DATA						18688.558	-1836.42
V62	VCCOPC						-14643.862	-1967.23

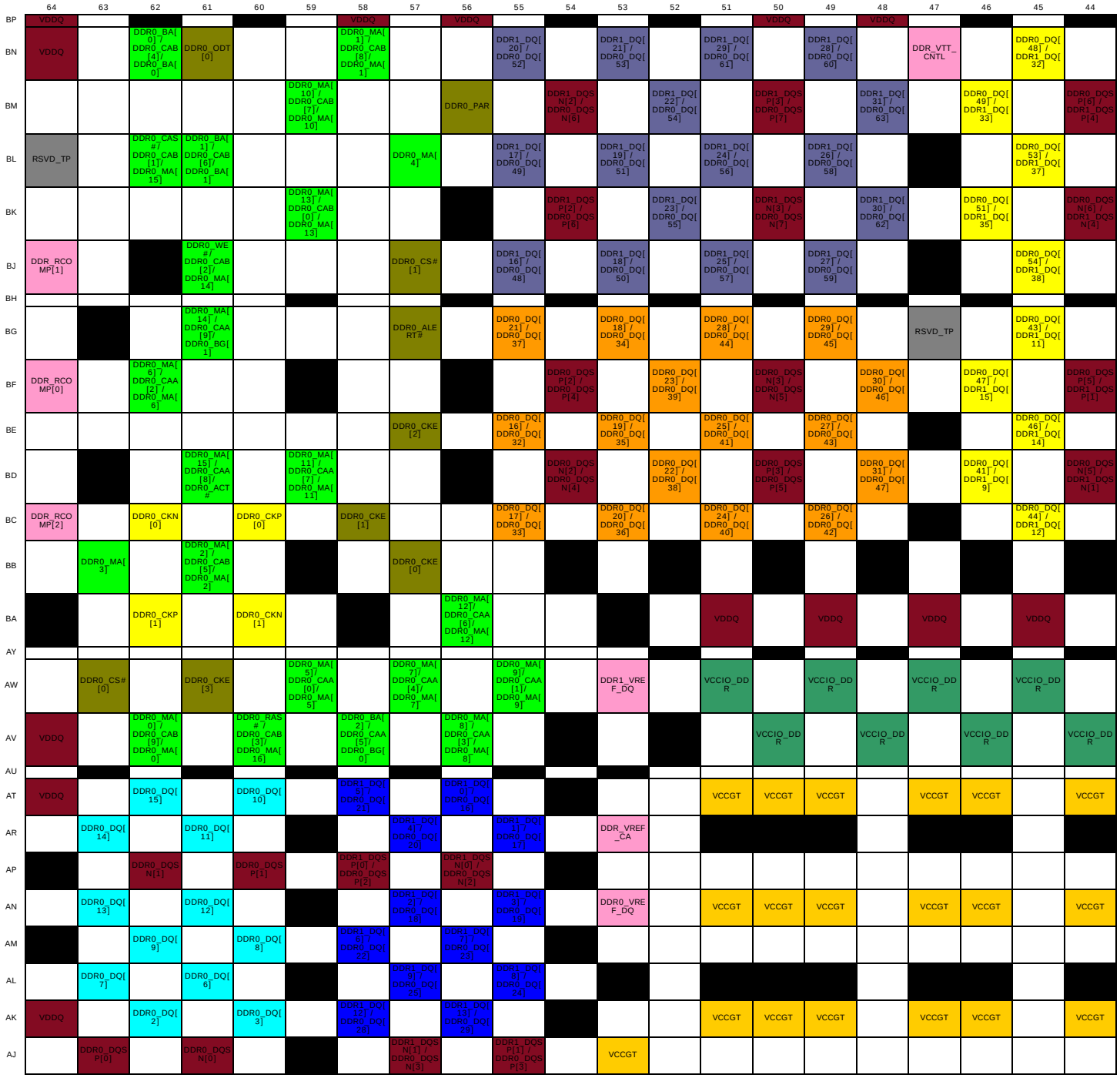
Table 9-1. U/U-Quad Core Processor Ball List (Sheet 39 of 39)

Ball #	Ball Name	DDR3L	LPDDR3	DDR4	Interleaved (IL)	Non-Interleaved (NIL)	X[um]	Y[um]
W1	GPP_C5 / SML0ALERT#						20314.158	-1173.48
W10	GPP_G5 / SD_CD#						14984.476	-1199.896
W11	GPP_G4 / SD_DATA3						14334.236	-1199.896
W12	GPP_G3 / SD_DATA2						13683.996	-1199.896
W13	VSS						13033.756	-1199.896
W2	GPP_C4 / SML0DATA						19663.918	-1173.48
W3	GPP_C6 / SML1CLK						19013.678	-1173.48
W4	GPP_C10 / UART0_RTS#						18363.438	-1173.48
W6	VSS						17585.436	-1199.896
W63	VCCGT						-15112.492	-1510.03
W64	VCCGT						-15762.732	-1510.03
W65	VCCGT						-16412.972	-1510.03
W66	VCCGT						-17063.212	-1510.03
W67	VCCGT						-17713.452	-1510.03
W68	VCCGT						-18363.692	-1510.03
W69	VCCGT						-19013.932	-1510.03
W7	GPP_G7 / SD_WP						16935.196	-1199.896
W70	VCCGT						-19664.172	-1510.03
W71	VCCGT						-20314.412	-1510.03
W8	GPP_G6 / SD_CLK						16284.956	-1199.896
W9	VSS						15634.716	-1199.896
Y15	VCCPGPPD						12188.19	-847.09
Y16	VCCPGPPC						11537.95	-847.09
Y17	VSS						10887.71	-847.09
Y18	VCCPRIM_1p0						10237.47	-847.09
Y19	VSS						9587.23	-847.09
Y20	VSS						8936.99	-847.09
Y21	VSS						8286.75	-847.09
Y62	VCCGT						-14643.862	-1052.83

9.2 Y-Processor Ball Information

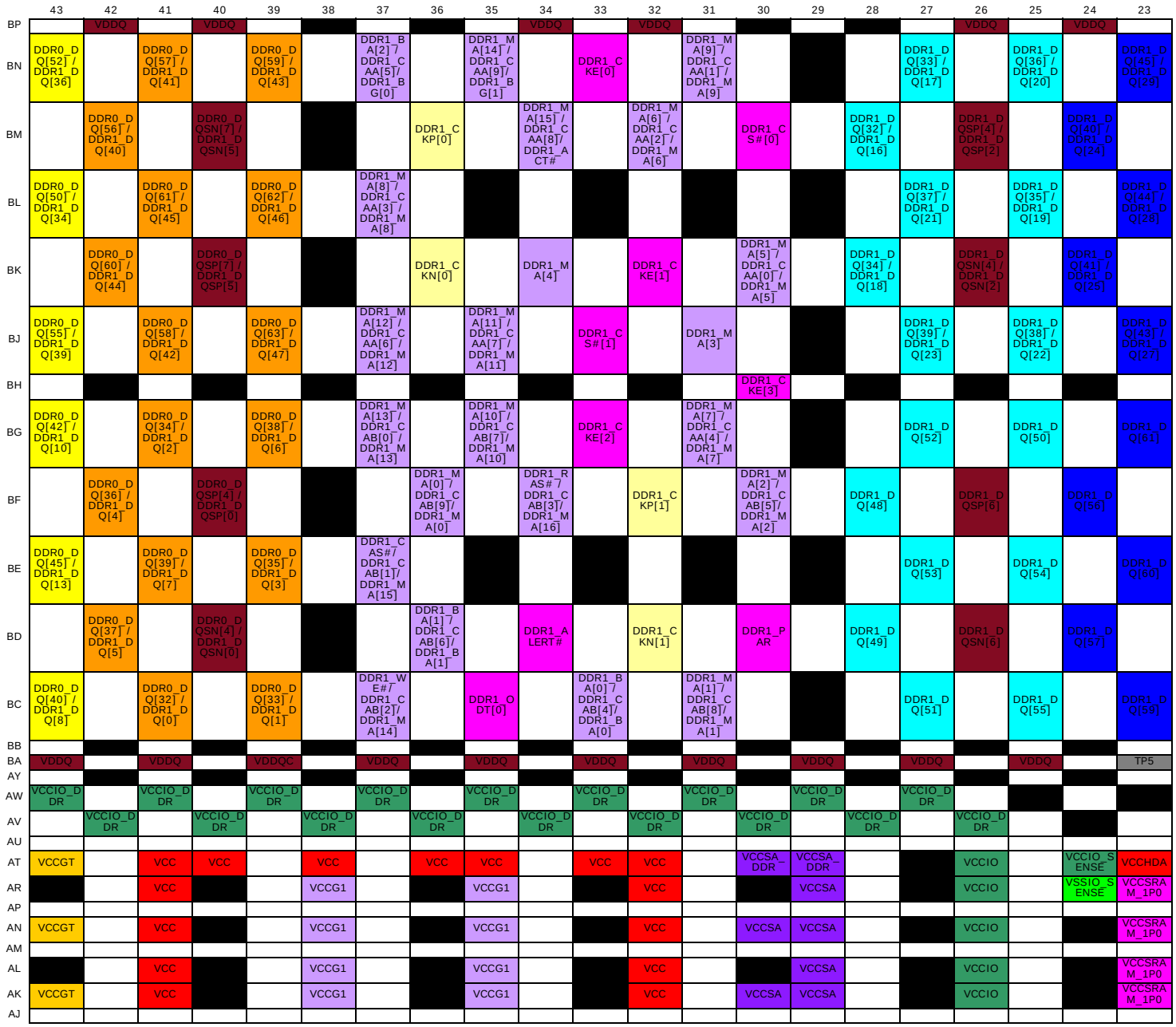
The Y-Processor is available in the BGA package (BGA1515). Figure 9-7 through Figure 9-12 provide a top view of the Ball map. Table 9-2 provides the Ball list.

Figure 9-7. Y-Processor Ball Map (Upper Left, Columns 64-44)



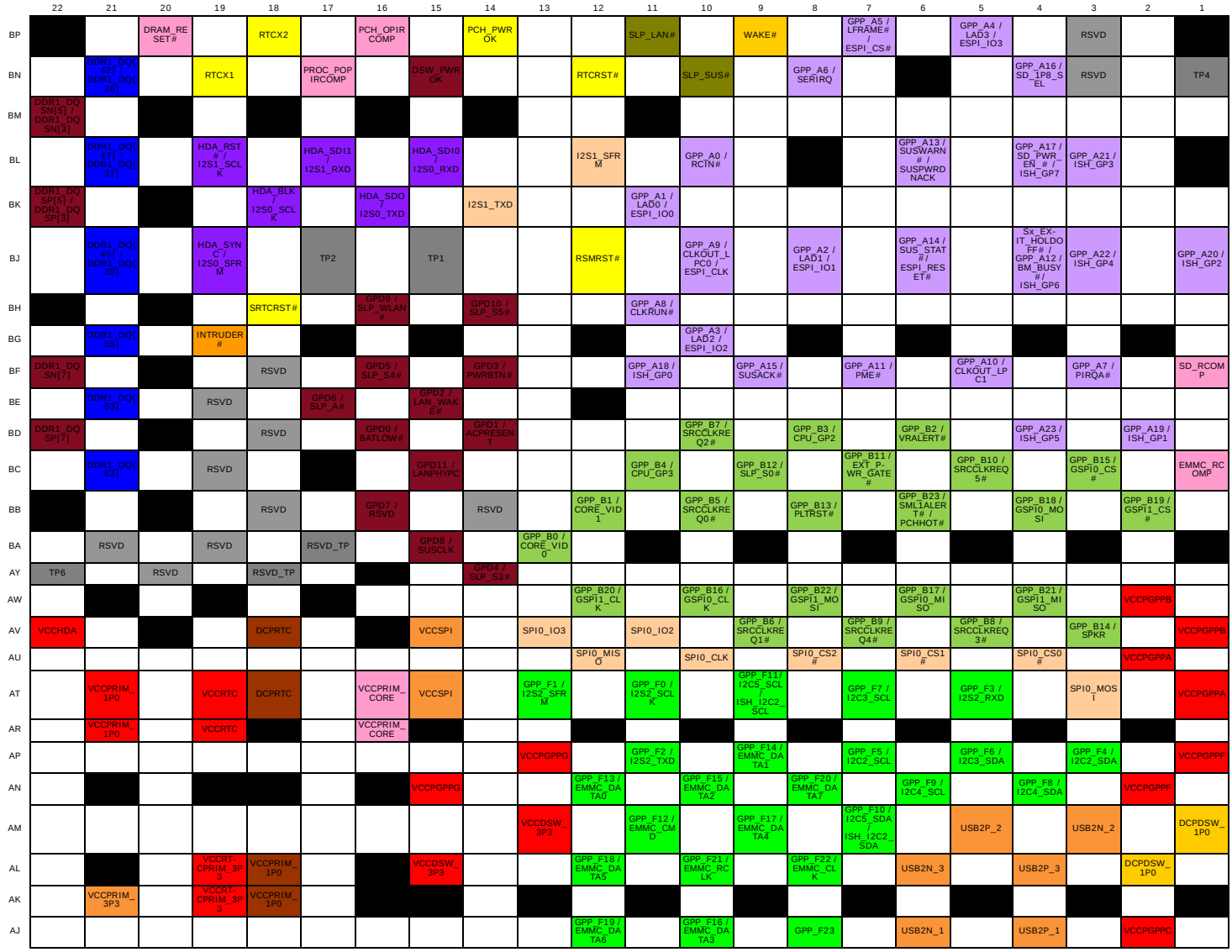
	64	63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48	47	46	45	44
BP	VDDQ						VDDQ		VDDQ						VDDQ		VDDQ				
BN	VDDQ		DDR0_BA[0] / DDR0_CAB[4]/ DDR0_BA[0]	DDR0_ODT[0]			DDR0_MA[1] / DDR0_CAB[8]/ DDR0_MA[1]			DDR1_DQ[20] / DDR0_DQ[52]		DDR1_DQ[21] / DDR0_DQ[53]		DDR1_DQ[29] / DDR0_DQ[61]		DDR1_DQ[28] / DDR0_DQ[60]		DDR_VTT_CNTL		DDR0_DQ[48] / DDR1_DQ[32]	
BM						DDR0_MA[10] / DDR0_CAB[7]/ DDR0_MA[10]			DDR0_PAR		DDR1_DQSN[2] / DDR0_DQSN[6]		DDR1_DQ[22] / DDR0_DQ[54]		DDR1_DQSP[3] / DDR0_DQSP[7]		DDR1_DQ[31] / DDR0_DQ[63]		DDR0_DQ[49] / DDR1_DQ[33]		DDR0_DQSP[6] / DDR1_DQSP[4]
BL	RSVD_TP		DDR0_CAS#7 DDR0_CAB[1]/ DDR0_MA[15]	DDR0_BA[1] / DDR0_CAB[6]/ DDR0_BA[1]				DDR0_MA[4]		DDR1_DQ[17] / DDR0_DQ[49]		DDR1_DQ[19] / DDR0_DQ[51]		DDR1_DQ[24] / DDR0_DQ[56]		DDR1_DQ[26] / DDR0_DQ[58]				DDR0_DQ[53] / DDR1_DQ[37]	
BK						DDR0_MA[13] / DDR0_CAB[0]/ DDR0_MA[13]				DDR1_DQSP[2] / DDR0_DQSP[6]		DDR1_DQ[23] / DDR0_DQ[55]		DDR1_DQSN[3] / DDR0_DQSN[7]		DDR1_DQ[30] / DDR0_DQ[62]		DDR0_DQ[51] / DDR1_DQ[35]		DDR0_DQSN[6] / DDR1_DQSN[4]
BJ	DDR_RCOMP[1]			DDR0_WE#/ DDR0_CAB[2]/ DDR0_MA[14]				DDR0_CS#[1]		DDR1_DQ[16] / DDR0_DQ[48]		DDR1_DQ[18] / DDR0_DQ[50]		DDR1_DQ[25] / DDR0_DQ[57]		DDR1_DQ[27] / DDR0_DQ[59]				DDR0_DQ[54] / DDR1_DQ[38]	
BH																					
BG				DDR0_MA[14] / DDR0_CAA[9]/ DDR0_BG[1]				DDR0_ALERT#		DDR0_DQ[21] / DDR0_DQ[37]		DDR0_DQ[18] / DDR0_DQ[34]		DDR0_DQ[28] / DDR0_DQ[44]		DDR0_DQ[29] / DDR0_DQ[45]		RSVD_TP		DDR0_DQ[43] / DDR1_DQ[11]	
BF	DDR_RCOMP[0]		DDR0_MA[6] / DDR0_CAA[2] / DDR0_MA[6]								DDR0_DQSP[2] / DDR0_DQSP[4]		DDR0_DQ[23] / DDR0_DQ[39]		DDR0_DQSN[3] / DDR0_DQSN[5]		DDR0_DQ[30] / DDR0_DQ[46]		DDR0_DQ[47] / DDR1_DQ[15]		DDR0_DQSP[5] / DDR1_DQSP[1]
BE								DDR0_CKE[2]		DDR0_DQ[16] / DDR0_DQ[32]		DDR0_DQ[19] / DDR0_DQ[35]		DDR0_DQ[25] / DDR0_DQ[41]		DDR0_DQ[27] / DDR0_DQ[43]				DDR0_DQ[46] / DDR1_DQ[14]	
BD				DDR0_MA[15] / DDR0_CAA[8]/ DDR0_ACT#		DDR0_MA[11] / DDR0_CAA[7] / DDR0_MA[11]					DDR0_DQSN[2] / DDR0_DQSN[4]		DDR0_DQ[22] / DDR0_DQ[38]		DDR0_DQSP[3] / DDR0_DQSP[5]		DDR0_DQ[31] / DDR0_DQ[47]		DDR0_DQ[41] / DDR1_DQ[9]		DDR0_DQSN[5] / DDR1_DQSN[1]
BC	DDR_RCOMP[2]		DDR0_CKN[0]		DDR0_CKP[0]		DDR0_CKE[1]			DDR0_DQ[17] / DDR0_DQ[33]		DDR0_DQ[20] / DDR0_DQ[36]		DDR0_DQ[24] / DDR0_DQ[40]		DDR0_DQ[26] / DDR0_DQ[42]				DDR0_DQ[44] / DDR1_DQ[12]	
BB		DDR0_MA[3]		DDR0_MA[2] / DDR0_CAB[5]/ DDR0_MA[2]				DDR0_CKE[0]													
BA			DDR0_CKP[1]		DDR0_CKN[1]				DDR0_MA[12]/ DDR0_CAA[6]/ DDR0_MA[12]					VDDQ		VDDQ		VDDQ		VDDQ	
AY																					
AW		DDR0_CS#[0]		DDR0_CKE[3]		DDR0_MA[5]/ DDR0_CAA[0]/ DDR0_MA[5]		DDR0_MA[7]/ DDR0_CAA[4]/ DDR0_MA[7]		DDR0_MA[9]/ DDR0_CAA[1]/ DDR0_MA[9]		DDR1_VREF_DQ		VCCIO_DDR		VCCIO_DDR		VCCIO_DDR		VCCIO_DDR	
AV	VDDQ		DDR0_MA[0] / DDR0_CAB[9]/ DDR0_MA[0]		DDR0_RAS# / DDR0_CAB[3]/ DDR0_MA[16]		DDR0_BA[2] / DDR0_CAA[5]/ DDR0_BG[0]		DDR0_MA[8] / DDR0_CAA[3] / DDR0_MA[8]						VCCIO_DDR		VCCIO_DDR		VCCIO_DDR		VCCIO_DDR
AU																					
AT	VDDQ		DDR0_DQ[15]		DDR0_DQ[10]		DDR1_DQ[5] / DDR0_DQ[21]		DDR1_DQ[0] / DDR0_DQ[16]					VCCGT	VCCGT	VCCGT		VCCGT	VCCGT		VCCGT
AR		DDR0_DQ[14]		DDR0_DQ[11]				DDR1_DQ[4] / DDR0_DQ[20]		DDR1_DQ[1] / DDR0_DQ[17]		DDR_VREF_CA									
AP			DDR0_DQSN[1]		DDR0_DQSP[1]		DDR1_DQSP[0] / DDR0_DQSP[2]		DDR1_DQSN[0] / DDR0_DQSN[2]												
AN		DDR0_DQ[13]		DDR0_DQ[12]				DDR1_DQ[2] / DDR0_DQ[18]		DDR1_DQ[3] / DDR0_DQ[19]		DDR0_VREF_DQ		VCCGT	VCCGT	VCCGT		VCCGT	VCCGT		VCCGT
AM			DDR0_DQ[9]		DDR0_DQ[8]		DDR1_DQ[6] / DDR0_DQ[22]		DDR1_DQ[7] / DDR0_DQ[23]												
AL		DDR0_DQ[7]		DDR0_DQ[6]				DDR1_DQ[9] / DDR0_DQ[25]		DDR1_DQ[8] / DDR0_DQ[24]											
AK	VDDQ		DDR0_DQ[2]		DDR0_DQ[3]		DDR1_DQ[12] / DDR0_DQ[28]		DDR1_DQ[13] / DDR0_DQ[29]					VCCGT	VCCGT	VCCGT		VCCGT	VCCGT		VCCGT
AJ		DDR0_DQSP[0]		DDR0_DQSN[0]				DDR1_DQSN[1] / DDR0_DQSN[3]		DDR1_DQSP[1] / DDR0_DQSP[3]		VCCGT									

Figure 9-8. Y-Processor Ball Map (Upper Middle, Columns 43-23)



	43	42	41	40	39	38	37	36	35	34	33	32	31	30	29	28	27	26	25	24	23
BP		VDDQ		VDDQ						VDDQ		VDDQ						VDDQ		VDDQ	
BN	DDR0_DQ[52] / DDR1_DQ[36]		DDR0_DQ[57] / DDR1_DQ[41]		DDR0_DQ[59] / DDR1_DQ[43]		DDR1_BA[2] / DDR1_CAA[5] / DDR1_BG[0]		DDR1_MA[14] / DDR1_CAA[9] / DDR1_BG[1]		DDR1_CKE[0]		DDR1_MA[9] / DDR1_CAA[1] / DDR1_MA[9]				DDR1_DQ[33] / DDR1_DQ[17]		DDR1_DQ[36] / DDR1_DQ[20]		DDR1_DQ[45] / DDR1_DQ[29]
BM		DDR0_DQ[56] / DDR1_DQ[40]		DDR0_DQSN[7] / DDR1_DQSN[5]				DDR1_CKP[0]		DDR1_MA[15] / DDR1_CAA[8] / DDR1_ACT#		DDR1_MA[6] / DDR1_CAA[2] / DDR1_MA[6]		DDR1_CS#[0]		DDR1_DQ[32] / DDR1_DQ[16]		DDR1_DQSP[4] / DDR1_DQSP[2]		DDR1_DQ[40] / DDR1_DQ[24]	
BL	DDR0_DQ[50] / DDR1_DQ[34]		DDR0_DQ[61] / DDR1_DQ[45]		DDR0_DQ[62] / DDR1_DQ[46]		DDR1_MA[8] / DDR1_CAA[3] / DDR1_MA[8]										DDR1_DQ[37] / DDR1_DQ[21]		DDR1_DQ[35] / DDR1_DQ[19]		DDR1_DQ[44] / DDR1_DQ[28]
BK		DDR0_DQ[60] / DDR1_DQ[44]		DDR0_DQSP[7] / DDR1_DQSP[5]				DDR1_CKN[0]		DDR1_MA[4]		DDR1_CKE[1]		DDR1_MA[5] / DDR1_CAA[0] / DDR1_MA[5]		DDR1_DQ[34] / DDR1_DQ[18]		DDR1_DQSN[4] / DDR1_DQSN[2]		DDR1_DQ[41] / DDR1_DQ[25]	
BJ	DDR0_DQ[55] / DDR1_DQ[39]		DDR0_DQ[58] / DDR1_DQ[42]		DDR0_DQ[63] / DDR1_DQ[47]		DDR1_MA[12] / DDR1_CAA[6] / DDR1_MA[12]		DDR1_MA[11] / DDR1_CAA[7] / DDR1_MA[11]		DDR1_CS#[1]		DDR1_MA[3]				DDR1_DQ[39] / DDR1_DQ[23]		DDR1_DQ[38] / DDR1_DQ[22]		DDR1_DQ[43] / DDR1_DQ[27]
BH														DDR1_CKE[3]							
BG	DDR0_DQ[42] / DDR1_DQ[10]		DDR0_DQ[34] / DDR1_DQ[2]		DDR0_DQ[38] / DDR1_DQ[6]		DDR1_MA[13] / DDR1_CAB[0] / DDR1_MA[13]		DDR1_MA[10] / DDR1_CAB[7] / DDR1_MA[10]		DDR1_CKE[2]		DDR1_MA[7] / DDR1_CAA[4] / DDR1_MA[7]				DDR1_DQ[52]		DDR1_DQ[50]		DDR1_DQ[61]
BF		DDR0_DQ[36] / DDR1_DQ[4]		DDR0_DQSP[4] / DDR1_DQSP[0]				DDR1_MA[0] / DDR1_CAB[9] / DDR1_MA[0]		DDR1_RAS# / DDR1_CAB[3] / DDR1_MA[16]		DDR1_CKP[1]		DDR1_MA[2] / DDR1_CAB[5] / DDR1_MA[2]		DDR1_DQ[48]		DDR1_DQSP[6]		DDR1_DQ[56]	
BE	DDR0_DQ[45] / DDR1_DQ[13]		DDR0_DQ[39] / DDR1_DQ[7]		DDR0_DQ[35] / DDR1_DQ[3]		DDR1_CAS# / DDR1_CAB[1] / DDR1_MA[15]										DDR1_DQ[53]		DDR1_DQ[54]		DDR1_DQ[60]
BD		DDR0_DQ[37] / DDR1_DQ[5]		DDR0_DQSN[4] / DDR1_DQSN[0]				DDR1_BA[1] / DDR1_CAB[6] / DDR1_BA[1]		DDR1_ALERT#		DDR1_CKN[1]		DDR1_PAR		DDR1_DQ[49]		DDR1_DQSN[6]		DDR1_DQ[57]	
BC	DDR0_DQ[40] / DDR1_DQ[8]		DDR0_DQ[32] / DDR1_DQ[0]		DDR0_DQ[33] / DDR1_DQ[1]		DDR1_WE# / DDR1_CAB[2] / DDR1_MA[14]		DDR1_ODT[0]		DDR1_BA[0] / DDR1_CAB[4] / DDR1_BA[0]		DDR1_MA[1] / DDR1_CAB[8] / DDR1_MA[1]				DDR1_DQ[51]		DDR1_DQ[55]		DDR1_DQ[59]
BB																					
BA	VDDQ		VDDQ		VDDQC		VDDQ		VDDQ		VDDQ		VDDQ		VDDQ		VDDQ		VDDQ		TP5
AY																					
AW	VCCIO_DDR		VCCIO_DDR		VCCIO_DDR		VCCIO_DDR		VCCIO_DDR		VCCIO_DDR		VCCIO_DDR		VCCIO_DDR		VCCIO_DDR				
AV		VCCIO_DDR		VCCIO_DDR		VCCIO_DDR		VCCIO_DDR		VCCIO_DDR		VCCIO_DDR		VCCIO_DDR		VCCIO_DDR		VCCIO_DDR			
AU																					
AT	VCCGT		VCC	VCC		VCC		VCC	VCC		VCC	VCC		VCCSA_DDR	VCCSA_DDR			VCCIO		VCCIO_SENSE	VCCHDA
AR			VCC			VCCG1			VCCG1			VCC			VCCSA			VCCIO		VSSIO_SENSE	VCCSRAM_1P0
AP																					
AN	VCCGT		VCC			VCCG1			VCCG1			VCC		VCCSA	VCCSA			VCCIO			VCCSRAM_1P0
AM																					
AL			VCC			VCCG1			VCCG1			VCC			VCCSA			VCCIO			VCCSRAM_1P0
AK	VCCGT		VCC			VCCG1			VCCG1			VCC		VCCSA	VCCSA			VCCIO			VCCSRAM_1P0
AJ																					

Figure 9-9. Y-Processor Ball Map (Upper Right, Columns 42-1)



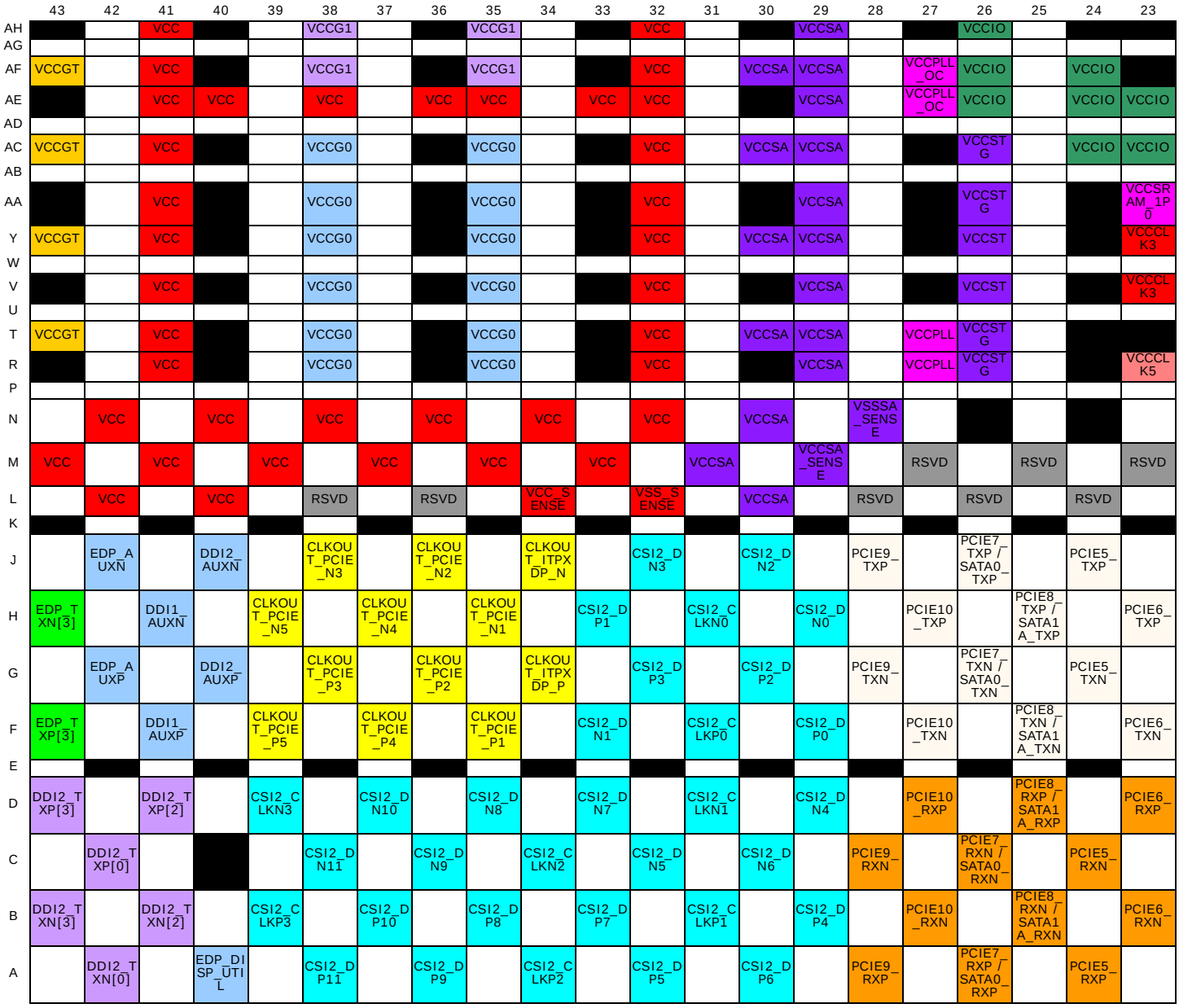
	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
BP			DRAM_RESET#		RTCX2		PCH_OPIRCOMP		PCH_PWROK			SLP_LAN#		WAKE#		GPP_A5 / LFRAME# / ESPI_CS#		GPP_A4 / LAD3 / ESPI_IO3		RSVD		
BN		DDR1_DQ[42] / DDR1_DQ[26]		RTCX1		PROC_POPIRCOMP		DSW_PWROK			RTCRST#		SLP_SUS#		GPP_A6 / SERIRQ				GPP_A16 / SD_1P8_SEL	RSVD		TP4
BM	DDR1_DQSN[5] / DDR1_DQSN[3]																					
BL		DDR1_DQ[47] / DDR1_DQ[31]		HDA_RST# / I2S1_SCLK		HDA_SDI1 / I2S1_RXD		HDA_SDI0 / I2S0_RXD			I2S1_SFRM		GPP_A0 / RCIN#				GPP_A13 / SUSWARN# / SUSPWRDNACK		GPP_A17 / SD_PWREN_# / ISH_GP7	GPP_A21 / ISH_GP3		
BK	DDR1_DQSP[5] / DDR1_DQSP[3]				HDA_BLK / I2S0_SCLK		HDA_SDO / I2S0_TXD		I2S1_TXD			GPP_A1 / LAD0 / ESPI_IO0										
BJ		DDR1_DQ[46] / DDR1_DQ[30]		HDA_SYNC / I2S0_SFRM		TP2		TP1			RSMRST#		GPP_A9 / CLKOUT_LPC0 / ESPI_CLK		GPP_A2 / LAD1 / ESPI_IO1		GPP_A14 / SUS_STAT# / ESPI_RESET#		SX_EXIT_HOLDOFF# / GPP_A12 / BM_BUSY# / ISH_GP6	GPP_A22 / ISH_GP4		GPP_A20 / ISH_GP2
BH					SRTCRST#		GPD9 / SLP_WLAN#		GPD10 / SLP_S5#			GPP_A8 / CLKRUN#										
BG		DDR1_DQ[58]		INTRUDER#									GPP_A3 / LAD2 / ESPI_IO2									
BF	DDR1_DQSN[7]				RSVD		GPD5 / SLP_S4#		GPD3 / PWRBTN#			GPP_A18 / ISH_GP0		GPP_A15 / SUSACK#		GPP_A11 / PME#		GPP_A10 / CLKOUT_LPC1		GPP_A7 / PIRQA#		SD_RCOMP
BE		DDR1_DQ[63]		RSVD		GPD6 / SLP_A#		GPD2 / LAN_WAKE#														
BD	DDR1_DQSP[7]				RSVD		GPD0 / BATLOW#		GPD1 / ACPRESENT				GPP_B7 / SRCCLKREQ2#		GPP_B3 / CPU_GP2		GPP_B2 / VRALERT#		GPP_A23 / ISH_GP5		GPP_A19 / ISH_GP1	
BC		DDR1_DQ[62]		RSVD				GPD11 / LANPHYPC				GPP_B4 / CPU_GP3		GPP_B12 / SLP_S0#		GPP_B11 / EXT_P-WR_GATE#		GPP_B10 / SRCCLKREQ5#		GPP_B15 / GSPI0_CS#		EMMC_RCOMP
BB					RSVD		GPD7 / RSVD		RSVD		GPP_B1 / CORE_VID1		GPP_B5 / SRCCLKREQ0#		GPP_B13 / PLTRST#		GPP_B23 / SML1ALERT# / PCHHOT#		GPP_B18 / GSPI0_MOSI		GPP_B19 / GSPI1_CS#	
BA		RSVD		RSVD		RSVD_TP		GPD8 / SUSCLK		GPP_B0 / CORE_VID0												
AY	TP6		RSVD		RSVD_TP				GPD4 / SLP_S3#													
AW											GPP_B20 / GSPI1_CLK		GPP_B16 / GSPI0_CLK		GPP_B22 / GSPI1_MOSI		GPP_B17 / GSPI0_MISO		GPP_B21 / GSPI1_MISO		VCCPGPPB	
AV	VCCHDA				DCPRTC			VCCSPI		SPI0_IO3		SPI0_IO2		GPP_B6 / SRCCLKREQ1#		GPP_B9 / SRCCLKREQ4#		GPP_B8 / SRCCLKREQ3#		GPP_B14 / SPKR		VCCPGPPB
AU											SPI0_MISO		SPI0_CLK		SPI0_CS2#		SPI0_CS1#		SPI0_CS0#		VCCPGPPA	
AT		VCCPRIM_1P0		VCCRTC	DCPRTC		VCCPRIM_CORE	VCCSPI		GPP_F1 / I2S2_SFRM		GPP_F0 / I2S2_SCLK		GPP_F11/ I2C5_SCL / ISH_I2C2_SCL		GPP_F7 / I2C3_SCL		GPP_F3 / I2S2_RXD		SPI0_MOSI		VCCPGPPA
AR		VCCPRIM_1P0		VCCRTC			VCCPRIM_CORE															
AP										VCCPGPPG		GPP_F2 / I2S2_TXD		GPP_F14 / EMMC_DATA1		GPP_F5 / I2C2_SCL		GPP_F6 / I2C3_SDA		GPP_F4 / I2C2_SDA		VCCPGPPF
AN								VCCPGPPG			GPP_F13 / EMMC_DATA0		GPP_F15 / EMMC_DATA2		GPP_F20 / EMMC_DATA7		GPP_F9 / I2C4_SCL		GPP_F8 / I2C4_SDA		VCCPGPPF	
AM										VCCDSW_3P3		GPP_F12 / EMMC_CMD		GPP_F17 / EMMC_DATA4		GPP_F10 / I2C5_SDA / ISH_I2C2_SDA		USB2P_2		USB2N_2		DCPDSW_1P0
AL				VCCRTCPRIM_3P3	VCCPRIM_1P0			VCCDSW_3P3			GPP_F18 / EMMC_DATA5		GPP_F21 / EMMC_RCLK		GPP_F22 / EMMC_CLK		USB2N_3		USB2P_3		DCPDSW_1P0	
AK		VCCPRIM_3P3		VCCRTCPRIM_3P3	VCCPRIM_1P0																	
AJ											GPP_F19 / EMMC_DATA6		GPP_F16 / EMMC_DATA3		GPP_F23		USB2N_1		USB2P_1		VCCPGPPC	

Figure 9-10. Y-Processor Ball Map (Lower Left, Columns 64-44)



	64	63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48	47	46	45	44
AH	VDDQ		DDR0_DQ[4]#		DDR0_DQ[1]#		DDR1_DQ[10]# / DDR0_DQ[26]		DDR1_DQ[11] / DDR0_DQ[27]#												
AG		DDR0_DQ[5]#		DDR0_DQ[0]#				DDR1_DQ[15]# / DDR0_DQ[31]		DDR1_DQ[14] / DDR0_DQ[30]#		VCCGT									
AF														VCCGT	VCCGT	VCCGT		VCCGT	VCCGT		VCCGT
AE		VCCGT		VCCGT		VCCGT		VCCGT		VCCGT		VCCGT									
AD	VCCGT		VCCGT		VCCGT		VCCGT		VCCGT		VCCGT										
AC		VCCGT		VCCGT		VCCGT		VCCGT		VCCGT		VCCGT		VCCGT	VCCGT	VCCGT		VCCGT	VCCGT		VCCGT
AB	VCCGT		VCCGT		VCCGT		VCCGT		VCCGT		VCCGT										
AA												VCCGT									
Y	VCCGT		VCCGT		VCCGT		VCCGT		VCCGT		VCCGT			VCCGT	VCCGT	VCCGT		VCCGT	VCCGT		VCCGT
W		VCCGT		VCCGT		VCCGT		VCCGT		VCCGT		VCCGT									
V	VCCGT		VCCGT		VCCGT		VCCGT		VCCGT		VCCGT										
U		VCCGT		VCCGT		VCCGT		VCCGT		VCCGT		VCCGT									
T											VCCGT			VCCGT	VCCGT	VCCGT		VCCGT	VCCGT		VCCGT
R		VCC		VCC		VCC		VCC				VCCGT		VCCGT							
P	VCC		VCC		VCC		VCC		VCC				VSSGT_SENSE								
N		VCC		VCC		VCC		VCC		VCC	VCC		VCCGT_SENSE		VCCGT		VCCGT		VCCGT		VCCGT
M	VCC		VCC		VCC		VCC		VCC			VCC		VCC		VCC		VCC		VCC	
L		VCC									VCC		VCC		VCC		VCC		VCC		VCC
K																					
J	VCC				CFG[12]		CFG[13]		CFG[19]		CFG[16]		CFG[2]		BPM#[1]		PROCHOT#		EDP_TXN[2]		EDP_TXN[1]
H		VCC		CFG[14]		CFG[15]				CFG[4]		CFG[3]		BPM#[0]		CATERR#		THERMTRIP#		EDP_TXN[0]	
G							CFG[9]		CFG[18]		CFG[17]		CFG[0]		BPM#[3]		PROC_TDO		EDP_TXP[2]		EDP_TXP[1]
F	VCC			CFG[11]						CFG[7]		CFG[1]		BPM#[2]		PECI		PROC_TRST#		EDP_TXP[0]	
E																					
D	VCC			CFG[8]				CFG[10]		CFG[5]		PROC_TCK		PROC_PRDY#		RSVD		DDI1_TXP[3]		DDI1_TXP[2]	
C						PROC_TMS			CFG[6]		PROC_TDI		PCH_TRST#		PCH_JTAG_TDI		DDI1_TXN[1]		DDI1_TXP[0]		DDI2_TXP[1]
B	VCC		SKTOCC#	VCCST_PWRGD			VIDALERT#			PROC_PREQ#		PCH_JTAG_TCK		PCH_JTAG_TDO		JTAGX		DDI1_TXN[3]		DDI1_TXN[2]	
A	VCC		PROCPWRGD		ITP_PMODE		VIDSOUT		VIDSCK		CFG_RCOMP		PCH_JTAG_TMS		eDP_RCOMP		DDI1_TXP[1]		DDI1_TXN[0]		DDI2_TXN[1]

Figure 9-11. Y-Processor Ball Map (Lower Middle, Columns 43-23)



	43	42	41	40	39	38	37	36	35	34	33	32	31	30	29	28	27	26	25	24	23
AH			VCC			VCCG1			VCCG1			VCC			VCCSA			VCCIO			
AG																					
AF	VCCGT		VCC			VCCG1			VCCG1			VCC		VCCSA	VCCSA		VCCPLL_OC	VCCIO		VCCIO	
AE			VCC	VCC		VCC		VCC	VCC		VCC	VCC			VCCSA		VCCPLL_OC	VCCIO		VCCIO	VCCIO
AD																					
AC	VCCGT		VCC			VCCG0			VCCG0			VCC		VCCSA	VCCSA			VCCSTG		VCCIO	VCCIO
AB																					
AA			VCC			VCCG0			VCCG0			VCC			VCCSA			VCCSTG			VCCSRAM_1P0
Y	VCCGT		VCC			VCCG0			VCCG0			VCC		VCCSA	VCCSA			VCCST			VCCCLK3
W																					
V			VCC			VCCG0			VCCG0			VCC			VCCSA			VCCST			VCCCLK3
U																					
T	VCCGT		VCC			VCCG0			VCCG0			VCC		VCCSA	VCCSA		VCCPLL	VCCSTG			
R			VCC			VCCG0			VCCG0			VCC			VCCSA		VCCPLL	VCCSTG			VCCCLK5
P																					
N		VCC		VCC		VCC		VCC		VCC		VCC		VCCSA		VSSSA_SENSE					
M	VCC		VCC		VCC		VCC		VCC		VCC		VCCSA		VCCSA_SENSE		RSVD		RSVD		RSVD
L		VCC		VCC		RSVD		RSVD		VCC_SENSE		VSS_SENSE		VCCSA		RSVD		RSVD		RSVD	
K																					
J		EDP_AUXN		DDI2_AUXN		CLKOUT_PCIE_N3		CLKOUT_PCIE_N2		CLKOUT_ITPXDP_N		CSI2_DN3		CSI2_DN2		PCIE9_TXP		PCIE7_TXP / SATA0_TXP		PCIE5_TXP	
H	EDP_TXN[3]		DDI1_AUXN		CLKOUT_PCIE_N5		CLKOUT_PCIE_N4		CLKOUT_PCIE_N1		CSI2_DP1		CSI2_CLKN0		CSI2_DN0		PCIE10_TXP		PCIE8_TXP / SATA1A_TXP		PCIE6_TXP
G		EDP_AUXP		DDI2_AUXP		CLKOUT_PCIE_P3		CLKOUT_PCIE_P2		CLKOUT_ITPXDP_P		CSI2_DP3		CSI2_DP2		PCIE9_TXN		PCIE7_TXN / SATA0_TXN		PCIE5_TXN	
F	EDP_TXP[3]		DDI1_AUXP		CLKOUT_PCIE_P5		CLKOUT_PCIE_P4		CLKOUT_PCIE_P1		CSI2_DN1		CSI2_CLKP0		CSI2_DP0		PCIE10_TXN		PCIE8_TXN / SATA1A_TXN		PCIE6_TXN
E																					
D	DDI2_TXP[3]		DDI2_TXP[2]		CSI2_CLKN3		CSI2_DN10		CSI2_DN8		CSI2_DN7		CSI2_CLKN1		CSI2_DN4		PCIE10_RXP		PCIE8_RXP / SATA1A_RXP		PCIE6_RXP
C		DDI2_TXP[0]				CSI2_DN11		CSI2_DN9		CSI2_CLKN2		CSI2_DN5		CSI2_DN6		PCIE9_RXN		PCIE7_RXN / SATA0_RXN		PCIE5_RXN	
B	DDI2_TXN[3]		DDI2_TXN[2]		CSI2_CLKP3		CSI2_DP10		CSI2_DP8		CSI2_DP7		CSI2_CLKP1		CSI2_DP4		PCIE10_RXN		PCIE8_RXN / SATA1A_RXN		PCIE6_RXN
A		DDI2_TXN[0]		EDP_DISP_UTIL		CSI2_DP11		CSI2_DP9		CSI2_CLKP2		CSI2_DP5		CSI2_DP6		PCIE9_RXP		PCIE7_RXP / SATA0_RXP		PCIE5_RXP	

Figure 9-12. Y-Processor Ball Map (Lower Right, Columns 42-1)



	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
AH		VCCPRIM_3P3		VCCPRIM_1P0	VCCPRIM_1P0			VCCPRIM_1P0		VCCPRIM_1P0		GPP_G1 / SD_DATA0		GPP_G0 / SD_CMD		RSVD		USB2N_5		USB2P_5		VCCPGPPC
AG											GPP_G2 / SD_DATA1		GPP_G6 / SD_CLK		GPP_G5 / SD_CD#		USB2N_9		USB2P_9		VCCPGPPD	
AF				VCCPRIM_CORE	VCCPRIM_CORE							GPP_G4 / SD_DATA3		GPP_G3 / SD_DATA2		USB2_ID		USB2N_7		USB2P_7		VCCPGPPD
AE				VCCPRIM_CORE	VCCPRIM_CORE		VCCATS	VCCATS			GPP_G7 / SD_WP						USB2_VBUSSENSE					
AD												GPP_C16 / I2C0_SDA		GPP_C23 / UART2_CTS#		GPP_C21 / UART2_TXD		GPP_C20 / UART2_RXD		GPP_C22 / UART2_RTS#		VCCPRIM_3P3
AC											GPP_C0 / SMBCLK		GPP_C4 / SML0DATA		GPP_C8 / UART0_RXD		GPP_C12 / UART1_RXD / ISH_UART1_RXD		GPP_C13 / UART1_TXD / ISH_UART1_TXD		VCCPRIM_3P3	
AB												GPP_C19 / I2C1_SCL		GPP_C18 / I2C1_SDA		GPP_C14 / UART1_RTS# / ISH_UART1_RTS#		GPP_C15 / UART1_CTS# / ISH_UART1_CTS#		GPP_C17 / I2C0_SCL		VCCPGPPE
AA		VCCSRAM_1P0		VCCAPLL_1P0	VCCAPLL_1P0		VCCPRIM_1P0	VCCPRIM_1P0			GPP_C11 / UART0_CTS#		GPP_C10 / UART0_RTS#		GPP_C9 / UART0_TXD		GPP_C5 / SML0ALERT#		GPP_C6 / SML1CLK		VCCPGPPE	
Y		VCCCLK4		VCCCLK2	VCCCLK1																	
W											GPP_D21		GPP_C7 / SML1DATA		GPP_C2 / SMBALERT#		GPP_C1 / SMBDATA		GPP_C3 / SML0CLK		VCCMPHYAON_1P0	
V		VCCCLK4		VCCCLK2	VCCCLK1		VCCAM-PHYPLL_1P0	VCCAM-PHYPLL_1P0				GPP_D20 / DMIC_DATA0		GPP_D16 / ISH_UART0_CTS# / SML0ALERT#		GPP_D22		GPP_D23 / I2S_MCLK		GPP_D19 / DMIC_CLK0		VCCMPHYAON_1P0
U											GPP_D17 / DMIC_CLK1		GPP_D13 / ISH_UART0_RXD / SML0BDATA		GPP_D18 / DMIC_DATA1		GPP_D15 / ISH_UART0_RTS#		GPP_D14 / ISH_UART0_TXD / SML0BCLK		VCCMPHYGT_1P0	
T				VCCCLK6			VCCMPHYGT_1P0	VCCMPHYGT_1P0				GPP_D12		GPP_D7 / ISH_I2C1_SDA		GPP_D10		GPP_D11		GPP_D8 / ISH_I2C1_SCL		VCCMPHYGT_1P0
R		VCCCLK5		VCCCLK6			VCCAPLLEBB_1P0	VCCAPLLEBB_1P0			RSVD											
P										RSVD		GPP_D9		GPP_D1		GPP_D5 / ISH_I2C0_SDA		GPP_D6 / ISH_I2C0_SCL		GPP_D3		XCLK_BIASREF
N											GPP_E9 / USB2_OC0#		GPP_E2 / SATAXPCIE2 / SATAGP2		GPP_D2		GPP_D0		GPP_D4 / FLASHTRIG		USB2_COMP	
M		RSVD		RSVD		RSVD		RSVD				GPP_E10 / USB2_OC1#		GPP_E7 / CPU_GP1		GPP_E15 / DDPD_HPD2		GPP_E22				XTAL24_IN
L	RSVD		RSVD		RSVD		RSVD						GPP_E14 / DDPC_HPD1		GPP_E6 / DEVSLP2		GPP_E18 / DDPB_CTRLCLK		GPP_E23		XTAL24_OUT	
K											RSVD											
J	PCIE3_TXP		PCIE1_TXP / USB3_5_TXP		USB3_3_TXP		USB3_1_TXP					GPP_E1 / SATAXPCIE1 / SATAGP1										SYS_PWROK
H		PCIE4_TXP		PCIE2_TXP / USB3_6_TXP		USB3_4_TXP		USB3_2_TXP / SSIC_TXP			RSVD		GPP_E5 / DEVSLP1		GPP_E8 / SATALED#		GPP_E19 / DDPB_CTRLDATA		GPP_E20 / DDPC_CTRLCLK		SYS_RESET#	
G	PCIE3_TXN		PCIE1_TXN / USB3_5_TXN		USB3_3_TXN		USB3_1_TXN					GPP_E0 / SATAXPCIE0 / SATAGP0										
F		PCIE4_TXN		PCIE2_TXN / USB3_6_TXN		USB3_4_TXN		USB3_2_TXN / SSIC_TXN			CL_CLK		GPP_E4 / DEVSLP0		GPP_E11 / USB2_OC2#		GPP_E16 / DDPE_HPD3		GPP_E21 / DDPC_CTRLDATA	RSVD		RSVD
E												GPP_E3 / CPU_GP0										
D		PCIE4_RXP		PCIE2_RXP / USB3_6_RXP		USB3_4_RXP		USB3_2_RXP / SSIC_RXP			CL_DATA								eDP_BKLEN	eDP_VDDEN		
C	PCIE3_RXN		PCIE1_RXN / USB3_5_RXN		USB3_3_RXN		USB3_1_RXN					GPP_E13 / DDPB_HPD0										
B		PCIE4_RXN		PCIE2_RXN / USB3_6_RXN		USB3_4_RXN		USB3_2_RXN / SSIC_RXN			CL_RST#		PCIE_RCOMPP		GPP_E12 / USB2_OC3#		eDP_BKLCTL		RSVD	RSVD		
A	PCIE3_RXP		PCIE1_RXP / USB3_5_RXP		USB3_3_RXP		USB3_1_RXP					CSI2_COMP		PCIE_RCOMPN		GPP_E17 / EDP_HPD						

Table 9-2. Y-Processor Ball List (Sheet 1 of 40)

Ball #	Ball Name	LPDDR3	Interleaved (IL)	Non-Interleaved (NIL)	X [um]	Y [um]
A11	CSI2_COMP				6763.51	-7541.01
A14	VSS				6119.37	-7541.01
A16	USB3_1_RXP				5475.22	-7541.01
A18	USB3_3_RXP				4831.08	-7541.01
A20	PCIE1_RXP / USB3_5_RXP				4186.94	-7541.01
A22	PCIE3_RXP				3542.79	-7541.01
A24	PCIE5_RXP				2898.65	-7541.01
A26	PCIE7_RXP / SATA0_RXP				2254.5	-7541.01
A28	PCIE9_RXP				1610.36	-7541.01
A30	CSI2_DP6				966.22	-7541.01
A32	CSI2_DP5				322.07	-7541.01
A34	CSI2_CLKP2				-322.07	-7541.01
A36	CSI2_DP9				-966.22	-7541.01
A38	CSI2_DP11				-1610.36	-7541.01
A40	EDP_DISP_UTIL				-2254.5	-7541.01
A42	DDI2_TXN[0]				-2898.65	-7541.01
A44	DDI2_TXN[1]				-3542.79	-7541.01
A46	DDI1_TXN[0]				-4186.94	-7541.01
A48	DDI1_TXP[1]				-4831.08	-7541.01
A5	VSS				8401.05	-7541.01
A50	eDP_RCOMP				-5475.22	-7541.01
A52	PCH_JTAG_TMS				-6119.37	-7541.01
A54	CFG_RCOMP				-6763.51	-7541.01
A56	VIDSCK				-7407.66	-7541.01
A58	VIDSOUT				-7953.09	-7541.01
A60	ITP_PMODE				-8401.05	-7541.01
A62	PROCPWRGD				-8855.71	-7541.01
A64	VCC				-9310.37	-7541.01
A7	GPP_E17 / EDP_HPD				7946.39	-7541.01
A9	PCIE_RCOMPN				7407.66	-7541.01
AA10	GPP_C10 / UART0_RTS#				7067.55	-1932.43
AA12	GPP_C11 / UART0_CTS#				6574.79	-1932.43
AA15	VCCPRIM_1P0				5846.1	-1869.71
AA16	VCCPRIM_1P0				5350.8	-1869.71
AA18	VCCAPLL_1P0				4855.5	-1869.71
AA19	VCCAPLL_1P0				4360.2	-1869.71
AA2	VCCPGPPE				9038.59	-1932.43
AA21	VCCSRAM_1P0				3864.9	-1869.71
AA23	VCCSRAM_1P0				3369.6	-1869.71

Table 9-2. Y-Processor Ball List (Sheet 2 of 40)

Ball #	Ball Name	LPDDR3	Interleaved (IL)	Non-Interleaved (NIL)	X [um]	Y [um]
AA24	VSS				2874.3	-1869.71
AA26	VCCSTG				2379	-1869.71
AA27	VSS				1883.7	-1869.71
AA29	VCCSA				1388.4	-1869.71
AA30	VSS				893.1	-1869.71
AA32	VCC				397.8	-1869.71
AA33	VSS				-97.5	-1869.71
AA35	VCCG0				-592.8	-1869.71
AA36	VSS				-1088.1	-1869.71
AA38	VCCG0				-1583.4	-1869.71
AA4	GPP_C6 / SML1CLK				8545.83	-1932.43
AA40	VSS				-2078.7	-1869.71
AA41	VCC				-2574	-1869.71
AA43	VSS				-3069.3	-1869.71
AA44	VSS				-3564.6	-1869.71
AA46	VSS				-4059.9	-1869.71
AA47	VSS				-4555.2	-1869.71
AA49	VSS				-5050.5	-1869.71
AA50	VSS				-5545.8	-1869.71
AA51	VSS				-6041.1	-1869.71
AA53	VCCGT				-6574.79	-1932.43
AA55	VSS				-7067.55	-1932.43
AA57	VSS				-7560.31	-1932.43
AA59	VSS				-8053.07	-1932.43
AA6	GPP_C5 / SML0ALERT#				8053.07	-1932.43
AA61	VSS				-8545.83	-1932.43
AA63	VSS				-9038.59	-1932.43
AA8	GPP_C9 / UART0_TXD				7560.31	-1932.43
AB1	VCCPGPPE				9310.37	-1610.36
AB11	GPP_C19 / I2C1_SCL				6821.17	-1610.36
AB13	VSS				6328.41	-1605.28
AB3	GPP_C17 / I2C0_SCL				8792.21	-1610.36
AB5	GPP_C15 / UART1_CTS# / ISH_UART1_CTS#				8299.45	-1610.36
AB54	VCCGT				-6821.17	-1610.36
AB56	VCCGT				-7313.93	-1610.36
AB58	VCCGT				-7806.69	-1610.36
AB60	VCCGT				-8299.45	-1610.36
AB62	VCCGT				-8792.21	-1610.36

Table 9-2. Y-Processor Ball List (Sheet 3 of 40)

Ball #	Ball Name	LPDDR3	Interleaved (IL)	Non-Interleaved (NIL)	X [um]	Y [um]
AB64	VCCGT				-9310.37	-1610.36
AB7	GPP_C14 / UART1_RTS# / ISH_UART1_RTS#				7806.69	-1610.36
AB9	GPP_C18 / I2C1_SDA				7313.93	-1610.36
AC10	GPP_C4 / SML0DATA				7067.55	-1288.29
AC12	GPP_C0 / SMBCLK				6574.79	-1288.29
AC15	VSS				5846.1	-1310.91
AC16	VSS				5350.8	-1310.91
AC18	VSS				4855.5	-1310.91
AC19	VSS				4360.2	-1310.91
AC2	VCCPRIM_3P3				9038.59	-1288.29
AC21	VSS				3864.9	-1310.91
AC23	VCCIO				3369.6	-1310.91
AC24	VCCIO				2874.3	-1310.91
AC26	VCCSTG				2379	-1310.91
AC27	VSS				1883.7	-1310.91
AC29	VCCSA				1388.4	-1310.91
AC30	VCCSA				893.1	-1310.91
AC32	VCC				397.8	-1310.91
AC33	VSS				-97.5	-1310.91
AC35	VCCG0				-592.8	-1310.91
AC36	VSS				-1088.1	-1310.91
AC38	VCCG0				-1583.4	-1310.91
AC4	GPP_C13 / UART1_TXD / ISH_UART1_TXD				8545.83	-1288.29
AC40	VSS				-2078.7	-1310.91
AC41	VCC				-2574	-1310.91
AC43	VCCGT				-3069.3	-1310.91
AC44	VCCGT				-3564.6	-1310.91
AC46	VCCGT				-4059.9	-1310.91
AC47	VCCGT				-4555.2	-1310.91
AC49	VCCGT				-5050.5	-1310.91
AC50	VCCGT				-5545.8	-1310.91
AC51	VCCGT				-6041.1	-1310.91
AC53	VCCGT				-6574.79	-1288.29
AC55	VCCGT				-7067.55	-1288.29
AC57	VCCGT				-7560.31	-1288.29
AC59	VCCGT				-8053.07	-1288.29
AC6	GPP_C12 / UART1_RXD / ISH_UART1_RXD				8053.07	-1288.29
AC61	VCCGT				-8545.83	-1288.29

Table 9-2. Y-Processor Ball List (Sheet 4 of 40)

Ball #	Ball Name	LPDDR3	Interleaved (IL)	Non-Interleaved (NIL)	X [um]	Y [um]
AC63	VCCGT				-9038.59	-1288.29
AC8	GPP_C8 / UART0_RXD				7560.31	-1288.29
AD1	VCCPRIM_3P3				9310.37	-966.22
AD11	GPP_C16 / I2C0_SDA				6821.17	-966.22
AD13	VSS				6328.41	-961.14
AD3	GPP_C22 / UART2_RTS#				8792.21	-966.22
AD5	GPP_C20 / UART2_RXD				8299.45	-966.22
AD54	VCCGT				-6821.17	-966.22
AD56	VCCGT				-7313.93	-966.22
AD58	VCCGT				-7806.69	-966.22
AD60	VCCGT				-8299.45	-966.22
AD62	VCCGT				-8792.21	-966.22
AD64	VCCGT				-9310.37	-966.22
AD7	GPP_C21 / UART2_TXD				7806.69	-966.22
AD9	GPP_C23 / UART2_CTS#				7313.93	-966.22
AE10	VSS				7067.55	-644.14
AE12	GPP_G7 / SD_WP				6574.79	-644.14
AE15	VCCATS				5846.1	-752.11
AE16	VCCATS				5350.8	-752.11
AE18	VCCPRIM_CORE				4855.5	-752.11
AE19	VCCPRIM_CORE				4360.2	-752.11
AE2	VSS				9038.59	-644.14
AE21	VSS				3864.9	-752.11
AE23	VCCIO				3369.6	-752.11
AE24	VCCIO				2874.3	-752.11
AE26	VCCIO				2379	-752.11
AE27	VCCPLL_OC				1883.7	-752.11
AE29	VCCSA				1388.4	-752.11
AE30	VSS				893.1	-752.11
AE32	VCC				397.8	-752.11
AE33	VCC				-97.5	-752.11
AE35	VCC				-592.8	-752.11
AE36	VCC				-1088.1	-752.11
AE38	VCC				-1583.4	-752.11
AE4	VSS				8545.83	-644.14
AE40	VCC				-2078.7	-752.11
AE41	VCC				-2574	-752.11
AE43	VSS				-3069.3	-752.11
AE44	VSS				-3564.6	-752.11

Table 9-2. Y-Processor Ball List (Sheet 5 of 40)

Ball #	Ball Name	LPDDR3	Interleaved (IL)	Non-Interleaved (NIL)	X [um]	Y [um]
AE46	VSS				-4059.9	-752.11
AE47	VSS				-4555.2	-752.11
AE49	VSS				-5050.5	-752.11
AE50	VSS				-5545.8	-752.11
AE51	VSS				-6041.1	-752.11
AE53	VCCGT				-6574.79	-644.14
AE55	VCCGT				-7067.55	-644.14
AE57	VCCGT				-7560.31	-644.14
AE59	VCCGT				-8053.07	-644.14
AE6	USB2_VBUSSENSE				8053.07	-644.14
AE61	VCCGT				-8545.83	-644.14
AE63	VCCGT				-9038.59	-644.14
AE8	VSS				7560.31	-644.14
AF1	VCCPGPPD				9310.37	-322.07
AF11	GPP_G4 / SD_DATA3				6821.17	-322.07
AF13	VSS				6328.41	-316.99
AF15	VSS				5846.1	-193.31
AF16	VSS				5350.8	-193.31
AF18	VCCPRIM_CORE				4855.5	-193.31
AF19	VCCPRIM_CORE				4360.2	-193.31
AF21	VSS				3864.9	-193.31
AF23	VSS				3369.6	-193.31
AF24	VCCIO				2874.3	-193.31
AF26	VCCIO				2379	-193.31
AF27	VCCPLL_OC				1883.7	-193.31
AF29	VCCSA				1388.4	-193.31
AF3	USB2P_7				8792.21	-322.07
AF30	VCCSA				893.1	-193.31
AF32	VCC				397.8	-193.31
AF33	VSS				-97.5	-193.31
AF35	VCCG1				-592.8	-193.31
AF36	VSS				-1088.1	-193.31
AF38	VCCG1				-1583.4	-193.31
AF40	VSS				-2078.7	-193.31
AF41	VCC				-2574	-193.31
AF43	VCCGT				-3069.3	-193.31
AF44	VCCGT				-3564.6	-193.31
AF46	VCCGT				-4059.9	-193.31
AF47	VCCGT				-4555.2	-193.31

Table 9-2. Y-Processor Ball List (Sheet 6 of 40)

Ball #	Ball Name	LPDDR3	Interleaved (IL)	Non-Interleaved (NIL)	X [um]	Y [um]
AF49	VCCGT				-5050.5	-193.31
AF5	USB2N_7				8299.45	-322.07
AF50	VCCGT				-5545.8	-193.31
AF51	VCCGT				-6041.1	-193.31
AF54	VSS				-6821.17	-322.07
AF56	VSS				-7313.93	-322.07
AF58	VSS				-7806.69	-322.07
AF60	VSS				-8299.45	-322.07
AF62	VSS				-8792.21	-322.07
AF64	VSS				-9310.37	-322.07
AF7	USB2_ID				7806.69	-322.07
AF9	GPP_G3 / SD_DATA2				7313.93	-322.07
AG10	GPP_G6 / SD_CLK				7067.55	0
AG12	GPP_G2 / SD_DATA1				6574.79	0
AG2	VCCPGPPD				9038.59	0
AG4	USB2P_9				8545.83	0
AG53	VCCGT				-6574.79	0
AG55	DDR1_DQ[14] / DDR0_DQ[30]		DDR1_DQ[14]	DDR0_DQ[30]	-7067.55	0
AG57	DDR1_DQ[15] / DDR0_DQ[31]		DDR1_DQ[15]	DDR0_DQ[31]	-7560.31	0
AG59	VSS				-8053.07	0
AG6	USB2N_9				8053.07	0
AG61	DDR0_DQ[0]				-8545.83	0
AG63	DDR0_DQ[5]				-9038.59	0
AG8	GPP_G5 / SD_CD#				7560.31	0
AH1	VCCPGPPC				9310.37	322.07
AH11	GPP_G1 / SD_DATA0				6821.17	322.07
AH13	VCCPRIM_1P0				6328.41	327.15
AH15	VCCPRIM_1P0				5846.1	365.49
AH16	VSS				5350.8	365.49
AH18	VCCPRIM_1P0				4855.5	365.49
AH19	VCCPRIM_1P0				4360.2	365.49
AH21	VCCPRIM_3P3				3864.9	365.49
AH23	VSS				3369.6	365.49
AH24	VSS				2874.3	365.49
AH26	VCCIO				2379	365.49
AH27	VSS				1883.7	365.49
AH29	VCCSA				1388.4	365.49
AH3	USB2P_5				8792.21	322.07
AH30	VSS				893.1	365.49

Table 9-2. Y-Processor Ball List (Sheet 7 of 40)

Ball #	Ball Name	LPDDR3	Interleaved (IL)	Non-Interleaved (NIL)	X [um]	Y [um]
AH32	VCC				397.8	365.49
AH33	VSS				-97.5	365.49
AH35	VCCG1				-592.8	365.49
AH36	VSS				-1088.1	365.49
AH38	VCCG1				-1583.4	365.49
AH40	VSS				-2078.7	365.49
AH41	VCC				-2574	365.49
AH43	VSS				-3069.3	365.49
AH44	VSS				-3564.6	365.49
AH46	VSS				-4059.9	365.49
AH47	VSS				-4555.2	365.49
AH49	VSS				-5050.5	365.49
AH5	USB2N_5				8299.45	322.07
AH50	VSS				-5545.8	365.49
AH51	VSS				-6041.1	365.49
AH54	VSS				-6821.17	322.07
AH56	DDR1_DQ[11] / DDR0_DQ[27]		DDR1_DQ[11]	DDR0_DQ[27]	-7313.93	322.07
AH58	DDR1_DQ[10] / DDR0_DQ[26]		DDR1_DQ[10]	DDR0_DQ[26]	-7806.69	322.07
AH60	DDR0_DQ[1]				-8299.45	322.07
AH62	DDR0_DQ[4]				-8792.21	322.07
AH64	VDDQ				-9310.37	322.07
AH7	RSVD				7806.69	322.07
AH9	GPP_G0 / SD_CMD				7313.93	322.07
AJ10	GPP_F16 / EMMC_DATA3				7067.55	644.14
AJ12	GPP_F19 / EMMC_DATA6				6574.79	644.14
AJ2	VCCPGPPC				9038.59	644.14
AJ4	USB2P_1				8545.83	644.14
AJ53	VCCGT				-6574.79	644.14
AJ55	DDR1_DQSP[1] / DDR0_DQSP[3]		DDR1_DQSP[1]	DDR0_DQSP[3]	-7067.55	644.14
AJ57	DDR1_DQSN[1] / DDR0_DQSN[3]		DDR1_DQSN[1]	DDR0_DQSN[3]	-7560.31	644.14
AJ59	VSS				-8053.07	644.14
AJ6	USB2N_1				8053.07	644.14
AJ61	DDR0_DQSN[0]				-8545.83	644.14
AJ63	DDR0_DQSP[0]				-9038.59	644.14
AJ8	GPP_F23				7560.31	644.14
AK1	VSS				9310.37	966.22
AK11	VSS				6821.17	966.22
AK13	VSS				6328.41	971.3
AK15	VSS				5846.1	924.29

Table 9-2. Y-Processor Ball List (Sheet 8 of 40)

Ball #	Ball Name	LPDDR3	Interleaved (IL)	Non-Interleaved (NIL)	X [um]	Y [um]
AK16	VSS				5350.8	924.29
AK18	VCCPRIM_1P0				4855.5	924.29
AK19	VCCRTCPRIM_3P3				4360.2	924.29
AK21	VCCPRIM_3P3				3864.9	924.29
AK23	VCCSRAM_1P0				3369.6	924.29
AK24	VSS				2874.3	924.29
AK26	VCCIO				2379	924.29
AK27	VSS				1883.7	924.29
AK29	VCCSA				1388.4	924.29
AK3	VSS				8792.21	966.22
AK30	VCCSA				893.1	924.29
AK32	VCC				397.8	924.29
AK33	VSS				-97.5	924.29
AK35	VCCG1				-592.8	924.29
AK36	VSS				-1088.1	924.29
AK38	VCCG1				-1583.4	924.29
AK40	VSS				-2078.7	924.29
AK41	VCC				-2574	924.29
AK43	VCCGT				-3069.3	924.29
AK44	VCCGT				-3564.6	924.29
AK46	VCCGT				-4059.9	924.29
AK47	VCCGT				-4555.2	924.29
AK49	VCCGT				-5050.5	924.29
AK5	VSS				8299.45	966.22
AK50	VCCGT				-5545.8	924.29
AK51	VCCGT				-6041.1	924.29
AK54	VSS				-6821.17	966.22
AK56	DDR1_DQ[13] / DDR0_DQ[29]		DDR1_DQ[13]	DDR0_DQ[29]	-7313.93	966.22
AK58	DDR1_DQ[12] / DDR0_DQ[28]		DDR1_DQ[12]	DDR0_DQ[28]	-7806.69	966.22
AK60	DDR0_DQ[3]				-8299.45	966.22
AK62	DDR0_DQ[2]				-8792.21	966.22
AK64	VDDQ				-9310.37	966.22
AK7	VSS				7806.69	966.22
AK9	VSS				7313.93	966.22
AL10	GPP_F21 / EMMC_RCLK				7067.55	1288.29
AL12	GPP_F18 / EMMC_DATA5				6574.79	1288.29
AL15	VCCDSW_3P3				5846.1	1483.09
AL16	VSS				5350.8	1483.09
AL18	VCCPRIM_1P0				4855.5	1483.09

Table 9-2. Y-Processor Ball List (Sheet 9 of 40)

Ball #	Ball Name	LPDDR3	Interleaved (IL)	Non-Interleaved (NIL)	X [um]	Y [um]
AL19	VCCRTCPRIM_3P3				4360.2	1483.09
AL2	DCPDSW_1P0				9038.59	1288.29
AL21	VSS				3864.9	1483.09
AL23	VCCSRAM_1P0				3369.6	1483.09
AL24	VSS				2874.3	1483.09
AL26	VCCIO				2379	1483.09
AL27	VSS				1883.7	1483.09
AL29	VCCSA				1388.4	1483.09
AL30	VSS				893.1	1483.09
AL32	VCC				397.8	1483.09
AL33	VSS				-97.5	1483.09
AL35	VCCG1				-592.8	1483.09
AL36	VSS				-1088.1	1483.09
AL38	VCCG1				-1583.4	1483.09
AL4	USB2P_3				8545.83	1288.29
AL40	VSS				-2078.7	1483.09
AL41	VCC				-2574	1483.09
AL43	VSS				-3069.3	1483.09
AL44	VSS				-3564.6	1483.09
AL46	VSS				-4059.9	1483.09
AL47	VSS				-4555.2	1483.09
AL49	VSS				-5050.5	1483.09
AL50	VSS				-5545.8	1483.09
AL51	VSS				-6041.1	1483.09
AL53	VSS				-6574.79	1288.29
AL55	DDR1_DQ[8] / DDR0_DQ[24]		DDR1_DQ[8]	DDR0_DQ[24]	-7067.55	1288.29
AL57	DDR1_DQ[9] / DDR0_DQ[25]		DDR1_DQ[9]	DDR0_DQ[25]	-7560.31	1288.29
AL59	VSS				-8053.07	1288.29
AL6	USB2N_3				8053.07	1288.29
AL61	DDR0_DQ[6]				-8545.83	1288.29
AL63	DDR0_DQ[7]				-9038.59	1288.29
AL8	GPP_F22 / EMMC_CLK				7560.31	1288.29
AM1	DCPDSW_1P0				9310.37	1610.36
AM11	GPP_F12 / EMMC_CMD				6821.17	1610.36
AM13	VCCDSW_3P3				6328.41	1615.44
AM3	USB2N_2				8792.21	1610.36
AM5	USB2P_2				8299.45	1610.36
AM54	VSS				-6821.17	1610.36
AM56	DDR1_DQ[7] / DDR0_DQ[23]		DDR1_DQ[7]	DDR0_DQ[23]	-7313.93	1610.36

Table 9-2. Y-Processor Ball List (Sheet 10 of 40)

Ball #	Ball Name	LPDDR3	Interleaved (IL)	Non-Interleaved (NIL)	X [um]	Y [um]
AM58	DDR1_DQ[6] / DDR0_DQ[22]		DDR1_DQ[6]	DDR0_DQ[22]	-7806.69	1610.36
AM60	DDR0_DQ[8]				-8299.45	1610.36
AM62	DDR0_DQ[9]				-8792.21	1610.36
AM64	VSS				-9310.37	1610.36
AM7	GPP_F10 / I2C5_SDA / ISH_I2C2_SDA				7806.69	1610.36
AM9	GPP_F17 / EMMC_DATA4				7313.93	1610.36
AN10	GPP_F15 / EMMC_DATA2				7067.55	1932.43
AN12	GPP_F13 / EMMC_DATA0				6574.79	1932.43
AN15	VCCPGPPG				5846.1	2041.89
AN16	VSS				5350.8	2041.89
AN18	VSS				4855.5	2041.89
AN19	VSS				4360.2	2041.89
AN2	VCCPGPPF				9038.59	1932.43
AN21	VSS				3864.9	2041.89
AN23	VCCSRAM_1P0				3369.6	2041.89
AN24	VSS				2874.3	2041.89
AN26	VCCIO				2379	2041.89
AN27	VSS				1883.7	2041.89
AN29	VCCSA				1388.4	2041.89
AN30	VCCSA				893.1	2041.89
AN32	VCC				397.8	2041.89
AN33	VSS				-97.5	2041.89
AN35	VCCG1				-592.8	2041.89
AN36	VSS				-1088.1	2041.89
AN38	VCCG1				-1583.4	2041.89
AN4	GPP_F8 / I2C4_SDA				8545.83	1932.43
AN40	VSS				-2078.7	2041.89
AN41	VCC				-2574	2041.89
AN43	VCCGT				-3069.3	2041.89
AN44	VCCGT				-3564.6	2041.89
AN46	VCCGT				-4059.9	2041.89
AN47	VCCGT				-4555.2	2041.89
AN49	VCCGT				-5050.5	2041.89
AN50	VCCGT				-5545.8	2041.89
AN51	VCCGT				-6041.1	2041.89
AN53	DDR0_VREF_DQ				-6574.79	1932.43
AN55	DDR1_DQ[3] / DDR0_DQ[19]		DDR1_DQ[3]	DDR0_DQ[19]	-7067.55	1932.43
AN57	DDR1_DQ[2] / DDR0_DQ[18]		DDR1_DQ[2]	DDR0_DQ[18]	-7560.31	1932.43
AN59	VSS				-8053.07	1932.43

Table 9-2. Y-Processor Ball List (Sheet 11 of 40)

Ball #	Ball Name	LPDDR3	Interleaved (IL)	Non-Interleaved (NIL)	X [um]	Y [um]
AN6	GPP_F9 / I2C4_SCL				8053.07	1932.43
AN61	DDR0_DQ[12]				-8545.83	1932.43
AN63	DDR0_DQ[13]				-9038.59	1932.43
AN8	GPP_F20 / EMMC_DATA7				7560.31	1932.43
AP1	VCCPGPPF				9310.37	2254.5
AP11	GPP_F2 / I2S2_TXD				6821.17	2254.5
AP13	VCCPGPPG				6328.41	2259.58
AP3	GPP_F4 / I2C2_SDA				8792.21	2254.5
AP5	GPP_F6 / I2C3_SDA				8299.45	2254.5
AP54	VSS				-6821.17	2254.5
AP56	DDR1_DQSN[0] / DDR0_DQSN[2]		DDR1_DQSN[0]	DDR0_DQSN[2]	-7313.93	2254.5
AP58	DDR1_DQSP[0] / DDR0_DQSP[2]		DDR1_DQSP[0]	DDR0_DQSP[2]	-7806.69	2254.5
AP60	DDR0_DQSP[1]				-8299.45	2254.5
AP62	DDR0_DQSN[1]				-8792.21	2254.5
AP64	VSS				-9310.37	2254.5
AP7	GPP_F5 / I2C2_SCL				7806.69	2254.5
AP9	GPP_F14 / EMMC_DATA1				7313.93	2254.5
AR10	VSS				7067.55	2576.58
AR12	VSS				6574.79	2576.58
AR15	VSS				5846.1	2600.69
AR16	VCCPRIM_CORE				5350.8	2600.69
AR18	VSS				4855.5	2600.69
AR19	VCCRTC				4360.2	2600.69
AR2	VSS				9038.59	2576.58
AR21	VCCPRIM_1P0				3864.9	2600.69
AR23	VCCSRAM_1P0				3369.6	2600.69
AR24	VSSIO_SENSE				2874.3	2600.69
AR26	VCCIO				2379	2600.69
AR27	VSS				1883.7	2600.69
AR29	VCCSA				1388.4	2600.69
AR30	VSS				893.1	2600.69
AR32	VCC				397.8	2600.69
AR33	VSS				-97.5	2600.69
AR35	VCCG1				-592.8	2600.69
AR36	VSS				-1088.1	2600.69
AR38	VCCG1				-1583.4	2600.69
AR4	VSS				8545.83	2576.58
AR40	VSS				-2078.7	2600.69
AR41	VCC				-2574	2600.69

Table 9-2. Y-Processor Ball List (Sheet 12 of 40)

Ball #	Ball Name	LPDDR3	Interleaved (IL)	Non-Interleaved (NIL)	X [um]	Y [um]
AR43	VSS				-3069.3	2600.69
AR44	VSS				-3564.6	2600.69
AR46	VSS				-4059.9	2600.69
AR47	VSS				-4555.2	2600.69
AR49	VSS				-5050.5	2600.69
AR50	VSS				-5545.8	2600.69
AR51	VSS				-6041.1	2600.69
AR53	DDR_VREF_CA				-6574.79	2576.58
AR55	DDR1_DQ[1] / DDR0_DQ[17]		DDR1_DQ[1]	DDR0_DQ[17]	-7067.55	2576.58
AR57	DDR1_DQ[4] / DDR0_DQ[20]		DDR1_DQ[4]	DDR0_DQ[20]	-7560.31	2576.58
AR59	VSS				-8053.07	2576.58
AR6	VSS				8053.07	2576.58
AR61	DDR0_DQ[11]				-8545.83	2576.58
AR63	DDR0_DQ[14]				-9038.59	2576.58
AR8	VSS				7560.31	2576.58
AT1	VCCPGPPA				9310.37	2898.65
AT11	GPP_F0 / I2S2_SCLK				6821.17	2898.65
AT13	GPP_F1 / I2S2_SFRM				6328.41	2903.73
AT15	VCCSPI				5846.1	3159.49
AT16	VCCPRIM_CORE				5350.8	3159.49
AT18	DCPRTC				4855.5	3159.49
AT19	VCCRTC				4360.2	3159.49
AT21	VCCPRIM_1P0				3864.9	3159.49
AT23	VCCHDA				3369.6	3159.49
AT24	VCCIO_SENSE				2874.3	3159.49
AT26	VCCIO				2379	3159.49
AT27	VSS				1883.7	3159.49
AT29	VCCSA_DDR				1388.4	3159.49
AT3	SPI0_MOSI				8792.21	2898.65
AT30	VCCSA_DDR				893.1	3159.49
AT32	VCC				397.8	3159.49
AT33	VCC				-97.5	3159.49
AT35	VCC				-592.8	3159.49
AT36	VCC				-1088.1	3159.49
AT38	VCC				-1583.4	3159.49
AT40	VCC				-2078.7	3159.49
AT41	VCC				-2574	3159.49
AT43	VCCGT				-3069.3	3159.49
AT44	VCCGT				-3564.6	3159.49

Table 9-2. Y-Processor Ball List (Sheet 13 of 40)

Ball #	Ball Name	LPDDR3	Interleaved (IL)	Non-Interleaved (NIL)	X [um]	Y [um]
AT46	VCCGT				-4059.9	3159.49
AT47	VCCGT				-4555.2	3159.49
AT49	VCCGT				-5050.5	3159.49
AT5	GPP_F3 / I2S2_RXD				8299.45	2898.65
AT50	VCCGT				-5545.8	3159.49
AT51	VCCGT				-6041.1	3159.49
AT54	VSS				-6821.17	2898.65
AT56	DDR1_DQ[0] / DDR0_DQ[16]		DDR1_DQ[0]	DDR0_DQ[16]	-7313.93	2898.65
AT58	DDR1_DQ[5] / DDR0_DQ[21]		DDR1_DQ[5]	DDR0_DQ[21]	-7806.69	2898.65
AT60	DDR0_DQ[10]				-8299.45	2898.65
AT62	DDR0_DQ[15]				-8792.21	2898.65
AT64	VDDQ				-9310.37	2898.65
AT7	GPP_F7 / I2C3_SCL				7806.69	2898.65
AT9	GPP_F11/ I2C5_SCL / ISH_I2C2_SCL				7313.93	2898.65
AU10	SPI0_CLK				7067.55	3220.72
AU12	SPI0_MISO				6574.79	3220.72
AU2	VCCPGPPA				9038.59	3220.72
AU4	SPI0_CS0#				8545.83	3220.72
AU53	VSS				-6574.79	3220.72
AU55	VSS				-7067.55	3220.72
AU57	VSS				-7560.31	3220.72
AU59	VSS				-8053.07	3220.72
AU6	SPI0_CS1#				8053.07	3220.72
AU61	VSS				-8545.83	3220.72
AU63	VSS				-9038.59	3220.72
AU8	SPI0_CS2#				7560.31	3220.72
AV1	VCCPGPPB				9310.37	3542.79
AV11	SPI0_IO2				6821.17	3542.79
AV13	SPI0_IO3				6328.41	3542.79
AV15	VCCSPI				5881.62	3573.53
AV16	VSS				5475.22	3573.53
AV18	DCPRTC				4831.08	3573.53
AV20	VSS				4186.94	3573.53
AV22	VCCHDA				3542.79	3573.53
AV24	VSS				2898.65	3573.53
AV26	VCCIO_DDR				2254.5	3573.53
AV28	VCCIO_DDR				1610.36	3573.53
AV3	GPP_B14 / SPKR				8792.21	3542.79
AV30	VCCIO_DDR				966.22	3573.53

Table 9-2. Y-Processor Ball List (Sheet 14 of 40)

Ball #	Ball Name	LPDDR3	Interleaved (IL)	Non-Interleaved (NIL)	X [um]	Y [um]
AV32	VCCIO_DDR				322.07	3573.53
AV34	VCCIO_DDR				-322.07	3573.53
AV36	VCCIO_DDR				-966.22	3573.53
AV38	VCCIO_DDR				-1610.36	3573.53
AV40	VCCIO_DDR				-2254.5	3573.53
AV42	VCCIO_DDR				-2898.65	3573.53
AV44	VCCIO_DDR				-3542.79	3573.53
AV46	VCCIO_DDR				-4186.94	3573.53
AV48	VCCIO_DDR				-4831.08	3573.53
AV5	GPP_B8 / SRCCLKREQ3#				8299.45	3542.79
AV50	VCCIO_DDR				-5475.22	3573.53
AV52	VSS				-6119.37	3573.53
AV54	VSS				-6821.17	3542.79
AV56	DDR0_MA[8] / DDR0_CAA[3] /DDR0_MA[8]	DDR0_CAA[3]			-7313.93	3542.79
AV58	DDR0_BA[2] / DDR0_CAA[5]/ DDR0_BG[0]	DDR0_CAA[5]			-7806.69	3542.79
AV60	DDR0_RAS# /DDR0_CAB[3]/DDR0_MA[16]	DDR0_CAB[3]			-8299.45	3542.79
AV62	DDR0_MA[0] /DDR0_CAB[9]/DDR0_MA[0]	DDR0_CAB[9]			-8792.21	3542.79
AV64	VDDQ				-9310.37	3542.79
AV7	GPP_B9 / SRCCLKREQ4#				7806.69	3542.79
AV9	GPP_B6 / SRCCLKREQ1#				7313.93	3542.79
AW10	GPP_B16 / GSPI0_CLK				7067.55	3864.86
AW12	GPP_B20 / GSPI1_CLK				6574.79	3864.86
AW17	VSS				5153.15	3819.91
AW19	VSS				4509.01	3819.91
AW2	VCCPGPPB				9038.59	3864.86
AW21	VSS				3864.86	3819.91
AW23	VSS				3220.72	3819.91
AW25	VSS				2576.58	3819.91
AW27	VCCIO_DDR				1932.43	3819.91
AW29	VCCIO_DDR				1288.29	3819.91
AW31	VCCIO_DDR				644.14	3819.91
AW33	VCCIO_DDR				0	3819.91
AW35	VCCIO_DDR				-644.14	3819.91
AW37	VCCIO_DDR				-1288.29	3819.91
AW39	VCCIO_DDR				-1932.43	3819.91
AW4	GPP_B21 / GSPI1_MISO				8545.83	3864.86
AW41	VCCIO_DDR				-2576.58	3819.91
AW43	VCCIO_DDR				-3220.72	3819.91
AW45	VCCIO_DDR				-3864.86	3819.91

Table 9-2. Y-Processor Ball List (Sheet 15 of 40)

Ball #	Ball Name	LPDDR3	Interleaved (IL)	Non-Interleaved (NIL)	X [um]	Y [um]
AW47	VCCIO_DDR				-4509.01	3819.91
AW49	VCCIO_DDR				-5153.15	3819.91
AW51	VCCIO_DDR				-5797.3	3819.91
AW53	DDR1_VREF_DQ				-6441.44	3827.53
AW55	DDR0_MA[9]/DDR0_CAA[1]/DDR0_MA[9]	DDR0_CAA[1]			-7067.55	3864.86
AW57	DDR0_MA[7]/DDR0_CAA[4]/DDR0_MA[7]	DDR0_CAA[4]			-7560.31	3864.86
AW59	DDR0_MA[5]/DDR0_CAA[0]/DDR0_MA[5]	DDR0_CAA[0]			-8053.07	3864.86
AW6	GPP_B17 / GSPI0_MISO				8053.07	3864.86
AW61	DDR0_CKE[3]				-8545.83	3864.86
AW63	DDR0_CS#[0]				-9038.59	3864.86
AW8	GPP_B22 / GSPI1_MOSI				7560.31	3864.86
AY14	GPD4 / SLP_S3#				5994.4	3959.86
AY16	VSS				5475.22	4066.29
AY18	RSVD_TP				4831.08	4066.29
AY20	RSVD				4186.94	4066.29
AY22	TP6				3542.79	4066.29
AY24	VSS				2898.65	4066.29
AY26	VSS				2254.5	4066.29
AY28	VSS				1610.36	4066.29
AY30	VSS				966.22	4066.29
AY32	VSS				322.07	4066.29
AY34	VSS				-322.07	4066.29
AY36	VSS				-966.22	4066.29
AY38	VSS				-1610.36	4066.29
AY40	VSS				-2254.5	4066.29
AY42	VSS				-2898.65	4066.29
AY44	VSS				-3542.79	4066.29
AY46	VSS				-4186.94	4066.29
AY48	VSS				-4831.08	4066.29
AY50	VSS				-5475.22	4066.29
AY52	VSS				-6119.37	4066.29
B10	PCIE_RCOMPP				7085.58	-7269.23
B12	CL_RST#				6441.44	-7269.23
B15	USB3_2_RXN / SSIC_RXN				5797.3	-7269.23
B17	USB3_4_RXN				5153.15	-7269.23
B19	PCIE2_RXN / USB3_6_RXN				4509.01	-7269.23
B21	PCIE4_RXN				3864.86	-7269.23
B23	PCIE6_RXN				3220.72	-7269.23
B25	PCIE8_RXN / SATA1A_RXN				2576.58	-7269.23

Table 9-2. Y-Processor Ball List (Sheet 16 of 40)

Ball #	Ball Name	LPDDR3	Interleaved (IL)	Non-Interleaved (NIL)	X [um]	Y [um]
B27	PCIE10_RXN				1932.43	-7269.23
B29	CSI2_DP4				1288.29	-7269.23
B3	RSVD				8881.11	-7111.75
B31	CSI2_CLKP1				644.14	-7269.23
B33	CSI2_DP7				0	-7269.23
B35	CSI2_DP8				-644.14	-7269.23
B37	CSI2_DP10				-1288.29	-7269.23
B39	CSI2_CLKP3				-1932.43	-7269.23
B4	RSVD				8451.85	-7111.75
B41	DDI2_TXN[2]				-2576.58	-7269.23
B43	DDI2_TXN[3]				-3220.72	-7269.23
B45	DDI1_TXN[2]				-3864.86	-7269.23
B47	DDI1_TXN[3]				-4509.01	-7269.23
B49	JTAGX				-5153.15	-7269.23
B51	PCH_JTAG_TDO				-5797.3	-7269.23
B53	PCH_JTAG_TCK				-6441.44	-7269.23
B55	PROC_PREQ#				-7085.58	-7269.23
B58	VIDALERT#				-7777.48	-7178.04
B6	eDP_BKLCTL				8022.59	-7111.75
B61	VCCST_PWRGD				-8479.79	-7111.75
B62	SKTOCC#				-8881.11	-7111.75
B64	VCC				-9310.37	-7086.35
B8	GPP_E12 / USB2_OC3#				7593.33	-7111.75
BA1	VSS				9310.37	4186.94
BA11	VSS				6821.17	4186.94
BA13	GPP_B0 / CORE_VID0				6328.41	4186.94
BA15	GPD8 / SUSCLK				5797.3	4312.67
BA17	RSVD_TP				5153.15	4312.67
BA19	RSVD				4509.01	4312.67
BA21	RSVD				3864.86	4312.67
BA23	TP5				3220.72	4312.67
BA25	VDDQ				2576.58	4312.67
BA27	VDDQ				1932.43	4312.67
BA29	VDDQ				1288.29	4312.67
BA3	VSS				8792.21	4186.94
BA31	VDDQ				644.14	4312.67
BA33	VDDQ				0	4312.67
BA35	VDDQ				-644.14	4312.67
BA37	VDDQ				-1288.29	4312.67

Table 9-2. Y-Processor Ball List (Sheet 17 of 40)

Ball #	Ball Name	LPDDR3	Interleaved (IL)	Non-Interleaved (NIL)	X [um]	Y [um]
BA39	VDDQC				-1932.43	4312.67
BA41	VDDQ				-2576.58	4312.67
BA43	VDDQ				-3220.72	4312.67
BA45	VDDQ				-3864.86	4312.67
BA47	VDDQ				-4509.01	4312.67
BA49	VDDQ				-5153.15	4312.67
BA5	VSS				8299.45	4186.94
BA51	VDDQ				-5797.3	4312.67
BA53	VSS				-6441.44	4320.29
BA56	DDR0_MA[12]/DDR0_CAA[6]/DDR0_MA[12]	DDR0_CAA[6]			-7313.93	4186.94
BA58	VSS				-7806.69	4186.94
BA60	DDR0_CKN[1]				-8299.45	4186.94
BA62	DDR0_CKP[1]				-8792.21	4186.94
BA64	VSS				-9310.37	4186.94
BA7	VSS				7806.69	4186.94
BA9	VSS				7313.93	4186.94
BB10	GPP_B5 / SRCCLKREQ0#				7067.55	4509.01
BB12	GPP_B1 / CORE_VID1				6548.63	4559.05
BB14	RSVD				6119.37	4559.05
BB16	GPD7 / RSVD				5475.22	4559.05
BB18	RSVD				4831.08	4559.05
BB2	GPP_B19 / GSPI1_CS#				9038.59	4509.01
BB20	VSS				4186.94	4559.05
BB22	VSS				3542.79	4559.05
BB24	VSS				2898.65	4559.05
BB26	VSS				2254.5	4559.05
BB28	VSS				1610.36	4559.05
BB30	VSS				966.22	4559.05
BB32	VSS				322.07	4559.05
BB34	VSS				-322.07	4559.05
BB36	VSS				-966.22	4559.05
BB38	VSS				-1610.36	4559.05
BB4	GPP_B18 / GSPI0_MOSI				8545.83	4509.01
BB40	VSS				-2254.5	4559.05
BB42	VSS				-2898.65	4559.05
BB44	VSS				-3542.79	4559.05
BB46	VSS				-4186.94	4559.05
BB48	VSS				-4831.08	4559.05
BB50	VSS				-5475.22	4559.05

Table 9-2. Y-Processor Ball List (Sheet 18 of 40)

Ball #	Ball Name	LPDDR3	Interleaved (IL)	Non-Interleaved (NIL)	X [um]	Y [um]
BB52	VSS				-6119.37	4559.05
BB54	VSS				-6763.51	4559.05
BB57	DDR0_CKE[0]				-7560.31	4509.01
BB59	VSS				-8053.07	4509.01
BB6	GPP_B23 / SML1ALERT# / PCHHOT#				8053.07	4509.01
BB61	DDR0_MA[2] /DDR0_CAB[5]/DDR0_MA[2]	DDR0_CAB[5]			-8545.83	4509.01
BB63	DDR0_MA[3]				-9038.59	4509.01
BB8	GPP_B13 / PLTRST#				7560.31	4509.01
BC1	EMMC_RCOMP				9310.37	4831.08
BC11	GPP_B4 / CPU_GP3				6695.44	4978.4
BC15	GPD11 / LANPHYPC				5797.3	4805.43
BC17	VSS				5153.15	4805.43
BC19	RSVD				4509.01	4805.43
BC21	DDR1_DQ[62]				3864.86	4805.43
BC23	DDR1_DQ[59]				3220.72	4805.43
BC25	DDR1_DQ[55]				2576.58	4805.43
BC27	DDR1_DQ[51]				1932.43	4805.43
BC29	VSS				1288.29	4805.43
BC3	GPP_B15 / GSPI0_CS#				8792.21	4831.08
BC31	DDR1_MA[1] /DDR1_CAB[8]/DDR1_MA[1]	DDR1_CAB[8]			644.14	4805.43
BC33	DDR1_BA[0] /DDR1_CAB[4]/DDR1_BA[0]	DDR1_CAB[4]			0	4805.43
BC35	DDR1_ODT[0]				-644.14	4805.43
BC37	DDR1_WE#/DDR1_CAB[2]/DDR1_MA[14]	DDR1_CAB[2]			-1288.29	4805.43
BC39	DDR0_DQ[33] / DDR1_DQ[1]		DDR0_DQ[33]	DDR1_DQ[1]	-1932.43	4805.43
BC41	DDR0_DQ[32] / DDR1_DQ[0]		DDR0_DQ[32]	DDR1_DQ[0]	-2576.58	4805.43
BC43	DDR0_DQ[40] / DDR1_DQ[8]		DDR0_DQ[40]	DDR1_DQ[8]	-3220.72	4805.43
BC45	DDR0_DQ[44] / DDR1_DQ[12]		DDR0_DQ[44]	DDR1_DQ[12]	-3864.86	4805.43
BC47	VSS				-4509.01	4805.43
BC49	DDR0_DQ[26] / DDR0_DQ[42]		DDR0_DQ[26]	DDR0_DQ[42]	-5153.15	4805.43
BC5	GPP_B10 / SRCCLKREQ5#				8299.45	4831.08
BC51	DDR0_DQ[24] / DDR0_DQ[40]		DDR0_DQ[24]	DDR0_DQ[40]	-5797.3	4805.43
BC53	DDR0_DQ[20] / DDR0_DQ[36]		DDR0_DQ[20]	DDR0_DQ[36]	-6441.44	4805.43
BC55	DDR0_DQ[17] / DDR0_DQ[33]		DDR0_DQ[17]	DDR0_DQ[33]	-7085.58	4805.43
BC58	DDR0_CKE[1]				-7806.69	4831.08
BC60	DDR0_CKP[0]				-8299.45	4831.08
BC62	DDR0_CKN[0]				-8792.21	4831.08
BC64	DDR_RCOMP[2]				-9310.37	4831.08
BC7	GPP_B11 / EXT_PWR_GATE#				7806.69	4831.08
BC9	GPP_B12 / SLP_S0#				7313.93	4831.08

Table 9-2. Y-Processor Ball List (Sheet 19 of 40)

Ball #	Ball Name	LPDDR3	Interleaved (IL)	Non-Interleaved (NIL)	X [um]	Y [um]
BD10	GPP_B7 / SRCCLKREQ2#				7067.55	5148.58
BD14	GPD1 / ACPRESENT				6119.37	5051.81
BD16	GPD0 / BATLOW#				5475.22	5051.81
BD18	RSVD				4831.08	5051.81
BD2	GPP_A19 / ISH_GP1				9038.59	5153.15
BD20	VSS				4186.94	5051.81
BD22	DDR1_DQSP[7]				3542.79	5051.81
BD24	DDR1_DQ[57]				2898.65	5051.81
BD26	DDR1_DQSN[6]				2254.5	5051.81
BD28	DDR1_DQ[49]				1610.36	5051.81
BD30	DDR1_PAR				966.22	5051.81
BD32	DDR1_CKN[1]				322.07	5051.81
BD34	DDR1_ALERT#				-322.07	5051.81
BD36	DDR1_BA[1] /DDR1_CAB[6]/DDR1_BA[1]	DDR1_CAB[6]			-966.22	5051.81
BD38	VSS				-1610.36	5051.81
BD4	GPP_A23 / ISH_GP5				8545.83	5153.15
BD40	DDR0_DQSN[4] / DDR1_DQSN[0]		DDR0_DQSN[4]	DDR1_DQSN[0]	-2254.5	5051.81
BD42	DDR0_DQ[37] / DDR1_DQ[5]		DDR0_DQ[37]	DDR1_DQ[5]	-2898.65	5051.81
BD44	DDR0_DQSN[5] / DDR1_DQSN[1]		DDR0_DQSN[5]	DDR1_DQSN[1]	-3542.79	5051.81
BD46	DDR0_DQ[41] / DDR1_DQ[9]		DDR0_DQ[41]	DDR1_DQ[9]	-4186.94	5051.81
BD48	DDR0_DQ[31] / DDR0_DQ[47]		DDR0_DQ[31]	DDR0_DQ[47]	-4831.08	5051.81
BD50	DDR0_DQSP[3] / DDR0_DQSP[5]		DDR0_DQSP[3]	DDR0_DQSP[5]	-5475.22	5051.81
BD52	DDR0_DQ[22] / DDR0_DQ[38]		DDR0_DQ[22]	DDR0_DQ[38]	-6119.37	5051.81
BD54	DDR0_DQSN[2] / DDR0_DQSN[4]		DDR0_DQSN[2]	DDR0_DQSN[4]	-6763.51	5051.81
BD56	VSS				-7407.66	5051.81
BD59	DDR0_MA[11] /DDR0_CAA[7] / DDR0_MA[11]	DDR0_CAA[7]			-8133.08	5237.48
BD6	GPP_B2 / VRALERT#				8053.07	5153.15
BD61	DDR0_MA[15] /DDR0_CAA[8]/DDR0_ACT#	DDR0_CAA[8]			-8545.83	5153.15
BD63	VSS				-9038.59	5153.15
BD8	GPP_B3 / CPU_GP2				7560.31	5153.15
BE12	VSS				6441.44	5298.19
BE15	GPD2 / LAN_WAKE#				5797.3	5298.19
BE17	GPD6 / SLP_A#				5153.15	5298.19
BE19	RSVD				4509.01	5298.19
BE21	DDR1_DQ[63]				3864.86	5298.19
BE23	DDR1_DQ[60]				3220.72	5298.19
BE25	DDR1_DQ[54]				2576.58	5298.19
BE27	DDR1_DQ[53]				1932.43	5298.19

Table 9-2. Y-Processor Ball List (Sheet 20 of 40)

Ball #	Ball Name	LPDDR3	Interleaved (IL)	Non-Interleaved (NIL)	X [um]	Y [um]
BE29	VSS				1288.29	5298.19
BE31	VSS				644.14	5298.19
BE33	VSS				0	5298.19
BE35	VSS				-644.14	5298.19
BE37	DDR1_CAS#/DDR1_CAB[1]/DDR1_MA[15]	DDR1_CAB[1]			-1288.29	5298.19
BE39	DDR0_DQ[35] / DDR1_DQ[3]		DDR0_DQ[35]	DDR1_DQ[3]	-1932.43	5298.19
BE41	DDR0_DQ[39] / DDR1_DQ[7]		DDR0_DQ[39]	DDR1_DQ[7]	-2576.58	5298.19
BE43	DDR0_DQ[45] / DDR1_DQ[13]		DDR0_DQ[45]	DDR1_DQ[13]	-3220.72	5298.19
BE45	DDR0_DQ[46] / DDR1_DQ[14]		DDR0_DQ[46]	DDR1_DQ[14]	-3864.86	5298.19
BE47	VSS				-4509.01	5298.19
BE49	DDR0_DQ[27] / DDR0_DQ[43]		DDR0_DQ[27]	DDR0_DQ[43]	-5153.15	5298.19
BE51	DDR0_DQ[25] / DDR0_DQ[41]		DDR0_DQ[25]	DDR0_DQ[41]	-5797.3	5298.19
BE53	DDR0_DQ[19] / DDR0_DQ[35]		DDR0_DQ[19]	DDR0_DQ[35]	-6441.44	5298.19
BE55	DDR0_DQ[16] / DDR0_DQ[32]		DDR0_DQ[16]	DDR0_DQ[32]	-7085.58	5298.19
BE57	DDR0_CKE[2]				-7729.73	5298.19
BF1	SD_RCOMP				9310.37	5475.22
BF11	GPP_A18 / ISH_GP0				6763.51	5544.57
BF14	GPD3 / PWRBTN#				6119.37	5544.57
BF16	GPD5 / SLP_S4#				5475.22	5544.57
BF18	RSVD				4831.08	5544.57
BF20	VSS				4186.94	5544.57
BF22	DDR1_DQSN[7]				3542.79	5544.57
BF24	DDR1_DQ[56]				2898.65	5544.57
BF26	DDR1_DQSP[6]				2254.5	5544.57
BF28	DDR1_DQ[48]				1610.36	5544.57
BF3	GPP_A7 / PIRQA#				8792.21	5475.22
BF30	DDR1_MA[2] /DDR1_CAB[5]/DDR1_MA[2]	DDR1_CAB[5]			966.22	5544.57
BF32	DDR1_CKP[1]				322.07	5544.57
BF34	DDR1_RAS# /DDR1_CAB[3]/DDR1_MA[16]	DDR1_CAB[3]			-322.07	5544.57
BF36	DDR1_MA[0] /DDR1_CAB[9]/DDR1_MA[0]	DDR1_CAB[9]			-966.22	5544.57
BF38	VSS				-1610.36	5544.57
BF40	DDR0_DQSP[4] / DDR1_DQSP[0]		DDR0_DQSP[4]	DDR1_DQSP[0]	-2254.5	5544.57
BF42	DDR0_DQ[36] / DDR1_DQ[4]		DDR0_DQ[36]	DDR1_DQ[4]	-2898.65	5544.57
BF44	DDR0_DQSP[5] / DDR1_DQSP[1]		DDR0_DQSP[5]	DDR1_DQSP[1]	-3542.79	5544.57
BF46	DDR0_DQ[47] / DDR1_DQ[15]		DDR0_DQ[47]	DDR1_DQ[15]	-4186.94	5544.57
BF48	DDR0_DQ[30] / DDR0_DQ[46]		DDR0_DQ[30]	DDR0_DQ[46]	-4831.08	5544.57
BF5	GPP_A10 / CLKOUT_LPC1				8299.45	5475.22
BF50	DDR0_DQSN[3] / DDR0_DQSN[5]		DDR0_DQSN[3]	DDR0_DQSN[5]	-5475.22	5544.57
BF52	DDR0_DQ[23] / DDR0_DQ[39]		DDR0_DQ[23]	DDR0_DQ[39]	-6119.37	5544.57

Table 9-2. Y-Processor Ball List (Sheet 21 of 40)

Ball #	Ball Name	LPDDR3	Interleaved (IL)	Non-Interleaved (NIL)	X [um]	Y [um]
BF54	DDR0_DQSP[2] / DDR0_DQSP[4]		DDR0_DQSP[2]	DDR0_DQSP[4]	-6763.51	5544.57
BF56	VSS				-7407.66	5544.57
BF59	VSS				-8163.56	5638.8
BF62	DDR0_MA[6] /DDR0_CAA[2] /DDR0_MA[6]	DDR0_CAA[2]			-8792.21	5475.22
BF64	DDR_RCOMP[0]				-9310.37	5475.22
BF7	GPP_A11 /PME#				7806.69	5475.22
BF9	GPP_A15 / SUSACK#				7308.85	5480.3
BG10	GPP_A3 / LAD2 / ESPI_IO2				7170.42	5890.26
BG12	VSS				6441.44	5790.95
BG15	VSS				5797.3	5790.95
BG17	VSS				5153.15	5790.95
BG19	INTRUDER#				4509.01	5790.95
BG2	VSS				9038.59	5797.3
BG21	DDR1_DQ[58]				3864.86	5790.95
BG23	DDR1_DQ[61]				3220.72	5790.95
BG25	DDR1_DQ[50]				2576.58	5790.95
BG27	DDR1_DQ[52]				1932.43	5790.95
BG29	VSS				1288.29	5790.95
BG31	DDR1_MA[7] /DDR1_CAA[4] /DDR1_MA[7]	DDR1_CAA[4]			644.14	5790.95
BG33	DDR1_CKE[2]				0	5790.95
BG35	DDR1_MA[10] /DDR1_CAB[7]/ DDR1_MA[10]	DDR1_CAB[7]			-644.14	5790.95
BG37	DDR1_MA[13] /DDR1_CAB[0] / DDR1_MA[13]	DDR1_CAB[0]			-1288.29	5790.95
BG39	DDR0_DQ[38] / DDR1_DQ[6]		DDR0_DQ[38]	DDR1_DQ[6]	-1932.43	5790.95
BG4	VSS				8545.83	5797.3
BG41	DDR0_DQ[34] / DDR1_DQ[2]		DDR0_DQ[34]	DDR1_DQ[2]	-2576.58	5790.95
BG43	DDR0_DQ[42] / DDR1_DQ[10]		DDR0_DQ[42]	DDR1_DQ[10]	-3220.72	5790.95
BG45	DDR0_DQ[43] / DDR1_DQ[11]		DDR0_DQ[43]	DDR1_DQ[11]	-3864.86	5790.95
BG47	RSVD_TP				-4509.01	5790.95
BG49	DDR0_DQ[29] / DDR0_DQ[45]		DDR0_DQ[29]	DDR0_DQ[45]	-5153.15	5790.95
BG51	DDR0_DQ[28] / DDR0_DQ[44]		DDR0_DQ[28]	DDR0_DQ[44]	-5797.3	5790.95
BG53	DDR0_DQ[18] / DDR0_DQ[34]		DDR0_DQ[18]	DDR0_DQ[34]	-6441.44	5790.95
BG55	DDR0_DQ[21] / DDR0_DQ[37]		DDR0_DQ[21]	DDR0_DQ[37]	-7085.58	5790.95
BG57	DDR0_ALERT#				-7729.73	5790.95
BG6	VSS				8053.07	5797.3
BG61	DDR0_MA[14] /DDR0_CAA[9]/ DDR0_BG[1]	DDR0_CAA[9]			-8545.83	5797.3
BG63	VSS				-9038.59	5797.3
BG8	VSS				7560.31	5797.3
BH11	GPP_A8 / CLKRUN#				6763.51	6037.33

Table 9-2. Y-Processor Ball List (Sheet 22 of 40)

Ball #	Ball Name	LPDDR3	Interleaved (IL)	Non-Interleaved (NIL)	X [um]	Y [um]
BH14	GPD10 / SLP_S5#				6119.37	6037.33
BH16	GPD9 / SLP_WLAN#				5475.22	6037.33
BH18	SRTCRST#				4831.08	6037.33
BH20	VSS				4186.94	6037.33
BH22	VSS				3542.79	6037.33
BH24	VSS				2898.65	6037.33
BH26	VSS				2254.5	6037.33
BH28	VSS				1610.36	6037.33
BH30	DDR1_CKE[3]				966.22	6037.33
BH32	VSS				322.07	6037.33
BH34	VSS				-322.07	6037.33
BH36	VSS				-966.22	6037.33
BH38	VSS				-1610.36	6037.33
BH40	VSS				-2254.5	6037.33
BH42	VSS				-2898.65	6037.33
BH44	VSS				-3542.79	6037.33
BH46	VSS				-4186.94	6037.33
BH48	VSS				-4831.08	6037.33
BH50	VSS				-5475.22	6037.33
BH52	VSS				-6119.37	6037.33
BH54	VSS				-6763.51	6037.33
BH56	VSS				-7407.66	6037.33
BH59	VSS				-8051.8	6037.33
BJ1	GPP_A20 / ISH_GP2				9310.37	6177.03
BJ10	GPP_A9 / CLKOUT_LPC0 / ESPI_CLK				7085.58	6283.71
BJ12	RSMRST#				6441.44	6283.71
BJ15	TP1				5797.3	6283.71
BJ17	TP2				5153.15	6283.71
BJ19	HDA_SYNC / I2S0_SFRM				4509.01	6283.71
BJ21	DDR1_DQ[46] / DDR1_DQ[30]		DDR1_DQ[46]	DDR1_DQ[30]	3864.86	6283.71
BJ23	DDR1_DQ[43] / DDR1_DQ[27]		DDR1_DQ[43]	DDR1_DQ[27]	3220.72	6283.71
BJ25	DDR1_DQ[38] / DDR1_DQ[22]		DDR1_DQ[38]	DDR1_DQ[22]	2576.58	6283.71
BJ27	DDR1_DQ[39] / DDR1_DQ[23]		DDR1_DQ[39]	DDR1_DQ[23]	1932.43	6283.71
BJ29	VSS				1288.29	6283.71
BJ3	GPP_A22 / ISH_GP4				8881.11	6253.23
BJ31	DDR1_MA[3]				644.14	6283.71
BJ33	DDR1_CS#[1]				0	6283.71
BJ35	DDR1_MA[11] /DDR1_CAA[7] / DDR1_MA[11]	DDR1_CAA[7]			-644.14	6283.71

Table 9-2. Y-Processor Ball List (Sheet 23 of 40)

Ball #	Ball Name	LPDDR3	Interleaved (IL)	Non-Interleaved (NIL)	X [um]	Y [um]
BJ37	DDR1_MA[12] /DDR1_CAA[6] / DDR1_MA[12]	DDR1_CAA[6]			-1288.29	6283.71
BJ39	DDR0_DQ[63] / DDR1_DQ[47]		DDR0_DQ[63]	DDR1_DQ[47]	-1932.43	6283.71
BJ4	Sx_EXIT_HOLDOFF# / GPP_A12 / BM_BUSY#/ISH_GP6				8451.85	6253.23
BJ41	DDR0_DQ[58] / DDR1_DQ[42]		DDR0_DQ[58]	DDR1_DQ[42]	-2576.58	6283.71
BJ43	DDR0_DQ[55] / DDR1_DQ[39]		DDR0_DQ[55]	DDR1_DQ[39]	-3220.72	6283.71
BJ45	DDR0_DQ[54] / DDR1_DQ[38]		DDR0_DQ[54]	DDR1_DQ[38]	-3864.86	6283.71
BJ47	VSS				-4509.01	6283.71
BJ49	DDR1_DQ[27] / DDR0_DQ[59]		DDR1_DQ[27]	DDR0_DQ[59]	-5153.15	6283.71
BJ51	DDR1_DQ[25] / DDR0_DQ[57]		DDR1_DQ[25]	DDR0_DQ[57]	-5797.3	6283.71
BJ53	DDR1_DQ[18] / DDR0_DQ[50]		DDR1_DQ[18]	DDR0_DQ[50]	-6441.44	6283.71
BJ55	DDR1_DQ[16] / DDR0_DQ[48]		DDR1_DQ[16]	DDR0_DQ[48]	-7085.58	6283.71
BJ57	DDR0_CS#[1]				-7729.73	6283.71
BJ6	GPP_A14 / SUS_STAT#/ ESPI_RESET#				8022.59	6253.23
BJ61	DDR0_WE#/DDR0_CAB[2]/DDR0_MA[14]	DDR0_CAB[2]			-8451.85	6253.23
BJ62	VSS				-8881.11	6253.23
BJ64	DDR_RCOMP[1]				-9310.37	6177.03
BJ8	GPP_A2 / LAD1 / ESPI_IO1				7593.33	6253.23
BK11	GPP_A1 / LAD0 / ESPI_IO0				6763.51	6530.09
BK14	I2S1_TXD				6119.37	6530.09
BK16	HDA_SDO / I2S0_TXD				5475.22	6530.09
BK18	HDA_BLK / I2S0_SCLK				4831.08	6530.09
BK20	VSS				4186.94	6530.09
BK22	DDR1_DQSP[5] / DDR1_DQSP[3]		DDR1_DQSP[5]	DDR1_DQSP[3]	3542.79	6530.09
BK24	DDR1_DQ[41] / DDR1_DQ[25]		DDR1_DQ[41]	DDR1_DQ[25]	2898.65	6530.09
BK26	DDR1_DQSN[4] / DDR1_DQSN[2]		DDR1_DQSN[4]	DDR1_DQSN[2]	2254.5	6530.09
BK28	DDR1_DQ[34] / DDR1_DQ[18]		DDR1_DQ[34]	DDR1_DQ[18]	1610.36	6530.09
BK30	DDR1_MA[5] /DDR1_CAA[0] /DDR1_MA[5]	DDR1_CAA[0]			966.22	6530.09
BK32	DDR1_CKE[1]				322.07	6530.09
BK34	DDR1_MA[4]				-322.07	6530.09
BK36	DDR1_CKN[0]				-966.22	6530.09
BK38	VSS				-1610.36	6530.09
BK40	DDR0_DQSP[7] / DDR1_DQSP[5]		DDR0_DQSP[7]	DDR1_DQSP[5]	-2254.5	6530.09
BK42	DDR0_DQ[60] / DDR1_DQ[44]		DDR0_DQ[60]	DDR1_DQ[44]	-2898.65	6530.09
BK44	DDR0_DQSN[6] / DDR1_DQSN[4]		DDR0_DQSN[6]	DDR1_DQSN[4]	-3542.79	6530.09
BK46	DDR0_DQ[51] / DDR1_DQ[35]		DDR0_DQ[51]	DDR1_DQ[35]	-4186.94	6530.09
BK48	DDR1_DQ[30] / DDR0_DQ[62]		DDR1_DQ[30]	DDR0_DQ[62]	-4831.08	6530.09
BK50	DDR1_DQSN[3] / DDR0_DQSN[7]		DDR1_DQSN[3]	DDR0_DQSN[7]	-5475.22	6530.09
BK52	DDR1_DQ[23] / DDR0_DQ[55]		DDR1_DQ[23]	DDR0_DQ[55]	-6119.37	6530.09

Table 9-2. Y-Processor Ball List (Sheet 24 of 40)

Ball #	Ball Name	LPDDR3	Interleaved (IL)	Non-Interleaved (NIL)	X [um]	Y [um]
BK54	DDR1_DQSP[2] / DDR0_DQSP[6]		DDR1_DQSP[2]	DDR0_DQSP[6]	-6763.51	6530.09
BK56	VSS				-7407.66	6530.09
BK59	DDR0_MA[13] /DDR0_CAB[0] / DDR0_MA[13]	DDR0_CAB[0]			-8102.6	6453.89
BL1	VSS				9310.37	6631.69
BL10	GPP_A0 / RCIN#				7085.58	6776.47
BL12	I2S1_SFRM				6441.44	6776.47
BL15	HDA_SDI0/ I2S0_RXD				5797.3	6776.47
BL17	HDA_SDI1 / I2S1_RXD				5153.15	6776.47
BL19	HDA_RST# /I2S1_SCLK				4509.01	6776.47
BL21	DDR1_DQ[47] / DDR1_DQ[31]		DDR1_DQ[47]	DDR1_DQ[31]	3864.86	6776.47
BL23	DDR1_DQ[44] / DDR1_DQ[28]		DDR1_DQ[44]	DDR1_DQ[28]	3220.72	6776.47
BL25	DDR1_DQ[35] / DDR1_DQ[19]		DDR1_DQ[35]	DDR1_DQ[19]	2576.58	6776.47
BL27	DDR1_DQ[37] / DDR1_DQ[21]		DDR1_DQ[37]	DDR1_DQ[21]	1932.43	6776.47
BL29	VSS				1288.29	6776.47
BL3	GPP_A21 / ISH_GP3				8881.11	6682.49
BL31	VSS				644.14	6776.47
BL33	VSS				0	6776.47
BL35	VSS				-644.14	6776.47
BL37	DDR1_MA[8] / DDR1_CAA[3] /DDR1_MA[8]	DDR1_CAA[3]			-1288.29	6776.47
BL39	DDR0_DQ[62] / DDR1_DQ[46]		DDR0_DQ[62]	DDR1_DQ[46]	-1932.43	6776.47
BL4	GPP_A17 / SD_PWR_EN# / ISH_GP7				8451.85	6682.49
BL41	DDR0_DQ[61] / DDR1_DQ[45]		DDR0_DQ[61]	DDR1_DQ[45]	-2576.58	6776.47
BL43	DDR0_DQ[50] / DDR1_DQ[34]		DDR0_DQ[50]	DDR1_DQ[34]	-3220.72	6776.47
BL45	DDR0_DQ[53] / DDR1_DQ[37]		DDR0_DQ[53]	DDR1_DQ[37]	-3864.86	6776.47
BL47	VSS				-4509.01	6776.47
BL49	DDR1_DQ[26] / DDR0_DQ[58]		DDR1_DQ[26]	DDR0_DQ[58]	-5153.15	6776.47
BL51	DDR1_DQ[24] / DDR0_DQ[56]		DDR1_DQ[24]	DDR0_DQ[56]	-5797.3	6776.47
BL53	DDR1_DQ[19] / DDR0_DQ[51]		DDR1_DQ[19]	DDR0_DQ[51]	-6441.44	6776.47
BL55	DDR1_DQ[17] / DDR0_DQ[49]		DDR1_DQ[17]	DDR0_DQ[49]	-7085.58	6776.47
BL57	DDR0_MA[4]				-7729.73	6768.85
BL6	GPP_A13 / SUSWARN# / SUSPWRDNACK				8022.59	6682.49
BL61	DDR0_BA[1] /DDR0_CAB[6]/DDR0_BA[1]	DDR0_CAB[6]			-8451.85	6682.49
BL62	DDR0_CAS#/DDR0_CAB[1]/DDR0_MA[15]	DDR0_CAB[1]			-8881.11	6682.49
BL64	RSVD_TP				-9310.37	6631.69
BL8	VSS				7593.33	6682.49
BM11	VSS				6763.51	7022.85
BM14	VSS				6119.37	7022.85
BM16	VSS				5475.22	7022.85

Table 9-2. Y-Processor Ball List (Sheet 25 of 40)

Ball #	Ball Name	LPDDR3	Interleaved (IL)	Non-Interleaved (NIL)	X [um]	Y [um]
BM18	VSS				4831.08	7022.85
BM20	VSS				4186.94	7022.85
BM22	DDR1_DQSN[5] / DDR1_DQSN[3]		DDR1_DQSN[5]	DDR1_DQSN[3]	3542.79	7022.85
BM24	DDR1_DQ[40] / DDR1_DQ[24]		DDR1_DQ[40]	DDR1_DQ[24]	2898.65	7022.85
BM26	DDR1_DQSP[4] / DDR1_DQSP[2]		DDR1_DQSP[4]	DDR1_DQSP[2]	2254.5	7022.85
BM28	DDR1_DQ[32] / DDR1_DQ[16]		DDR1_DQ[32]	DDR1_DQ[16]	1610.36	7022.85
BM30	DDR1_CS#[0]				966.22	7022.85
BM32	DDR1_MA[6] /DDR1_CAA[2] /DDR1_MA[6]	DDR1_CAA[2]			322.07	7022.85
BM34	DDR1_MA[15] /DDR1_CAA[8]/DDR1_ACT#	DDR1_CAA[8]			-322.07	7022.85
BM36	DDR1_CKP[0]				-966.22	7022.85
BM38	VSS				-1610.36	7022.85
BM40	DDR0_DQSN[7] / DDR1_DQSN[5]		DDR0_DQSN[7]	DDR1_DQSN[5]	-2254.5	7022.85
BM42	DDR0_DQ[56] / DDR1_DQ[40]		DDR0_DQ[56]	DDR1_DQ[40]	-2898.65	7022.85
BM44	DDR0_DQSP[6] / DDR1_DQSP[4]		DDR0_DQSP[6]	DDR1_DQSP[4]	-3542.79	7022.85
BM46	DDR0_DQ[49] / DDR1_DQ[33]		DDR0_DQ[49]	DDR1_DQ[33]	-4186.94	7022.85
BM48	DDR1_DQ[31] / DDR0_DQ[63]		DDR1_DQ[31]	DDR0_DQ[63]	-4831.08	7022.85
BM50	DDR1_DQSP[3] / DDR0_DQSP[7]		DDR1_DQSP[3]	DDR0_DQSP[7]	-5475.22	7022.85
BM52	DDR1_DQ[22] / DDR0_DQ[54]		DDR1_DQ[22]	DDR0_DQ[54]	-6119.37	7022.85
BM54	DDR1_DQSN[2] / DDR0_DQSN[6]		DDR1_DQSN[2]	DDR0_DQSN[6]	-6763.51	7022.85
BM56	DDR0_PAR				-7407.66	7022.85
BM59	DDR0_MA[10] /DDR0_CAB[7]/ DDR0_MA[10]	DDR0_CAB[7]			-8098.79	6923.28
BN1	TP4				9310.37	7086.35
BN10	SLP_SUS#				7085.58	7269.23
BN12	RTCRST#				6441.44	7269.23
BN15	DSW_PWROK				5797.3	7269.23
BN17	PROC_POPIRCOMP				5153.15	7269.23
BN19	RTCX1				4509.01	7269.23
BN21	DDR1_DQ[42] / DDR1_DQ[26]		DDR1_DQ[42]	DDR1_DQ[26]	3864.86	7269.23
BN23	DDR1_DQ[45] / DDR1_DQ[29]		DDR1_DQ[45]	DDR1_DQ[29]	3220.72	7269.23
BN25	DDR1_DQ[36] / DDR1_DQ[20]		DDR1_DQ[36]	DDR1_DQ[20]	2576.58	7269.23
BN27	DDR1_DQ[33] / DDR1_DQ[17]		DDR1_DQ[33]	DDR1_DQ[17]	1932.43	7269.23
BN29	VSS				1288.29	7269.23
BN3	RSVD				8881.11	7111.75
BN31	DDR1_MA[9] /DDR1_CAA[1] /DDR1_MA[9]	DDR1_CAA[1]			644.14	7269.23
BN33	DDR1_CKE[0]				0	7269.23
BN35	DDR1_MA[14] /DDR1_CAA[9]/ DDR1_BG[1]	DDR1_CAA[9]			-644.14	7269.23
BN37	DDR1_BA[2] /DDR1_CAA[5]/ DDR1_BG[0]	DDR1_CAA[5]			-1288.29	7269.23
BN39	DDR0_DQ[59] / DDR1_DQ[43]		DDR0_DQ[59]	DDR1_DQ[43]	-1932.43	7269.23

Table 9-2. Y-Processor Ball List (Sheet 26 of 40)

Ball #	Ball Name	LPDDR3	Interleaved (IL)	Non-Interleaved (NIL)	X [um]	Y [um]
BN4	GPP_A16 / SD_1P8_SEL				8451.85	7111.75
BN41	DDR0_DQ[57] / DDR1_DQ[41]		DDR0_DQ[57]	DDR1_DQ[41]	-2576.58	7269.23
BN43	DDR0_DQ[52] / DDR1_DQ[36]		DDR0_DQ[52]	DDR1_DQ[36]	-3220.72	7269.23
BN45	DDR0_DQ[48] / DDR1_DQ[32]		DDR0_DQ[48]	DDR1_DQ[32]	-3864.86	7269.23
BN47	DDR_VTT_CNTL				-4509.01	7269.23
BN49	DDR1_DQ[28] / DDR0_DQ[60]		DDR1_DQ[28]	DDR0_DQ[60]	-5153.15	7269.23
BN51	DDR1_DQ[29] / DDR0_DQ[61]		DDR1_DQ[29]	DDR0_DQ[61]	-5797.3	7269.23
BN53	DDR1_DQ[21] / DDR0_DQ[53]		DDR1_DQ[21]	DDR0_DQ[53]	-6441.44	7269.23
BN55	DDR1_DQ[20] / DDR0_DQ[52]		DDR1_DQ[20]	DDR0_DQ[52]	-7085.58	7269.23
BN58	DDR0_MA[1] /DDR0_CAB[8]/DDR0_MA[1]	DDR0_CAB[8]			-7777.48	7178.04
BN6	VSS				8022.59	7111.75
BN61	DDR0_ODT[0]				-8451.85	7111.75
BN62	DDR0_BA[0] /DDR0_CAB[4]/DDR0_BA[0]	DDR0_CAB[4]			-8881.11	7111.75
BN64	VDDQ				-9310.37	7086.35
BN8	GPP_A6 / SERIRQ				7593.33	7111.75
BP1	VSS				9310.37	7541.01
BP11	SLP_LAN#				6763.51	7541.01
BP14	PCH_PWROK				6119.37	7541.01
BP16	PCH_OPIRCOMP				5475.22	7541.01
BP18	RTCX2				4831.08	7541.01
BP20	DRAM_RESET#				4186.94	7541.01
BP22	VSS				3542.79	7541.01
BP24	VDDQ				2898.65	7541.01
BP26	VDDQ				2254.5	7541.01
BP28	VSS				1610.36	7541.01
BP3	RSVD				8855.71	7541.01
BP30	VSS				966.22	7541.01
BP32	VDDQ				322.07	7541.01
BP34	VDDQ				-322.07	7541.01
BP36	VSS				-966.22	7541.01
BP38	VSS				-1610.36	7541.01
BP40	VDDQ				-2254.5	7541.01
BP42	VDDQ				-2898.65	7541.01
BP44	VSS				-3542.79	7541.01
BP46	VSS				-4186.94	7541.01
BP48	VDDQ				-4831.08	7541.01
BP5	GPP_A4 / LAD3 / ESPI_IO3				8401.05	7541.01
BP50	VDDQ				-5475.22	7541.01
BP52	VSS				-6119.37	7541.01

Table 9-2. Y-Processor Ball List (Sheet 27 of 40)

Ball #	Ball Name	LPDDR3	Interleaved (IL)	Non-Interleaved (NIL)	X [um]	Y [um]
BP54	VSS				-6763.51	7541.01
BP56	VDDQ				-7407.66	7541.01
BP58	VDDQ				-7946.39	7541.01
BP60	VSS				-8401.05	7541.01
BP62	VSS				-8855.71	7541.01
BP64	VDDQ				-9310.37	7541.01
BP7	GPP_A5 / LFRAME# / ESPI_CS#				7946.39	7541.01
BP9	WAKE#				7407.66	7541.01
C11	GPP_E13 / DDPB_HPD0				6763.51	-7022.85
C14	VSS				6119.37	-7022.85
C16	USB3_1_RXN				5475.22	-7022.85
C18	USB3_3_RXN				4831.08	-7022.85
C20	PCIE1_RXN / USB3_5_RXN				4186.94	-7022.85
C22	PCIE3_RXN				3542.79	-7022.85
C24	PCIE5_RXN				2898.65	-7022.85
C26	PCIE7_RXN / SATA0_RXN				2254.5	-7022.85
C28	PCIE9_RXN				1610.36	-7022.85
C30	CSI2_DN6				966.22	-7022.85
C32	CSI2_DN5				322.07	-7022.85
C34	CSI2_CLKN2				-322.07	-7022.85
C36	CSI2_DN9				-966.22	-7022.85
C38	CSI2_DN11				-1610.36	-7022.85
C40	VSS				-2254.5	-7022.85
C42	DDI2_TXP[0]				-2898.65	-7022.85
C44	DDI2_TXP[1]				-3542.79	-7022.85
C46	DDI1_TXP[0]				-4186.94	-7022.85
C48	DDI1_TXN[1]				-4831.08	-7022.85
C50	PCH_JTAG_TDI				-5475.22	-7022.85
C52	PCH_TRST#				-6119.37	-7022.85
C54	PROC_TDI				-6763.51	-7022.85
C56	CFG[6]				-7403.09	-7022.85
C59	PROC_TMS				-8110.22	-6918.2
D1	VSS				9310.37	-6631.69
D10	VSS				7085.58	-6776.47
D12	CL_DATA				6441.44	-6776.47
D15	USB3_2_RXP / SSIC_RXP				5797.3	-6776.47
D17	USB3_4_RXP				5153.15	-6776.47
D19	PCIE2_RXP / USB3_6_RXP				4509.01	-6776.47
D21	PCIE4_RXP				3864.86	-6776.47

Table 9-2. Y-Processor Ball List (Sheet 28 of 40)

Ball #	Ball Name	LPDDR3	Interleaved (IL)	Non-Interleaved (NIL)	X [um]	Y [um]
D23	PCIE6_RXP				3220.72	-6776.47
D25	PCIE8_RXP / SATA1A_RXP				2576.58	-6776.47
D27	PCIE10_RXP				1932.43	-6776.47
D29	CSI2_DN4				1288.29	-6776.47
D3	eDP_VDDEN				8881.11	-6682.49
D31	CSI2_CLKN1				644.14	-6776.47
D33	CSI2_DN7				0	-6776.47
D35	CSI2_DN8				-644.14	-6776.47
D37	CSI2_DN10				-1288.29	-6776.47
D39	CSI2_CLKN3				-1932.43	-6776.47
D4	eDP_BKLEN				8451.85	-6682.49
D41	DDI2_TXP[2]				-2576.58	-6776.47
D43	DDI2_TXP[3]				-3220.72	-6776.47
D45	DDI1_TXP[2]				-3864.86	-6776.47
D47	DDI1_TXP[3]				-4509.01	-6776.47
D49	RSVD				-5153.15	-6776.47
D51	PROC_PRDY#				-5797.3	-6776.47
D53	PROC_TCK				-6441.44	-6776.47
D55	CFG[5]				-7149.08	-6687.57
D57	CFG[10]				-7724.65	-6756.15
D6	VSS				8022.59	-6682.49
D61	CFG[8]				-8451.85	-6682.49
D62	VSS				-8881.11	-6682.49
D64	VCC				-9310.37	-6631.69
D8	VSS				7593.33	-6682.49
E11	GPP_E3 / CPU_GP0				6763.51	-6530.09
E14	VSS				6119.37	-6530.09
E16	VSS				5475.22	-6530.09
E18	VSS				4831.08	-6530.09
E20	VSS				4186.94	-6530.09
E22	VSS				3542.79	-6530.09
E24	VSS				2898.65	-6530.09
E26	VSS				2254.5	-6530.09
E28	VSS				1610.36	-6530.09
E30	VSS				966.22	-6530.09
E32	VSS				322.07	-6530.09
E34	VSS				-322.07	-6530.09
E36	VSS				-966.22	-6530.09
E38	VSS				-1610.36	-6530.09

Table 9-2. Y-Processor Ball List (Sheet 29 of 40)

Ball #	Ball Name	LPDDR3	Interleaved (IL)	Non-Interleaved (NIL)	X [um]	Y [um]
E40	VSS				-2254.5	-6530.09
E42	VSS				-2898.65	-6530.09
E44	VSS				-3542.79	-6530.09
E46	VSS				-4186.94	-6530.09
E48	VSS				-4831.08	-6530.09
E50	VSS				-5475.22	-6530.09
E52	VSS				-6119.37	-6530.09
E54	VSS				-6763.51	-6530.09
E56	VSS				-7509.26	-6403.09
E59	VSS				-8088.88	-6413.25
F1	RSVD				9310.37	-6177.03
F10	GPP_E4 / DEVSLP0				7085.58	-6283.71
F12	CL_CLK				6441.44	-6283.71
F15	USB3_2_TXN / SSIC_TXN				5797.3	-6283.71
F17	USB3_4_TXN				5153.15	-6283.71
F19	PCIE2_TXN / USB3_6_TXN				4509.01	-6283.71
F21	PCIE4_TXN				3864.86	-6283.71
F23	PCIE6_TXN				3220.72	-6283.71
F25	PCIE8_TXN / SATA1A_TXN				2576.58	-6283.71
F27	PCIE10_TXN				1932.43	-6283.71
F29	CSI2_DP0				1288.29	-6283.71
F3	RSVD				8881.11	-6253.23
F31	CSI2_CLKP0				644.14	-6283.71
F33	CSI2_DN1				0	-6283.71
F35	CLKOUT_PCIE_P1				-644.14	-6283.71
F37	CLKOUT_PCIE_P4				-1288.29	-6283.71
F39	CLKOUT_PCIE_P5				-1932.43	-6283.71
F4	GPP_E21 / DDPC_CTRLDATA				8451.85	-6253.23
F41	DDI1_AUXP				-2576.58	-6283.71
F43	EDP_TXP[3]				-3220.72	-6283.71
F45	EDP_TXP[0]				-3864.86	-6283.71
F47	PROC_TRST#				-4509.01	-6283.71
F49	PECI				-5153.15	-6283.71
F51	BPM#[2]				-5797.3	-6283.71
F53	CFG[1]				-6441.44	-6283.71
F55	CFG[7]				-7085.58	-6283.71
F6	GPP_E16 / DDPE_HPD3				8022.59	-6253.23
F61	CFG[11]				-8477.25	-6253.23
F62	VSS				-8881.11	-6253.23

Table 9-2. Y-Processor Ball List (Sheet 30 of 40)

Ball #	Ball Name	LPDDR3	Interleaved (IL)	Non-Interleaved (NIL)	X [um]	Y [um]
F64	VCC				-9310.37	-6171.03
F8	GPP_E11 / USB2_OC2#				7593.33	-6253.23
G11	GPP_E0 / SATAXPCIE0 / SATAGP0				6763.51	-6037.33
G14	VSS				6119.37	-6037.33
G16	USB3_1_TXN				5475.22	-6037.33
G18	USB3_3_TXN				4831.08	-6037.33
G20	PCIE1_TXN / USB3_5_TXN				4186.94	-6037.33
G22	PCIE3_TXN				3542.79	-6037.33
G24	PCIE5_TXN				2898.65	-6037.33
G26	PCIE7_TXN / SATA0_TXN				2254.5	-6037.33
G28	PCIE9_TXN				1610.36	-6037.33
G30	CSI2_DP2				966.22	-6037.33
G32	CSI2_DP3				322.07	-6037.33
G34	CLKOUT_ITPXDP_P				-322.07	-6037.33
G36	CLKOUT_PCIE_P2				-966.22	-6037.33
G38	CLKOUT_PCIE_P3				-1610.36	-6037.33
G40	DDI2_AUXP				-2254.5	-6037.33
G42	EDP_AUXP				-2898.65	-6037.33
G44	EDP_TXP[1]				-3542.79	-6037.33
G46	EDP_TXP[2]				-4186.94	-6037.33
G48	PROC_TDO				-4831.08	-6037.33
G50	BPM#[3]				-5475.22	-6037.33
G52	CFG[0]				-6119.37	-6037.33
G54	CFG[17]				-6763.51	-6037.33
G56	CFG[18]				-7417.82	-6010.66
G58	CFG[9]				-7818.63	-6095.75
H10	GPP_E5 / DEVSLP1				7170.42	-5890.26
H12	RSVD				6441.44	-5790.95
H15	USB3_2_TXP / SSIC_TXP				5797.3	-5790.95
H17	USB3_4_TXP				5153.15	-5790.95
H19	PCIE2_TXP / USB3_6_TXP				4509.01	-5790.95
H2	SYS_RESET#				9038.59	-5797.3
H21	PCIE4_TXP				3864.86	-5790.95
H23	PCIE6_TXP				3220.72	-5790.95
H25	PCIE8_TXP / SATA1A_TXP				2576.58	-5790.95
H27	PCIE10_TXP				1932.43	-5790.95
H29	CSI2_DN0				1288.29	-5790.95
H31	CSI2_CLKN0				644.14	-5790.95
H33	CSI2_DP1				0	-5790.95

Table 9-2. Y-Processor Ball List (Sheet 31 of 40)

Ball #	Ball Name	LPDDR3	Interleaved (IL)	Non-Interleaved (NIL)	X [um]	Y [um]
H35	CLKOUT_PCIE_N1				-644.14	-5790.95
H37	CLKOUT_PCIE_N4				-1288.29	-5790.95
H39	CLKOUT_PCIE_N5				-1932.43	-5790.95
H4	GPP_E20 / DDPC_CTRLCLK				8545.83	-5797.3
H41	DDI1_AUXN				-2576.58	-5790.95
H43	EDP_TXN[3]				-3220.72	-5790.95
H45	EDP_TXN[0]				-3864.86	-5790.95
H47	THERMTRIP#				-4509.01	-5790.95
H49	CATERR#				-5153.15	-5790.95
H51	BPM#[0]				-5797.3	-5790.95
H53	CFG[3]				-6441.44	-5790.95
H55	CFG[4]				-7085.58	-5783.33
H59	CFG[15]				-8130.79	-5839.21
H6	GPP_E19 / DDPB_CTRLDATA				8053.07	-5797.3
H61	CFG[14]				-8545.83	-5797.3
H63	VCC				-9038.59	-5797.3
H8	GPP_E8 / SATALED#				7560.31	-5797.3
J1	SYS_PWROK				9310.37	-5475.22
J11	GPP_E1 / SATAXPCIE1 / SATAGP1				6763.51	-5544.57
J14	VSS				6119.37	-5544.57
J16	USB3_1_TXP				5475.22	-5544.57
J18	USB3_3_TXP				4831.08	-5544.57
J20	PCIE1_TXP / USB3_5_TXP				4186.94	-5544.57
J22	PCIE3_TXP				3542.79	-5544.57
J24	PCIE5_TXP				2898.65	-5544.57
J26	PCIE7_TXP / SATA0_TXP				2254.5	-5544.57
J28	PCIE9_TXP				1610.36	-5544.57
J3	VSS				8792.21	-5475.22
J30	CSI2_DN2				966.22	-5544.57
J32	CSI2_DN3				322.07	-5544.57
J34	CLKOUT_ITPXDP_N				-322.07	-5544.57
J36	CLKOUT_PCIE_N2				-966.22	-5544.57
J38	CLKOUT_PCIE_N3				-1610.36	-5544.57
J40	DDI2_AUXN				-2254.5	-5544.57
J42	EDP_AUXN				-2898.65	-5544.57
J44	EDP_TXN[1]				-3542.79	-5544.57
J46	EDP_TXN[2]				-4186.94	-5544.57
J48	PROCHOT#				-4831.08	-5544.57
J5	VSS				8299.45	-5475.22

Table 9-2. Y-Processor Ball List (Sheet 32 of 40)

Ball #	Ball Name	LPDDR3	Interleaved (IL)	Non-Interleaved (NIL)	X [um]	Y [um]
J50	BPM#[1]				-5475.22	-5544.57
J52	CFG[2]				-6119.37	-5544.57
J54	CFG[16]				-6763.51	-5544.57
J56	CFG[19]				-7407.66	-5544.57
J58	CFG[13]				-7805.93	-5605.53
J60	CFG[12]				-8299.45	-5475.22
J62	VSS				-8792.21	-5475.22
J64	VCC				-9310.37	-5475.22
J7	VSS				7806.69	-5475.22
J9	VSS				7313.93	-5475.22
K12	RSVD				6441.44	-5298.19
K15	VSS				5797.3	-5298.19
K17	VSS				5153.15	-5298.19
K19	VSS				4509.01	-5298.19
K21	VSS				3864.86	-5298.19
K23	VSS				3220.72	-5298.19
K25	VSS				2576.58	-5298.19
K27	VSS				1932.43	-5298.19
K29	VSS				1288.29	-5298.19
K31	VSS				644.14	-5298.19
K33	VSS				0	-5298.19
K35	VSS				-644.14	-5298.19
K37	VSS				-1288.29	-5298.19
K39	VSS				-1932.43	-5298.19
K41	VSS				-2576.58	-5298.19
K43	VSS				-3220.72	-5298.19
K45	VSS				-3864.86	-5298.19
K47	VSS				-4509.01	-5298.19
K49	VSS				-5153.15	-5298.19
K51	VSS				-5797.3	-5298.19
K53	VSS				-6441.44	-5298.19
K55	VSS				-7085.58	-5298.19
L10	GPP_E14 / DDPC_HPD1				7067.55	-5153.15
L14	VSS				6119.37	-5051.81
L16	RSVD				5475.22	-5051.81
L18	RSVD				4831.08	-5051.81
L2	XTAL24_OUT				9038.59	-5153.15
L20	RSVD				4186.94	-5051.81
L22	RSVD				3542.79	-5051.81

Table 9-2. Y-Processor Ball List (Sheet 33 of 40)

Ball #	Ball Name	LPDDR3	Interleaved (IL)	Non-Interleaved (NIL)	X [um]	Y [um]
L24	RSVD				2898.65	-5051.81
L26	RSVD				2254.5	-5051.81
L28	RSVD				1610.36	-5051.81
L30	VCCSA				966.22	-5051.81
L32	VSS_SENSE				322.07	-5051.81
L34	VCC_SENSE				-322.07	-5051.81
L36	RSVD				-966.22	-5051.81
L38	RSVD				-1610.36	-5051.81
L4	GPP_E23				8545.83	-5153.15
L40	VCC				-2254.5	-5051.81
L42	VCC				-2898.65	-5051.81
L44	VCC				-3542.79	-5051.81
L46	VCC				-4186.94	-5051.81
L48	VCC				-4831.08	-5051.81
L50	VCC				-5475.22	-5051.81
L52	VCC				-6119.37	-5051.81
L54	VCC				-6763.51	-5051.81
L57	VSS				-7660.64	-5232.4
L59	VSS				-8053.07	-5153.15
L6	GPP_E18 / DDPB_CTRLCLK				8053.07	-5153.15
L61	VSS				-8545.83	-5153.15
L63	VCC				-9038.59	-5153.15
L8	GPP_E6 / DEVSLP2				7560.31	-5153.15
M1	XTAL24_IN				9310.37	-4831.08
M11	GPP_E10 / USB2_OC1#				6821.17	-4831.08
M15	RSVD				5797.3	-4805.43
M17	RSVD				5153.15	-4805.43
M19	RSVD				4509.01	-4805.43
M21	RSVD				3864.86	-4805.43
M23	RSVD				3220.72	-4805.43
M25	RSVD				2576.58	-4805.43
M27	RSVD				1932.43	-4805.43
M29	VCCSA_SENSE				1288.29	-4805.43
M3	VSS				8792.21	-4831.08
M31	VCCSA				644.14	-4805.43
M33	VCC				0	-4805.43
M35	VCC				-644.14	-4805.43
M37	VCC				-1288.29	-4805.43
M39	VCC				-1932.43	-4805.43

Table 9-2. Y-Processor Ball List (Sheet 34 of 40)

Ball #	Ball Name	LPDDR3	Interleaved (IL)	Non-Interleaved (NIL)	X [um]	Y [um]
M41	VCC				-2576.58	-4805.43
M43	VCC				-3220.72	-4805.43
M45	VCC				-3864.86	-4805.43
M47	VCC				-4509.01	-4805.43
M49	VCC				-5153.15	-4805.43
M5	GPP_E22				8299.45	-4831.08
M51	VCC				-5797.3	-4805.43
M53	VCC				-6441.44	-4805.43
M56	VCC				-7341.87	-4989.83
M58	VCC				-7806.69	-4831.08
M60	VCC				-8299.45	-4831.08
M62	VCC				-8792.21	-4831.08
M64	VCC				-9310.37	-4831.08
M7	GPP_E15 / DDPD_HPD2				7806.69	-4831.08
M9	GPP_E7 / CPU_GP1				7313.93	-4831.08
N10	GPP_E2 / SATAXPCIE2 / SATAGP2				7067.55	-4509.01
N12	GPP_E9 / USB2_OC0#				6574.79	-4509.01
N14	VSS				6119.37	-4559.05
N16	VSS				5475.22	-4559.05
N18	VSS				4831.08	-4559.05
N2	USB2_COMP				9038.59	-4509.01
N20	VSS				4186.94	-4559.05
N22	VSS				3542.79	-4559.05
N24	VSS				2898.65	-4559.05
N26	VSS				2254.5	-4559.05
N28	VSSSA_SENSE				1610.36	-4559.05
N30	VCCSA				966.22	-4559.05
N32	VCC				322.07	-4559.05
N34	VCC				-322.07	-4559.05
N36	VCC				-966.22	-4559.05
N38	VCC				-1610.36	-4559.05
N4	GPP_D4 / FLASHTRIG				8545.83	-4509.01
N40	VCC				-2254.5	-4559.05
N42	VCC				-2898.65	-4559.05
N44	VCCGT				-3542.79	-4559.05
N46	VCCGT				-4186.94	-4559.05
N48	VCCGT				-4831.08	-4559.05
N50	VCCGT				-5475.22	-4559.05
N52	VCCGT_SENSE				-6119.37	-4559.05

Table 9-2. Y-Processor Ball List (Sheet 35 of 40)

Ball #	Ball Name	LPDDR3	Interleaved (IL)	Non-Interleaved (NIL)	X [um]	Y [um]
N54	VCC				-6777.48	-4586.99
N55	VCC				-7176.77	-4625.34
N57	VCC				-7560.31	-4509.01
N59	VCC				-8053.07	-4509.01
N6	GPP_D0				8053.07	-4509.01
N61	VCC				-8545.83	-4509.01
N63	VCC				-9038.59	-4509.01
N8	GPP_D2				7560.31	-4509.01
P1	XCLK_BIASREF				9310.37	-4186.94
P11	GPP_D9				6821.17	-4186.94
P13	RSVD				6328.41	-4181.86
P3	GPP_D3				8792.21	-4186.94
P5	GPP_D6 / ISH_I2C0_SCL				8299.45	-4186.94
P52	VSSGT_SENSE				-6423.66	-4277.36
P54	VSS				-6821.17	-4186.94
P56	VCC				-7313.93	-4186.94
P58	VCC				-7806.69	-4186.94
P60	VCC				-8299.45	-4186.94
P62	VCC				-8792.21	-4186.94
P64	VCC				-9310.37	-4186.94
P7	GPP_D5 / ISH_I2C0_SDA				7806.69	-4186.94
P9	GPP_D1				7313.93	-4186.94
R10	VSS				7067.55	-3864.86
R12	RSVD				6574.79	-3864.86
R15	VCCAPLLEBB_1P0				5846.1	-4104.91
R16	VCCAPLLEBB_1P0				5350.8	-4104.91
R18	VSS				4855.5	-4104.91
R19	VCCCLK6				4360.2	-4104.91
R2	VSS				9038.59	-3864.86
R21	VCCCLK5				3864.9	-4104.91
R23	VCCCLK5				3369.6	-4104.91
R24	VSS				2874.3	-4104.91
R26	VCCSTG				2379	-4104.91
R27	VCCPLL				1883.7	-4104.91
R29	VCCSA				1388.4	-4104.91
R30	VSS				893.1	-4104.91
R32	VCC				397.8	-4104.91
R33	VSS				-97.5	-4104.91
R35	VCCG0				-592.8	-4104.91

Table 9-2. Y-Processor Ball List (Sheet 36 of 40)

Ball #	Ball Name	LPDDR3	Interleaved (IL)	Non-Interleaved (NIL)	X [um]	Y [um]
R36	VSS				-1088.1	-4104.91
R38	VCCG0				-1583.4	-4104.91
R4	VSS				8545.83	-3864.86
R40	VSS				-2078.7	-4104.91
R41	VCC				-2574	-4104.91
R43	VSS				-3069.3	-4104.91
R44	VSS				-3564.6	-4104.91
R46	VSS				-4059.9	-4104.91
R47	VSS				-4555.2	-4104.91
R49	VSS				-5050.5	-4104.91
R50	VSS				-5545.8	-4104.91
R51	VCCGT				-6041.1	-4104.91
R53	VCCGT				-6574.79	-3864.86
R55	VSS				-7067.55	-3864.86
R57	VCC				-7560.31	-3864.86
R59	VCC				-8053.07	-3864.86
R6	VSS				8053.07	-3864.86
R61	VCC				-8545.83	-3864.86
R63	VCC				-9038.59	-3864.86
R8	VSS				7560.31	-3864.86
T1	VCCMPHYGT_1P0				9310.37	-3542.79
T11	GPP_D12				6821.17	-3542.79
T13	VSS				6328.41	-3537.71
T15	VCCMPHYGT_1P0				5846.1	-3546.11
T16	VCCMPHYGT_1P0				5350.8	-3546.11
T18	VSS				4855.5	-3546.11
T19	VCCCLK6				4360.2	-3546.11
T21	VSS				3864.9	-3546.11
T23	VSS				3369.6	-3546.11
T24	VSS				2874.3	-3546.11
T26	VCCSTG				2379	-3546.11
T27	VCCPLL				1883.7	-3546.11
T29	VCCSA				1388.4	-3546.11
T3	GPP_D8 / ISH_I2C1_SCL				8792.21	-3542.79
T30	VCCSA				893.1	-3546.11
T32	VCC				397.8	-3546.11
T33	VSS				-97.5	-3546.11
T35	VCCG0				-592.8	-3546.11
T36	VSS				-1088.1	-3546.11

Table 9-2. Y-Processor Ball List (Sheet 37 of 40)

Ball #	Ball Name	LPDDR3	Interleaved (IL)	Non-Interleaved (NIL)	X [um]	Y [um]
T38	VCCG0				-1583.4	-3546.11
T40	VSS				-2078.7	-3546.11
T41	VCC				-2574	-3546.11
T43	VCCGT				-3069.3	-3546.11
T44	VCCGT				-3564.6	-3546.11
T46	VCCGT				-4059.9	-3546.11
T47	VCCGT				-4555.2	-3546.11
T49	VCCGT				-5050.5	-3546.11
T5	GPP_D11				8299.45	-3542.79
T50	VCCGT				-5545.8	-3546.11
T51	VCCGT				-6041.1	-3546.11
T54	VCCGT				-6821.17	-3542.79
T56	VSS				-7313.93	-3542.79
T58	VSS				-7806.69	-3542.79
T60	VSS				-8299.45	-3542.79
T62	VSS				-8792.21	-3542.79
T64	VSS				-9310.37	-3542.79
T7	GPP_D10				7806.69	-3542.79
T9	GPP_D7 / ISH_I2C1_SDA				7313.93	-3542.79
U10	GPP_D13 / ISH_UART0_RXD / SML0BDATA				7067.55	-3220.72
U12	GPP_D17 / DMIC_CLK1				6574.79	-3220.72
U2	VCCMPHYGT_1P0				9038.59	-3220.72
U4	GPP_D14 / ISH_UART0_TXD / SML0BCLK				8545.83	-3220.72
U53	VCCGT				-6574.79	-3220.72
U55	VCCGT				-7067.55	-3220.72
U57	VCCGT				-7560.31	-3220.72
U59	VCCGT				-8053.07	-3220.72
U6	GPP_D15 / ISH_UART0_RTS#				8053.07	-3220.72
U61	VCCGT				-8545.83	-3220.72
U63	VCCGT				-9038.59	-3220.72
U8	GPP_D18 / DMIC_DATA1				7560.31	-3220.72
V1	VCCMPHYAON_1P0				9310.37	-2898.65
V11	GPP_D20 / DMIC_DATA0				6821.17	-2898.65
V13	VSS				6328.41	-2893.57
V15	VCCAMPHYPLL_1P0				5846.1	-2987.31
V16	VCCAMPHYPLL_1P0				5350.8	-2987.31
V18	VCCCLK1				4855.5	-2987.31
V19	VCCCLK2				4360.2	-2987.31
V21	VCCCLK4				3864.9	-2987.31

Table 9-2. Y-Processor Ball List (Sheet 38 of 40)

Ball #	Ball Name	LPDDR3	Interleaved (IL)	Non-Interleaved (NIL)	X [um]	Y [um]
V23	VCCCLK3				3369.6	-2987.31
V24	VSS				2874.3	-2987.31
V26	VCCST				2379	-2987.31
V27	VSS				1883.7	-2987.31
V29	VCCSA				1388.4	-2987.31
V3	GPP_D19 / DMIC_CLK0				8792.21	-2898.65
V30	VSS				893.1	-2987.31
V32	VCC				397.8	-2987.31
V33	VSS				-97.5	-2987.31
V35	VCCG0				-592.8	-2987.31
V36	VSS				-1088.1	-2987.31
V38	VCCG0				-1583.4	-2987.31
V40	VSS				-2078.7	-2987.31
V41	VCC				-2574	-2987.31
V43	VSS				-3069.3	-2987.31
V44	VSS				-3564.6	-2987.31
V46	VSS				-4059.9	-2987.31
V47	VSS				-4555.2	-2987.31
V49	VSS				-5050.5	-2987.31
V5	GPP_D23 / I2S_MCLK				8299.45	-2898.65
V50	VSS				-5545.8	-2987.31
V51	VSS				-6041.1	-2987.31
V54	VCCGT				-6821.17	-2898.65
V56	VCCGT				-7313.93	-2898.65
V58	VCCGT				-7806.69	-2898.65
V60	VCCGT				-8299.45	-2898.65
V62	VCCGT				-8792.21	-2898.65
V64	VCCGT				-9310.37	-2898.65
V7	GPP_D22				7806.69	-2898.65
V9	GPP_D16 / ISH_UART0_CTS# / SML0BALERT#				7313.93	-2898.65
W10	GPP_C7 / SML1DATA				7067.55	-2576.58
W12	GPP_D21				6574.79	-2576.58
W2	VCCMPHYAON_1P0				9038.59	-2576.58
W4	GPP_C3 / SML0CLK				8545.83	-2576.58
W53	VCCGT				-6574.79	-2576.58
W55	VCCGT				-7067.55	-2576.58
W57	VCCGT				-7560.31	-2576.58
W59	VCCGT				-8053.07	-2576.58

Table 9-2. Y-Processor Ball List (Sheet 39 of 40)

Ball #	Ball Name	LPDDR3	Interleaved (IL)	Non-Interleaved (NIL)	X [um]	Y [um]
W6	GPP_C1 / SMBDATA				8053.07	-2576.58
W61	VCCGT				-8545.83	-2576.58
W63	VCCGT				-9038.59	-2576.58
W8	GPP_C2 / SMBALERT#				7560.31	-2576.58
Y1	VSS				9310.37	-2254.5
Y11	VSS				6821.17	-2254.5
Y13	VSS				6328.41	-2249.42
Y15	VSS				5846.1	-2428.51
Y16	VSS				5350.8	-2428.51
Y18	VCCCLK1				4855.5	-2428.51
Y19	VCCCLK2				4360.2	-2428.51
Y21	VCCCLK4				3864.9	-2428.51
Y23	VCCCLK3				3369.6	-2428.51
Y24	VSS				2874.3	-2428.51
Y26	VCCST				2379	-2428.51
Y27	VSS				1883.7	-2428.51
Y29	VCCSA				1388.4	-2428.51
Y3	VSS				8792.21	-2254.5
Y30	VCCSA				893.1	-2428.51
Y32	VCC				397.8	-2428.51
Y33	VSS				-97.5	-2428.51
Y35	VCCG0				-592.8	-2428.51
Y36	VSS				-1088.1	-2428.51
Y38	VCCG0				-1583.4	-2428.51
Y40	VSS				-2078.7	-2428.51
Y41	VCC				-2574	-2428.51
Y43	VCCGT				-3069.3	-2428.51
Y44	VCCGT				-3564.6	-2428.51
Y46	VCCGT				-4059.9	-2428.51
Y47	VCCGT				-4555.2	-2428.51
Y49	VCCGT				-5050.5	-2428.51
Y5	VSS				8299.45	-2254.5
Y50	VCCGT				-5545.8	-2428.51
Y51	VCCGT				-6041.1	-2428.51
Y54	VCCGT				-6821.17	-2254.5
Y56	VCCGT				-7313.93	-2254.5
Y58	VCCGT				-7806.69	-2254.5
Y60	VCCGT				-8299.45	-2254.5
Y62	VCCGT				-8792.21	-2254.5

Table 9-2. Y-Processor Ball List (Sheet 40 of 40)

Ball #	Ball Name	LPDDR3	Interleaved (IL)	Non-Interleaved (NIL)	X [um]	Y [um]
Y64	VCCGT				-9310.37	-2254.5
Y7	VSS				7806.69	-2254.5
Y9	VSS				7313.93	-2254.5

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