CH334/CH335 Datasheet

V1.6

Overview

CH334 and CH335 are 4-port USB HUB controllers which comply with USB Specification Revision 2.0. The upstream facing port supports both USB2.0 high-speed and full-speed modes, and the downstream facing ports support USB2.0 high-speed (480Mbps), full-speed (12Mbps) and low-speed (1.5Mbps) modes. The CH334 and CH335 not only support low-cost STT mode (single TT time-sharing schedules 4 downstream ports), but also support high-performance MTT mode (4 TTs process concurrently, each for one port).

One of the downstream facing ports of CH335 supports USB3.0 SuperSpeed passthrough upstream facing port.

CH334 and CH335 are industrial-grade designed, with simplified peripherals, can be applied to computers, industrial computer motherboards, peripherals, embedded systems, etc.

Features

- 4-port USB HUB controller, provides 4 downstream facing ports which comply with Universal Serial Bus Specification Revision 2.0, and backward compatible to USB Specification Revision 1.1
- Support both individual and GANG modes of power management for each port.
- Support both individual and GANG modes of over-current detection for each port, support 5V tolerant over-current signal input.
- Support high-performance MTT mode. MTT provides respective TT control logics for each port, to achieve full bandwidth concurrent transmission. The total bandwidth is 4 times that of STT.
- Supported port status LEDs.
- Configurations of device compound/non-compound setting, device removable/non-removable setting, VID/PID setting and ports control can be implemented by external EEPROM.
- Manufacturer/product information and configuration can be customized in batches according to the special needs of the industry.
- In-house developed dedicated USB PHY with low power. Compared with the first generation HUB IC, the power is greatly reduced. Support self-powered and bus-powered modes.
- Configuration of self/bus power mode setting can be implemented by either I/O pins or external EEPROM.
- Provide crystal oscillator, built-in capacitor. Support external 12MHz input. The built-in PLL provides 480MHz clock for USB PHY.
- Built-in upstream 1.5KΩ pull high. Built-in downstream pull-down resistors that are required by USB Host.
- Built-in LDO, which can convert USB bus power supply to 3.3V operating supply
- 6KV enhanced ESD performance, Class 3A.
- Industrial temperature range: -40~85℃
- Multiple packages with features of small size, low cost and easy processing: QFN28, SOP16, QSOP28.

Chapter 1 Pinning information

1.1 Pinouts

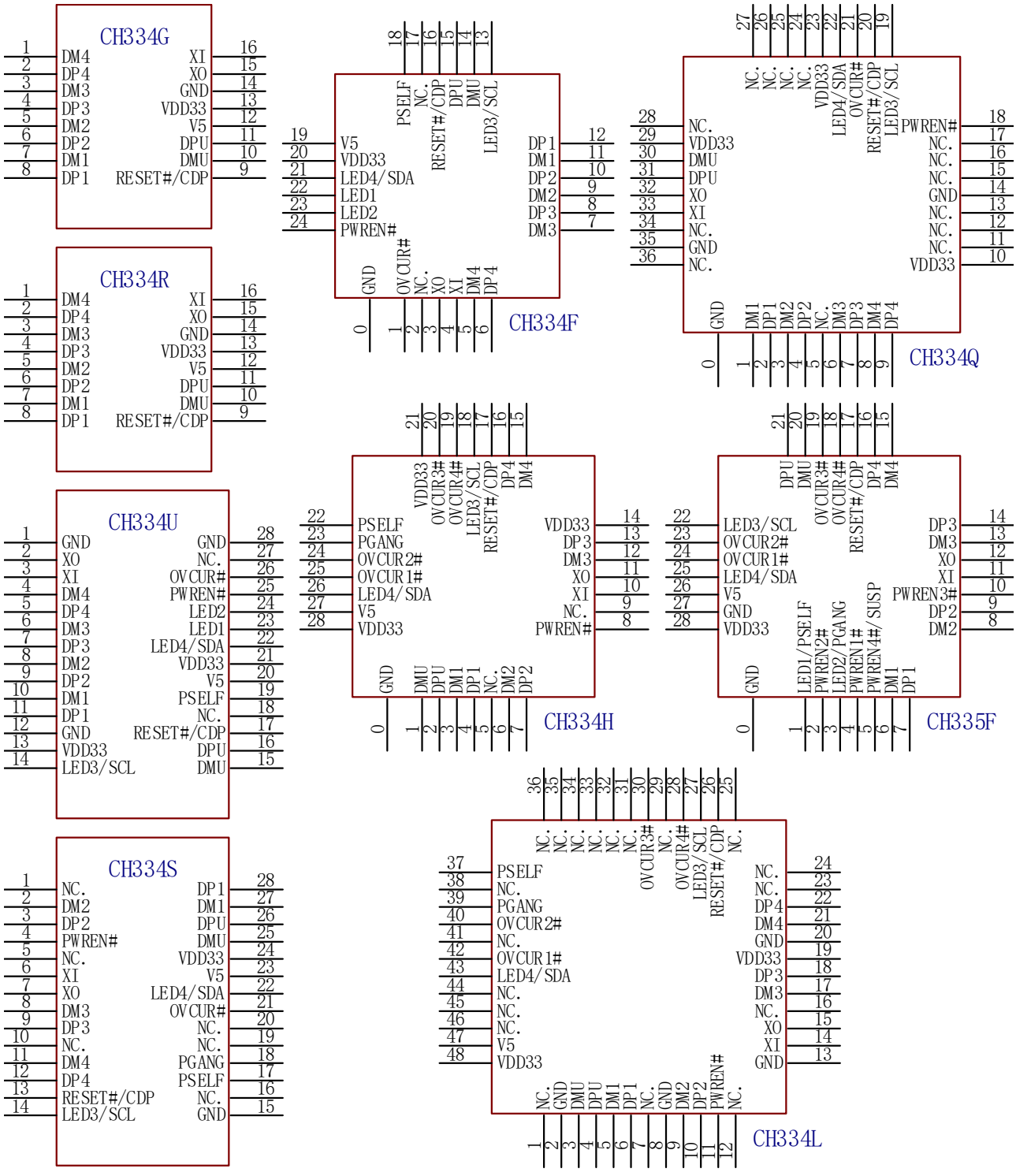


Figure 1-1 CH334 and CH335 pinouts

Note: Pin 0# refers to the EPAD of QFN package.

1.2 Comparison

Table 1-1 Comparison between CH334 and CH335

Part No. / Feature	CH334G	CH334R	CH334U CH334F	CH334S CH334Q	CH334H CH334L	CH335F
TT mode	STT	MTT	MTT	MTT	MTT	MTT
Over current detection	×	×	GANG	GANG	Individual	Individual/ GANG
Power management	×	×	GANG	GANG	GANG	Individual/ GANG
LED indicator	×	×	5/9	1	1	5/9
I/0 pin configuration in power supply mode	×	×	√	√	√	√
External EEPROM for configuration	×	×	√	√	√	√
Customized configuration	√	√	√	√	√	√
USB3.0 passthrough	×	—	—	—	—	√

1.3 Packages

Table 1-2 CH334/CH335 packages

Package	Body size		Lead pitch		Description	Part No.
SOP16	3.9mm	150mil	1.27mm	50mil	Standard 16-pin patch	CH334G
QSOP16	3.9mm	150mil	0.635mm	25mil	Quarter-sized 16-pin patch	CH334R
QSOP28	3.9mm	150mil	0.635mm	25mil	Quarter-sized 28-pin patch	CH334U
SSOP28	5.3mm	209mil	0.65mm	25mil	Shrink small outline 28-pin patch	CH334S
QFN24_4x4	4*4mm		0.5mm	19.7mil	Quad no-lead 24-pin	CH334F
QFN28_5x5	5*5mm		0.5mm	19.7mil	Quad no-lead 28-pin	CH334H
QFN36_6x6	6*6mm		0.5mm	19.7mil	Quad no-lead 36-pin	CH334Q
LQFP48	7*7mm		0.5mm	19.7mil	Standard LQFP 48-pin patch	CH334L
QFN28_4x4	4*4mm		0.4mm	15.7mil	Quad no-lead 28-pin	CH335F

Note: Some devices only support bulk pre-order, such as CH334S/Q/L. In addition, devices in QFN_3*3 package whose size is smaller are available in bulk.

1.4 Pin definitions

Table 1-3 CH334/CH335 pin definitions

Pin No. (For different packages, see description of pin with the same name)							Pin Name	Type	Description
335F	G/R	334F	334U	334S	334H	334L			
20	10	14	15	25	1	3	DMU	USB	Upstream facing port USB2.0 signal D-.
21	11	15	16	26	2	4	DPU	USB	Upstream facing port USB2.0 signal D+.
6	7	11	10	27	3	5	DM1	USB	1# downstream facing port USB signal D-.
7	8	12	11	28	4	6	DP1	USB	1# downstream facing port USB signal D+.
8	5	9	8	2	6	9	DM2	USB	2# downstream facing port USB signal D-.
9	6	10	9	3	7	10	DP2	USB	2# downstream facing port USB signal D+.
13	3	7	6	8	12	17	DM3	USB	3# downstream facing port USB signal D-.
14	4	8	7	9	13	18	DP3	USB	3# downstream facing port USB signal D+.
15	1	5	4	11	15	21	DM4	USB	4# downstream facing port USB signal D-.
16	2	6	5	12	16	22	DP4	USB	4# downstream facing port USB signal D+.
11	16	4	3	6	10	14	XI	I	12MHz Crystal Oscillator input.
12	15	3	2	7	11	15	XO	O	12MHz Crystal Oscillator output.
17	9	16	17	13	17	26	RESET# CDP	5I	RESET#: Active low. External reset input, with built-in pull-up resistor. It is recommended to be suspended when not reset.
26	12	19	20	23	27	47	V5	P	5V or 3.3V power input – a 1uF or larger capacitor is required.
28	13	20	21	24	28	48	VDD33	P	LDO output and 3.3V input – a 0.1uF decoupling capacitor and a 10uF decoupling capacitor are required, or a 1uF decoupling capacitor.
-	-	-	13	-	14 21	19	VDD33	P	3.3V power input – a 1uF decoupling capacitor is required.
27	14	-	1 12 28	15	-	2 8 13 20	GND	P	Ground.
0	-	0	-	-	0	-	GND	P	Ground (EPAD).
24	-	1	26	21	25	42	OVCUR# OVCUR1#	5I	Downstream facing ports over current detection input in GANG mode; Active low. 1# downstream facing port over current detection input.

23	-	-	-	-	24	40	OVCUR2#	5I	Active low. 2# downstream facing port over current detection input.
19	-	-	-	-	20	30	OVCUR3#	5I	Active low. 3# downstream facing port over current detection input.
18	-	-	-	-	19	28	OVCUR4#	5I	Active low. 4# downstream facing port over current detection input.
4	-	24	25	4	8	11	PWREN# PWREN1#	O	Downstream facing ports power output enable in GANG mode; Active low. 1# downstream facing port power output enable.
2	-	-	-	-	-	-	PWREN2#	O	Active low. 2# downstream facing port power output enable.
10	-	-	-	-	-	-	PWREN3#	O	Active low. 3# downstream facing port power output enable.
5	-	-	-	-	-	-	SUSP PWREN4#	O	SUSPEND sleep state output in GANG mode, 1 - suspend , 0 - normal; Active low. 4# downstream facing port power output enable.
-	-	18	19	17	22	37	PSELF	I	Power mode configuration, built-in pull-up resistor. 1 - self-powered mode, 0 - bus-powered mode.
-	-	-	-	18	23	39	PGANG	I/O	Power over-current protection mode configuration during reset, built-in pull-up resistor, set to sleep/normal output after reset: By default, GANG over current detection and GANG power control when at high level. After reset, output low for normal mode, and output high for sleep state; Individual over current detection when an external pull-down resistor is added and set to low. After reset, output high for normal mode, and output low for sleep mode.
1	-	22	23	-	-	-	LED1 PSELF	I/O	LED1: Port status indicator signal 1. PSELF: Power mode configuration during reset, built-in pull-up resistor. 1 - self-powered mode, 0 - bus-powered mode.
3	-	23	24	-	-	-	LED2 PGANG	I/O	LED2: Port status indicator signal 2. PGANG: Power over current protection mode

									configuration during reset, built-in pull-up resistor. 1 - GANG over current detection and GANG power control mode, 0 - individual over current detection mode.
22	-	13	14	14	18	27	LED3 SCL	I/O	LED3: Port status indicator signal 3. SCL: EEPROM clock signal output during reset.
25	-	21	22	22	26	43	LED4 SDA	I/O	LED4: Port status indicator signal 4 SDA: EEPROM bidirectional data signal during reset.
-	-	2 17	18 27	1 5 10 16 19 20	5 9	*	NC.		No connection and reserved pins, which cannot be connected.

Type:

(1) I: 3.3V signal input

(2) O: 3.3V signal output. PWREN means 3.3V to 4.5V signal output.

(3) 5I: Rated 3.3V signal input, support 5V tolerant.

(4) P: Power/Ground

Chapter 2 System architecture

2.1 System architecture

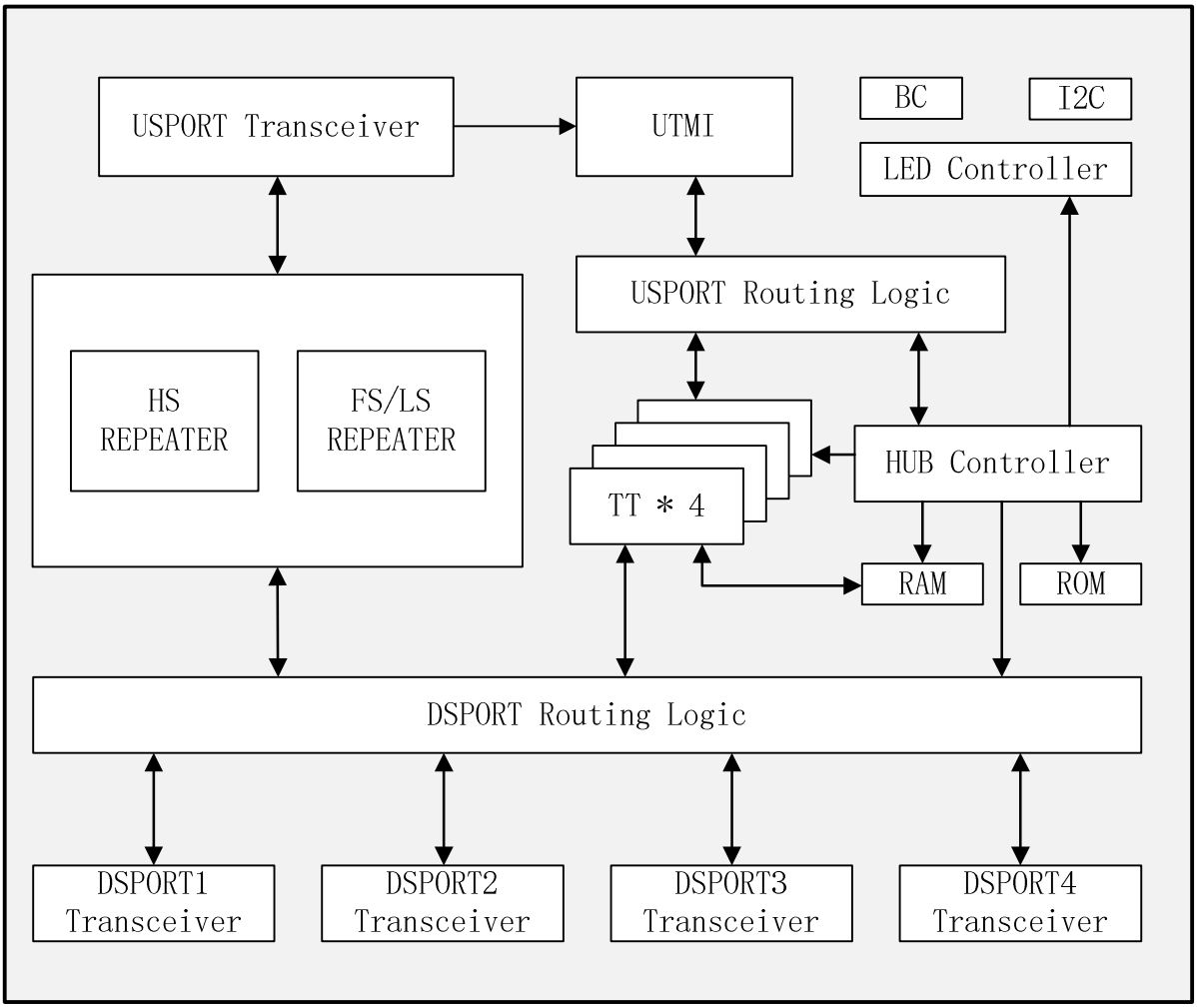


Figure 2-1 System architecture diagram

The internal architecture block diagram of the HUB controller system is shown in Figure 2-1. The HUB controller mainly includes 3 modules: Repeater, TT and controller. The controller is similar to the MCU processor for global management and control. When the speed of the upstream facing port is the same as the speed of the downstream facing port, the routing logic will connect the port to the Repeater. When the speed of the upstream facing port is different from the speed of the downstream facing port, the routing logic will connect the port to the TT.

TT is divided into 2 types: single TT (STT) and multiple TT (MTT). STT refers that single TT core time-sharing to schedule and process the transactions sent by the USB host to all downstream facing ports. MTT refers that multiple TTs run simultaneously, that is, the 4 TT cores respectively process one transaction of a corresponding downstream facing port in real time, so MTT can provide a fuller bandwidth for the access devices of each downstream facing port, and better support the concurrent transmission of large amounts of data on multiple ports.

Note:

USPORT Transceiver: Upstream facing port transceiver PHY

DSPORT Transceiver: Downstream facing port transceiver PHY

REPEATER: HUB repeater

TT: Transaction translator

Chapter 3 Functional description

3.1 Over current detection

CH334/CH335 supports 3 types of over current protection mode: Individual power management and individual over current detection, GANG power management and individual over current detection, and GANG power management and GANG over current detection. As shown in Table 3-1:

Table 3-1 Descriptions of over current protection control pins

Over current protection mode	Power control pin	Sampling pins for over current detection	Schematic for reference
Dual individual mode	PWREN1#, PWREN2#, PWREN3#, PWREN4#	OVCUR1#, OVCUR2#, OVCUR3#, OVCUR4#	Figure 3-1-1
GANG management and individual detection mode	PWREN1# or PWREN#	OVCUR1#, OVCUR2#, OVCUR3#, OVCUR4#	Figure 3-1-2
GANG mode	PWREN1# or PWREN#	OVCUR1# or OVCUR#	Figure 3-1-3

CH335F supports dual individual mode and GANG mode. CH334H/L supports GANG management and individual detection mode, and also supports GANG mode. CH334U/S/F/Q only supports GANG mode. CH334G/R does not support over current detection.

3.1.1 Dual individual mode

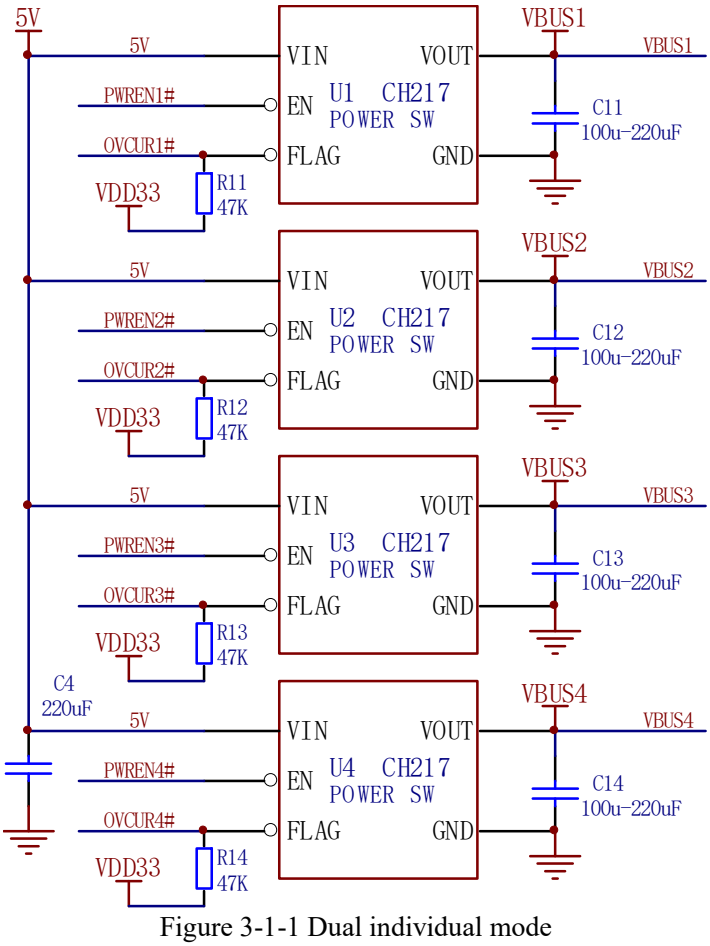


Figure 3-1-1 Dual individual mode

Devices U1, U2, U3 and U4 are USB current-limit power switches, which integrate overcurrent detection and are used for VBUS power management, such as CH217 or devices with similar functions. In 5V applications without external power supply, it is recommended to set the current limit below 1A or even 500mA. The FLAG pins of devices U1~U4 are open-drain outputs, and resistors R11~R14 need to be pulled up respectively. In the default configuration, OC_LEVEL=0, and resistors R11~R14 can be omitted as the OVCUR# pin of the HUB device provides built-in weak pull-up current. The capacitance of capacitors C11~C14 can be selected as required, and the minimum is 120uF in the specification. In dual individual mode, configure GANG_MODE=0 to select individual overcurrent detection mode.

As shown in Figure 3-1-1, VBUS1/VBUS2/VBUS3/VBUS4 are connected to VBUS power pins of the downstream facing port1/2/3/4 respectively.

3.1.2 GANG management and individual detection mode

The preferred GANG management and individual detection circuit is modified based on the Figure 3-1-1 Dual individual mode circuit, and PWREN# is used to control devices U1~U4 at the same time. Considering that capacitors C11~C14 are charged at the same time when the 4 switches are turned on, it is recommended that the capacitance of C4 should not be less than the cumulative capacitance of C11~C14.

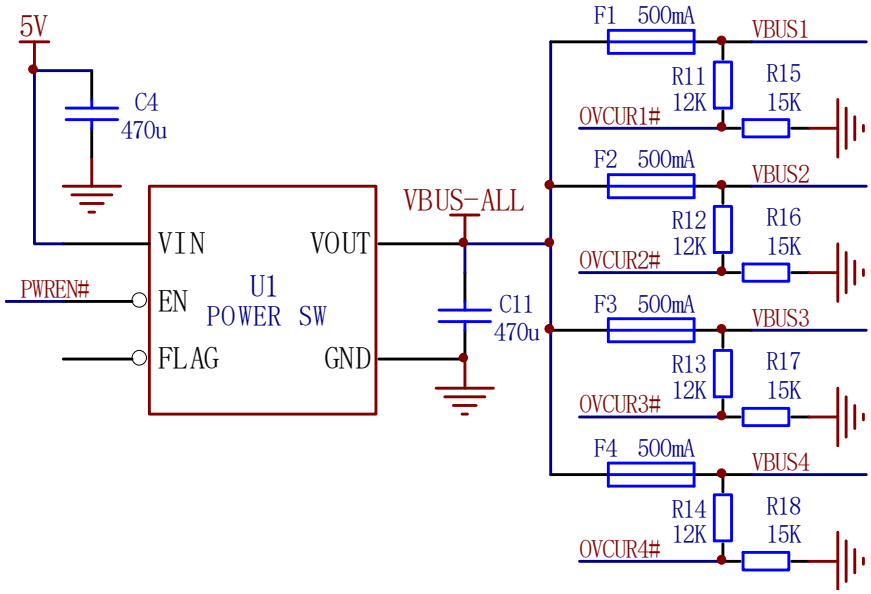


Figure 3-1-2 Another GANG management and individual detection mode circuit (not preferred)

Figure 3-1-2 shows another circuit. The U1 device is a shared power switch. The F1 to F4 are fuse resistors. Select C11 as required.

In addition, a simplified application circuit with power control removed is also available, based on Figure 3-1-2, omitting U1/C4 and shorting VBUS-ALL to 5V.

3.1.3 GANG mode

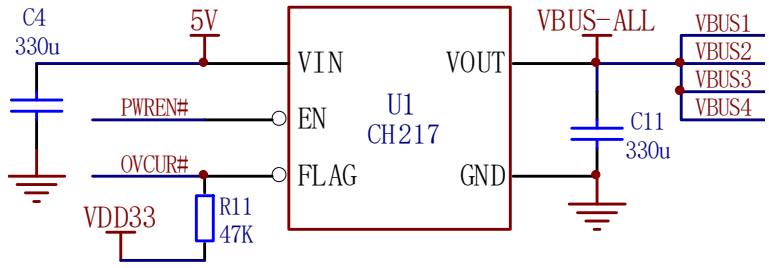


Figure 3-1-3 GANG mode

The U1 is a USB current-limit power switch. R11 can be omitted in the default configuration. Select C11 as required. VBUS-ALL is connected to the VBUS power pins of downstream facing port1/2/3/4. The setting of the current limit value of U1 needs to consider the 4 downstream facing ports and whether U1 is self-powered.

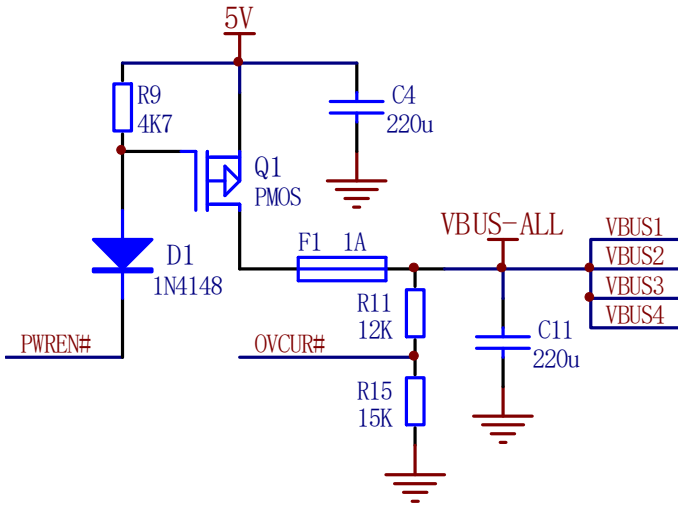


Figure 3-1-4 Simplified GANG mode power control and over current detection circuit

Figure 3-1-4 is a simplified schematic diagram, for principle reference only. In the default configuration, OC_LEVEL=0, the R11 and R15 resistors divide the voltage, and the voltage on the overcurrent detection point is about 4V. If OC_LEVEL=1, R15 can be removed and the resistance of R11 can be changed to 1K.

3.2 Reset

The chip has built-in power-on reset module. Generally, an external reset signal is not needed. The chip provides an alternate pin RESET#/CDP for external reset input, which has a built-in pull-up resistor.

3.2.1 Power on reset

When powered on, the internal power on reset module (POR) generates power-on reset timing, and delays (Trpor) about 12mS to wait for the power supply to stabilize. During operation, when the supply voltage is lower than V_{lvr}, the internal low-voltage reset module (LVR) generates low-voltage reset until the voltage rises, and delay to wait for the power supply to stabilize. Power on reset process and low-voltage reset process are shown in Figure 3-2.

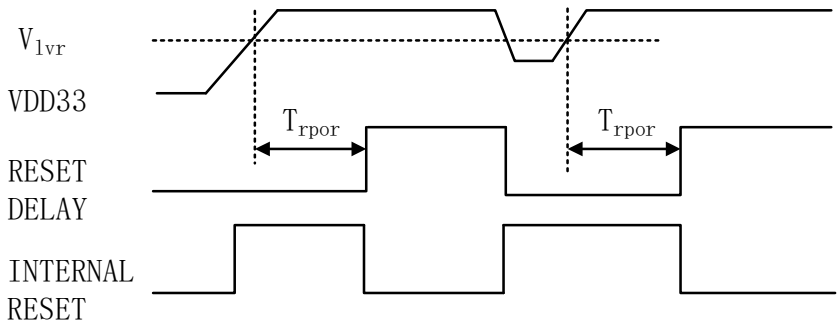


Figure 3-2 Power on reset

3.2.2 External reset

The external reset input pin (RESET#/CDP) has a built-in 25KΩ pull-up resistor. If external reset is needed, set this pin to low, and it is recommended that the driving internal resistance should not be greater than 800Ω and the low level pulse width for reset should be greater than 4uS.

For applications where the MCU pin directly drives the RESET#/CDP pin of HUB chip, the charging function of CH334/CH335 may be enabled and low-power Sleep mode may be disabled if the MCU pin outputs high level when power on. To avoid charging function to be enabled and to reduce sleep current, a diode should be connected in series between the MCU pin and the RESET#/CDP pin of HUB chip (cathode is connected with MCU pin).

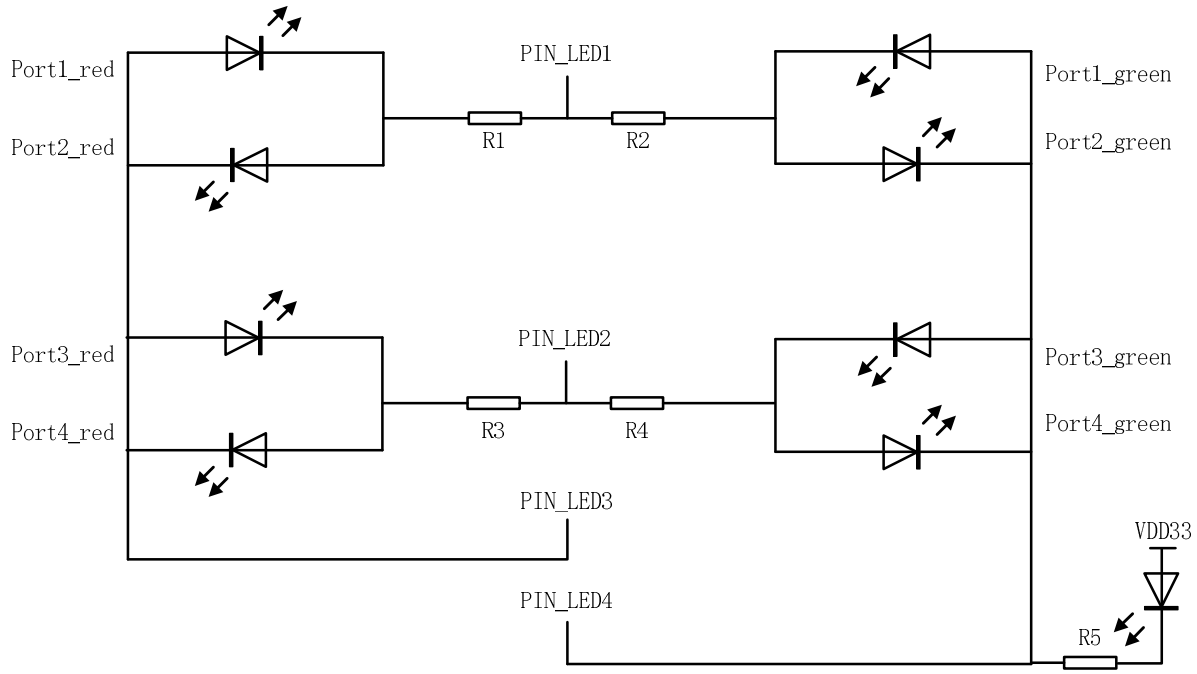
3.2.3 Charging function

In addition to CDP, Type-C and USB PD high-voltage fast charging complete solutions are available.

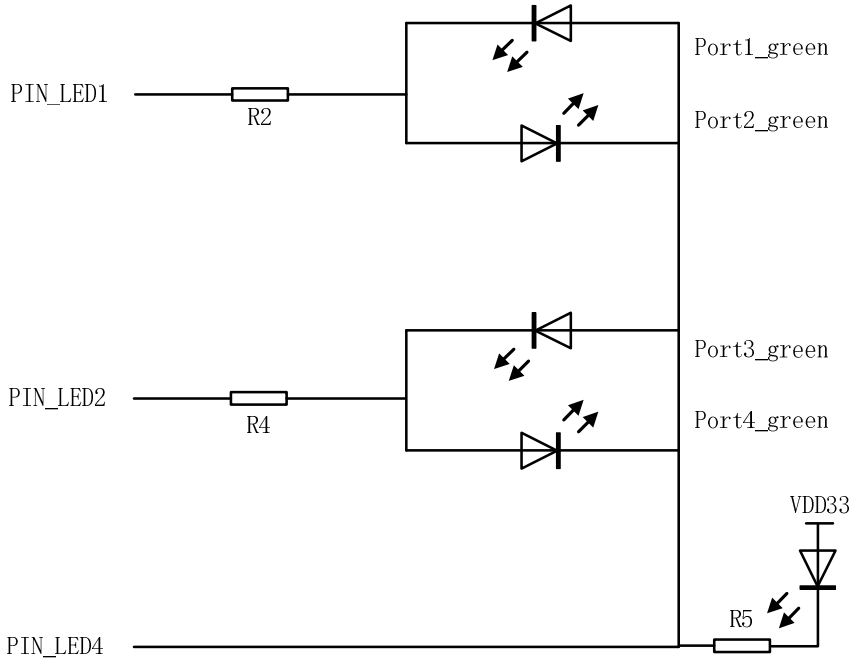
3.3 LED indicator

According to USB2.0 protocol specification, CH334/CH335 provides downstream facing port status LED indicator control pins. The green LED is on to indicate that the port is in normal state. The green LED is off to indicate that the port is not connected with a device or the port is suspended. The red LED is on to indicate that the port is abnormal. CH334/CH335 supports single LED mode (the blue LED in series with R5, ON means Active, and OFF means Suspend), 5-LED mode and 9-LED mode depending on different packages. The details is shown in figure 3-3, the resistance of the LED current limiting resistors (R1~R5) is 220Ω, and the resistance is optional, which can range from 100Ω to 1KΩ.

The LED1 and LED2 can also be used to configure PSELF and PGANG. For configuration, an external 10KΩ pull-down resistor is required, and the resistance can range from 3KΩ to 12KΩ. Since they are also used as LED driver outputs, LED1 and LED2 cannot be directly shorted to GND. For CH335, it is not recommended to configure LED1/PSELF or LED2/PGANG pull-down (may conflict) if LED1 or LED2 is connected to LED, EEPROM configuration and custom configuration are recommended.



(a) 9-LED mode



(b) 5-LED mode

Figure 3-3 LED indicators diagram

3.4 EEPROM configuration interface

CH334 and CH335 both provide I2C interface to communicate with external EEPROM memory chip. The address of the EEPROM chip is 0. The EEPROM chip has stored custom manufacturer ID, product ID, configuration and other information. The output clock frequency of SCL pin is 187.5 KHz. The SDA pin has built-in around 250uA pull-up current to support open-drain bidirectional data communication, and no external pull-up resistor is required.

3.5 EEPROM content

CH334/CH335 supports load VID, PID and other configuration information from the external EEPROM. After powered on, data in the internal ROM is firstly loaded. And the data in the external EEPROM is loaded after that. If CHKSUM of the data in EEPROM is invalid, the data in EEPROM will be abandoned. If the CHKSUM is valid, the data in EEPROM is loaded. The details of EEPROM address assignment is shown in Table 3-3. The address descriptions of EEPROM is shown in Table 3-4.

Table 3-3 EEPROM address assignment

	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F
00h	VID_L	VID_H	PID_L	PID_H	CHK SUM	FF	Device Removable	Port Number	Max Power	SIG	CFG	FF	FF	FF	FF	FF
10h	Vendor Length	Vendor String (UNICODE)														
20h																
30h	Vendor String End															
40h	Product Length	Product String (UNICODE)														
50h																
60h	Product String End															
70h	SN Length	Serial Number String (UNICODE)														
80h-BFh	Serial Number String End															
C0h-FFh	Reserved															

Table 3-4 EEPROM address descriptions

Byte address	Parameter name	Description	Default value
00h	VID_L	Low byte of VID	86h
01h	VID_H	High byte of VID	1Ah
02h	PID_L	Low byte of PID	depend on the chosen device
03h	PID_H	High byte of PID	80h
04h	CHKSUM	CHKSUM must be equal to VID_H+VID_L+PID_L+PID_H+1. Otherwise all data in EEPROM is ignored.	
06h	Device	Bit7~Bit5: Reserved.	00h

	Removable	Bit4: The device connected to the downstream facing port 4 can be removed. 1 – unremovable, 0 – removable; Bit3: The device connected to the downstream facing port 3 can be removed. 1 – unremovable, 0 – removable; Bit2: The device connected to the downstream facing port 2 can be removed. 1 – unremovable, 0 – removable; Bit1: The device connected to the downstream facing port 1 can be removed. 1 – unremovable, 0 – removable. Bit0: Reserved.	
07h	Port Number	Number of downstream facing ports. The valid value ranges from 1 to 4.	04h
08h	Max Power	Maximum operating current. The unit is 2mA.	32h
09h	SIG	Signature of 0Ah information CFG valid. It must be 5Ah, otherwise CFG is invalid.	5Ah
0Ah	CFG	Bit7: Reserved. Bit6: EEPROM write enable. 0=write protection. 1=allowed to be written by USB tool. Bit5: Overcurrent detection level threshold select (OC_LEVEL). It is 0 by default. 0=2.4V and weak pulled up. 1=4.1V and weak pulled down. Select 4.1V when PMOS is used to simplify power control, otherwise select 2.4V. Bit4&3: Select how long to delay the detection of overcurrent after power on (OC_DELAY): 00: Around 300uS. Selected when the turn-on is fast and the VBUS capacitance is small; 01: Around 3mS; 10: Around 10mS; 11: Around 30mS. Selected when the turn-on is slow and the VBUS capacitance is large. Bit2: Configure the supply mode (SELF_POWER). It is 1 by default. 1=self-powered (recommended). 0=bus-powered. The EEPROM configuration takes precedence over the PSELF pin setting. Bit1: Indicator enable (INDICATOR_EN). It is 0 by default.	

		1=indicator enabled. 0=indicator disabled. Bit0: Configure the overcurrent protection mode of power supply (GANG_MODE). It is 1 by default. 1=GANG overcurrent detection. 0=Individual overcurrent detection. The EEPROM configuration takes precedence over the PGANG pin setting.	

Chapter 4 Parameters

4.1 Absolute maximum ratings

Stresses at or above the absolute maximum ratings listed in the table below may cause permanent damage to the device.

Symbol	Description	Min.	Max.	Unit
TA	Operating ambient temperature	-40	85	℃
TS	Storage ambient temperature	-55	150	℃
V5	LDO input voltage (V5 pin is connected to power, GND pin is connected to ground)	-0.4	5.5	V
VDD33	Operating voltage (VDD33 pin is connected to power, GND pin is connected to ground)	-0.4	4.0	V
V5I	Voltage on 5 V-tolerant input pins	-0.4	5.3	V
VUSB	Voltage on USB signal pins	-0.4	VDD33+0.4	V
VGPIO	Voltage on other (3.3V) input or output pins	-0.4	VDD33+0.4	V
VESD	ESD voltage on USB signal pins (human body model)	5K	7K	V

4.2 Electrical characteristics

Test conditions: TA=25℃, V5=5V or V5=VDD33=3.3V

Symbol	Description		Min.	Typ.	Max.	Unit
V5	LDO input voltage @V5	Internal LDO enabled	4.6	5.0	5.25	V
	For those with a “0” in the 5th digit from last of the batch number	Internal LDO enabled	3.8	4.2	4.5	
	External supply voltage @V5	Internal LDO is not required	3.2	3.3	3.4	
VDD33	LDO output voltage @VDD33	Internal LDO enabled	3.2	3.3	3.5	V
	External 3.3V voltage @VDD33	Internal LDO is not required	3.2	3.3	3.4	
ILDO	Internal LDO external load capability				20	mA
ICC	Operating current	Upstream High-Speed 4 downstream high-speed ports		85		mA
		Upstream High-Speed Single downstream high-speed port		42		mA
		Upstream High-Speed 4 downstream full-speed ports		25		mA

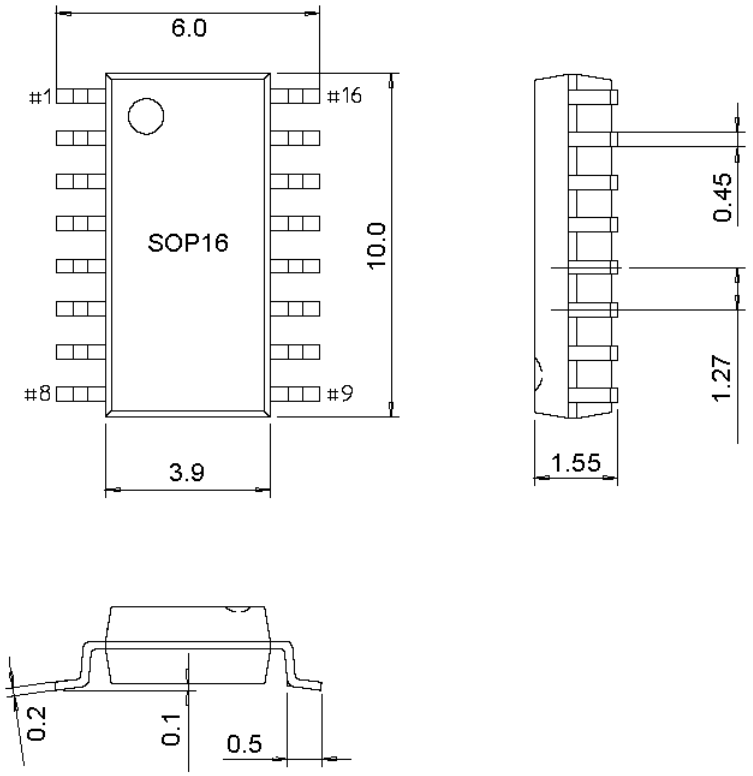
		Upstream High-Speed	Single downstream full-speed port		21		mA
		Upstream Full-Speed	4 downstream full-speed ports		20		mA
		Upstream High-Speed Upstream Full-Speed	No downstream device With a 1.5 KΩ pull-up resistor		0.27		mA
ISLP	Deep sleep supply current (with no 1.5KΩ pull-up) Or: Self sleep supply current (not connected to USB host)				0.07	0.3	mA
VIL	Low level input voltage for pins except over-current detection pins			0		0.8	V
VIH	High level input voltage for pins except over-current detection pins			1.9		VDD33	V
VILRST	Low level input voltage for RESET# pin			0		0.75	V
VIX	Error of over-current detection voltage threshold (OC_LEVEL)				±0.2		V
VOL	Low level output voltage	LED pins, input 15mA current			0.5	0.6	V
		PWREN# pins, input 4mA current			0.4	0.6	V
VOH	High level output voltage	LED pins, output 10mA current		VDD33-0.6	VDD33-0.5		V
		PWREN# pins, output 1mA current			4.0		V
IPU	Pull-up current	LED1/2/3/PSELF/PGANG pins		30	50	80	uA
IPUOC	Pull-up current	OVCUR# pin		9	14	22	uA
IPDOC	Pull-down current	OVCUR# pin		2	5	40	uA
Vlvr	Low voltage reset threshold			2.4	2.8	3.1	V

Chapter 5 Package information

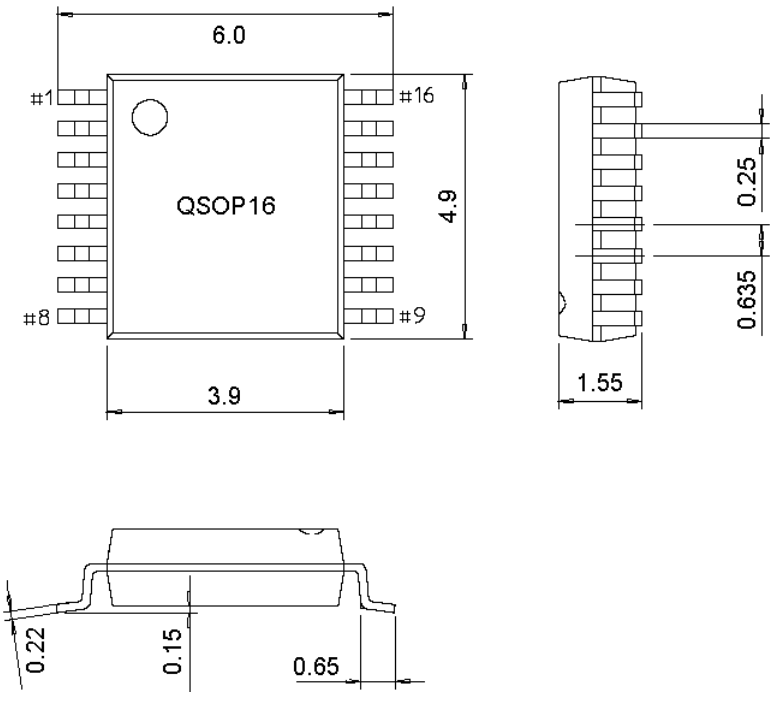
Note: All dimensions are in millimeters.

The pin center spacing values are nominal values, with no error. And the error of other dimensions is not more than ±0.2mm.

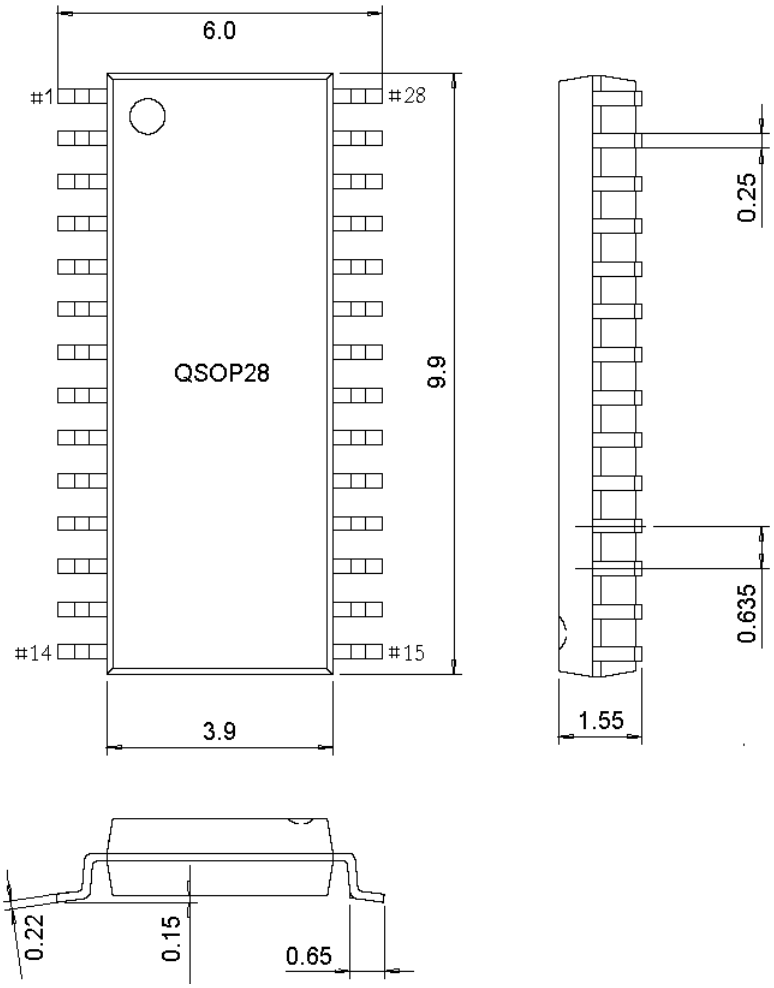
5.1 SOP16



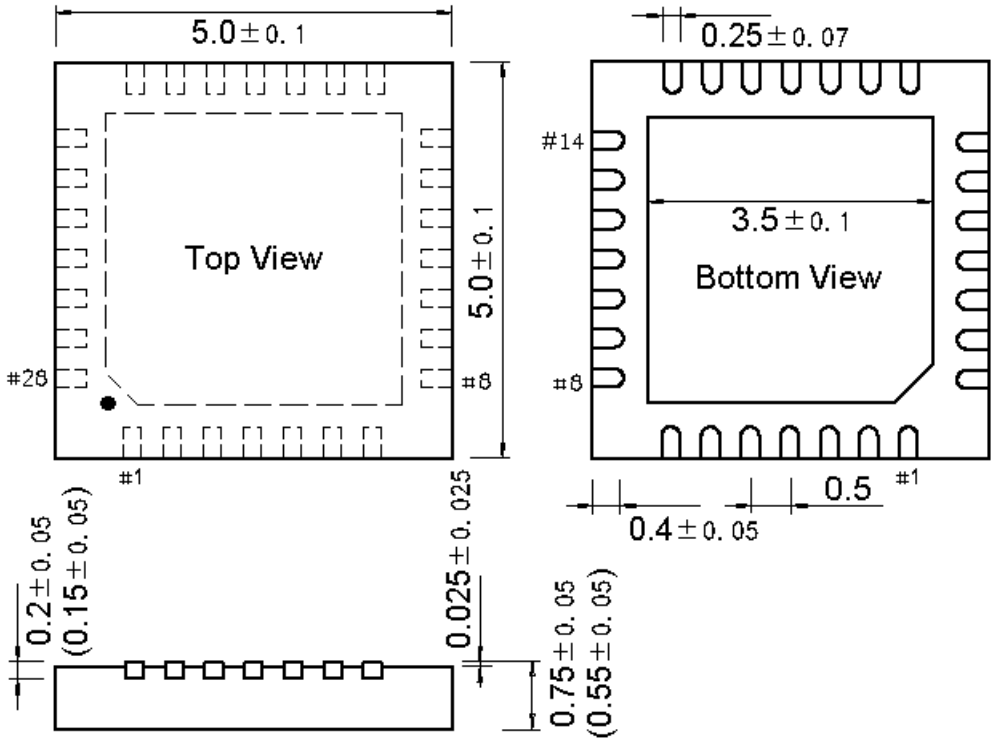
5.2 QSOP16



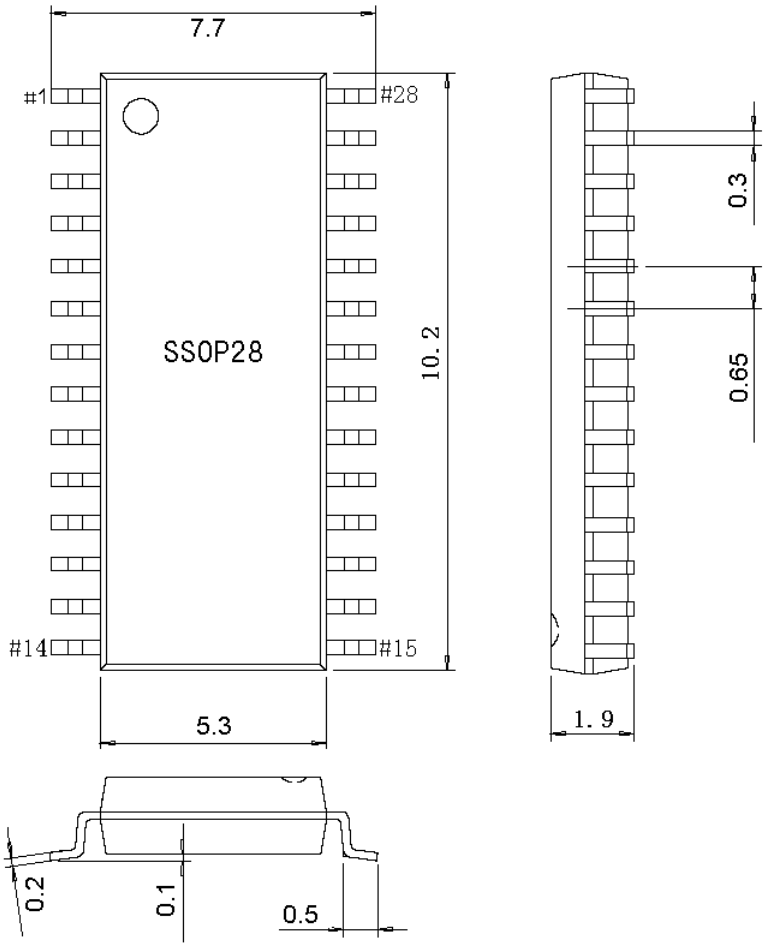
5.3 QSOP28



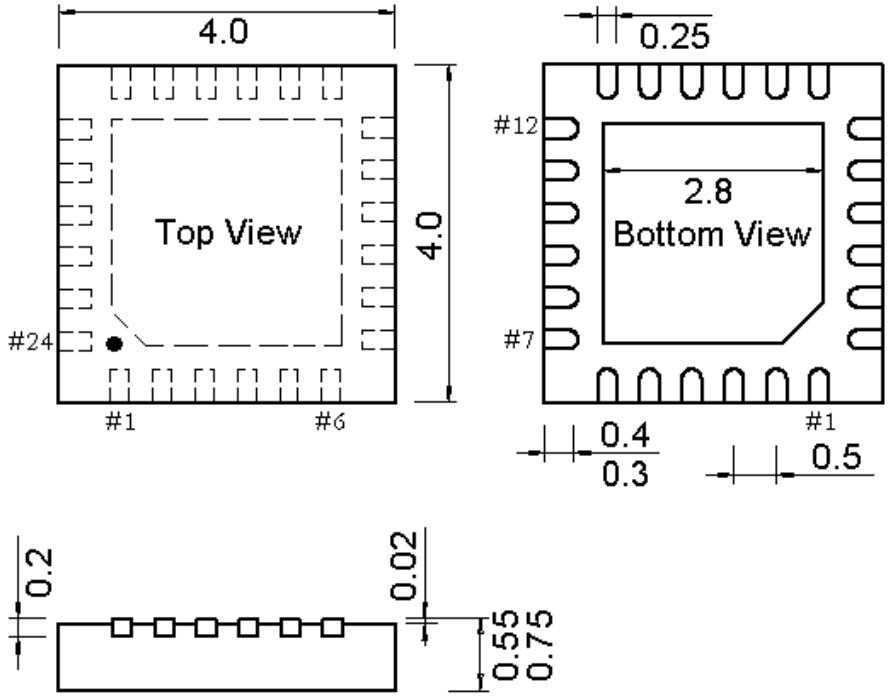
5.4 QFN28_5x5



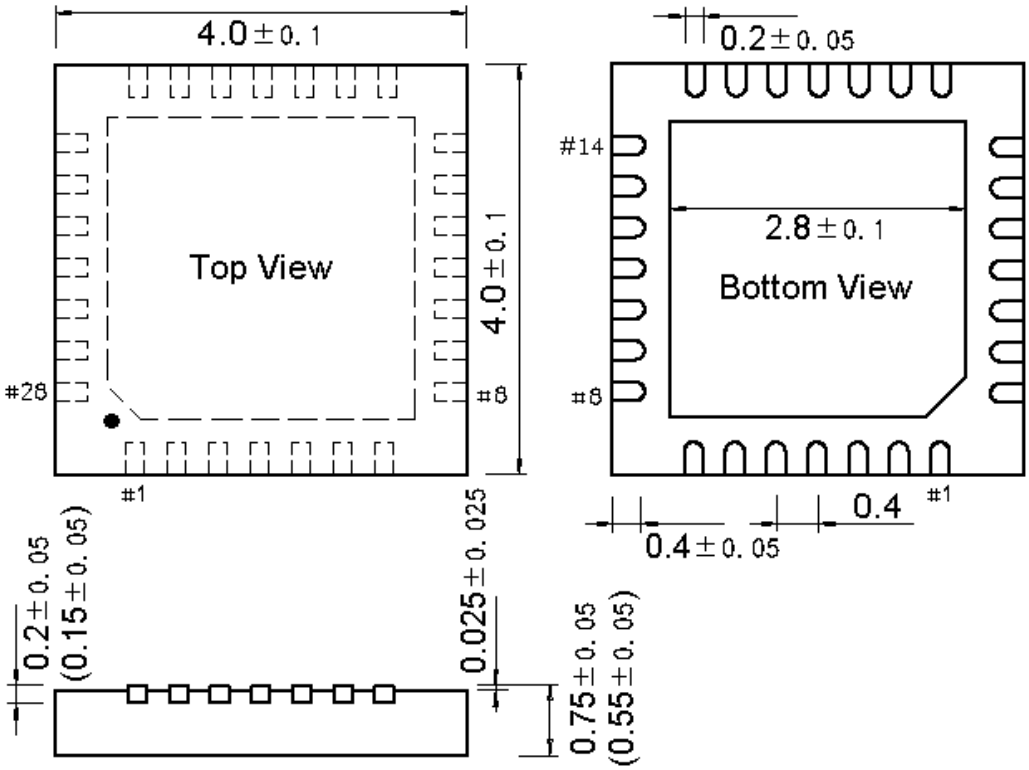
5.5 SSOP28



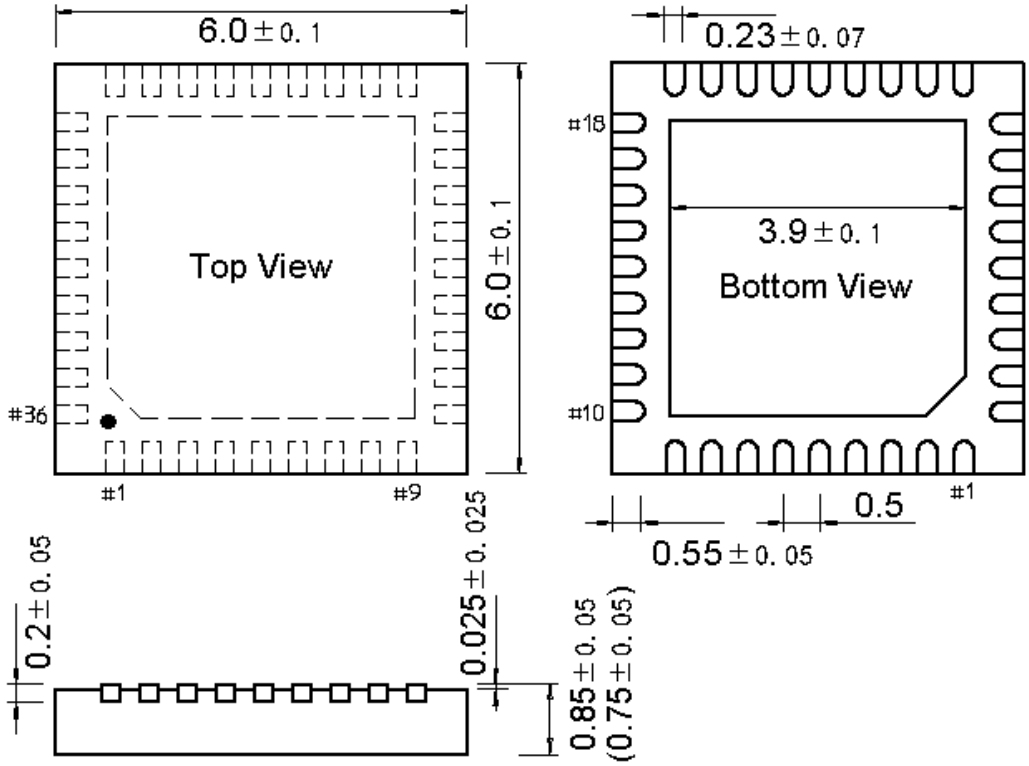
5.6 QFN24_4x4



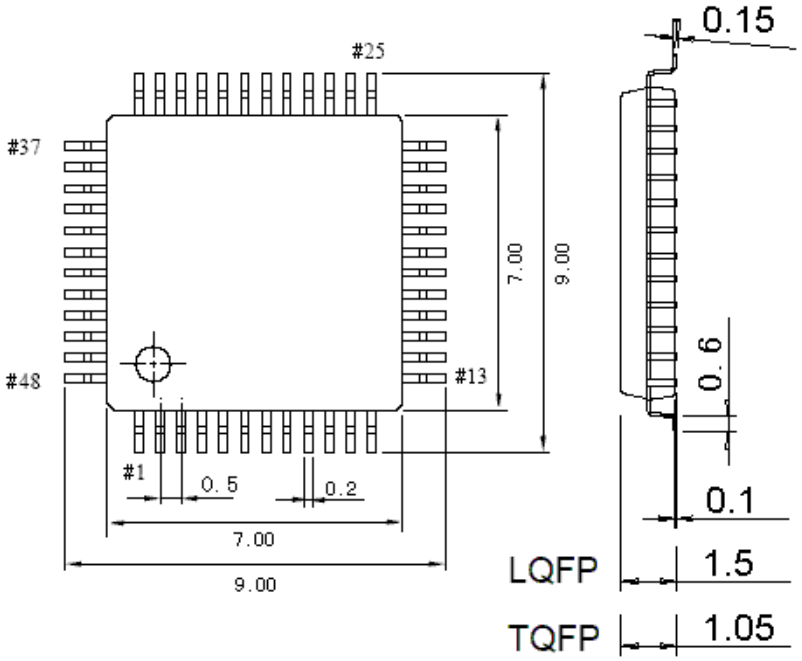
5.7 QFN28_4x4



5.8 QFN36_6x6

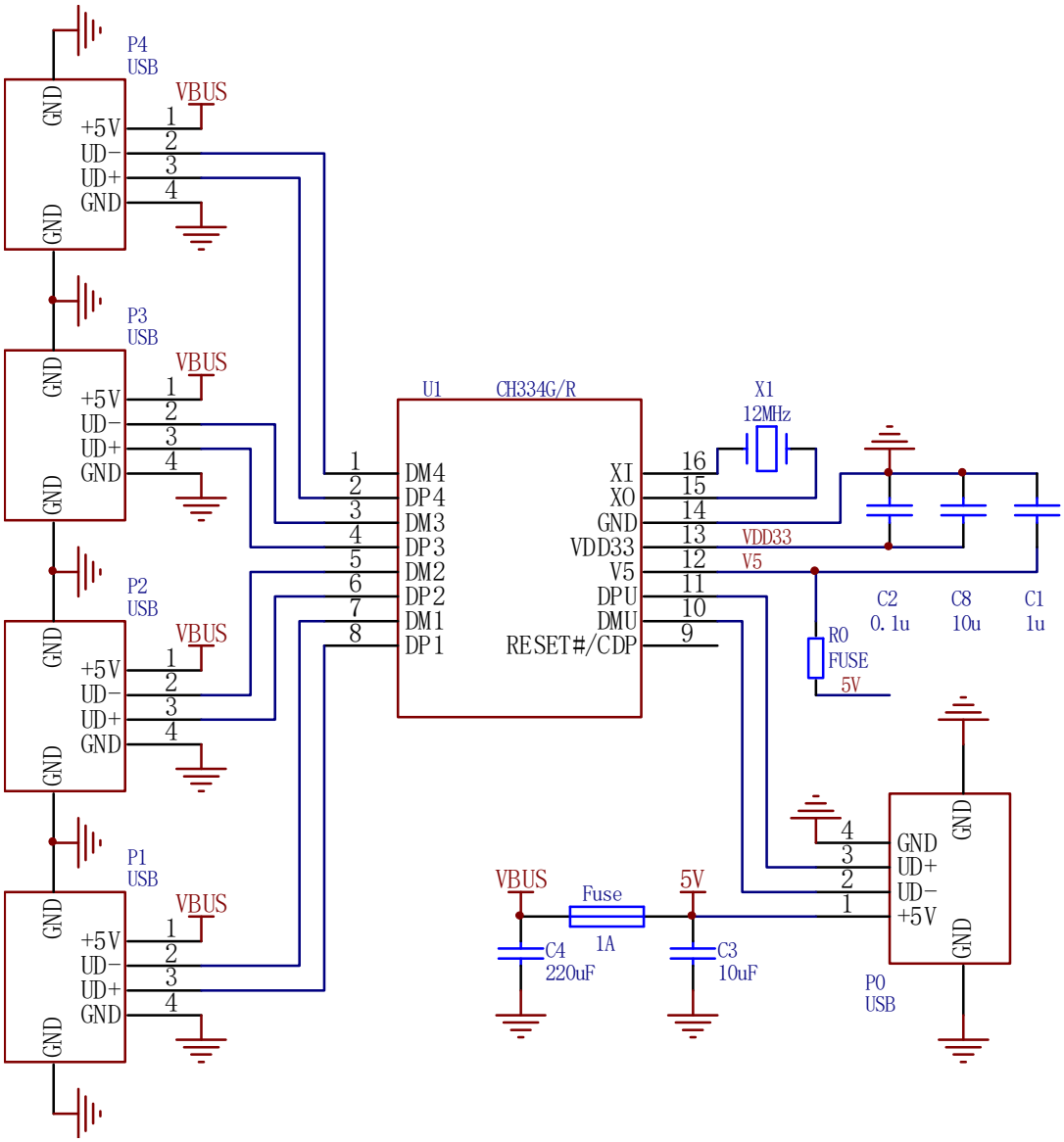


5.9 LQFP48



Chapter 6 Applications

6.1 Simplified application



R0 is a 100mA fuse resistor, and the resistance can be 0Ω in simplified applications. If there is an overvoltage protection device, connect it to the V5 pin.

For the first version of CH334 with a "0" in the 5th digit from last of the batch number, please replace R0 with a 1N4001 diode or similar.

The fuse resistor between 5V and VBUS can be replaced by a USB current-limit power switch chip, which is more effective.

For industrial-grade applications, V5 and VDD33 are recommended to be connected to external 3.3V power supply, to reduce the maximum power consumption of the HUB IC from 85mA*5V to 85mA*3.3V. This helps reduce the pressure drop and temperature rise of the HUB IC. The extended industrial-grade temperature can range from -40 ℃ to 105 ℃ (measured actually), and the chip works for a short time at 125 ℃ (parameters are not guaranteed). Note that the fuse resistors and USB power switches may not support high temperature.

At the moment when the USB device is hot-plugged into/out of the downstream facing port, the dynamic load may cause that the voltage on VBUS and 5V drops instantaneously, causing a low voltage reset (LVR), and then the entire HUB is disconnected and re-connected. The following improvements can be made: ① Increase the electrolytic capacitor of the 5V power supply within the allowable range (increase the capacitance of C4 as shown in the figure), to alleviate the 5V drop. ② Increase the capacitor connected to the LDO output of the HUB IC (increase the capacitance of C8, such as 22uF). ③ Disable the internal LDO of the HUB IC, externally supply 3.3V power to V5 and VDD33 pins, and increase the capacitor of the 3.3V power supply. ④ Enhance 5V power supply capability or change to self-powered. In addition, improve the quality of the USB cable and the power supply capability will be improved.

To implement power management and overcurrent protection, U1 in the figure can be replaced with other models of CH335 or CH334. It is noticed that overcurrent detection pins should not be suspended, and the unconnected OVCUR# pins are recommended to be pulled up by a 10KΩ resistor or directly connected to VDD33 (pulled up to V5 if OC_LEVEL=1), to avoid the unconnected OVCUR# pins being disturbed and in a false overcurrent state.

6.2 On-board embedded HUB

If there is an onboard 3.3V power supply, it is recommended to connect both V5 and VDD33 of the HUB IC to the 3.3V power supply. In this case, C8 and C2 can be combined and replaced with a 1uF capacitor (optional).

If the USB device is also always on-board, the USB device to the corresponding downstream facing port can be set to be non-removable, VBUS power control can be simplified, 5V can be directly supplied to the USB device, and the overcurrent detection can be simplified or cancelled.