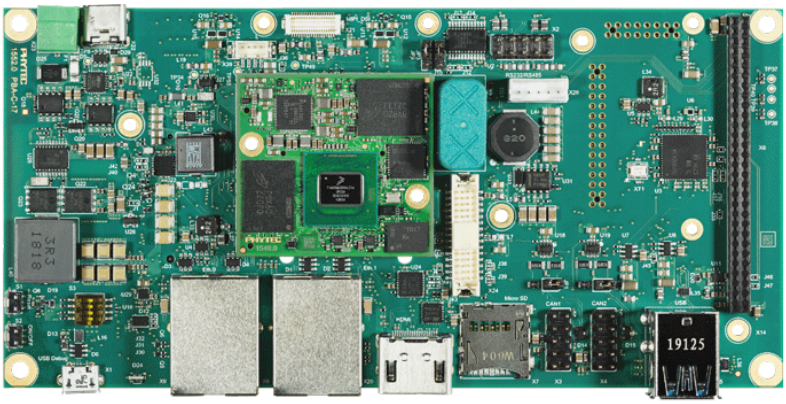
Hardware Manual - phyCORE-i.MX 8M Plus/ phyBOARD-Pollux (1549.3/1552.3) (L-1009e.A4)



Please Note

Information on the DSC version of the phyCORE-i.MX 8M Plus is highlighted in bold green. For more information, read Section 1.1 "Direct Solder Connection"

Thermal Management

Hardware Manual - phyCORE-i.MX 8M Plus/phyBOARD-Pollux (1549.3/1552.3) (L-1009e.A4)	
Document Title	Hardware Manual - phyCORE-i.MX 8M Plus/phyBOARD-Pollux (1549.3/1552.3) (L-1009e.A4)
Article Number	L-1009e.A4
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SOM Prod. No.	PCM-070 **/ PCL-070 (DSC)**
SOM PCB No.	1549.3 **/ 1561.1 (DSC)**
SBC Prod. No.:	PBA-C-17
CB PCB No.:	1552.3
Edition:	August 2026

1 Information on this Manual

This hardware manual describes the PCM-070 System on Module, referred to as phyCORE®-i.MX 8M Plus, and the PBA-C-17, referred to as phyBOARD®-Pollux. This manual also specifies the phyCORE-i.MX 8M Plus and phyBOARD-Pollux' design and function. Precise specifications for the NXP® Semiconductor i.MX 8M Plus microcontrollers can be found in the i.MX 8M Plus Microcontroller Data Sheet/Reference Manual.

There will be several changes and additions to this manual. New versions will be released in the future with no notice. Please make sure that you are using the latest version of this manual when working with your product.

1.1 Direct Solder Connection

PHYTEC produces a Direct Solder Connection (DSC) version of the phyCORE-i.MX 8M Plus SOM (PCL-070). PHYTEC uses a Direct Solder Connection Technology (DSC) for soldering SOMs directly onto the carrier board PCB.

The “Direct Solder Connect” of the SOM to carrier board eliminates costly PCB to PCB connectors, thereby reducing the board height. The DSC technology has an improved heat connection to the Carrier Board. It is characterized by high mechanical strength and adheres to standard norms such as those needed for railroad applications.

Information on the DSC version of the phyCORE-i.MX 8M Plus is highlighted in bold green. Please ensure you are using the correct information when working with your board.

1.2 Design Considerations

The schematics shown in this hardware manual are believed to be correct. However, correctness can not be guaranteed. The schematics have been pulled from PHYTEC's designs that have been built, tested, and is known to work. The schematics have been re-formatted to fit better in this hardware manual.

Many hardware examples and suggestions are given in the following pages. Designing the phyCORE System on Module onto a Carrier Board is generally straightforward. However, before committing to a particular active component selection when designing a carrier board, it is wise to check out the software driver support for those components. A particular device may be supported in, say, for example, Linux but not in Windows Embedded Compact 7. Your overall project may go smoother if you pick components that are already supported in your target OS. The premade selections for our reference designs, for example our Single Board Computers, are typically focused on using components that are well supported under Linux.

Specific details may need to be considered when designing a customer-specific carrier board. For design information on carrier board components, please check the ***Design Considerations*** in each component section of phyCORE-i.MX 8M Plus on the phyBOARD-Pollux. Be aware that not all components need to be considered when designing your own carrier board.

2 Preface

As a member of PHYTEC's phyCORE® product family, the phyCORE-i.MX 8M Plus is one of a series of PHYTEC System on Modules (SOMs) that can be populated with different controllers, various types of memory (RAM, NAND flash, eMMC), and many other features. This, in turn, offers increased types of functions and configurations. PHYTEC supports a variety of 8/16/32/64-bit controllers in two ways:

1. As the basis for Rapid Development Kits which serve as a reference and evaluation platform
2. As insert-ready, fully functional phyCORE® OEM modules, which can be embedded directly into the user's peripheral hardware design.

Implementation of an OEM-able SOM subassembly as the "core" of your embedded design allows for increased focus on hardware peripherals and firmware without expending resources to "reinvent" microcontroller circuitry. Furthermore, much of the value of the phyCORE® module lies in its layout and test.

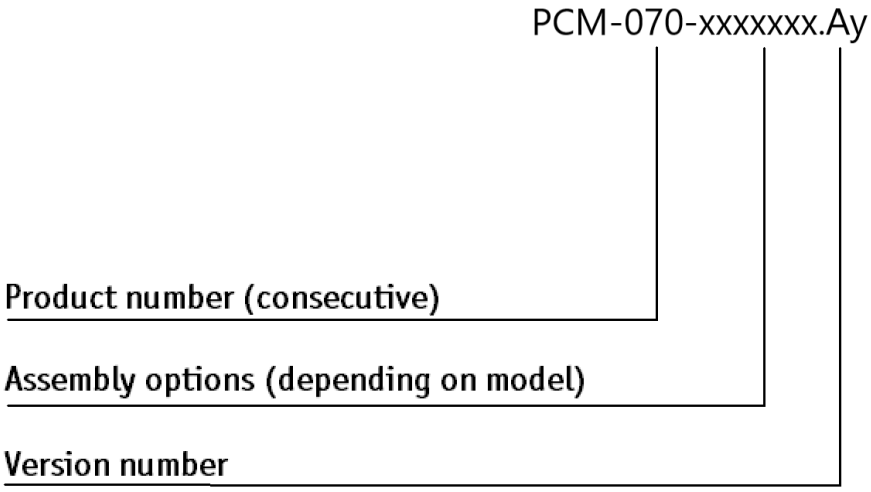
Production-ready Board Support Packages (BSPs) and Design Services for our hardware will further reduce development time and risk and allows for increased focus on product expertise. Take advantage of PHYTEC products to shorten time-to-market, reduce development costs, and avoid substantial design issues and risks. With this new innovative, full-system solution, new ideas can be brought to market in the most timely and cost-efficient manner.

For more information go to:

http://www.phytec.de/leistungen/entwicklungsunterstuetzung.html
or
http://www.phytec.eu/europe/oem-integration/evaluation-start-up.html

2.1 Ordering Information

The part numbering of the phyCORE PCM-070 has the following structure:



The part numbering for the DSC module of the phyCORE PCL-070 is following the same numbering schema.

2.2 Product Specific Information and Technical Support

In order to receive product-specific information on all future changes and updates, we recommend registering at: http://www.phytec.de/support/registrierung.html or http://www.phytec.eu/europe/support/registration.html

For technical support and additional information concerning your product, please visit the support section of our website which provides product-specific information, such as errata sheets, application notes, FAQs, etc.
https://www.phytec.de/produkte/system-on-modules/phycore-imx-8m-plus/
or
https://www.phytec.com/product/phycore-i-mx-8m-plus/

Note

Assembly Options include a choice of Controller, RAM (Size/Type), Size of NAND Flash, interfaces available, vanishing, temperature range, and other features. Please contact our sales team to get more information on the ordering options available.

2.3 Declaration of Electro Magnetic Conformity of the PHYTEC phyCORE®-i.MX 8M Plus CE

PHYTEC System on Modules are designed for installation in electrical appliances or as dedicated Evaluation Boards (i.e.: for use as a test and prototype platform for hardware/software development) in laboratory environments.

Warning

PHYTEC products lacking protective enclosures are subject to damage by ESD and, therefore, must be unpacked, handled, or operated in environments in which sufficient precautionary measures have been taken with respect to ESD dangers. Only appropriately trained personnel such as qualified electricians, technicians, and engineers should handle and/or operate these products. Moreover, PHYTEC products should not be operated without protection circuitry if connections to the product's pin header rows are longer than 3 m.

PHYTEC products fulfill the norms of the European Union's Directive for Electro Magnetic Conformity in accordance with the descriptions and rules of usage indicated in this hardware manual (particularly in respect to the pin header row connectors, power connector, and serial interface to a host-PC).

Tip

Implementation of PHYTEC products into target devices, as well as user modifications and extensions of PHYTEC products, is subject to renewed establishment of conformity to and certification of Electro Magnetic Directives. Users should ensure conformity following any modifications to a product as well as the implementation of a product into target systems.

2.4 Product Change Management and Information Regarding Parts Populated on the SOM / SBC

With the purchase of a PHYTEC SOM / SBC, you will, in addition to our hardware and software possibilities, receive free obsolescence maintenance service for the hardware we provide. Our PCM (Product Change Management) team of developers is continuously processing all incoming PCNs (Product Change Notifications) from vendors and distributors concerning parts that are used in our products. Possible impacts on the functionality of our products due to changes in functionality or obsolesce of certain parts are constantly being evaluated in order to take the right measures either in purchasing decisions or within our hardware/software design.

Our general philosophy here is: **We will never discontinue a product as long as there is a demand for it.**

To fulfill this, we have established a set of methods to fulfill our philosophy:

Avoidance strategies:

- Avoid changes by evaluating the longevity of parts during the design-in phase.
- Ensure the availability of equivalent second source parts.
- Stay in close contact with part vendors to keep up with roadmap strategies.

Change management in the rare event of an obsolete and non-replaceable part:

- Ensure long-term availability by stocking parts through last-time buy management according to product forecasts.
- Offer long-term frame contracts to customers.

Change management in cases of functional changes:

- Avoid impacts on product functionality by choosing equivalent replacement parts.
- Avoid impacts on product functionality by compensating for changes through hardware redesign or backward-compatible software maintenance.
- Provide early change notifications concerning functional, relevant changes to our products.

We refrain from providing detailed part-specific information within this manual, which can be subject to continuous changes, due to part maintenance for our products.
In order to receive reliable, up-to-date, and detailed information concerning parts used for our product, please contact our support team through the contact information given within this manual.

2.5 PHYTEC Documentation

PHYTEC will provide a variety of hardware and software documentation for all of our products. This includes any or all of the following:

- **QS Guide**: A short guide on how to set up and boot a phyCORE board along with brief information on building a BSP, the device tree, and accessing peripherals.
- **Hardware Manual**: A detailed description of the System on Module and accompanying carrier board.
- **Yocto Guide**: A comprehensive guide for the Yocto version the phyCORE uses. This guide contains an overview of Yocto; introducing, installing, and customizing the PHYTEC BSP; how to work with programs like Poky and Bitbake; and much more.
- **BSP Manual**: A manual specific to the BSP version of the phyCORE. Information such as how to build the BSP, booting, updating software, device tree, and accessing peripherals can be found here.
- **Development Environment Guide**: This guide shows how to work with the Virtual Machine (VM) Host PHYTEC has developed and prepared to run various Development Environments. There are detailed step-by-step instructions for Eclipse and Qt Creator, which are included in the VM. There are instructions for running demo projects for these programs on a phyCORE product as well. Information on how to build a Linux host PC yourself is also a part of this guide.
- **Pin Muxing Table**: phyCORE SOMs have an accompanying pin table (in Excel format). This table will show the complete default signal path, from processor to carrier board. The default device tree muxing option will also be included. This gives a developer all the information needed in one location to make muxing changes and design options when developing a specialized carrier board or adapting a PHYTEC phyCORE SOM to an application.

On top of these standard manuals and guides, PHYTEC will also provide Product Change Notifications, Application Notes, and Technical Notes. These will be done on a case-by-case basis. Most of the documentation can be found on the applicable download page of our products.

Tip

After finishing the Quickstart Guide, we recommend working through the Development Environment Guide. This will give you a comprehensive overview of the features and functions of both the SOM and carrier board.

These manuals and more can be found in the download section of phyCORE-i.MX 8M Plus Product page.

3 Conversions, Abbreviations, and Acronyms

Tip

Due to part maintenance for our products (which are subject to continuous changes), we refrain from providing detailed, part-specific information within this manual. Please read the section Product Change Management and Information Regarding Parts Populated on the SOM / SBC within the Preface for more information.

Tip

The BSP delivered with the phyCORE-i.MX 8M Plus usually includes drivers and/or software for controlling all components such as interfaces, memory, etc. Programming close to hardware at the register level is not necessary in most cases. For this reason, this manual does not contain detailed descriptions of the controller's registers or information relevant to software development. Please refer to the i.MX 8M Plus Reference Manual, if any information not found in this manual is needed to connect customer-designed applications.

3.1 Conventions

The conventions used in this manual are as follows:

- Signals that are preceded by an "n", "/", or “#”character (e.g.: nRD, /RD, or #RD), or that have a dash on top of the signal name (e.g.: RD) are designated as active low signals. That is, their active state is when they are driven low or are driving low.
- A "0" indicates a logic zero or low-level signal, while a "1" represents a logic one or high-level signal.
- The hex-numbers given for addresses of I2C devices always represent the 7 MSB of the address byte. The correct value of the LSB, which depends on the desired command (read (1), or write (0)), must be added to get the complete address byte. For example, if the given address in this manual is 0x41 =>, the complete address byte = 0x83 to read from the device and 0x82 to write to the device
- Tables that describe all settings show the default position in **bold, blue text**.

3.2 Types of Signals

Different types of signals are brought out at the phyCORE-Connector. The following table lists the abbreviations used to specify the type of signal.

TABLE 1: Signal Types

Signal Type	Description	Abbreviation
Power In	Supply voltage input	PWR_I
Power Out	Supply voltage output	PWR_O
Ref-Voltage	Reference voltage output	REF_O
Input	Digital input	I
Output	Digital output	O
I/O	Bidirectional input/push-pull output	I/O
Input/OD-Output	Input / open-drain output requires an external pull up	I/OD
OC-Bidir PU	Open collector input/output with pull up	OC-BI-PU
OC-Output	Open collector output without pull up requires an external pull up	OC
OD-Bidir PU	Open-drain input/output with pull up	OD-BI-PU
OD-Output	Open-drain output without pull up requires an external pull up	OD
5 V Input PD	5 V tolerant input with pull-down	5V-PD
USB IO	Differential line pairs 90 Ohm USB level bidirectional input/output	USB_I/O
ETHERNET Input	Differential line pairs 100 Ohm Ethernet level input	ETH_I
ETHERNET Output	Differential line pairs 100 Ohm Ethernet level output	ETH_O
ETHERNET IO	Differential line pairs 100 Ohm Ethernet level bidirectional input/output	ETH_I/O
PCIe Input	Differential line pairs 85 Ohm PCIe level input	PCIe_I
PCIe Output	Differential line pairs 85 Ohm PCIe level output	PCIe_O

Signal Type	Description	Abbreviation
PCIe IO	Differential line pairs 85 Ohm PCIe level input or output	PCIe_I/O
HDMI Input	Differential line pairs 100 Ohm HDMI level input	HDMI_I
HDMI Output	Differential line pairs 100 Ohm HDMI level output	HDMI_O
MIPI CSI-2 Input	Differential line pairs 100 Ohm MIPI CSI-2 level input	CSI2_I
MIPI DSI-2 Output	Differential line pairs 100 Ohm MIPI DSI-2 level output	DSI2_O
CAN FD IO	Differential line pairs 120 Ohm CAN FD level bidirectional input/output	CAN_I/O

3.3 Abbreviations and Acronyms

Many acronyms and abbreviations are used throughout this manual. Use the following table to navigate unfamiliar terms used in this document.

TABLE 2: Abbreviations and Acronyms Used in this Manual

Abbreviation	Definition
BGA	Ball Grid Array
BSP	Board Support Package (software delivered with the Development Kit, including an operating system (Windows or Linux) preinstalled on the module and development tools)
CB	Carrier board; used in reference to the phyCORE development kit carrier board
DSC	**Direct Soldering Contact**
EMI	Electromagnetic Interference
GPI	General-purpose input
GPIO	General-purpose input and output
GPO	General-purpose output
IRAM	Internal RAM: the internal static RAM on the NXP® Semiconductor i.MX 8M Plus microcontroller
J	Solder jumpers; these types of jumpers require solder equipment to remove and place
JP	Solderless jumpers; these types of jumpers can be removed and placed by hand with no special tools
OEM	Original Equipment Manufacturers
PCB	Printed circuit board
PCM	Product Change Management
PCN	Product Change Notification
PMIC	Power management IC

Abbreviation	Definition
RTC	Real-time clock
SBC	Single Board Computer
SMT	Surface mount technology
SOM	System on Module; used in reference to the PCM-070 /phyCORE®-i.MX 8M Plus module
Sx	User button Sx (e.g. S1, S2, etc.) used in reference to the available user buttons, or DIP-Switches on the carrier board
Sx_y	Switch y of DIP-Switch Sx; used in reference to the DIP-Switch on the carrier board
VM	Virtual Machine

4 phyCORE-i.MX 8M Plus Introduction

The phyCORE-i.MX 8M Plus belongs to PHYTEC's phyCORE System on Module family. The phyCORE SOMs represent the continuous development of the PHYTEC System on Module technology. Like its mini-, micro-, and nanoMODUL predecessors, phyCORE boards integrate all core elements of a microcontroller system on a subminiature board and are designed in a manner that ensures their easy expansion and embedding in peripheral hardware developments.

Independent research indicates that approximately 70 % of all EMI (Electro-Magnetic Interference) problems are caused by insufficient supply voltage grounding of electronic components in high-frequency environments. The phyCORE board design features an increased pin package, which allows for the dedication of approximately 20 % of all connector pins on the phyCORE boards to Ground. This improves EMI and EMC characteristics and makes it easier to design complex applications meeting EMI and EMC guidelines using phyCORE boards, even in high-noise environments.

phyCORE boards achieve their small size through modern SMT and multi-layer design. Due to the complexity of our modules, 0201-packaged SMT components and laser-drilled microvias are used on the boards, providing phyCORE users with access to this cutting-edge miniaturization technology for integration into their own design.

The phyCORE-i.MX 8M Plus is a subminiature (40 mm x 37 mm) insert-ready System on Module populated with the NXP® Semiconductor i.MX 8M Plus microcontroller. Its universal design enables it to be inserted into a wide range of embedded applications. All controller signals and ports extend from the controller to high-density pitch, or surface mount technology (SMT **1.27 mm grid**) connectors (all pitch 0.5 mm) aligning two sides of the board, allowing it to be plugged or soldered into any target application like a "big chip".

The descriptions in this manual are based on the NXP® Semiconductor i.MX 8M Plus. Descriptions of compatible microcontroller derivative functions are not included, as such functions are not relevant for the basic functioning of the phyCORE-i.MX 8M Plus.

4.1 phyCORE-i.MX 8M Plus Features

The phyCORE-i.MX 8M Plus offers the following features:

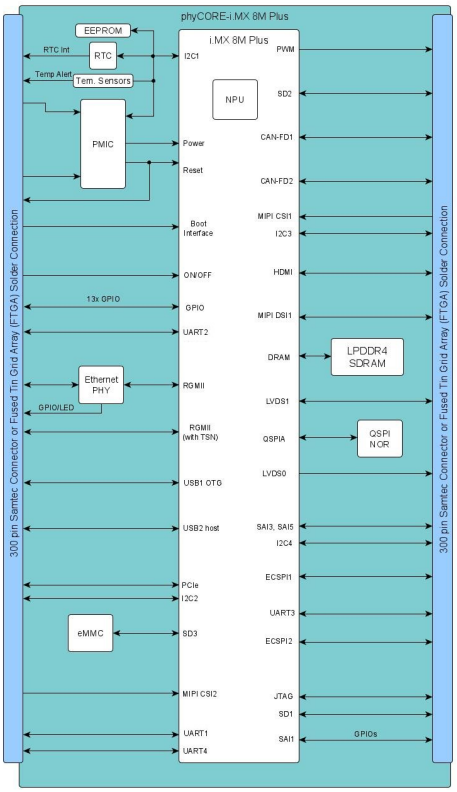
- Insert-ready, sub-miniature (40 mm x 37 mm) System on Module (SOM) subassembly in low EMI design, achieved through advanced SMD technology
- Mounted using Samtec Connectors or using a Direct Solder Connector (DSC)
- Populated with the NXP® Semiconductor i.MX 8M Plus microcontroller (BGA548 packaging)
- Up to 4 ARM-A53 cores (clock frequency up to 1.8 GHz)
- Machine Learning Neuronal Processing Unit (NPU) with 2.3 TOPS
- 1x Cortex M7 core (800 MHz). All Cortex M7 dedicated interfaces are explicitly made available on the SOM connector.
- Tensilica Hifi4 Audio DSP (800 MHz)
- 3D GPU GC7000UL and 2D GPU GC520L
- Neural Network Accelerator (up to 2.3TOPS)
- on-board Image Signal Processor (up to 12MP resolution/ up to 375MP/s)
- Boot from different memory devices (eMMC Flash standard)
- Single supply voltage of +3.3 V with on-board power management
- Selectable IO voltage between 1.8 V and 3.3 V
- All controller-required supplies are generated on-board using sophisticated on-board Power Management
- Improved interference safety achieved through multi-layer PCB technology and dedicated ground pins
- up to 8 GB[1] LPDDR4 RAM
- up to 64 GB[1] on-board eMMC in the commercial temperature range (up to 32 GB for I-Temp)
- up to 64 MB[1]Quad SPI Nor Flash

- 4kB[1] I^2C EEPROM
- 2x USB 3.0/2.0 Dual-Role interfaces with PHY
- 2x 1Gbit Ethernet interfaces with TSN support (either one of them with Ethernet transceiver on the phyCORE-i.MX 8 M Plus enabling a direct connection to an existing Ethernet network; the second as RGMII Signals at logic-level at the signal pins instead.)
- 3x I^2C interfaces
- 2x SPI interfaces
- 1x PCIe interface
- 4x UART interfaces
- 2x CAN-FD interfaces
- 4x PWM outputs
- 1x MIPI DSI-2 interface
- 1x HDMI interface
- 2x MIPI CSI-2 camera interfaces
- 1x LVDS Tx interface 2 channels x4
- 1x 4-bit SD-Card interface
- 1x 8-bit SDIO interface
- 2x SAI audio interfaces
- 1x SPDIF interface
- Extreme Low Power RTC Module
- 4x temperature sensors to monitor the board's temperature profile
- All processor interfaces available at the SOM Connector
- Available for different temperature grades (see Product Temperature Grades)

[1] The maximum memory size is listed as of the printing of this manual.
Please contact PHYTEC for more information about additional or new module configurations available.

4.2 phyCORE-i.MX 8M Plus Block Diagram

FIGURE 1: phyCORE-i.MX 8M Plus Block Diagram



4.3 phyCORE-i.MX 8M Plus Component Placement

FIGURE 2: phyCORE-i.MX 8M Plus Component Placement (1549.3 Top View)

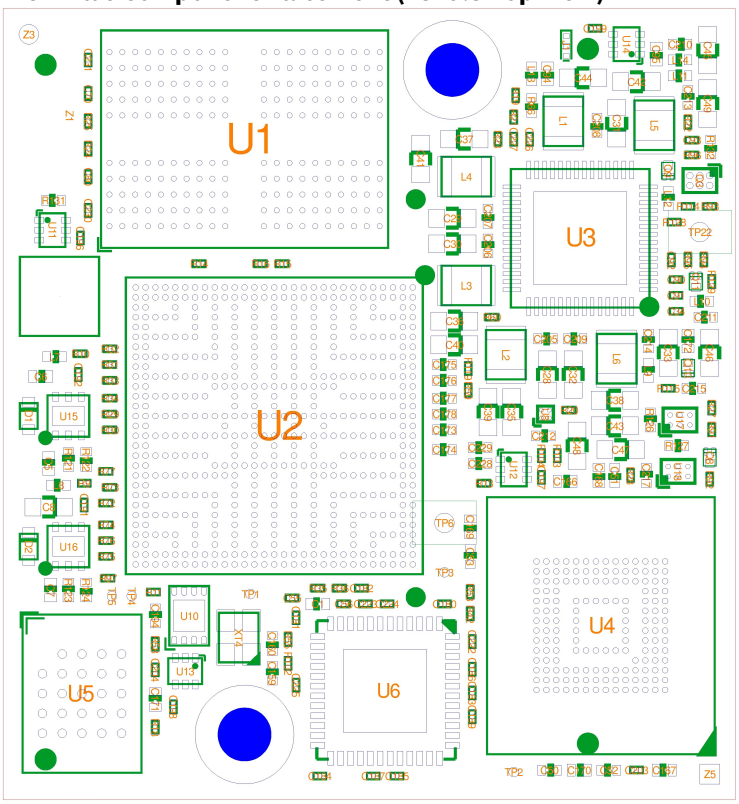


FIGURE 3: phyCORE-i.MX 8M Plus Component Placement (1549.3 Bottom View)



FIGURE 4: phyCORE-i.MX 8M Plus DSC Component Placement (1561.1 Top View)

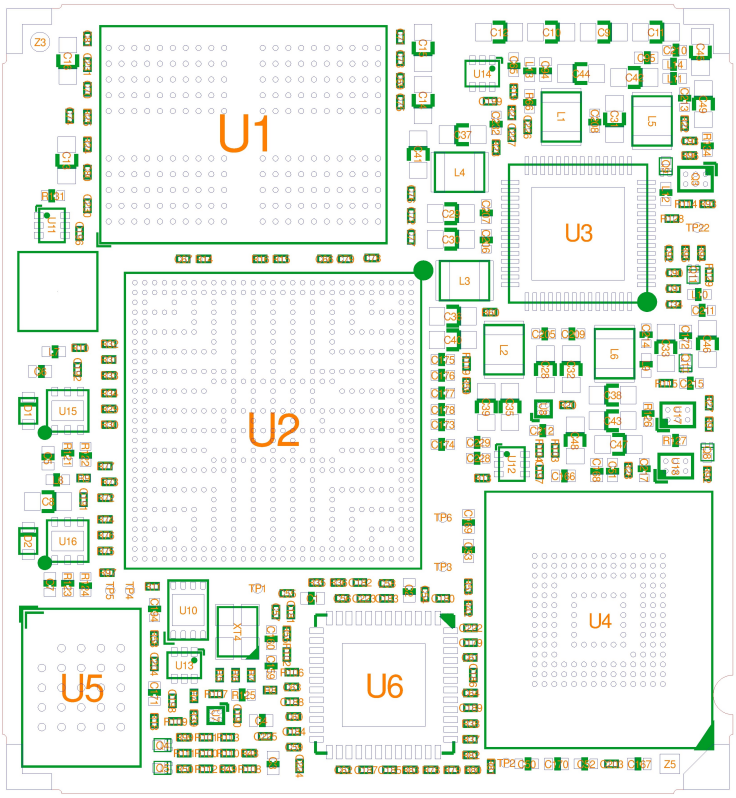
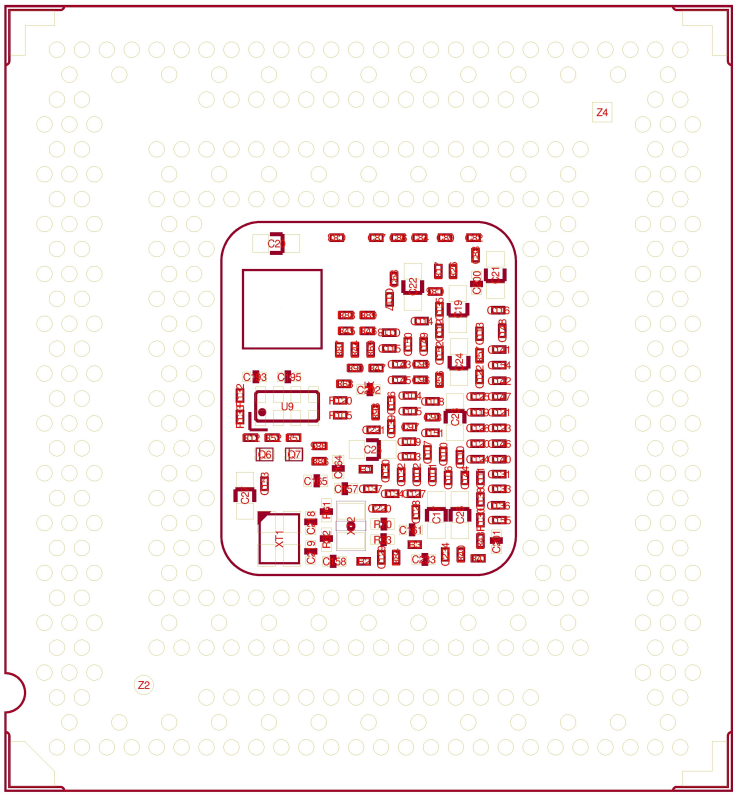


FIGURE 5: phyCORE-i.MX 8M Plus DSC Component Placement (1561.1 Bottom View)



4.4 phyCORE-i.MX 8M Plus Minimum Operating Requirements

Warning

We recommend connecting all available +3.3 V input pins to the power supply system on a custom carrier board housing the phyCORE-i.MX 8M Plus and, at a minimum, the matching number of GND balls neighboring the +3.3 V balls. In addition, proper implementation of the phyCORE-i.MX 8M Plus module into a target application also requires connecting all GND pins.
Refer to Power for more information.

Before the phyCORE-i.MX 8M plus can be used, please make sure the host system meets the minimum operating requirements. These include:

- The stable and clean input power supply of 3.3 V with low ESR bulk capacitors (e.g. 2x 100µ/6.3V MLCC) paired with some HF blocking capacitors (e.g. 100nF MLCC) connected to the input pins as near as possible (phyCORE-i.MX 8M Plus Power Consumption)
- Appropriate configuration of the I/O voltage (3.3 V or 1.8 V) configured by signal X_VIO_Ctrl (External Logic IO Supply Voltage)
- Supply voltage for externally connected peripherals should be controlled by signal X_nPWR_READY to avoid reverse currents (External Logic IO Supply Voltage)
- If external peripherals need a longer reset delay, hold reset signal X_POR_B_VIO as long as low as needed (Reset)
- Desired boot configuration - default configuration is "Boot from on-board eMMC" (System Boot Configuration)
- To back up the on-board I2C-RTC, connect a buffer voltage source to input pin VBAT (Backup Power (VBAT / VIN_SNVS_1V8), RTC)

5 Pin Description

Warning

Module connections **must** not exceed their expressed maximum voltage or current. Maximum signal input values are indicated in the corresponding controller manuals/datasheets. As damage from improper connections varies according to use and application, the user must take appropriate safety measures to ensure that the module connections are protected from overloading through connected peripherals.

All controller signals extend to surface mount technology (SMT) connectors (0.5 mm). These connectors line two sides of the module (referred to as phyCORE-Connectors). This enables phyCORE-i.MX 8 Plus to be plugged into any target application like a "big chip".

PHYTEC provides a complete pinout table for the phyCORE-i.MX 8M Plus Connector (X1). This table contains a complete signal path for the phyCORE-i.MX 8M Plus and the carrier board phyBOARD-Pollux, including signal names, pin muxing paths, and descriptions specific to each pin. It also provides the appropriate voltage domain, signal type (ST), and a functional grouping of the signals. The signal type also includes information about the signal direction. A table describing the signal types can be found with the phyCORE-i.MX 8M Plus Pinout Table.

Warning

- The NXP® Semiconductor i.MX 8M Plus is a multi-voltage operated microcontroller and, as such, special attention should be paid to the interface voltage levels to avoid unintentional damage to the microcontroller and other on-board components. Please refer to the *NXP Semiconductor i.MX 8M Plus Reference Manual* for details on the functions and features of controller signals and port pins.
- As some of the signals that are brought out on the phyCORE-Connector are used to configure the boot mode for specific boot options, please make sure that these signals are not driven by any device on the baseboard during reset. The signals that may affect the boot configuration are shown in phyCORE-Connector Boot Configuration Pins.
- It is necessary to avoid voltages at the IO pins of the phyCORE-i.MX 8M Plus, which are sourced from the supply voltage of peripheral devices attached to the SOM during power-up or power-down. These voltages can cause a current flow into the controller, especially if peripheral devices attached to the interfaces of the i.MX 8M Plus are supposed to be powered while the phyCORE-i.MX 8M Plus is in suspend mode or turned off. To avoid this, bus switches are either supplied by VDD_3V3 on the phyCORE side or have their output enabled to the SOM controlled by the X_nPWR_READY signal (see Supply Voltage for External Logic) must be used.

Pin Muxing Warning

If pin settings are changed from the PHYTEC standard configuration, make sure that the settings of the pull resistors are adjusted accordingly. Never rely on the SoC-internal pull resistor.

6 Jumpers

The phyCORE-i.MX 8M Plus (PCM-070) has only one pre-configured solder jumper (J1), **meanwhile the DSC variant PCL-070 is jumperless**. There are, however, a few jumpers on the phyCORE-Pollux. Information on these jumpers can be found in Jumpers.

Warning

Due to the small footprint of the solder jumpers (J), PHYTEC does not recommend manual jumper modifications. This may also render the warranty invalid. Contact our sales team if you need jumper configurations different from the default configuration.

FIGURE 6: Typical Jumper Pad Numbering Scheme

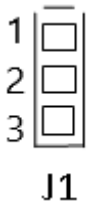
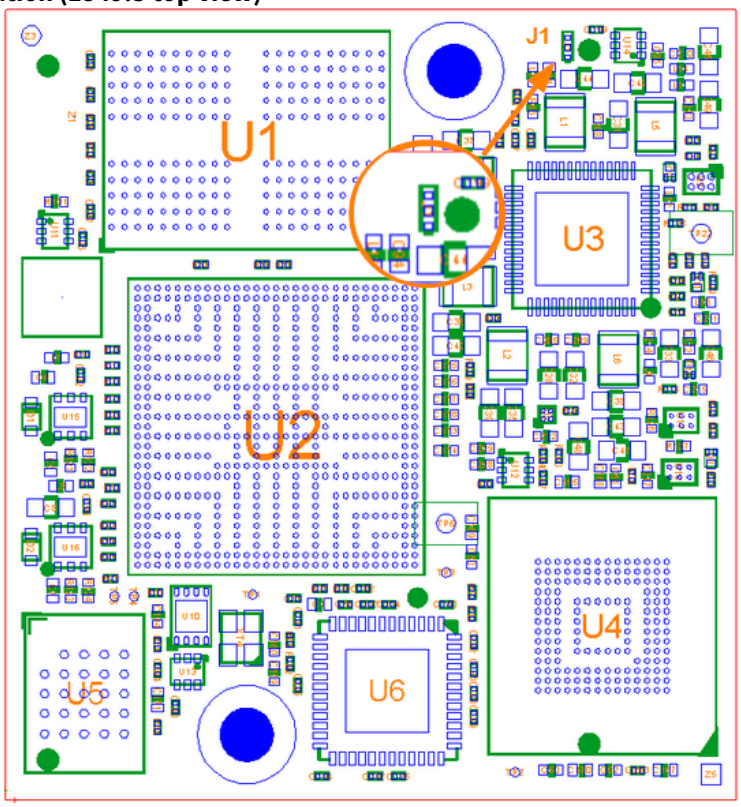


FIGURE 7: Jumper Location (1549.3 top view)



The jumpers (J = solder jumper) have the following functions.

TABLE 3: Jumper Settings

Jumper	Position	Description	Type	Section
J1*	**1+2 (default)**	**RTC_CLKOUT is connected to X_RTC_CLKOUT/nTEMP_ALERT**	0201	RTC
	2+3	nTEMP_ALERT is connected to X_RTC_CLKOUT/nTEMP_ALERT		Temperature Sensors

Info

***PCL-070 has no jumper and provides dedicated DSC contacts for both signals.**

7 Power

The phyCORE-i.MX 8M Plus operates off a single power supply voltage. The following section discusses the primary power pins on the phyCORE i.MX 8M Plus Connector X1 in detail.

7.1 Primary System Power (VIN_3V3)

The phyCORE-i.MX 8M Plus is powered by a primary voltage supply with a nominal value of +3.3 V. on-board switching regulators generate the voltage supplies required by the i.MX 8M Plus MCU and on-board components from the primary 3.3 V supplied to the SOM.

For proper operation, the phyCORE-i.MX 8M Plus must be supplied with a voltage source of 3.2...3.5 V with a maximum power consumption of a 4 A load at the VCC pins on the phyCORE.

VIN_3V3: X1 → C1..C4, D1..D4 **(DSC B160, B161, B163, B164, B166, B167)**

Connect all +3.3 V VCC input pins to your power supply and, at a minimum, the matching number of GND pins.

Corresponding GND: X1 → C5..C7, C15, D5..D7, D13 **(DSC B152, B157, B162, B165, B168, B171)**

Please refer to the section Pin Description for information on additional GND Pins located at the phyCORE i.MX 8M Plus Connector X1.

For information on various power consumption scenarios that PHYTEC has run, go to phyCORE-i.MX 8M Plus Power Consumption.

Warning

As a general design rule, PHYTEC recommends connecting all GND pins to neighboring signals that are being used in the application circuitry. For maximum EMI performance, all GND pins should be connected to a solid ground plane. Additionally, take care of a solid, low impedance connection of the power supply line to avoid voltage drop. It is recommended to place a couple of bulk capacitors as near as possible to the phyCORE's system power input (VIN_3V3) to compensate for the trace inductance.

7.2 Power Management IC (PMIC) (U3)

The phyCORE-i.MX 8M Plus provides an on-board Power Management IC (PMIC) at position U3 to generate different voltages required by the microcontroller and the on-board components. The PMIC supports many functions, including dynamic voltage control, different low-power modes, and regulator supervision. It is connected to the i.MX 8M Plus via the on-board I^2C bus (I2C1). The I^2C address of the PMIC is 0x25.

7.3 Power Domains

External voltages to supply the board:

- VIN_3V3 3.3 V main supply voltage (3.2 .. 3.5 V / max. 4A)
- optional: VIN_SNVS_1V8 low power supply voltage input (1.8 V ±5% / 10mA; if left open, it is provided on-board if VIN_3V3 is present)
- VBAT backup supply voltage for the on-board I2C-Bus RTC U9 (RV-3028-C7)

7.4 External Logic IO Supply Voltage

The voltage level (VDD_IO) of the phyCORE's logic interface circuitry is VDD_3V3 (3.3 V) or VDD_1V8 (1.8 V), which is determined by the configuration input signal X_VIO_Ctrl (X1-D8). Connect X_VIO_Ctrl to the module input supply voltage VIN_3V3 to configure VDD_IO=3.3 V interface voltage level or connect it to GND to select VDD_IO=1.8 V interface voltage level.

In order to follow the power-up and power-down sequencing mandatory for the i.MX 8M Plus, external devices connected to the phyCORE interface circuitry have to be supplied by an external power supply, which is controlled by the output signal X_nPWR_READY (OD driver), which is brought out at pin X1-C14. X_nPWR_READY should control the external supply voltage which is used to supply the external interface circuitry connected to the phyCORE's interfaces. X_nPWR_READY switches to GND to start the external voltage supply or to switch over a power switch. If the on-board interface voltage (VDD_IO) switches off, X_nPWR_READY is released to high impedance. To raise the signal, an external pull-up resistor (eg, 4k7) is needed. It can be connected to voltage levels up to max. 12V, depending on the external power supply control signal requirement. Use of X_nPWR_READY ensures that external components are only supplied when the supply voltages of the i.MX 8M Plus is stable and avoids undefined return currents while the system is powered down.

Warning

It is recommended to monitor the externally generated power supply voltages by a voltage supervisor. The supervisor should hold X_POR_B_VIO (X1-C13) low, as long as the externally generated voltages are not in proper shape. To drive X_POR_B_VIO to GND, use an open-drain driver (OD) or N-channel FET (e.g. DMN1260UFA). X_POR_B_VIO has an on-board pull-up resistor to VDD_IO.

7.5 Backup Power (VBAT / VIN_SNVS_1V8)

To back up the on-board I2C-Bus RTC U9 (RV-3028-C7), an external voltage source must be added at Pin X1-C9 (VBAT). The RTC has an extremely low backup current consumption of only 40nA (@3 V). It is also possible to supply the internal RTC and some critical registers of the i.MX 8M Plus' low power domain (NVCC_SNVS_1V8). NVCC_SNVS_1V8 can be supplied over Pin X1-C8 if VIN_3V3 is not present.

7.6 Manual Power Switch (X_OnOff)

The signal X_OnOff (Pin X1-D9) is used to manually switch the power of the SOM. The X_OnOff signal can be left unconnected if not used. It has a weak on-board pull-up resistor against NVCC_SNVS_1V8 and is held high as long as VIN_3V3 is present or external backup voltage VIN_SNVS_1V8 is supplied. To drive the signal to ground, use an open-collector driver or a push-button switch. For more information about ON/OFF, refer to the *NXP Semiconductor i.MX 8M Plus Reference Manual*.

8 Reset

The X_PMIC_RST_B signal (Pin X1-C11) on the phyCORE-Connector is designated as a "cold reset" input. Driving X_PMIC_RST_B to low (has a weak pull-up to SNVS_1V8) will restart the system, performing a complete power recycle. X_PMIC_RST_B has a 50ms debouncing circuit. This input can be used for a mechanical reset switch button. X_POR_B_VIO Signal (Pin X1-C13) can be used to prevent bootup of the i.MX 8M Plus. This can be used as a startup as described in the section Power Management IC.

9 System Boot Configuration

Most features of the i.MX 8 Plus microcontroller are configured and/or programmed during the initialization routine. Other features, which impact program execution, must be configured prior to initialization via pin termination.

The system start-up configuration includes:

- Boot mode selection
- Boot device selection
- Boot device configuration

The internal ROM code is the first code executed during the initialization process of the i.MX 8M Plus after POR. The ROM code detects the boot mode by using the boot mode pins (BOOT_MODE[3:0]), while the boot device is selected and configured by determining the state of the eFUSEs and/or the corresponding GPIO input pins (X_BOOT_MODE[3:0]).

9.1 Boot Mode Selection

The boot mode of the i.MX 8M Plus microcontroller is determined by the configuration of four boot mode inputs BOOT_MODE[3:0] during the reset cycle of the operating system. These inputs are brought out at the phyCORE processor pins X_BOOT_MODE[3:0] (X1-D22, X1-D23, X1-D24, X1-D25). phyCORE-i.MX 8M Plus Boot Modes shows the possible settings of pins X_BOOT_MODE[3:0] and the resulting boot configuration of the i.MX 8M Plus.

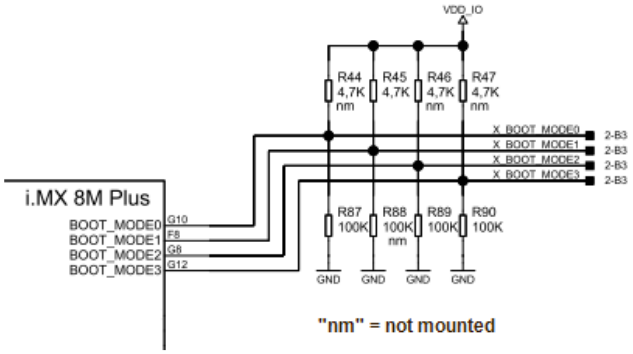
TABLE 4: phyCORE-i.MX 8M Plus Boot Modes

Boot Mode	X_BOOT_MODE3	X_BOOT_MODE2	X_BOOT_MODE1	X_BOOT_MODE0	Boot Source
0	0	0	0	0	Boot from internal fuses
1	0	0	0	1	USB Serial Downloader
2	0	0	1	0	Boot from on-board eMMC U4
3	0	0	1	1	Boot from ext. SD-Card on SD2
6	0	1	1	0	Boot from on-board QSPI Flash U5
15	1	1	1	1	JTAG mode

The X_BOOT_MODE[3,2,0] lines have 100 kΩ pull-down resistors populated (and unpopulated pull-up resistors) while X_BOOT_MODE[1] has a 4,7 kΩ pull-up resistor on the module in parallel to the internal pull-down resistors of the i.MX8 M Plus. Leaving the four pins unconnected sets the controller to boot mode 1, boot from on-board eMMC U4 memory device. The boot configuration settings can be changed by changing the populated resistors

configuration on the module or by connecting configuration resistors (e.g. 4,7 kΩ pull-up) to the X_BOOT_MODE configuration signals. The pull-up resistors must be supplied by the right VDD_IO voltage level of 1.8 V or 3.3 V, depending on the VDD_IO configuration (see section External Logic IO Supply Voltage).

FIGURE 8: phyCORE-i.MX 8M Plus onboard Boot Configuration Schematic



No.	X_BOOT_MODE[3..0]	Boot Modes
0	0000	Boot from internal fuses
1	0001	USB serial download
2	0010	Boot from onboard eMMC (default)
3	0011	Boot from ext. SD-Card on SD2
6	0110	Boot from onboard QSPI Flash
15	1111	JTAG mode

The BOOT_MODE is initialized by sampling the BOOT_MODE inputs on the rising edge of the POR_B. After these inputs are sampled, their subsequent state does not affect the contents of the BOOT_MODE internal register, and the pins can be used for GPIO operation.

TABLE 5: phyCORE-i.MX 8M Plus Boot Configuration Pins

SOM Connector Pin (DSC Contact) / phyBOARD-Pollux Carrier Board Connector Pin	SOM Signal Name	SOM Voltage Domain	Signal Level	Signal Type	Description
D22 **(B192)**	X_BOOT_MODE0	VDD_IO	1.8 V / 3.3 V	I/O	Boot configuration pin 0 during reset has on-board 100k pull-down resistor (SMD 0201)
D23 **(B193)**	X_BOOT_MODE1	VDD_IO	1.8 V / 3.3 V	I/O	Boot configuration pin 1 during reset has on-board 4,7 k pull-down resistor (SMD 0201)
D24 **(B194)**	X_BOOT_MODE2	VDD_IO	1.8 V / 3.3 V	I/O	Boot configuration pin 2 during reset has on-board 100k pull-down resistor (SMD 0201)
D25 **(B195)**	X_BOOT_MODE3	VDD_IO	1.8 V / 3.3 V	I/O	Boot configuration pin 3 during reset has on-board 100k pull-down resistor (SMD 0201)

Warning

Modules up to revision PCM-070-0F3243I.A1, PCM-070-0F3243I.S1, PCM-070-0F5443I.A0 **and PCL-070-0F3243I.A0** are configured for boot from internal fuses. These modules have a populated 100 kΩ pull-down resistor R88, and the 4,7 kΩ pull-up resistor R45 is unpopulated.

10 System Memory

The phyCORE-i.MX 8M Plus provides three types of on-board memory:

TABLE 6: phyCORE-i.MX 8M Plus Onboard Memory Types

	Basic-Version	Kit-Version	Exclusive-Version	Maximum Available
One bank LPDDR4 RAM	1 GByte	2 GByte	4 GByte	8 GByte
eMMC	4 GByte	8 GByte	32 GByte	64 GByte
QSPI NOR Flash	no	64 MB Byte	64 MByte	256 MByte

Additionally, an I²C-EEPROM with 4 kB is mounted on every SOM. Details for each memory type used on the phyCORE-i.MX 8M Plus are below.

10.1 LPDDR4-RAM (U1)

The RAM memory interface of the phyCORE-i.MX 8M Plus supports one 32-bit LPDDR4-RAM chip (U1). The LPDDR4 memory is accessible starting at addresses 0x4000 0000 and 1 0000 0000.

Typically, the LPDDR4-RAM initialization is performed by a boot loader or operating system following a power-on reset and must not be changed at a later point by any application code. When writing custom code independent of an operating system or boot loader, the RAM must be initialized by accessing the appropriate RAM configuration registers on the i.MX 8M Plus controller. Refer to the *NXP Semiconductor i.MX 8M Plus Reference Manual* to access and configure these registers.

10.2 eMMC Flash Memory (U4)

The main flash memory of the i.MX 8M Plus is eMMC and is populated at U4. The eMMC device is programmable with 1.8 V. No dedicated programming voltage is required. The eMMC Flash memory is connected to the SD3 interface of the i.MX 8M Plus.

For more information about the eMMC Flash interface, please refer to the *NXP Semiconductor i.MX 8M Plus Reference Manual*.

10.3 I²C EEPROM (U10)

The phyCORE-i.MX 8M Plus is populated with a non-volatile 4 kB I²C EEPROM at U10. This memory can be used to store configuration data or other general-purpose data. This device is accessed through I²C port 1 on the i.MX 8M Plus. The control registers for I²C port 1 are mapped between addresses 0x30A2 0000 and 0x30A3 0000. Please see the *NXP Semiconductor i.MX 8M Plus Reference Manual* for detailed information on the registers.

The three lower address bits are fixed to 0x1, which means that the EEPROM can be accessed at I²C address 0x51. The EEPROM has a second address on 0x59, which is called the Identification Page, and is reserved for internal PHYTEC use only.

10.4 QSPI NOR Flash (U5)

The QSPI NOR Flash memory of the phyCORE-i.MX 8M Plus at U5 can be used to store configuration data or any other general-purpose data. It can also be used as a boot device and a recovery boot device. The device is accessed through QSPIA SS0 on the i.MX 8 Plus. The control registers for QSPI are mapped between addresses 0x30BB 0000 and 0x30BB FFFF. Please see the *NXP Semiconductor i.MX 8M Plus Reference Manual* for detailed information on the registers.

As of the printing of this manual, these SPI Flash devices generally have a life expectancy of at least 100,000+ erase/program cycles and a data retention rate of 20 years. This makes the QSPI Flash a reliable and secure solution to store the first and second-level bootloaders.

11 Serial Interfaces

The phyCORE-i.MX 8M Plus provides numerous dedicated serial interfaces, some of which are equipped with a transceiver to enable direct connection to external devices:

1. 1x 4-bit SDIO interface (SD2) with controlled IO voltage
2. 1x 8-bit SDIO interface (SD1)
3. 4x high-speed UARTs
4. 2x CAN-FD interfaces
5. 2x USB 3.0/2.0 Dual-Role interfaces with PHY
6. 2x 1Gbit Ethernet interfaces with TSN support (ENET1 with Ethernet transceiver on the phyCORE-i.MX 8 M Plus enabling a direct connection to an existing Ethernet network; ENET0 as RGMII Signals at logic level at the signal pins instead)
7. 3x I^2C interfaces
8. 2x Serial Peripheral Interfaces (SPI)
9. 2x SAI audio interface
10. 1x SPDIF interface
11. 1x PCI Express with x1 interface
12. 2x MIPI CSI-2 camera interfaces
13. 1x MIPI DSI-2 display interface

Details for each of these serial interfaces and any applicable jumper configurations are below.

11.1 SDIO Interface

The SDIO interface can be used to connect external SD cards, eMMC, or any other device requiring an SDIO interface (i.e, WiFI, I/O expansion, etc). The phyCORE bus features one SDIO interface on the phyCORE-i.MX 8M Plus, the interface signals extend from the first and second Ultra Secure Digital (SD1 and SD2) Host controllers to the phyCORE-Connector.

The table below shows the location of the different interface signals on the phyCORE-Connector. The MMC/SD/SDIO Host Controller is fully compatible with the SD Memory Card Specification 3.0. The interface supports SD cards with 3.3 V and 1.8 V I/O signals.

11.2 SDIO SD2 (4-bit)

SDIO SD2 is a 4-bit wide interface with controlled I/O voltage to support high-speed modes that require 1.8 V I/O voltage. During runtime, the I/O voltage can be switched from 3.3 V (default) to 1.8 V by the processor via the GPIO signal X_PMIC_SD_VSEL/GPIO1_IO04, which controls the PMIC integrated voltage regulator. X_VDDSW_SD2 will be used exclusively to supply an external SD or MicroSD memory card. X_VDDSW_SD2 is monitored by the PMIC load switch circuit for overcurrent and short circuits. For more details, please refer to the PMIC data sheet provided by NXP.

TABLE 7: SDIO Interface Pinout of SD2

SOM Connector Pin (DSC Contact) / phyBOARD-Pollux Carrier Board Connector Pin	SOM Signal Name	SOM Voltage Domain	Signal Level	Signal Type	Description
B36 **(A34 and A35)**	X_VDDSW_SD2	VDD_3V3	3.3 V	PWR_O	Controlled SD Card Supply Voltage
B37 **(A36)**	X_SD2_CD_B	NVCC_SD2	1.8 V / 3.3 V	I	SD2 Card Detect
B38 **(A37)**	X_SD2_WP	NVCC_SD2	1.8 V / 3.3 V	I	SD2 Write Protect
B39 **(A39)**	X_SD2_CMD	NVCC_SD2	1.8 V / 3.3 V	O	SD2 Command
B40 **(A40)**	X_SD2_CLK	NVCC_SD2	1.8 V / 3.3 V	O	SD2 Clock
B42 **(A41)**	X_SD2_DATA0	NVCC_SD2	1.8 V / 3.3 V	I/O	SD2 Data 0
B43 **(A42)**	X_SD2_DATA1	NVCC_SD2	1.8 V / 3.3 V	I/O	SD2 Data 1
B44 **(A44)**	X_SD2_DATA2	NVCC_SD2	1.8 V / 3.3 V	I/O	SD2 Data 2

SOM Connector Pin (DSC Contact) / phyBOARD-Pollux Carrier Board Connector Pin	SOM Signal Name	SOM Voltage Domain	Signal Level	Signal Type	Description
B45 (A45)	X_SD2_DATA3	NVCC_SD2	1.8 V / 3.3 V	I/O	SD2 Data 3

11.3 SDIO SD1 (8-bit)

SDIO SD1 is an 8-bit wide interface. The I/O voltage is determined by VDD_IO, which is statically configured for the system to 3.3 V or 1.8 V (refer to External Logic IO Supply Voltage).

TABLE 8: SDIO Interface Pinout of SD1

SOM Connector Pin (DSC Contact) / phyBOARD-Pollux Carrier Board Connector Pin	SOM Signal Name	SOM Voltage Domain	Signal Level	Signal Type	Description
B46 **(B38)**	X_SD1_RESET_B	VDD_IO	1.8 V / 3.3 V	I/O	SD1 Reset
B48 **(B39)**	X_SD1_CMD	VDD_IO	1.8 V / 3.3 V	O	SD1 Command
B49 **(B40)**	X_SD1_STROBE	VDD_IO	1.8 V / 3.3 V	O	SD1 Strobe
B50 **(B41)**	X_SD1_CLK	VDD_IO	1.8 V / 3.3 V	O	SD1 Clock
B51 **(B43)**	X_SD1_DATA0	VDD_IO	1.8 V / 3.3 V	I/O	SD1 Data 0
B52 **(B44)**	X_SD1_DATA1	VDD_IO	1.8 V / 3.3 V	I/O	SD1 Data 1
B53 **(B45)**	X_SD1_DATA2	VDD_IO	1.8 V / 3.3 V	I/O	SD1 Data 2
B55 **(B46)**	X_SD1_DATA3	VDD_IO	1.8 V / 3.3 V	I/O	SD1 Data 3

SOM Connector Pin (DSC Contact) / phyBOARD-Pollux Carrier Board Connector Pin	SOM Signal Name	SOM Voltage Domain	Signal Level	Signal Type	Description
B56 **(B48)**	X_SD1_DATA4	VDD_IO	1.8 V / 3.3 V	I/O	SD1 Data 4
B57 **(B49)**	X_SD1_DATA5	VDD_IO	1.8 V / 3.3 V	I/O	SD1 Data 5
B58 **(B51)**	X_SD1_DATA6	VDD_IO	1.8 V / 3.3 V	I/O	SD1 Data 6
B59 **(B52)**	X_SD1_DATA7	VDD_IO	1.8 V / 3.3 V	I/O	SD1 Data 7

11.4 Universal Asynchronous Interfaces (UARTs)

The phyCORE-i.MX 8M Plus provides four high-speed universal asynchronous interfaces. The following table shows the location of the signals on the phyCORE-Connector.

TABLE 9: UART Signal Locations

SOM Connector Pin (DSC Contact) / phyBOARD-Pollux Carrier Board Connector Pin	SOM Signal Name	SOM Voltage Domain	Signal Level	Signal Type	Description
A2 **(A87)**	X_UART1_RXD	VDD_IO	1.8 V / 3.3 V	I	UART1 Receive Data (Usually used as A53 Debug)
A3 **(A86)**	X_UART1_TXD	VDD_IO	1.8 V / 3.3 V	O	UART1 Transmit Data (Usually used as A53 Debug)
B2 **(B113)**	X_UART2_RXD	VDD_IO	1.8 V / 3.3 V	I	UART2 Receive Data
B3 **(B112)**	X_UART2_TXD	VDD_IO	1.8 V / 3.3 V	O	UART2 Transmit Data
A4 **(A84)**	X_UART3_RXD	VDD_IO	1.8 V / 3.3 V	I	UART3 Receive Data
A5 **(A83)**	X_UART3_TXD	VDD_IO	1.8 V / 3.3 V	O	UART3 Transmit Data

SOM Connector Pin (DSC Contact) / phyBOARD-Pollux Carrier Board Connector Pin	SOM Signal Name	SOM Voltage Domain	Signal Level	Signal Type	Description
B4 (B110)	X_UART4_RXD	VDD_IO	1.8 V / 3.3 V	I	UART4 Receive Data (Usually used as M7 Debug)
B5 (B109)	X_UART4_TXD	VDD_IO	1.8 V / 3.3 V	O	UART4 Transmit Data (Usually used as M7 Debug)

11.5 USB Interfaces

The phyCORE-i.MX 8M Plus provides two USB 3.0/2.0 dual role interfaces, which support super-speed (5Bbit/s), high-speed (480 Mbit/s), full-speed (12 Mbit/s), and low-speed (1.5 Mbit/s) operation. The applicable interface signals can be found on the phyCORE-Connector X1. If overcurrent and power enable signals are needed for the USB host interface, the functionality can be easily implemented with GPIOs.

TABLE 10: USB 1 Signal Locations

SOM Connector Pin (DSC Contact) / phyBOARD-Pollux Carrier Board Connector Pin	SOM Signal Name	SOM Voltage Domain	Signal Level	Signal Type	Description
C16 **(A128)**	X_USB1_VBUS	VDD_3V3	3.3 V / 5 V	I	USB 1 bus voltage detection (5 V compliant)
C17 **(A129)**	X_USB1_ID	VDD_3V3	-	USB-I/O	(do not use, has no function in the CPU)
C18 **(A131)**	X_USB1_D_N	VDD_3V3	-	USB_I/O	USB 1 Data-
C19 **(A132)**	X_USB1_D_P	VDD_3V3	-	USB_I/O	USB 1 Data+
C21 **(A133)**	X_USB1_TX_N	VDD_3V3	-	USB_I/O	USB 1 Transmit Data-
C22 **(A134)**	X_USB1_TX_P	VDD_3V3	-	USB_I/O	USB 1 Transmit Data+
C23 **(A136)**	X_USB1_RX_N	VDD_3V3	-	USB_I/O	USB 1 Receive Data-
C24 **(A137)**	X_USB1_RX_P	VDD_3V3	-	USB_I/O	USB 1 Receive Data+

TABLE 11: USB 2 Signal Locations

SOM Connector Pin (DSC Contact) / phyBOARD-Pollux Carrier Board Connector Pin	SOM Signal Name	SOM Voltage Domain	Signal Level	Signal Type	Description
C26 **(A138)**	X_USB2_VBUS	VDD_3V3	3.3 V / 5 V	I	USB 2 bus voltage detection (5 V compliant)
C27 **(A139)**	X_USB2_ID	VDD_3V3	-	USB_I/O	(do not use, has no function in the CPU)
C28 **(A141)**	X_USB2_D_N	VDD_3V3	-	USB_I/O	USB 2 Data-
C29 **(A142)**	X_USB2_D_P	VDD_3V3	-	USB_I/O	USB 2 Data+
C31 **(A143)**	X_USB2_TX_N	VDD_3V3	-	USB_I/O	USB 2 Transmit Data-
C32 **(A144)**	X_USB2_TX_P	VDD_3V3	-	USB_I/O	USB 2 Transmit Data+
C33 **(A146)**	X_USB2_RX_N	VDD_3V3	-	USB_I/O	USB 2 Receive Data-
C34 **(A147)**	X_USB2_RX_P	VDD_3V3	-	USB_I/O	USB 2 Receive Data+

11.6 Ethernet Interfaces ENET0 and ENET1

The phyCORE-i.MX 8M Plus provides two Ethernet Interfaces, ENET0 with TSN support and ENET1. Connection of the phyCORE-i.MX 8M Plus to the World Wide Web or a local area network (LAN) is possible using the on-board GbE PHY at U6. It is connected to the RGMII interface of ENET1. The PHY operates with a data transmission speed of 10 Mbit/s, 100 Mbit/s, or 1000 Mbit/s. Additionally, the RGMII interface of ENET0, which is available on the phyCORE-Connector, can be used to connect an external PHY. (ENET0 RGMII Interface).

Note

Please note that only ENET0 has TSN support.
PHYTEC has chosen to make the ETH1 available as RGMII for customers to accommodate their individual needs when it comes to choosing the right PHY or switching components applicable to their network topology.
As an example, we have connected a TSN-capable Ethernet PHY to ENET0 on the carrier board, which may be used for reference in your own design. See Ethernet (X8/X9) for details.

11.6.1 ENET1 Ethernet PHY (U6)

With an Ethernet PHY mounted at U6, the phyCORE-i.MX 8M Plus has been designed for use in 10Base-T, 100Base-T, and 1000Base-T networks. The 10/100/1000Base-T interface with its LED signals extends to the phyCORE-Connector X1. **In a Linux environment, the ENET1 interface is called eth0 as it is the port with the on-board PHY.**

TABLE 12: Ethernet PHY Signal Locations

SOM Connector Pin (DSC Contact) / phyBOARD-Pollux Carrier Board Connector Pin	SOM Signal Name	SOM Voltage Domain	Signal Level	Signal Type	Description
D47 (B217)	X_ETH_A_N	-	-	ETH_I/O	Data A-
D48 (B218)	X_ETH_A_P	-	-	ETH_I/O	Data A+
D49 (B219)	X_ETH_B_N	-	-	ETH_I/O	Data B-
D50 (B220)	X_ETH_B_P	-	-	ETH_I/O	Data B+
D52 (B222)	X_ETH_C_N	-	-	ETH_I/O	Data C-
D53 (B223)	X_ETH_C_P	-	-	ETH_I/O	Data C+
D54 (B224)	X_ETH_D_N	-	-	ETH_I/O	Data D-
D55 (B225)	X_ETH_D_P	-	-	ETH_I/O	Data D+

SOM Connector Pin (DSC Contact) / phyBOARD-Pollux Carrier Board Connector Pin	SOM Signal Name	SOM Voltage Domain	Signal Level	Signal Type	Description
D57 (B227)	X_ETH_GPIO0	VDD_1V8	1.8 V	I/O	GPIO0
D58 (B228)	X_ETH_GPIO1	VDD_1V8	1.8 V	I/O	GPIO1
D59 (B229)	X_ETH_LED0_LINK	-	-	OD	Link
D60 (B230)	X_ETH_LED2_ACT	-	-	OD	Activity

11.6.1.1 Ethernet Signal Locations of ENET1

The on-board GbE PHY supports HP Auto-MDIX technology, eliminating the need for a direct-connect LAN or cross-over patch cable. It detects the TX and RX pins of the connected device and automatically configures the PHY TX and RX pins accordingly. The Ethernet PHY also features an auto-negotiation to automatically determine the best speed and duplex mode.

The Ethernet PHY is connected to the RGMII interface ENET1 of the i.MX 8M Plus. Please refer to the *NXP Semiconductor i.MX 8M Plus Reference Manual* for more information about this interface.

In order to connect the module to an existing 10/100/1000Base-T network, some external circuitry is required. The required termination resistors on the analog signals (ETH_A±, ETH_B±, ETH_C±, ETH_D±) are integrated into the chip, so there is no need to connect external termination resistors to these signals. Connection to external Ethernet magnetics should be done using very short signal traces. The A+/A-, B+/B-, C+/C-, and D+/D- signals should be routed as 100 Ohm differential pairs. The same applies to the signal lines after the transformer circuit. The carrier board layout should avoid any other signal lines crossing the Ethernet signals.

Warning

Please refer to the Ethernet PHY datasheet when designing the Ethernet transformer circuitry or request the schematic of the applicable carrier board (phyBOARD-Pollux i.MX 8M Plus).

11.6.2 Reset of the Ethernet Controller

The reset input of the Ethernet PHY at U6 is connected to the system reset POR_B.

11.6.3 MAC Address

In a computer network such as a local area network (LAN), the MAC (Media Access Control) address is a unique computer hardware number. For a connection to the internet, a table is used to convert the assigned IP address to the hardware's MAC address. In order to guarantee that the MAC address is unique, all addresses are managed in a central location. PHYTEC has acquired a pool of MAC addresses. The MAC address of the phyCORE-i.MX 8M Plus is located on the bar code sticker attached to the module. This number is a 12-digit HEX value.

11.6.4 ENET0 RGMII Interface

In order to use an external Ethernet PHY, the RGMII interface (ENET0) of the i.MX 8M Plus is brought out at phyCORE-Connector X1. ENET0 is primarily used for TSN network operation. For that use case, an external TSN-ready Ethernet switch device is used. **In a Linux environment, the ENET0 interface is called eth1 as it is the port with the external PHY.**

TABLE 13: ENET0 RGMII Interface Signal Locations

SOM Connector Pin (DSC Contact) / phyBOARD-Pollux Carrier Board Connector Pin	SOM Signal Name	SOM Voltage Domain	Signal Level**	Signal Type	Description
A15 (B98)	X_ENET_MDIO	VDD_1V8	1.8 V	I/O	Management Data
A17 (B97)	X_ENET_RGMII_TD0	VDD_1V8	1.8 V	O	Transmit Data 0
A18 (B95)	X_ENET_RGMII_TD1	VDD_1V8	1.8 V	O	Transmit Data 1
A19 (B94)	X_ENET_RGMII_TD2	VDD_1V8	1.8 V	O	Transmit Data 2
A20 (B93)	X_ENET_RGMII_TD3	VDD_1V8	1.8 V	O	Transmit Data 3
A22 (B92)	X_ENET_RGMII_TX_CTL	VDD_1V8	1.8 V	O	Transmit Control
A23 (B90)	X_ENET_RGMII_TXC	VDD_1V8	1.8 V	O	Transmit Clock

SOM Connector Pin (DSC Contact) / phyBOARD-Pollux Carrier Board Connector Pin	SOM Signal Name	SOM Voltage Domain	Signal Level**	Signal Type	Description
A24 (B89)	X_ENET_RGMII_RX_CTL	VDD_1V8	1.8 V	I	Receive Control
A25 (B88)	X_ENET_RGMII_RXC	VDD_1V8	1.8 V	I	Receive Clock
A27 (B87)	X_ENET_RGMII_RXD0	VDD_1V8	1.8 V	I	Receive Data 0
A28 (B85)	X_ENET_RGMII_RXD1	VDD_1V8	1.8 V	I	Receive Data 1
A29 (B84)	X_ENET_RGMII_RXD2	VDD_1V8	1.8 V	I	Receive Data 2
A30 (B83)	X_ENET_RGMII_RXD3	VDD_1V8	1.8 V	I	Receive Data 3
A32 (B82)	X_ENET_MDC	VDD_1V8	1.8 V	O	Management Clock

11.7 SPI Interface

The Serial Peripheral Interface (SPI) is a four-wire, bidirectional serial bus that provides a simple and efficient method for data exchange among devices. The phyCORE provides two SPI on the phyCORE-Connector X1. The SPI provides one chip select signal for each interface. The Enhanced Configurable SPI (eCSPI) of the i.MX 8M Plus has three separate modules (eCSPI1, eCSPI2, and eCSPI3) which support clock rates of up to 60 MHz. The interface signals of the first and second modules (eCSPI1, eCSPI2) are made available on the phyCORE-Connector. These modules are master/slave configurable. The following table lists the SPI signals on the phyCORE-Connector.

TABLE 14: SPI Interface Signal Locations

SOM Connector Pin (DSC Contact) / phyBOARD-Pollux Carrier Board Connector Pin	SOM Signal Name	SOM Voltage Domain	Signal Level	Signal Type	Description
B26 (A55)	X_ECSPI1_SS0	VDD_IO	1.8 V / 3.3 V	O	eCSPI1 Chip Select
B27 (A54)	X_ECSPI1_MOSI	VDD_IO	1.8 V / 3.3 V	I/O	eCSPI1 Master Out
B28 (A52)	X_ECSPI1_MISO	VDD_IO	1.8 V / 3.3 V	I/O	eCSPI1 Master In
B29 (A51)	X_ECSPI1_SCLK	VDD_IO	1.8 V / 3.3 V	O	eCSPI1 Clock
B31 (A50)	X_ECSPI2_SS0	VDD_IO	1.8 V / 3.3 V	O	eCSPI2 Chip Select
B32 (A49)	X_ECSPI2_MOSI	VDD_IO	1.8 V / 3.3 V	I/O	eCSPI2 Master Out
B33 (A47)	X_ECSPI2_MISO	VDD_IO	1.8 V / 3.3 V	I/O	eCSPI2 Master In

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SOM Connector Pin (DSC Contact) / phyBOARD-Pollux Carrier Board Connector Pin	SOM Signal Name	SOM Voltage Domain	Signal Level	Signal Type	Description
B34 (A46)	X_ECSPI2_SCLK	VDD_IO	1.8 V / 3.3 V	O	eCSPI2 Clock

11.8 I²C Interface

The Inter-Integrated Circuit (I²C) interface is a two-wire, bidirectional serial bus that provides a simple and efficient method for data exchange among devices. The i.MX 8M Plus contains four identical and independent Multimaster fast-mode I²C modules. The interface of 3 modules is available on the phyCORE-Connector X1. I2C1 is reserved for controlling on the SOM.

Tip

To ensure the proper functioning of the I²C interface, external pull resistors matching the load at the interface must be connected. There are no pull-up resistors mounted on the module. For detailed information on the voltage levels for the pull-up resistors, please refer to the *i.MX 8M Plus Datasheet.*

The following table lists the I²C ports on the phyCORE-Connector:

TABLE 15: I2C Interface Signal Locations

SOM Connector Pin (DSC Contact) / phyBOARD-Pollux Carrier Board Connector Pin	SOM Signal Name	SOM Voltage Domain	Signal Level	Signal Type	Description
B13 (A75)	X_I2C2_SCL	VDD_IO	1.8 V / 3.3 V	I/OD	I2C2 Clock
B14 (A74)	X_I2C2_SDA	VDD_IO	1.8 V / 3.3 V	I/OD	I2C2 Data
B15 (A72)	X_I2C3_SCL	VDD_IO	1.8 V / 3.3 V	I/OD	I2C3 Clock
B16 (A71)	X_I2C3_SDA	VDD_IO	1.8 V / 3.3 V	I/OD	I2C3 Data
E11 (A70)	X_I2C4_SCL	VDD_IO	1.8 V / 3.3 V	I/OD	I2C4 Clock
E12 (A69)	X_I2C4_SDA	VDD_IO	1.8 V / 3.3 V	I/OD	I2C4 Data

11.9 Audio Interface

The i.MX 8M Plus supports multiple audio interfaces as listed below:

TABLE 16: phyCORE-i.MX 8M Plus Audio Interfaces

Interface	RX Data Line	TX Data Line
SAI-1	2	2
SAI-2	1	1
SAI-3	1	1
SAI-5	4	0
SPDIF-1	1	1

11.9.1 I^2S Audio Interface (SAI)

The phyCORE-i.MX 8M Plus features a Synchronous Audio Interface that supports full-duplex serial interfaces with frame synchronization, such as I2S, AC97, and TDM. The interface is divided into four sub-interfaces: SAI1, SAI2, SAI3, and SAI5. All signals are routed directly to the phyCORE-Connector X1.

The tables below show the signal locations for each SAI and SPDIF interface.

11.9.1.1 SAI1 Interface

Warning

** SAI1 and SAI5 have fixed 1.8 V I/O voltage levels.

SAI1 is originally an 8-bit wide interface, but some of the signals are used only for the Ethernet RGMII interface of ENET1, which is connected to the on-board PHY U6.

TABLE 17: SAI1 Interface Signal Locations

SOM Connector Pin (DSC Contact) / phyBOARD-Pollux Carrier Board Connector Pin	SOM Signal Name	SOM Voltage Domain	Signal Level**	Signal Type	Description
A7 **(B107)**	X_SAI1_MCLK	VDD_1V8	1.8V	I/O	SAI1 MCLK
A8 **(B105)**	X_SAI1_TXD6	VDD_1V8	1.8V	I/O	SAI1 TXD6 is connected to the X_PMIC_IRQ_B signal via R131 and acts as an interrupt recognition for PMIC events.
A9 **(B104)**	X_SAI1_TXD7	VDD_1V8	1.8V	I/O	SAI1 TXD7
A10 **(B103)**	X_SAI1_RXFS	VDD_1V8	1.8V	I/O	SAI1 RXFS
A12 **(B102)**	X_SAI1_RXC	VDD_1V8	1.8V	I/O	SAI1 RXC
A13 **(B100)**	X_SAI1_RXD0	VDD_1V8	1.8V	I/O	SAI1 RXD0
A14 **(B99)**	X_SAI1_RXD1	VDD_1V8	1.8V	I/O	SAI1 RXD1

11.9.1.2 SAI2 Interface

TABLE 18: SAI2 Interface Signal Locations

SOM Connector Pin (DSC Contact) / phyBOARD-Pollux Carrier Board Connector Pin	SOM Signal Name	SOM Voltage Domain	Signal Level	Signal Type	Description
A33 **(B80)**	X_SAI2_MCLK	VDD_IO	1.8V / 3.3 V	I/O	SAI2 MCLK
A34 **(B79)**	X_SAI2_TXFS	VDD_IO	1.8V / 3.3 V	I/O	SAI2 TXFS
A35 **(B78)**	X_SAI2_TXC	VDD_IO	1.8V / 3.3 V	I/O	SAI2 TXC
A37 **(B77)**	X_SAI2_TXD0	VDD_IO	1.8V / 3.3 V	I/O	SAI2 TXD0
A38 **(B75)**	X_SAI2_RXFS	VDD_IO	1.8V / 3.3 V	I/O	SAI2 RXFS
A39 **(B74)**	X_SAI2_RXC	VDD_IO	1.8V / 3.3 V	I/O	SAI2 RXC
A40 **(B73)**	X_SAI2_RXD0	VDD_IO	1.8V / 3.3 V	I/O	SAI2 RXD0

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11.9.1.3 SAI3 Interface

TABLE 19: SAI3 Interface Signal Locations

SOM Connector Pin (DSC Contact) / phyBOARD-Pollux Carrier Board Connector Pin	SOM Signal Name	SOM Voltage Domain	Signal Level	Signal Type	Description
B18 (A64)	X_SAI3_MCLK	VDD_IO	1.8V / 3.3 V	I/O	SAI3 MCLK
B19 (A62)	X_SAI3_TXFS	VDD_IO	1.8V / 3.3 V	I/O	SAI3 TXFS
B20 (A61)	X_SAI3_TXC	VDD_IO	1.8V / 3.3 V	I/O	SAI3 TXC
B21 (A60)	X_SAI3_TXD	VDD_IO	1.8V / 3.3 V	I/O	SAI3 TXD
B22 (A59)	X_SAI3_RXFS	VDD_IO	1.8V / 3.3 V	I/O	SAI3 RXFS
B23 (A57)	X_SAI3_RXC	VDD_IO	1.8V / 3.3 V	I/O	SAI3 RXC
B24 (A56)	X_SAI3_RXD	VDD_IO	1.8V / 3.3 V	I/O	SAI3 RXD

11.9.1.4 SAI5 Interface

Warning

** SAI1 and SAI5 have fixed 1.8 V I/O voltage levels.

TABLE 20: SAI5 Interface Signal Locations

SOM Connector Pin (DSC Contact) / phyBOARD-Pollux Carrier Board Connector Pin	SOM Signal Name	SOM Voltage Domain	Signal Level**	Signal Type	Description
E18 **(A19)**	X_SAI5_RXD3	VDD_1V8	1.8 V	I/O	SAI5 RXD3
E19 **(A20)**	X_SAI5_RXD2	VDD_1V8	1.8 V	I/O	SAI5 RXD2
E20 **(A21)**	X_SAI5_RXD1	VDD_1V8	1.8 V	I/O	SAI5 RXD1
E21 **(A22)**	X_SAI5_RXD0	VDD_1V8	1.8 V	I/O	SAI5 RXD0
E22 **(A24)**	X_SAI5_RXC	VDD_1V8	1.8 V	I/O	SAI5 RXC
E23 **(A25)**	X_SAI5_RXFS	VDD_1V8	1.8 V	I/O	SAI5 RXFS
E24 **(A26)**	X_SAI5_MCLK	VDD_1V8	1.8 V	I/O	SAI5 MCLK

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11.9.1.5 SPDIF Interface

TABLE 21: SPDIF Interface Signal Locations

SOM Connector Pin (DSC Contact) / phyBOARD-Pollux Carrier Board Connector Pin	SOM Signal Name	SOM Voltage Domain	Signal Level	Signal Type	Description
E14 (A67)	X_SPDIF_RX	VDD_IO	1.8V / 3.3 V	I	SPDIF RX
E15 (A66)	X_SPDIF_TX	VDD_IO	1.8V / 3.3 V	O	SPDIF TX
E16 (A65)	X_SPDIF_EXT_CLK	VDD_IO	1.8V / 3.3 V	I	SPDIF Ext. CLK

11.10 PCI Express Interface

The one 1-lane PCI Express interface of the phyCORE-i.MX 8M Plus provides PCIe Gen. 3.0 functionality, which supports up to 8 GT/s operations. Additional control signals, which might be required (e.g., “present” and “wake”), can be implemented with GPIOs. Please refer to the schematic of a suitable PHYTEC carrier board (e.g., phyBOARD-Pollux) for a circuit example.

The position of the PCIe signals on the phyCORE-Connector X1 is shown below:

TABLE 22: PCIe Interface Signal Locations

SOM Connector Pin (DSC Contact) / phyBOARD-Pollux Carrier Board Connector Pin	SOM Signal Name	SOM Voltage Domain	Signal Level	Signal Type	Description
D27 (B197)	X_PCIE_TXN_N	VDDA_1V8	LVDS	PCIe_O	PCIe1 TXN-
D28 (B198)	X_PCIE_TXN_P	VDDA_1V8	LVDS	PCIe_O	PCIe1 TXN+
D29 (B199)	X_PCIE_RXN_N	VDDA_1V8	LVDS	PCIe_I	PCIe1 RXN-
D30 (B200)	X_PCIE_RXN_P	VDDA_1V8	LVDS	PCIe_I	PCIe1 RXN+
D32 (B202)	X_PCIE_REF_PAD_CLK_N	VDDA_1V8	LVDS	PCIe_I/O	PCIe1 Ref CLK- Input
D33 (B203)	X_PCIE_REF_PAD_CLK_P	VDDA_1V8	LVDS	PCIe_I/O	PCIe1 Ref CLK+ Input

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11.11 General Purpose I/Os

All pins not used by any of the other interfaces specifically described in this manual can be used as GPIO without harming other features of the phyCORE-i.MX 8M Plus. These pins are shown below:

TABLE 23: GPIO Pin Locations

SOM Connector Pin (DSC Contact) / phyBOARD-Pollux Carrier Board Connector Pin	SOM Signal Name	SOM Voltage Domain	Signal Level	Signal Type	Description
D14 **(B183)**	X_GPIO1_IO00	VDD_IO	1.8V / 3.3 V	I/O	GPIO1_IO00
D15 **(B184)**	X_GPIO1_IO01	VDD_IO	1.8V / 3.3 V	I/O	GPIO1_IO01
C12 **(B179)**	X_PMIC_WDOG_B / GPIO1_IO02	VDD_IO	1.8V / 3.3 V	I/O	GPIO1_IO02 is used to trigger the PMIC WDOG_B input from the i.MX 8M Plus to perform a "cold reset".
D16 **(B185)**	X_GPIO1_IO03	VDD_IO	1.8V / 3.3 V	I/O	GPIO1_IO03
D17 **(B187)**	X_PMIC_SD_VSEL / GPIO1_IO04	VDD_IO	1.8V / 3.3 V	O	GPIO1_IO04 is on-board used to switch the NVCC_SD2 I/O voltage via the PMIC U3 from 3.3 V to 1.8 V for the high-speed data rates. Low means NVCC_SD2 = 3.3 V and high means 1.8 V.
D18 **(B188)**	X_GPIO1_IO05	VDD_IO	1.8V / 3.3 V	I/O	GPIO1_IO05 is output high during reset and changes to input with PU after reset.

SOM Connector Pin (DSC Contact) / phyBOARD-Pollux Carrier Board Connector Pin	SOM Signal Name	SOM Voltage Domain	Signal Level	Signal Type	Description
D20 **(B189)**	X_GPIO1_IO06	VDD_IO	1.8V / 3.3 V	I/O	GPIO1_IO06
D21 **(B190)**	X_GPIO1_IO07	VDD_IO	1.8V / 3.3 V	I/O	GPIO1_IO07
E2 **(A114)**	X_nETHPHY_INT / GPIO1_IO15	VDD_IO	1.8V / 3.3 V	I/O	GPIO1_15 is connected to the nINT output of the Ethernet PHY U6 for supporting interrupt connection to the i.MX 8M Plus.
E3 **(A113)**	X_GPIO1_IO14	VDD_IO	1.8V / 3.3 V	I/O	GPIO1_14
E4 **(A112)**	X_GPIO1_IO13	VDD_IO	1.8V / 3.3 V	I/O	GPIO1_13
E5 **(A111)**	X_GPIO1_IO12	VDD_IO	1.8V / 3.3 V	I/O	GPIO1_12
E6 **(A109)**	X_GPIO1_IO11	VDD_IO	1.8V / 3.3 V	I/O	GPIO1_11

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SOM Connector Pin (DSC Contact) / phyBOARD-Pollux Carrier Board Connector Pin	SOM Signal Name	SOM Voltage Domain	Signal Level	Signal Type	Description
E8 **(A108)**	X_GPIO1_IO10	VDD_IO	1.8V / 3.3 V	I/O	GPIO1_10
E9 **(A107)**	X_GPIO1_IO09	VDD_IO	1.8V / 3.3 V	I/O	GPIO1_09
E10 **(A106)**	X_GPIO1_IO08	VDD_IO	1.8V / 3.3 V	I/O	GPIO1_08

Besides these pins, most of the i.MX 8M Plus signals, which are connected directly to the module connector, can be configured to act as GPIOs, due to the multiplexing functionality of most controller pins. Normally, pins with signal type I/O are able to work as a GPIO.

11.11.1 GPIO Changing I/O Voltage

I/O voltage can be configured to 3.3 V or 1.8 V. Please refer to the section External Logic IO Supply Voltage. Be aware that changing the I/O voltage alters all interfaces that are in reference to VDD_IO.

12 Debug Interface

The phyCORE-i.MX 8M Plus is equipped with a JTAG interface to download program code into the external flash, internal controller RAM, or any debugging programs being executed. The location of the JTAG pins on the phyCORE-Connector X1 is below:

TABLE 24: Debug Interface Signal Locations

SOM Connector Pin (DSC Contact) / phyBOARD-Pollux Carrier Board Connector Pin	SOM Signal Name	SOM Voltage Domain	Signal Level	Signal Type	Description
B7 (A81)	X_JTAG_TCK	VDD_IO	1.8V / 3.3 V	I	JTAG clock signal. Has 10 kOhm pull-down.
B8 (A80)	X_JTAG_TDI	VDD_IO	1.8V / 3.3 V	I	JTAG data in signal
B9 (A79)	X_JTAG_TDO	VDD_IO	1.8V / 3.3 V	O	JTAG data out signal
B10 (A77)	X_JTAG_TMS	VDD_IO	1.8V / 3.3 V	I	JTAG test mode select signal
B11 (A76)	X_JTAG_MOD	VDD_IO	1.8V / 3.3 V	I	JTAG mode signal. To enable JTAG mode, this signal must be driven high. Signal has 10 kOhm pull-down.

12.1 UART Debug

The default debug UART Interfaces (TTL) are UART1 for Cortex-A53 Cores and UART4 for Cortex-M7 Core. UART1 is accessible on connector X1 pins B2 (RXD) and B3 (TXD), and UART4 on pins B4 (RXD) and B5 (TXD).

For more information, also refer to Universal Asynchronous Interfaces (UARTs).

13 Display Interfaces

13.1 High Definition Multimedia Interface (HDMI)

The High Definition Multimedia Interface (HDMI) of the phyCORE-i.MX 8M Plus is compliant with HDMI 2.0a for up to 1920x1080 at 60 Hz display resolutions. Please refer to the *NXP Semiconductor i.MX 8M Plus Reference Manual* for more information.

The location of the HDMI signals on the phyCORE-Connector X1 are shown below:

TABLE 25: HDMI Interface Signal Locations

SOM Connector Pin (DSC Contact) / phyBOARD-Pollux Carrier Board Connector Pin	SOM Signal Name	SOM Voltage Domain	Signal Level	Signal Type	Description
A42 (B72)	X_HDMI_DDC_SCL	VDD_IO	1.8V / 3.3 V	I/O	Display Data Channel SCL
A43 (B70)	X_HDMI_DDC_SDA	VDD_IO	1.8V / 3.3 V	I/O	Display Data Channel SDA
A44 (B69)	X_HDMI_HPD	VDD_IO	1.8V / 3.3 V	I/O	Hot Plug Detect
A45 (B68)	X_HDMI_CEC	VDD_IO	1.8V / 3.3 V	I/O	Consumer Electronics Control
A46 (B67)	X_HDMI_EARC_AUX	VDDA_1V8	1.8 V	I	HDMI EARC AUX
A48 (B65)	X_HDMI_EARC_N_HPD	VDDA_1V8	LVDS	HDMI_I	HDMI EARC- / HPD
A49 (B64)	X_HDMI_EARC_P_UTIL	VDDA_1V8	LVDS	HDMI_I	HDMI EARC+ / UTIL
A50 (B63)	X_HDMI_TX0_N	VDDA_1V8	LVDS	HDMI_O	HDMI TX0-

SOM Connector Pin (DSC Contact) / phyBOARD-Pollux Carrier Board Connector Pin	SOM Signal Name	SOM Voltage Domain	Signal Level	Signal Type	Description
A51 **(B62)**	X_HDMI_TX0_P	VDDA_1V8	LVDS	HDMI_O	HDMI TX0+
A53 **(B60)**	X_HDMI_TXC_N	VDDA_1V8	LVDS	HDMI_O	HDMI TX Clock -
A54 **(B59)**	X_HDMI_TXC_P	VDDA_1V8	LVDS	HDMI_O	HDMI TX Clock +
A56 **(B58)**	X_HDMI_TX1_N	VDDA_1V8	LVDS	HDMI_O	HDMI TX1-
A57 **(B57)**	X_HDMI_TX1_P	VDDA_1V8	LVDS	HDMI_O	HDMI TX1+
A58 **(B55)**	X_HDMI_TX2_N	VDDA_1V8	LVDS	HDMI_O	HDMI TX2-
A59 **(B54)**	X_HDMI_TX2_P	VDDA_1V8	LVDS	HDMI_O	HDMI TX2+

13.2 Low Voltage Differential Signal Display Interface (LVDS)

The phyCORE-i.MX 8M Plus offers one LVDS display interface, which supports two output channels.

The locations of the LVDS signals are shown below:

TABLE 26: Display Interface LVDS Signal Locations

SOM Connector Pin (DSC Contact) / phyBOARD-Pollux Carrier Board Connector Pin	SOM Signal Name	SOM Voltage Domain	Signal Level	Signal Type	Description
LVDS channel 1					
C36 **(A1)**	X_LVDS1_D0_N	VDDA_1V8	LVDS	LVDS_O	LVDS1 DATA0-
C37 **(A2)**	X_LVDS1_D0_P	VDDA_1V8	LVDS	LVDS_O	LVDS1 DATA0+
C38 **(A4)**	X_LVDS1_D1_N	VDDA_1V8	LVDS	LVDS_O	LVDS1 DATA1-
C39 **(A5)**	X_LVDS1_D1_P	VDDA_1V8	LVDS	LVDS_O	LVDS1 DATA1+
C41 **(A6)**	X_LVDS1_CLK_N	VDDA_1V8	LVDS	LVDS_O	LVDS1 Clock-
C42 **(A7)**	X_LVDS1_CLK_P	VDDA_1V8	LVDS	LVDS_O	LVDS1 Clock+
C43 **(A9)**	X_LVDS1_D2_N	VDDA_1V8	LVDS	LVDS_O	LVDS1 DATA2-

SOM Connector Pin (DSC Contact) / phyBOARD-Pollux Carrier Board Connector Pin	SOM Signal Name	SOM Voltage Domain	Signal Level	Signal Type	Description
C44 **(A10)**	X_LVDS1_D2_P	VDDA_1V8	LVDS	LVDS_O	LVDS1 DATA2+
C46 **(A11)**	X_LVDS1_D3_N	VDDA_1V8	LVDS	LVDS_O	LVDS1 DATA3-
C47 **(A12)**	X_LVDS1_D3_P	VDDA_1V8	LVDS	LVDS_O	LVDS1 DATA3+
LVDS channel 0					
C48 **(B1)**	X_LVDS0_D0_N	VDDA_1V8	LVDS	LVDS_O	LVDS0 DATA0-
C49 **(B2)**	X_LVDS0_D0_P	VDDA_1V8	LVDS	LVDS_O	LVDS0 DATA0+
C51 **(B4)**	X_LVDS0_D1_N	VDDA_1V8	LVDS	LVDS_O	LVDS0 DATA1-
C52 **(B5)**	X_LVDS0_D1_P	VDDA_1V8	LVDS	LVDS_O	LVDS0 DATA1+

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SOM Connector Pin (DSC Contact) / phyBOARD-Pollux Carrier Board Connector Pin	SOM Signal Name	SOM Voltage Domain	Signal Level	Signal Type	Description
C53 **(B7)**	X_LVDS0_CLK_N	VDDA_1V8	LVDS	LVDS_O	LVDS0 Clock-
C54 **(B8)**	X_LVDS0_CLK_P	VDDA_1V8	LVDS	LVDS_O	LVDS0 Clock+
C56 **(B10)**	X_LVDS0_D2_N	VDDA_1V8	LVDS	LVDS_O	LVDS0 DATA2-
C57 **(B11)**	X_LVDS0_D2_P	VDDA_1V8	LVDS	LVDS_O	LVDS0 DATA2+
C58 **(B13)**	X_LVDS0_D3_N	VDDA_1V8	LVDS	LVDS_O	LVDS0 DATA3-
C59 **(B14)**	X_LVDS0_D3_P	VDDA_1V8	LVDS	LVDS_O	LVDS0 DATA3+

13.3 MIPI-DSI Display Interface (DSI)

The phyCORE-i.MX 8M Plus offers one MIPI-DSI display interface. MIPI-DSI has 4 channels, supporting one display with a resolution of up to 1920 x 1080 at 60Hz.

The locations of the MIPI-DSI signals are shown below:

TABLE 27: Display Interface MIPI / DSI Signal Locations

SOM Connector Pin (DSC Contact) / phyBOARD-Pollux Carrier Board Connector Pin	SOM Signal Name	SOM Voltage Domain	Signal Level	Signal Type	Description
F6 (A127)	X_MIPI_DSI1_D0_N	VDDA_1V8	LVDS	DSI2_O	DSI DATA0-
F7 (A126)	X_MIPI_DSI1_D0_P	VDDA_1V8	LVDS	DSI2_O	DSI DATA0+
F8 (A124)	X_MIPI_DSI1_D1_N	VDDA_1V8	LVDS	DSI2_O	DSI DATA1-
F9 (A123)	X_MIPI_DSI1_D1_P	VDDA_1V8	LVDS	DSI2_O	DSI DATA1+
F11 (A122)	X_MIPI_DSI1_CLK_N	VDDA_1V8	LVDS	DSI2_O	DSI Clock-
F12 (A121)	X_MIPI_DSI1_CLK_P	VDDA_1V8	LVDS	DSI2_O	DSI Clock+
F13 (A119)	X_MIPI_DSI1_D2_N	VDDA_1V8	LVDS	DSI2_O	DSI DATA2-
F14 (A118)	X_MIPI_DSI1_D2_P	VDDA_1V8	LVDS	DSI2_O	DSI DATA2+

SOM Connector Pin (DSC Contact) / phyBOARD-Pollux Carrier Board Connector Pin	SOM Signal Name	SOM Voltage Domain	Signal Level	Signal Type	Description
F16 **(A117)**	X_MIPI_DSI1_D3_N	VDDA_1V8	LVDS	DSI2_O	DSI DATA3-
F17 **(A116)**	X_MIPI_DSI1_D3_P	VDDA_1V8	LVDS	DSI2_O	DSI DATA3+

14 Camera Connections

The phyCORE-i.MX 8M Plus offers 2 MIPI-CSI interfaces to connect digital cameras with a resolution of up to 12MP. The two MIPI/CSI-2 camera interfaces of the i.MX 8M Plus extends to the phyCORE-Connector X1 with 4 data lanes and one clock lane.

The locations of the MIPI-CSI signals are shown below:

TABLE 28: Camera Interface MIPI / CSI-2 Signal Locations

SOM Connector Pin (DSC Contact) / phyBOARD-Pollux Carrier Board Connector Pin	SOM Signal Name	SOM Voltage Domain	Signal Level	Signal Type	Description
D34 (B204)	X_MIPI_CSI1_D0_N	VDDA_1V8	LVDS	CSI2_I	CSI1 DATA0-
D35 (B205)	X_MIPI_CSI1_D0_P	VDDA_1V8	LVDS	CSI2_I	CSI1 DATA0+
D37 (B207)	X_MIPI_CSI1_D1_N	VDDA_1V8	LVDS	CSI2_I	CSI1 DATA1-
D38 (B208)	X_MIPI_CSI1_D1_P	VDDA_1V8	LVDS	CSI2_I	CSI1 DATA1+
D39 (B209)	X_MIPI_CSI1_CLK_N	VDDA_1V8	LVDS	CSI2_I	CSI1 Clock-
D40 (B210)	X_MIPI_CSI1_CLK_P	VDDA_1V8	LVDS	CSI2_I	CSI1 Clock+
D42 (B212)	X_MIPI_CSI1_D2_N	VDDA_1V8	LVDS	CSI2_I	CSI1 DATA2-

SOM Connector Pin (DSC Contact) / phyBOARD-Pollux Carrier Board Connector Pin	SOM Signal Name	SOM Voltage Domain	Signal Level	Signal Type	Description
D43 (B213)	X_MIPI_CSI1_D2_P	VDDA_1V8	LVDS	CSI2_I	CSI1 DATA2+
D44 (B214)	X_MIPI_CSI1_D3_N	VDDA_1V8	LVDS	CSI2_I	CSI1 DATA3-
D45 (B215)	X_MIPI_CSI1_D3_P	VDDA_1V8	LVDS	CSI2_I	CSI1 DATA3+
F18 (A148)	X_MIPI_CSI2_D3_N	VDDA_1V8	LVDS	CSI2_I	CSI2 DATA3-
F19 (A149)	X_MIPI_CSI2_D3_P	VDDA_1V8	LVDS	CSI2_I	CSI2 DATA3+
F21 (A151)	X_MIPI_CSI2_D2_N	VDDA_1V8	LVDS	CSI2_I	CSI2 DATA2-
F22 (A152)	X_MIPI_CSI2_D2_P	VDDA_1V8	LVDS	CSI2_I	CSI2 DATA2+

SOM Connector Pin (DSC Contact) / phyBOARD-Pollux Carrier Board Connector Pin	SOM Signal Name	SOM Voltage Domain	Signal Level	Signal Type	Description
F23 **(A153)**	X_MIPI_CSI**2**_CLK_N	VDDA_1V8	LVDS	CSI2_I	CSI2 Clock-
F24 **(A154)**	X_MIPI_CSI**2**_CLK_P	VDDA_1V8	LVDS	CSI2_I	CSI2 Clock+
F26 **(A156)**	X_MIPI_CSI**2**_D1_N	VDDA_1V8	LVDS	CSI2_I	CSI2 DATA1-
F27 **(A157)**	X_MIPI_CSI**2**_D1_P	VDDA_1V8	LVDS	CSI2_I	CSI2 DATA1+
F28 **(A158)**	X_MIPI_CSI**2**_D0_N	VDDA_1V8	LVDS	CSI2_I	CSI2 DATA0-
F29 **(A159)**	X_MIPI_CSI**2**_D0_P	VDDA_1V8	LVDS	CSI2_I	CSI2 DATA0+

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15 RTC

The i.MX 8M Plus has an on-board, externally mounted RTC. The RV-3028 is the newest generation of RTC from Micro Crystal with an extremely low backup current of typically 40nA at 25 degrees. PHYTEC uses the most optimal implementation in each phyCORE design to give the most optimal usage for all customers.

The RTC is accessible over I2C1 on Address 0x52. In a normal operation state, the RTC power is supplied from the SOM voltage VDD_3V3. If the SOM is not powered and RTC backup is needed, the VBACKUP Pin of the RTC can be supplied over the VBAT pin X1-C9.

The RTC provides an interrupt output signal (X_RTC_INT), which is fed to the module connector X1-C10. This signal is an open drain (OD). The on-board pull-up resistor R12 is, by default, not mounted. To use the X_RTC_INT signal, add an external pull-up resistor (e.g., 10k) to an appropriate I/O voltage level (e.g., VBAT).

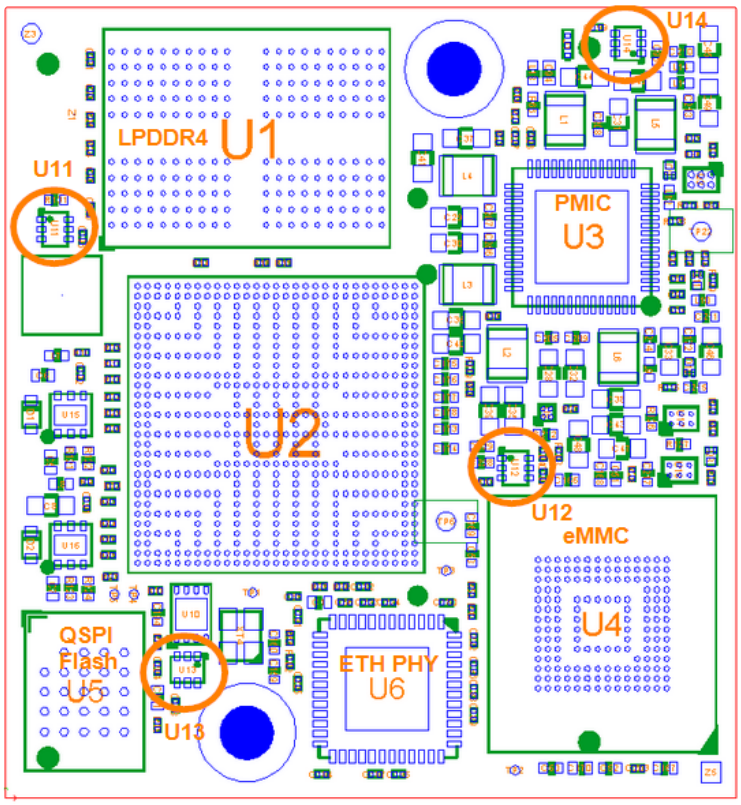
Furthermore, the RTC is able to supply a programmable clock output signal (push-pull) RTC_CLKOUT. Frequencies of 1/32/64/1024/8192 Hz and 32.768 Hz (default) are programmable. The RTC_CLKOUT signal is fed via soldering jumper J1 to the module connector at X1-D12. For a detailed description of the programming capabilities of the RTC, refer to the *Micro Crystal RV-3020 App-Manua*l.

16 Temperature Sensors

The phyCORE-i.MX 8M Plus supports two internally sensored thermal zones in the i.MX 8M Plus CPU as well as 4 externally sensored thermal zones for monitoring board-level temperatures. The presence of the sensors depends on the delivery variant of the module.

The external temperature sensors are located at the following positions.

FIGURE 9: Temperature Sensor Locations



The TMP102 temperature sensor devices used are connected to the I2C1 bus. TMP102 measures temperatures from -40 °C to +125 °C. For a more detailed description of TMP102, refer to the Texas Instruments *TMP102 Datasheet*.

TABLE 29: I2C1 Temperature Sensor Slave Addresses

Sensor	I2C slave address
U11	0x48
U12	0x49
U13	0x4A
U14	0x4B

17 CPU Core Frequency Scaling

The phyCORE-i.MX 8M Plus on the phyBOARD-Pollux is able to scale the clock frequency and voltage. This is used to save power and reduce heat dissipation when the full performance of the CPU is not needed. Scaling the frequency and voltage is referred to as 'Dynamic Voltage and Frequency Scaling' (DVFS).

The phyCORE-i.MX 8M Plus BSP supports the DVFS feature. The *Linux* kernel provides a DVFS framework that allows each CPU core to have a min/max frequency as well as the applicable voltage and a governor that governs these values depending on the system load. Depending on the i.MX 8M Plus variant used; several different frequencies are supported. Further details on how to configure this governor can be found in the phyCORE-i.MX 8M Plus BSP Manual.

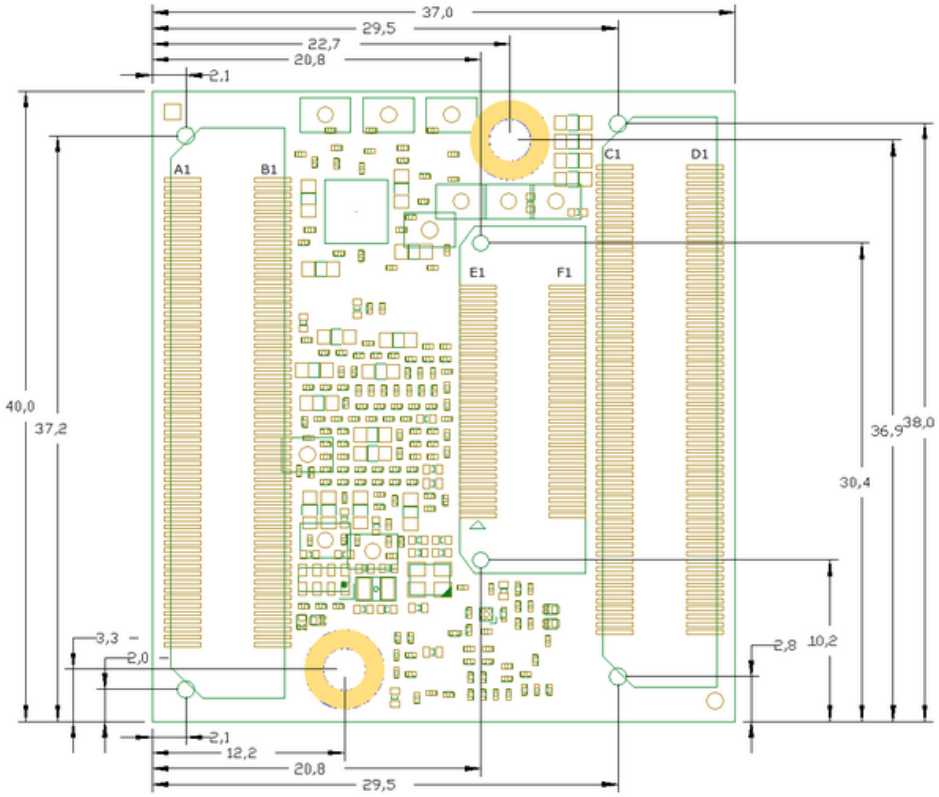
18 Technical Specifications

Warning

Due to changes in functionality and design that are currently being developed, there are several values that cannot be determined in time for the release of this manual. All values with "TBD (To Be Determined)" are currently being evaluated. These values will be added to future manual editions.

The module's profile is max. 6 mm thick, with a maximum component height of 1.0 mm on the bottom (connector) side of the PCB and approximately 1.2 mm on the top (microcontroller) side. The board itself is approximately 1.6 mm thick. The phyCORE-i.MX 8M Plus Footprint can be seen below.

FIGURE 10: phyCORE-i.MX 8M Plus Footprint (top to bottom view; unit in mm)



The DSC version has a profile of max. 4 mm thick, with a maximum component height of 1.0 mm on the bottom side of the PCB and approximately 1.5 mm on the top side. The board itself is approximately 1.5 mm thick. The phyCORE-8.MX 8M Plus DSC footprint can be seen below.

FIGURE 11: phyCORE-i.MX 8M Plus DSC footprint (top view; unit is mm)

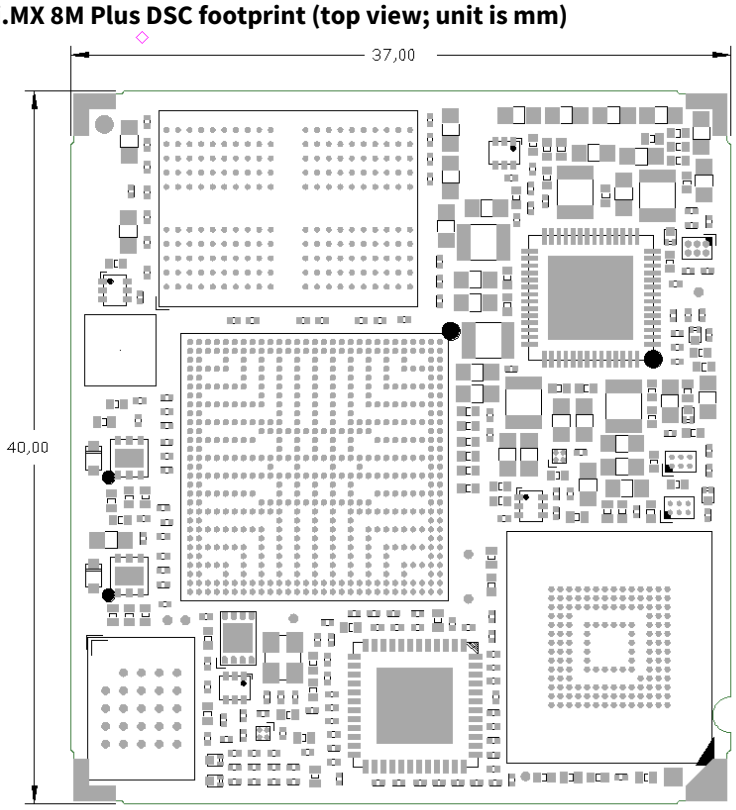
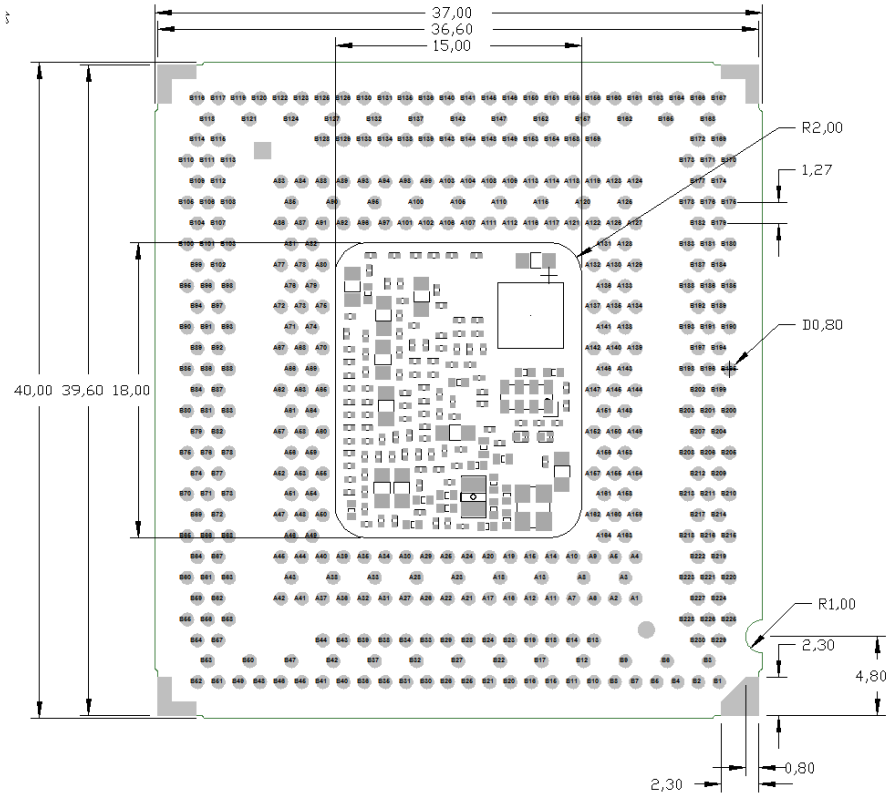


FIGURE 12: phyCORE-i.MX 8M Plus DSC footprint (bottom view top down; unit is mm)



Tip

For a downloadable version of the phyCORE-i.MX 8M Plus footprint, go to the download section of our product website:
https://www.phytec.de/produkte/system-on-modules/phycore-imx-8m-plus/#downloads

Additional specifications:

TABLE 30: Technical Specifications

Dimensions:	40 x 37 mm
Weight:	11 g **(8 g)**
Storage Temperature:	-40 to +85 °C
Operating Temperature:	Product Temperature Grades
Humidity:	10 % - 90 % (non-condensing)
Operating Voltage:	3.2 V .. 3.5 V
Power Consumption:	phyCORE-i.MX 8M Plus Power Consumption

These specifications describe the standard configuration of the phyCORE-i.MX 8M Plus as of the printing of this manual.

18.1 phyCORE-i.MX 8M Plus Power Consumption

The values listed in the table below are a guideline to determine the required dimensions of the power supply circuitry on a carrier board. They do not take application-specific load situations into account. These values have been generated by looking at the maximum power consumption measured using different load scenarios and adding a voltage source of 3.3 V. These values are based on internal PHYTEC testing. Customers need to consider their application power requirements to ensure they do not generate a load greater than the values listed here.

TABLE 31: phyCORE-i.MX 8M Plus Power Consumption

Required Supply Voltage	3.3 V
Ramp-Up Time (10 %-90 %)	100 µs to 10 ms
Allowed Tolerance of Supply Voltage	3.2 V .. 3.5 V (Abs. max 3.8 V)
Max. current consumption	4 A

For power measurement, a SOM (PCL-070-0F3243I.A0) with 2 GB RAM, 8GB eMMC, ETH0, HDMI, and an IMX8ML8DVNLZAA was used together with PD21.1.2.

TABLE 32: phyCORE-i.MX 8M Plus Power Consumption Test Scenarios

	Case 1	Case 2	Case 3	Case 4	Case 5	Case 6
eMMC-Boot system idle DVFS ondemand	X	X	X	X	X	X
iperf3 client eth0 (~900MBit/s)		X	X	X	X	X
CPU-Load (4x dd from /dev/urandom to /dev/null)			X	X	X	X
RAM-Load (memtester)				X	X	X
GPU-Load (qt5-opengles2-test)					X	
VPU-Load (video 1080p)						X
Power Consumption [Watt]	2.2 W	2.5 W	2.9 W	3.3 W	3.6 W	3.8 W
CPU Thermal Zone 0 [°C]	50	53	59	62	68	68
CPU Thermal Zone 1 [°C]	51	55	62	66	72	73
CPU Surface Temperature [°C]	50	54	60	63	69	70
RAM Surface Temperature [°C]	44	47	49	52	59	57
Eth-PHY Surface Temperature [°C]	48	51	53	55	59	58
PMIC Surface Temperature [°C]	43	46	49	52	57	56
Ambient [°C]	22	22	22	22	22	22

Additionally, there are some values that cannot be tested. Situations such as suspending to RAM, suspend freeze, and standby mode must be tested on a case-by-case basis to ensure the application's power consumption stays within the guidelines stated above.

Tip

For further information and assistance regarding your application's power consumption, please contact PHYTEC sales.

18.2 Product Temperature Grades

Warning

The right temperature grade for the module greatly depends on the use case. It is necessary to determine if the use case suits the temperature range of the chosen module (see below). A heat spreader can be used if temperature compensation is required.

The feasible operating temperature of the SOM highly depends on the use case of your software application. Modern high-performance microcontrollers and other active parts, such as the ones described within this manual, are usually rated by qualifications based on tolerable junction or case temperatures. Therefore, making a general statement about minimum or maximum ambient temperature ratings for the described SOM is not possible.

However, the above-mentioned parts are available at different temperature qualification levels by the producers. We offer our SOMs in different configurations, making use of those temperature qualifications. To indicate which level of temperature qualification is used for active and passive parts of a SOM configuration, we have categorized our SOMs into three temperature grades.

The table below describes these grades in detail. This table describes a set of components that, in combination, add up to a useful set of product options with different temperature grades. This enables us to make use of cost optimizations depending on the required temperature range.

In order to determine the right temperature grade and whether the minimum or maximum qualification levels are met within an application, the following conditions must be defined by considering the use case:

- Determined the processing load for the given software use case
- Maximum temperature ranges of components (table below)
- Power consumption resulting from a baseload and the calculating power required (in consideration of peak loads as well as time periods for system cooldown)
- Surrounding temperatures and existing airflow in case the system is mounted into a housing
- Heat resistance of the heat dissipation paths within the system along with the considered usage of a heat spreader or a heat sink to optimize heat dissipation

TABLE 33: Product Temperature Grades

Product Temperature Grade	Controller Range (Junction Temperature)	RAM (Case Temperature)	Other (Ambient)
I	Industrial: -40 °C to +105 °C	Industrial: -40 °C to +95 °C	Industrial: -40 °C to +85 °C
C	Commercial: 0 °C to +95 °C	Consumer: 0 °C to +95 °C	Consumer: 0 °C to +70 °C

Tip

Core temperature is typically monitored by the operating system. The Linux kernel for industrial-grade controllers generates a warning at 95°C and a shutdown at 100°C. Commercial-grade controllers generate a warning at 85°C and a shutdown at 90°C. If the system starts at the shutdown temperature, the system won't boot and will stop operating. Please refer to the Thermal Management section of our BSP manual.

18.3 Connectors on the phyCORE-i.MX 8M Plus

TABLE 34: phyCORE-Connector (X1 2x120+60 pins)

Manufacturer	Samtec
phyCORE-Connector (X1 2x120+60 pins)	
240 pins main connectors X1-A/B and X1-C/D	Two main connectors with 2x60 pins each.
Samtec part number (lead-free)	BSH-060-01-L-D-A-TR / REF-177857-02
PHYTEC part number (lead-free)	VB211
60 pins extension connectors X1-E/F	One extension connector with 2x 30 pins.
Samtec part number (lead-free)	BSH-030-01-L-D-A / REF-177855-01
PHYTEC part number (lead-free)	VB118

Information on the receptacle sockets that correspond to the connectors populating the underside of the phyCORE-i.MX 8 is provided below. The given connector height indicates the distance between the two connected PCBs when the module is mounted on the corresponding carrier board. In order to get the exact spacing, the maximum component height (1 mm) on the bottom side of the phyCORE must be subtracted.

Mating Connector

TABLE 35: To connect phyCORE-Connector (X1) with 5mm distance board-to-board

Manufacturer	Samtec
To connect phyCORE-Connector (X1) with 5mm distance board-to-board	
240 pins main connectors X1-A/B and X1-C/D	Two main connectors with 2x60 pins each.
Samtec part number (lead-free)	BTH-060-01-L-D-A-K-TR / REF-177862-03
PHYTEC part number (lead-free)	VM240
60 pins extension connectors X1-E/F	One extension connector with 2x 30 pins.
Samtec part number (lead-free)	BTH-030-01-L-D-A-K-TR
PHYTEC part number (lead-free)	VM368

Please refer to the corresponding data sheets and mechanical specifications provided by Samtec (www.samtec.com).

19 Hints for Integrating and Handling the phyCORE-i.MX 8M Plus

19.1 Integrating the phyCORE-i.MX 8M Plus

Besides this hardware manual, more information is available to facilitate the integration of the phyCORE-i.MX 8M Plus into customer applications.

1. The design of the phyBOARD-Pollux can be used as a reference for any customer application.
2. Many answers to common questions can be found at: https://www.phytec.de/produkte/system-on-modules/phycore-imx-8m/#downloads
3. The link “Carrier Board” within the category Dimensional Drawing leads to the layout data phyCORE-i.MX 8M Plus Footprint. It is available in different file formats. The use of this data allows the user to integrate the phyCORE-i.MX 8M Plus SOM as a single component into their design.
4. Different support packages are available for support in all stages of embedded development. Please visit https://www.phytec.de/support/support-pakete/ or https://www.phytec.eu/support/support-packages/ or contact our sales team for more details.

19.2 Handling the phyCORE-i.MX 8M Plus

19.2.1 phyCORE Module Modifications

The removal of various components, such as the microcontroller or the standard quartz, is not advisable given the compact nature of the module. Should this nonetheless be necessary, please ensure that the board, as well as surrounding components and sockets, remain undamaged while desoldering. Overheating the board can cause the solder pads to loosen, rendering the module inoperable. If soldered components need to be removed, the use of a desoldering pump, desoldering braid, an infrared desoldering station, desoldering tweezers, hot air rework station, or other desoldering method is strongly recommended. Follow the instructions carefully for whatever method of removal is used.

Warning

If any modifications to the module are performed, regardless of their nature, the manufacturer's guarantee may be null and void.

19.2.2 Integrating the phyCORE into a Target Application

Successful integration in the user target circuitry greatly depends on adherence to the layout design rules for the GND connections of the phyCORE module. For maximum EMI performance, PHYTEC recommends, as a general design rule, connecting all GND pins to a solid ground plane. At a minimum, all GND pin neighboring signals that are being used in the application circuitry should be connected to GND.

Tip

Specific details may need to be considered when designing a customer-specific carrier board. For design information on carrier board components, please check the ***Design Considerations*** in each component section of phyCORE-i.MX 8M Plus on the phyBOARD-Pollux. Be aware that not all components need to be considered when designing your own carrier board.

20 phyCORE-i.MX 8M Plus on the phyBOARD-Pollux

20.1 Hardware Overview

The phyBOARD-Pollux for phyCORE-i.MX 8M Plus is a low-cost, feature-rich software development platform supporting the NXP Semiconductors i.MX 8M Plus microcontroller. Due to numerous standard interfaces, the phyBOARD-Pollux i.MX 8M Plus can serve as the bedrock for any application. At the core of the phyBOARD-Pollux is the PCM-070/phyCORE-i.MX 8M Plus System On Module (SOM) containing the processor, LPDDR4 RAM, eMMC Flash, power regulation, supervision, transceivers, and other core functions required to support the i.MX 8M Plus processor. Surrounding the SOM is the PB-03123/phyBOARD-Pollux carrier board, adding power input, buttons, connectors, signal breakout, and Ethernet connectivity, along with other peripherals.

The PCM-070 System On Module connects to the phyBOARD-Pollux carrier board using 3 Samtec BTH connectors. This solution offers a highly flexible Single Board Computer for the i.MX 8M Plus processor, while maintaining most of the advantages of the SOM concept.

20.2 phyBOARD-Pollux Concept

PHYTEC phyCORE carrier boards are fully equipped with all mechanical and electrical components necessary for a fast, secure start-up. Subsequent communication to and programming of applicable PHYTEC System on Modules (SOM) is made easy. phyCORE carrier boards are designed for evaluation, testing, and prototyping of PHYTEC System on Modules in laboratory environments prior to their use in customer-designed applications.

This modular development platform concept includes the following components:

- The **phyCORE-i.MX 8M Plus Module** populated with the i.MX 8M Plus microcontroller and all applicable SOM circuitry, such as LPDDR4 SDRAM, eMMC-Flash, Ethernet-PHY, PMIC, etc.
- The **phyBOARD-Pollux Carrier Board** offers all essential components and connectors for a start-up, including a power supply for 24 V input voltage and interface connectors such as **HDMI**, **USB**, and **Ethernet**, which enable the use of the SOM's interfaces with a standard cable.

The carrier board can also serve as a reference design for developing custom target hardware in which the phyCORE SOM can be deployed. Carrier board schematics are available under a Non-Disclosure Agreement (NDA). The reuse of carrier board circuitry enables users of PHYTEC SOMs to shorten time-to-market, reduce development costs, and avoid substantial design issues and risks.

SBCplus Concept

The SBCplus concept was developed to meet the many small differences in customer requirements with little development effort. This greatly reduces the time-to-market. The core of the SBCplus concept is the SBC design library (a kind of construction set) that consists of a large number of function blocks (so-called "building blocks") that are continuously being refined and updated.

Recombining these function blocks allows PHYTEC to develop a customer-specific SBC within a short time. We are able to deliver production-ready custom single-board computers within a few weeks at very low costs. The already developed SBCs, such as the phyBOARD-Pollux, each represent a combination of different customer wishes. This means all necessary interfaces are already available on the standard versions, allowing PHYTEC SBCs to be integrated into a large number of applications without modification.

For any necessary detail adjustment, extension connectors are available, which enable a wide variety of functions to be added.

Tip

For further information, please contact PHYTEC sales.

20.3 phyBOARD-Pollux Features

The phyBOARD-Pollux supports the following features:

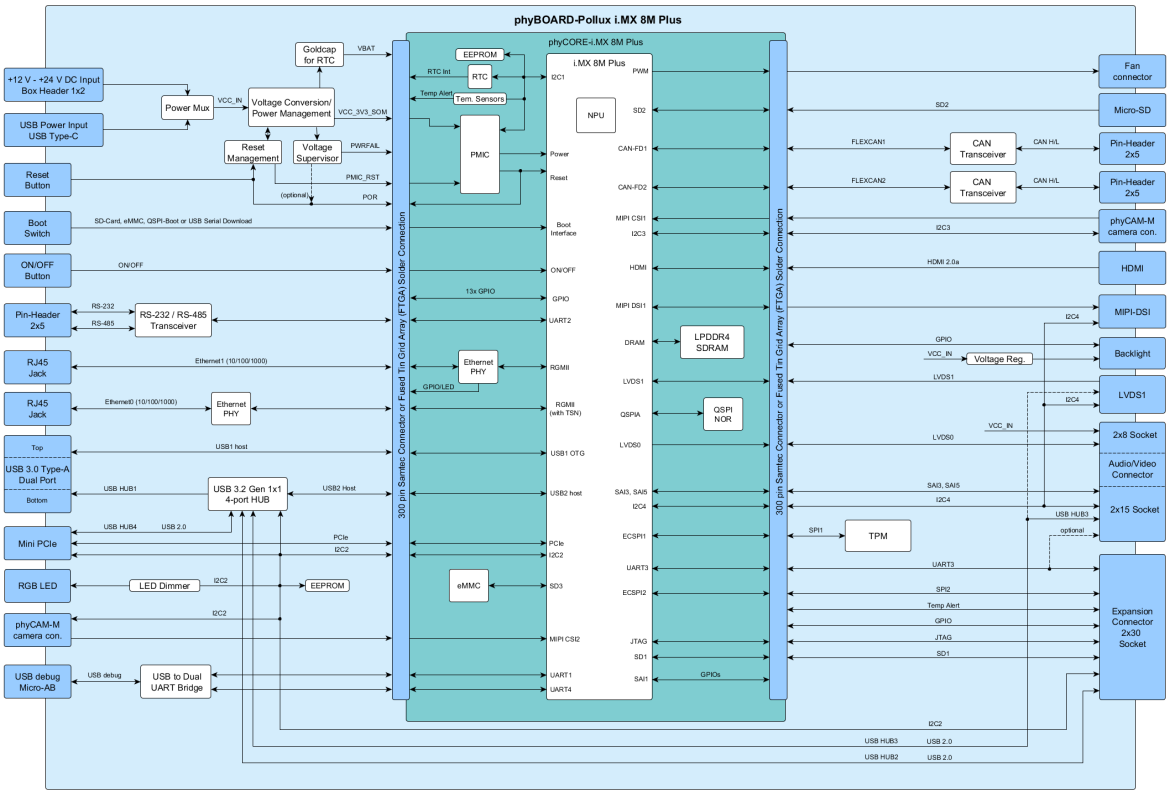
- Developed in accordance with PHYTEC's SBCplus concept (SBCplus Concept)
- Populated with PHYTEC's phyCORE-i.MX 8M Plus SOM
- Dimensions of 160 mm × 73 mm
- Boot from eMMC, SD Card, or over USB with the Serial Downloader
- Max. 1.3 GHz core clock frequency and up to four cores (at I-Temp Kit Version)
- 24 V power supply
- 2GB RAM (at Kit Version)
- 8GB eMMC (at Kit Version)
- 32MB NOR (at Kit Version)
- 4kB EEPROM
- 2x RJ45 jack for 10/100/1000 Mbps Ethernet
- 1x USB-PD (USB Power Delivery)
- 1x USB 3.0 host interface connected to a USB 3.0 4-port HUB. The 3.0 interface is brought out to an upright USB Standard-A connector. The other 3 ports are connected to the Mini PCI express connector, the Audio/ Video connector, and the expansion connector[2]
- 1x USB 3.0 host interface connected to phyCORE-i.MX 8M Plus Module
- 1x Secure Digital / MultiMedia Memory Card interface brought out to a Micro-SD connector
- 1x HDMI interface brought out to a standard Type-A connector
- 1x MIPI-DSI brought out via an A/V Connector
- 2x MIPI-CSI-2 camera interfaces brought out as a phyCAM-M interface
- 1x PCI interface brought out to a Mini PCI Express connector
- RS-232 and RS-485 multiprotocol transceiver supporting RS-232 including a handshake, RS-485 Half-Duplex, and RS-485 Full-Duplex signals with data rates of up to 20 Mbps (RS-485) / 1 Mbps (RS-232) (2×5 pin header 2.54 mm)
- Reset button
- ON/OFF button
- One multicolor LED
- SAI Audio is brought out via an A/V connector
- Digital I/O via an Expansion Connector
- JTAG via an Evaluation Adapter connected to the Expansion Connector
- Expansion connector for different interfaces
  - I^2C
  - SPI
  - UART
  - QSPI
  - USB
- RTC
  - Goldcap Backup supply for RTC
- on-board measurement of SOM Power Consumption
- on-board TPM Security Chip
- All processor interfaces available on-board (may be limited by predefined muxing)

Warning

2. There is no protective circuit for the USB interfaces brought out at the Mini PCI Express connector, expansion connector. and A/V connectors.

20.4 Block Diagram

FIGURE 13: phyBOARD-Pollux Block Diagram



20.5 Temperature Range

The vast majority of components on the phyBOARD Pollux have an operating temperature range of -40 °C to 85 °C. The following components are the exception:

TABLE 36: phyBOARD-Pollux Component Temperature Range

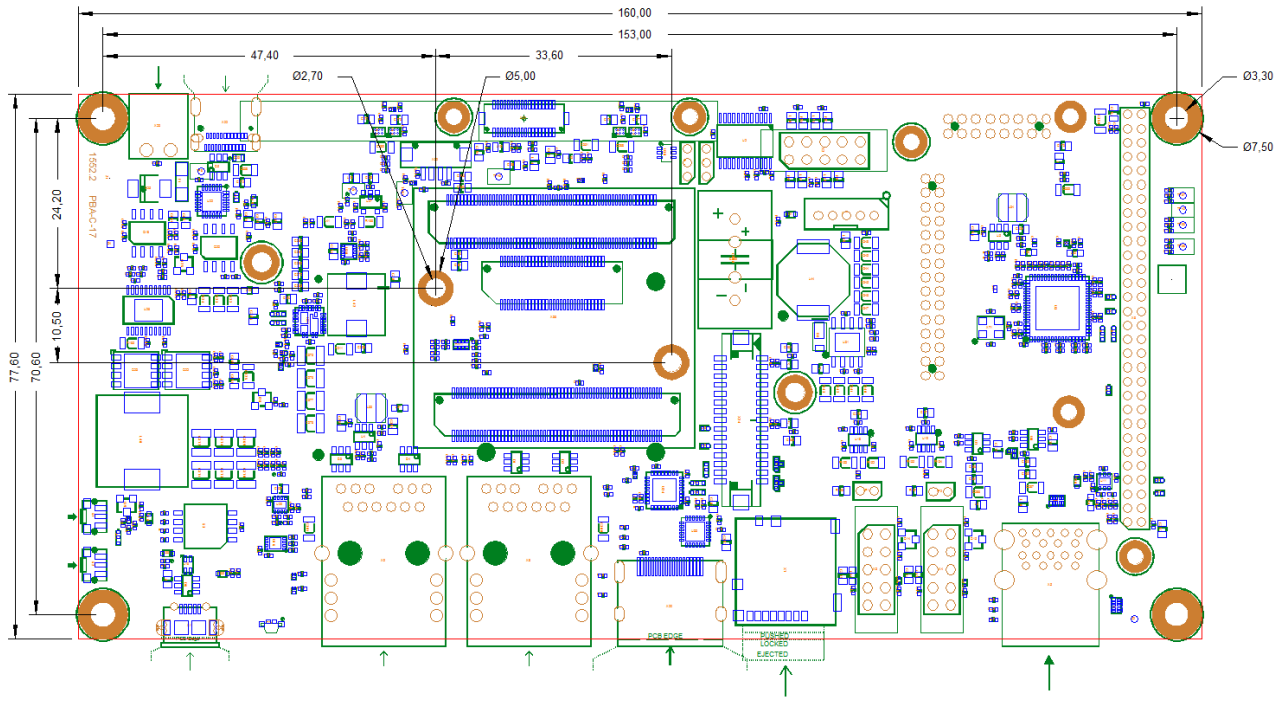
BOM No.	Component Description	Temperature Range	Advice
C398	GoldCap for RTC Backup	-20 °C to 85 °C	As alternative C399 with -40°C to 85 °C can be mounted
X5	Dual USB Connector	-20 °C to 85 °C	There is a drop-in replacement available from -40 °C to 85 °C
X20	HDMI Connector	-25 °C to 85 °C	There is no replacement available
X24	LVDS1 Data Connector	-35 °C to 85 °C	There is no replacement available
X26	LVDS1 Backlight Connector	-25 °C to 85 °C	There is no replacement available
X7	Micro SD-Card Slot	-25 °C to 85 °C	The SD-Card slot can be used in the range of -40 °C to 85 °C without mechanical changes
U24	Trusted Platform Module (TPM)	-20 °C to 85 °C	There is a drop-in replacement available from -40 °C to 85 °C

For this reason, the operation temperature range for the kit variant is: -20 °C to 85 °C. The storage temperature range is: -40 °C to 85 °C.

20.6 Mechanical Dimensions

For detailed dimensions, refer to the provided CAD data (e.g., DXF file) in the download section of our phyBOARD-Pollux download page.

FIGURE 14: phyBOARD-Pollux Mechanical Dimensions



21 phyBOARD-Pollux Components

Tip

For high-resolution pictures of the phyBOARD-Pollux, please go to the download section of our phyBOARD-Pollux download page.

Note

For easy reference, Pin 1 for each component has been highlighted.

21.1 phyBOARD-Pollux Component Placement Diagram

FIGURE 15: phyBOARD-Pollux Components (Top)

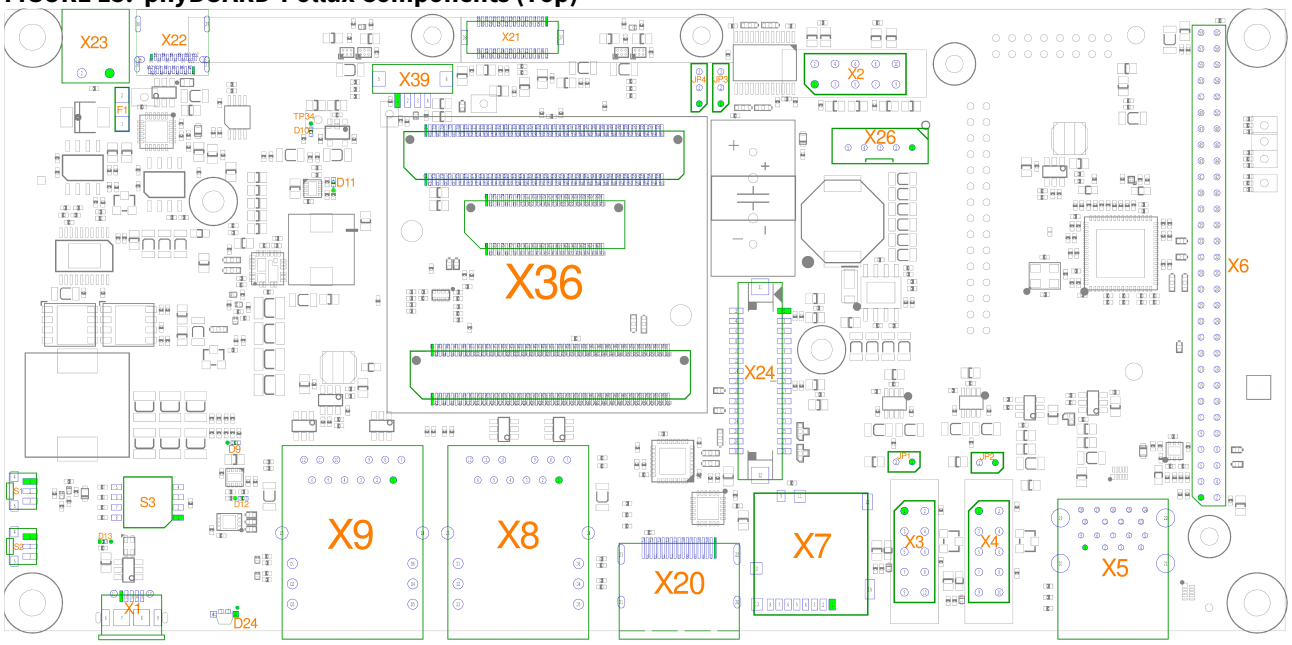
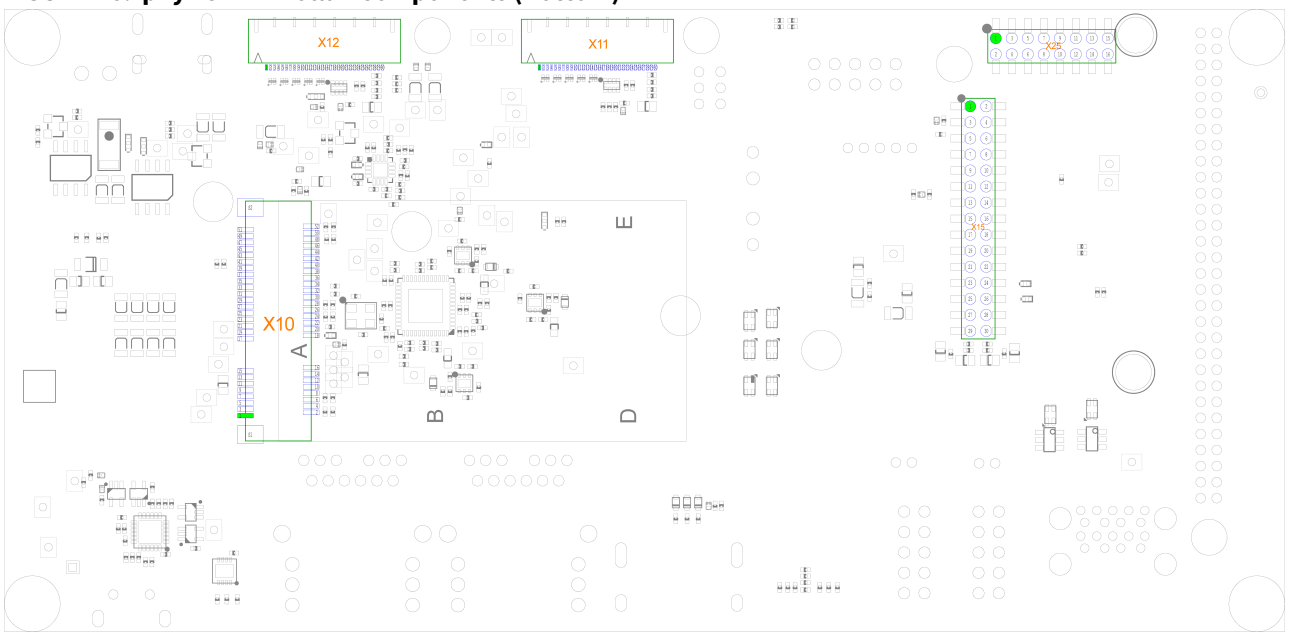


FIGURE 16: phyBOARD-Pollux Components (Bottom)



21.2 phyBOARD-Pollux Component Overview

The phyBOARD-Pollux features many different interfaces and is equipped with the components listed in the table Connectors and Pin Header. For a more detailed description of each component, refer to the appropriate section listed in the table below. phyBOARD-Pollux Components (Top) and phyBOARD-Pollux Components (Bottom) highlight the location of each component for easy identification.

21.2.1 Connectors and Pin Header

The table below lists all available connectors on the phyBOARD-Pollux.

TABLE 37: phyBOARD-Pollux Connectors and Pin HeaderPollux Component Temperature Range

Reference Designator	Description	Section
X1	USB Debug	USB Debug
X2	RS-232 / RS-485	RS-232 and RS-485
X3	CAN-FD1	CAN-FD
X4	CAN-FD2	
X5	USB1 / USB2 (via Hub)	USB Interfaces
X6	Expansion	Expansion Connector

Reference Designator	Description	Section
X7	Micro SD Card	Secure Digital Memory Card / MultiMedia Card
X8	Ethernet1	Ethernet
X9	Ethernet0	
X10	Mini-PCIe	PCIe
X11	CSI1	Camera Connectivity
X12	CSI2	
X15	SAI5 A/V-Connector	Audio/Video
X20	HDMI	HDMI
X21	MIPI-DSI	MIPI-DSI
X22	USB-PD In	Power Supply
X23	Power-In	
X24	LVDS1	LVDS
X25	LVDS0	Audio/Video
X26	Backlight for LVDS1	LVDS
X36	phyCORE Connector	phyCORE Connector
X39	Fan	Fan

Warning

Ensure that all module connections do not exceed their expressed maximum voltage or current. Maximum signal input values are indicated in the corresponding controller User's Manual/Data Sheets. As damage from improper connections varies according to use and application, the user must take appropriate safety measures to ensure that the module connections are protected from overloading through connected peripherals.

21.2.2 LEDs

The phyBOARD-Pollux is populated with 6 LEDs. One to indicate the status of the USB VBUS voltage of the USB Debug Interface, four to indicate the main board voltages. The sixth (D24) is user-programmable. phyBOARD-Pollux Components (Top) and phyBOARD-Pollux Components (Bottom) show the location of the LEDs. Their functions are listed in the table below:

TABLE 38: phyBOARD-Pollux LED Descriptions

LED	Color	Description	Section
D9	Green	Indicator for VCC_5V_MAIN	Power Supply
D10	Green	Indicator for VCC_3V3_SOM	
D11	Green	Indicator for VCC_3V3_SW	
D12	Green	Indicator for VCC_5V_SW	
D13	Green	Indicator for VBUS of USB Debug Interface	USB Debug
D24	RGB	User-programmable RGB LED	Multicolor (RGB) LED

21.2.3 Switches

The phyBOARD-Pollux is populated with three switches. The table below shows their functions:

TABLE 39: phyBOARD-Pollux Switches

Switch	Description	Section
S1	RESET	System Reset Button
S2	ON/OFF	System ON/OFF Button
S3	Boot Switch	Boot Switch

21.2.4 Jumpers

The phyBOARD-Pollux comes pre-configured with several removable jumpers (JP) and solder jumpers (J). These jumpers enable the flexible configuration of a limited number of features for development purposes.

Warning

Due to the small footprint of the solder jumpers (J), PHYTEC does not recommend manual jumper modifications. This may also render the warranty invalid. Only the removable jumper (JP) is described in this section. Contact our sales team if you need jumper configurations different from the default configuration.

The function of the removable jumper on the phyBOARD-Pollux is shown below. More detailed information can be found in the appropriate section. The locations of the removable jumpers can be found in phyBOARD-Pollux Components (Top).

TABLE 40: phyBOARD-Pollux Jumper Settings

Jumper	Position	Default	Description	Section
JP1	open	no	No 120 Ohms termination for CAN1	CAN-FD
	1+2	yes	**CAN1 terminated with 120 Ohms**	
JP2	open	no	No 120 Ohms termination for CAN2	
	1+2	yes	**CAN2 terminated with 120 Ohms**	
JP3	open	no	do not use	RS-232 and RS-485
	1+2	no	Enable RS-485 Mode for X2	
	2+3	yes	**Enable RS-232 Mode for X2**	
JP4	open	no	do not use	
	1+2	yes	**Half-Duplex RS-485 Mode for X2 (JP3 1+2)**	
	2+3	no	Full-Duplex RS-485 Mode for X2 (JP3 1+2)	

21.3 phyBOARD-Pollux SBC Component Detail

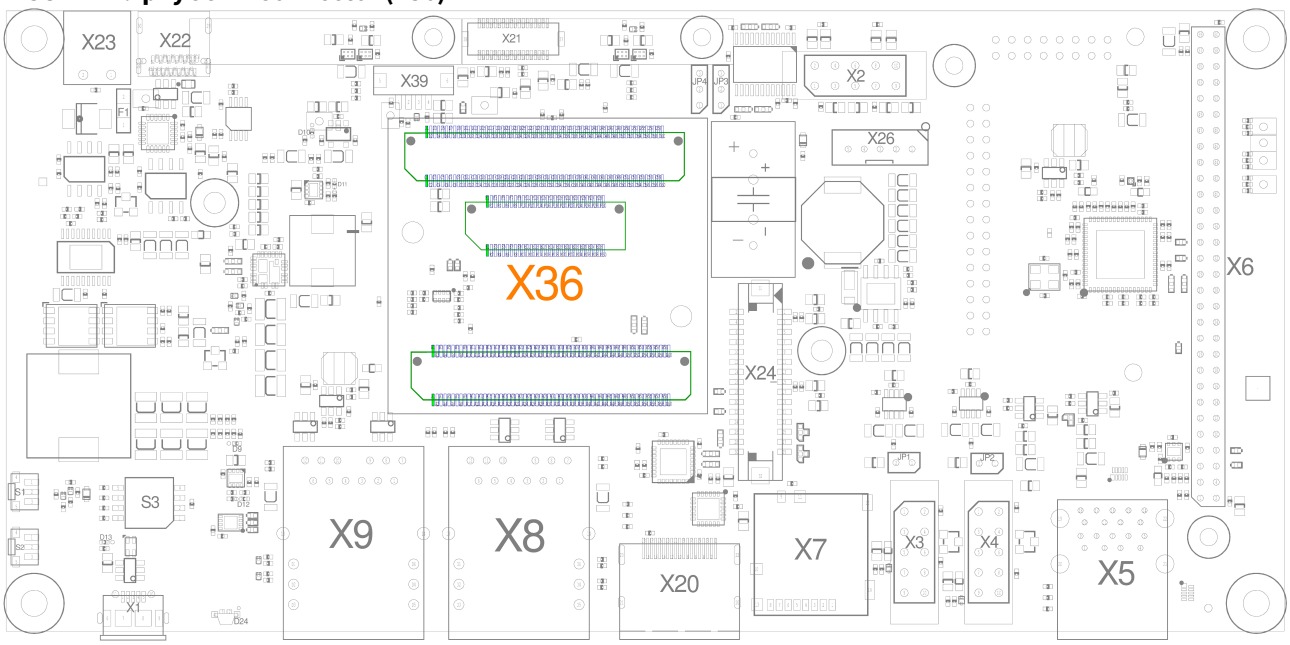
This section provides a more detailed look at the phyBOARD-Pollux components. Each subsection details a particular connector/interface and associated jumpers for configuring that interface.

Tip

Where possible, we also provide useful information regarding design considerations for components. This can be used if you plan to design your own carrier board.

21.3.1 phyCORE Connector (X36)

FIGURE 17: phyCORE Connector (X36)

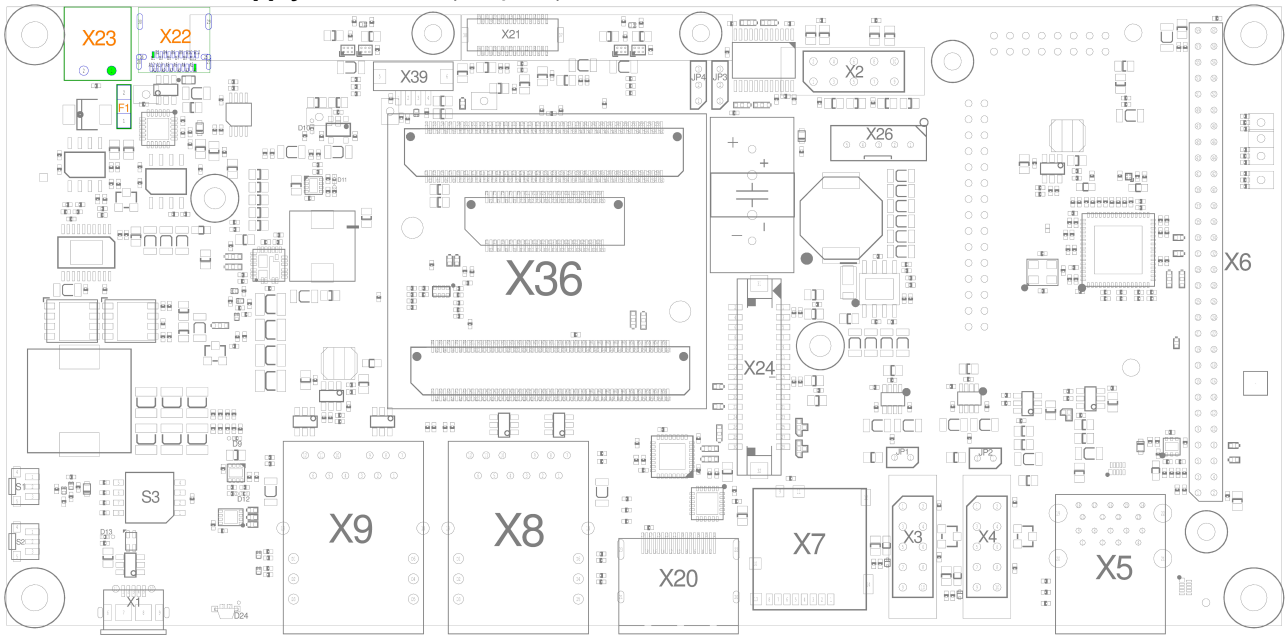


21.3.2 Power Supply (X22/X23)

Warning

Do not change modules or jumper settings while the phyBOARD-Pollux is supplied with power!

FIGURE 18: Power Supply Connectors (X22/X23)



The phyBOARD-Pollux can be powered either by a 2-pole Phoenix Contact MINI COMBICON base strip 3.5 mm connector (X23) or by a USB Power Delivery Supply (X22).

Warning

Do not power phyBOARD-Pollux via X22 and X23 at the same time!

The phyBOARD-Pollux is available with one power supply connector, a 2-pole Phoenix Contact MINI COMBICON base strip 3.5 mm connector (X23) suitable for a single 12 V/24 V supply voltage. The required current load capacity for all power supply solutions depends on the specific configuration of the phyCORE mounted on the phyBOARD-Pollux, the particular interfaces enabled while executing software, as well as whether an optional expansion board is connected to the carrier board.

The permissible input voltage is 12 V to 24 V DC if your SBC is equipped with a 2-pole Phoenix Contact MINI COMBICON base strip. A 24 V adapter with a minimum supply of 1.0 A is recommended to supply the board via the 2-pole base strip. The pin assignment for power supply connector X23:

TABLE 41: X23 Pin Assignment

Interface Pin #	Signal	Description
1	VCC_IN_PWR_CON	12 V (2A) to 24 V (1A) power supply (min./max. 10.8 V ... 26.4 V)
2	GND	Ground

21.3.2.1 USB Power Delivery Connector (X22)

The phyBOARD-Pollux can be powered by a USB Power Delivery Supply. The phyBOARD-Pollux provides the needed voltage and current with the connected supply and enables the on-board voltages. A 30 W USB-PD supply is recommended to power the phyBOARD-Pollux.

Note

Please note that the connector X22 is only usable as a power supply. It doesn't offer any USB communication interface functionality.

21.3.2.2 RTC Backup Supply

The phyBOARD-Pollux has a supercapacitor equipped to back up the VRTC rail of the phyCORE-i.MX 8M Plus. There is a multi-footprint to provide the most suitable Supercapacitor for customer applications. By default, a 220 mF type is mounted that can be replaced by a 470 mF type. Using the 220 mF type, the calculated minimum backup time is 176 h at 25 °C ambient temperature, or 313 h at 25 °C ambient temperature using the 470 mF type. The maximum permissible backup time can be much longer depending on the charging time, the actual dark current, and in particular, the ambient temperature.

21.3.3 UARTs

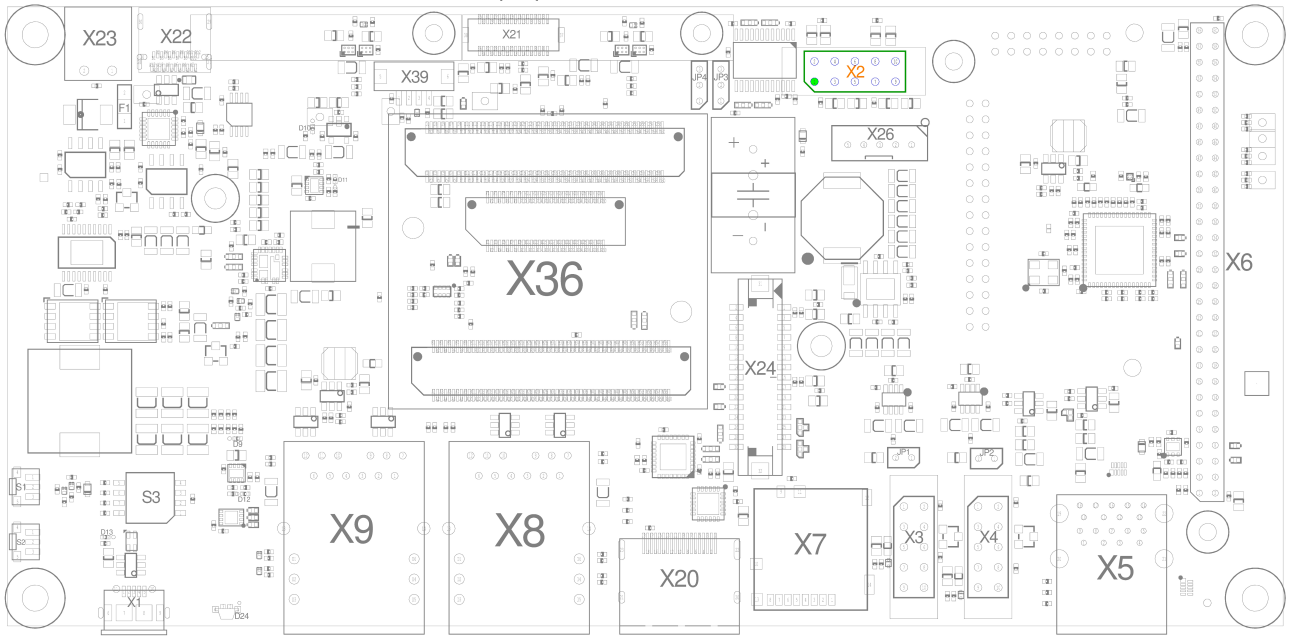
The phyCORE-i.MX 8M Plus supports up to 4 UART units. On the phyBOARD-Pollux, TTL-level signals of UART1 (the standard console) and UART4 are routed to the Silicon Labs CP2105 UART to USB converter expansion. This USB is brought out at Micro-USB connector X1. UART2 is connected to a multi-protocol transceiver for RS-232 and RS-485, available at pin header connector X2 at the RS-232 level, or at the RS-485 level. UART3 is at X6 (Expansion Connector) at the TTL level.

21.3.3.1 UART Design Considerations

When designing a custom carrier board, remember the TTL level is 3.3 V.

21.3.4 RS-232 and RS-485 (X2)

FIGURE 19: RS-232 and RS-485 Connector (X2)



Pin header connector X2 provides the UART2 signals of the i.MX 8M Plus at either the RS-232 or RS-485 level. The mode is selected by setting JP3 and JP4. The RS-232 interface is intended to be used as data terminal equipment (DTE) and allows for a 5-wire connection, including the signals RTS and CTS for hardware flow control. The RS-485 can be used as a Half-Duplex (3-wire) or Full-Duplex (5-wire). The table below shows the signal mapping of the RS-232 and RS-485 level signals at connector X2. The pinout is chosen to fit the official standard RS-232 pinout on a DE-9 plug (D-Sub 9 pin). Where TXD is pin 3, RXD is pin 2, RTS is pin 7, CTS is pin 8, and GND is pin 5. Suitable cables can be found in the table below.

TABLE 42: RS-232 and RS-485 selection

JP3	JP4	Mode
1+2	1+2	RS-485 Half-Duplex
1+2	2+3	RS-485 Full-Duplex
2+3	X	RS-232 (DTE)

TABLE 43: RS-232 and RS-485 Cable Options

PHYTEC Art-No.	Description
WF072	Insulation-displacement connector to DE-9 female
WF228	Insulation-displacement connector to DE-9 male
WK161	DE-9 RS-232 extension cable 1:1 3 m

PHYTEC Art-No.	Description
WK041	DE-9 null modem cable 1.8 m

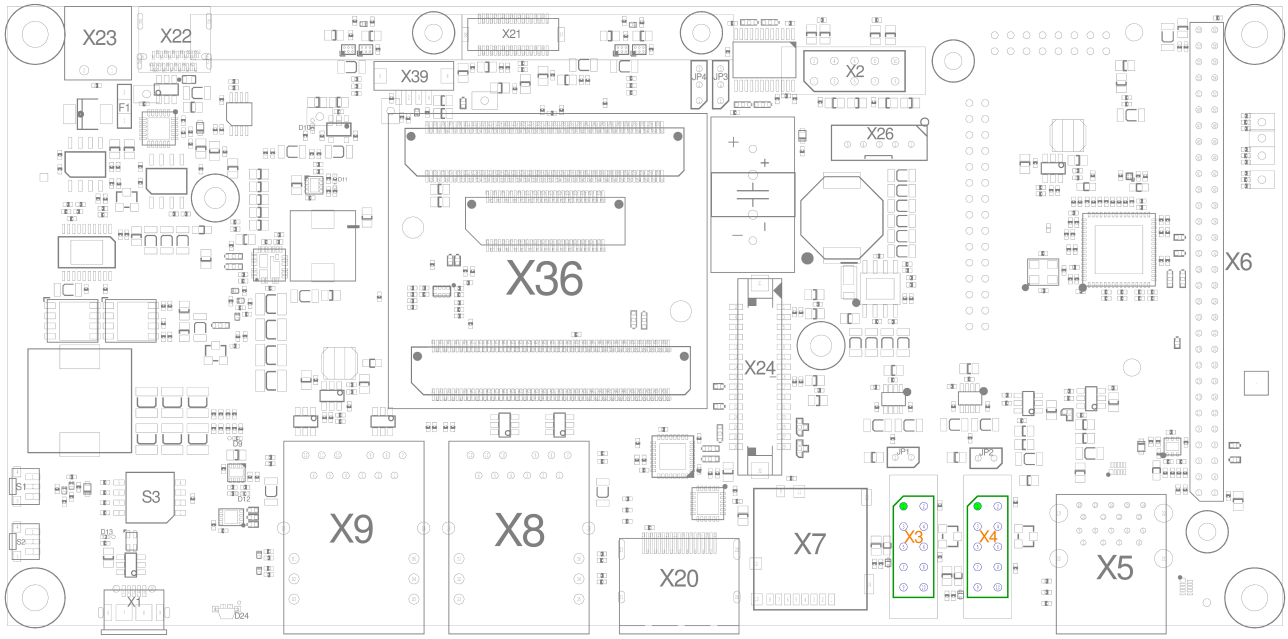
TABLE 44: RS-232/RS-485 (X2) Pin Assignment

Interface Pin #	Signal name	Signal Type	Signal Level	Description
1	N.C.	-	-	not connected
2	N.C.	-	-	not connected
3	RS-232_RXD RS-485_RX+	RS232_I RS485_I	- -	Input depends on JP3 and JP4 settings. See above.
4	RS-232_RTS RS-485_TX+ RS-485_D+	RS232_O RS485_O RS485_I/O	-	Input/Output depends on JP3 and JP4 settings. See above.
5	RS-232_TXD RS-485_TX- RS-486_D-	RS232_O RS485_O RS485_I/O	-	Input/Output depends on JP3 and JP4 settings. See above.
6	RS-232_CTS RS-485_RX-	RS232_I RS485_I	-	Input depends on JP3 and JP4 settings. See above.
7	N.C.	-	-	not connected
8	N.C.	-	-	not connected

Interface Pin #	Signal name	Signal Type	Signal Level	Description
9	GND	-	-	Ground
10	N.C.	-	-	not connected

21.3.5 CAN FD (X3/X4)

FIGURE 20: CAN FD (X3/X4)



The phyCORE i.MX 8M Plus FLEXCAN1 and FLEXCAN2 interfaces are brought out at X3 and X4, each as CAN FD. The maximum permissible CAN FD data rate is 8 Mbit/s. A 5 V power output is available to power a CAN device if needed. For development purposes, a 120 Ohms termination can be added by closing JP1 (CAN1) or JP2 (CAN2). For standard use, it is possible to mount a more suitable split termination in a customer-specific BOM.

The pinout is chosen to fit the unofficial standard CAN pinout on a DE-9 plug (D-Sub 9 pin), where CAN_L is pin 2, CAN_H is pin 7, GND is pin 3, and VCC_5V is pin 9. Suitable cables can be found in the table below.

TABLE 45: CAN FD Cable Options

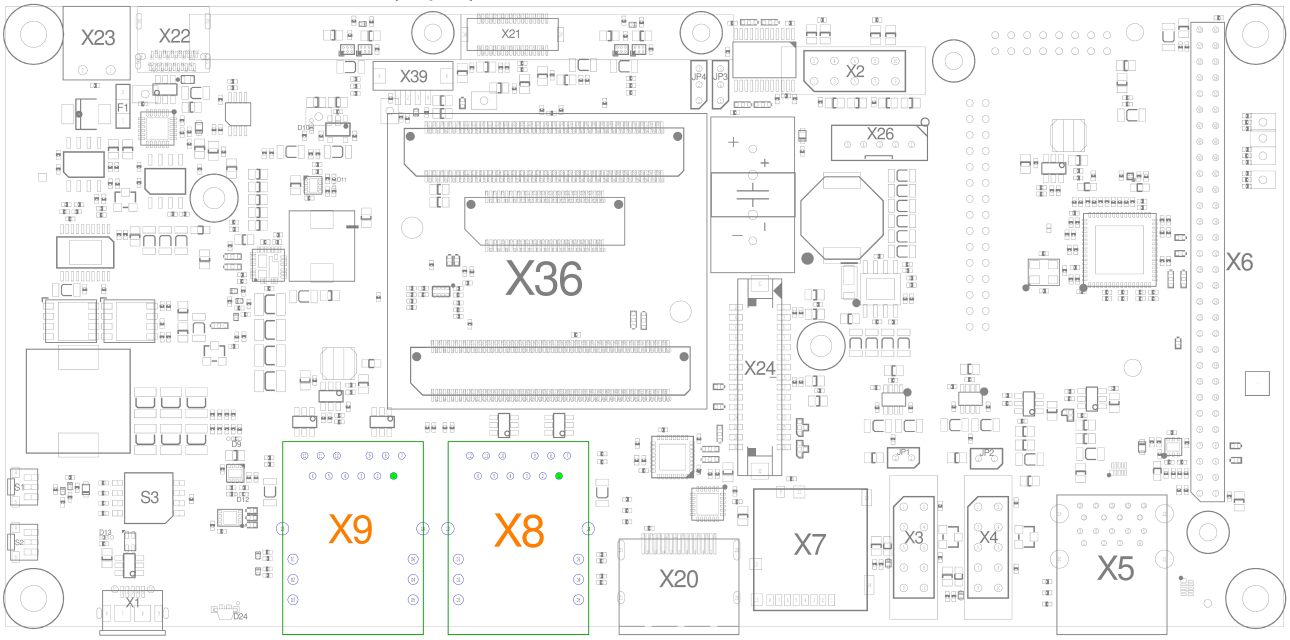
PHYTEC Art-No.	Description
WF072	Insulation-displacement connector to DE-9 female
WF228	Insulation-displacement connector to DE-9 male

TABLE 46: CAN FD1 (X3) Pin Assignment

Interface Pin #	Signal name	Signal Type	Signal Level	Description
1	N.C.	-	-	not connected
2	N.C.	-	-	not connected
3	CAN1_L	CAN_I/O	-	Low-level CAN bus input/output line
4	CAN1_H	CAN_I/O	-	High-level CAN bus input/output line
5	GND	-	-	Ground
6	N.C.	-	-	not connected
7	N.C.	-	-	not connected
8	VCC_5V_CAN1	PWR_O	5 V	5 V Supply
9	N.C.	-	-	not connected
10	N.C.	-	-	not connected

21.3.6 Ethernet (X8/X9)

FIGURE 21: Ethernet Connectors (X8/X9)



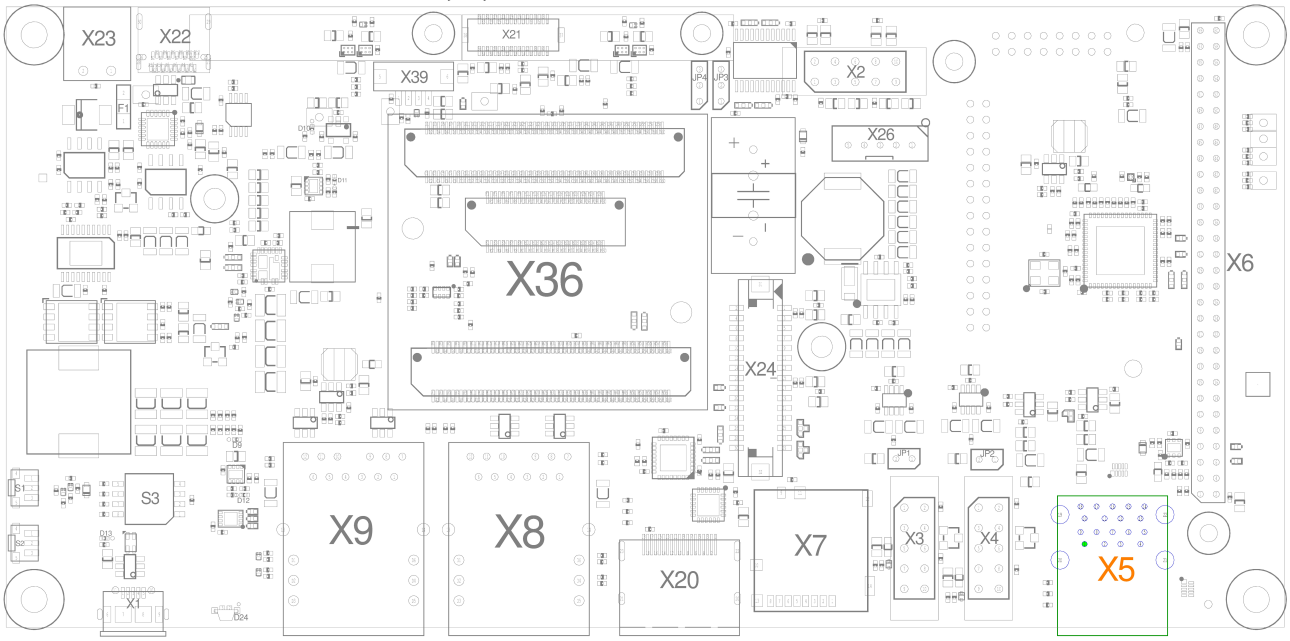
The phyBOARD-Pollux is equipped with 2 RJ45 connectors supporting a 10/100/1000Base-T network connection. The LEDs for LINK (green) and ACTIVITY (orange) indications are integrated into the connector. The Ethernet transceiver supports Auto MDI-X, eliminating the need for a direct connect LAN or cross-over path cable. They detect the TX and RX pins of the connected device and automatically configure the PHY TX and RX pins accordingly.

21.3.6.1 Ethernet Design Consideration (X8)

The data lanes should be routed with a differential impedance of 100 Ohms. The center taps of each pair's transformer have to be connected to GND through a 100nF capacitor. The LED pins are open-drain outputs of the SOM without a resistor, so they should be connected to the cathodes of the LEDs through a resistor.

21.3.7 USB 3.2 Gen1 Interfaces (X5)

FIGURE 22: USB 3.2 Gen1 Connectors (X5)



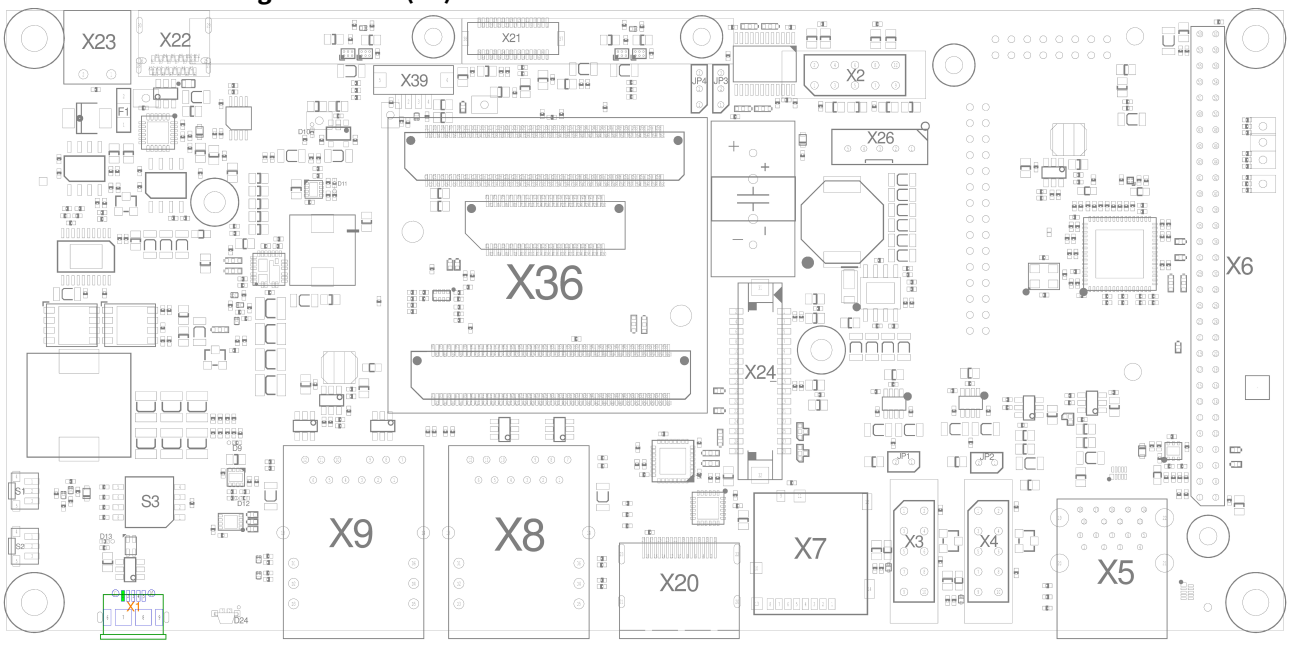
The phyBOARD-Pollux provides two USB 3.2 Gen1 (5 Gbps) interfaces. USB1 is accessible at the upper socket as a host. Using an A-plug to A-plug cable, it is possible to provide USB in dual role mode at this socket. USB dual role mode can be used for downloading program code into the external flash, internal controller RAM, or for debugging programs currently executing. The lower socket is connected via a USB 3.2 Gen 1 hub to USB2 of the phyCORE i.MX 8M Plus.

21.3.7.1 USB 3.2 Gen1 Design Considerations

Series capacitors are already present on the phyCORE-i.MX 8M Plus. It is not necessary to provide additional series capacitors in the TX lines. Take care to double-check the signal direction of the high-speed lines where TX is output and RX is input on phyCORE-i.MX 8M Plus. The TX and RX lines should be routed with an impedance of 50 Ohms to a ground plane and 100 Ohms differential impedance. Route USB D lines with 45 Ohms to Ground and 90 Ohms differential impedance.

21.3.8 USB Debug (X1)

FIGURE 23: USB Debug Connector (X1)



The main debug interface is UART1. UART4 is the debug interface for the M7 core. Both UART interfaces are connected to a UART-to-USB Converter (Silicon Labs CP2105). The USB interface is brought out at a Micro-USB-AB socket (X1). Use the following terminal settings to connect to phyBOARD-Pollux serial interfaces:

- Speed: 115200 baud
- Data bits: 8
- Stop bits: 1
- Parity: None
- Flow control: None

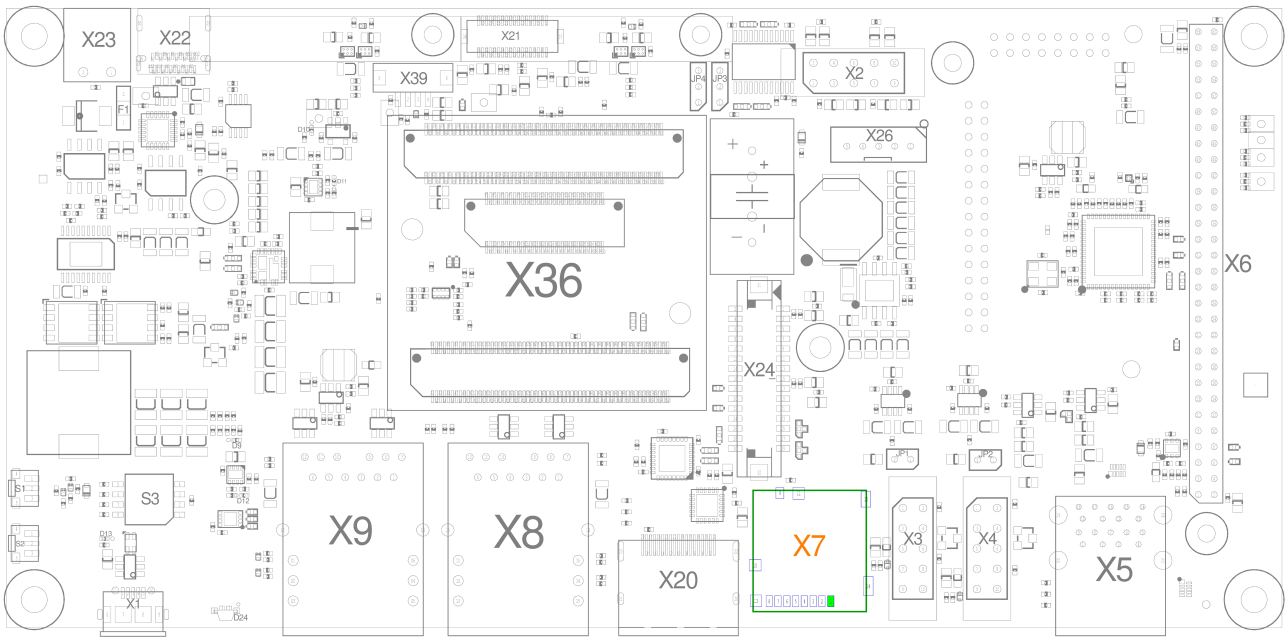
The table below shows the pinout of the USB Debug connector:

TABLE 47: X1 Pin Assignment

Interface Pin #	Signal name	Signal Type	Signal Level	Description
1	VCC_USB_DEBUG	PWR_I	5 V	VBUS Voltage input of Debug USB Port
2	USB_DEBUG_D_N	USB_I/O	-	USB 2.0 Negative Lane
3	USB_DEBUG_D_P	USB_I/O	-	USB 2.0 Positive Lane
4	ID	-	-	not connected
5	GND	-	-	Ground
6	SHIELD1	-	-	Ground
7	SHIELD2	-	-	Ground
8	SHIELD3	-	-	Ground
9	SHIELD4	-	-	Ground
10	SHIELD5	-	-	Ground
11	SHIELD6	-	-	Ground

21.3.9 Secure Digital Memory Card / MultiMedia Card (X7)

FIGURE 24: SD / MM Card Connector (X7)



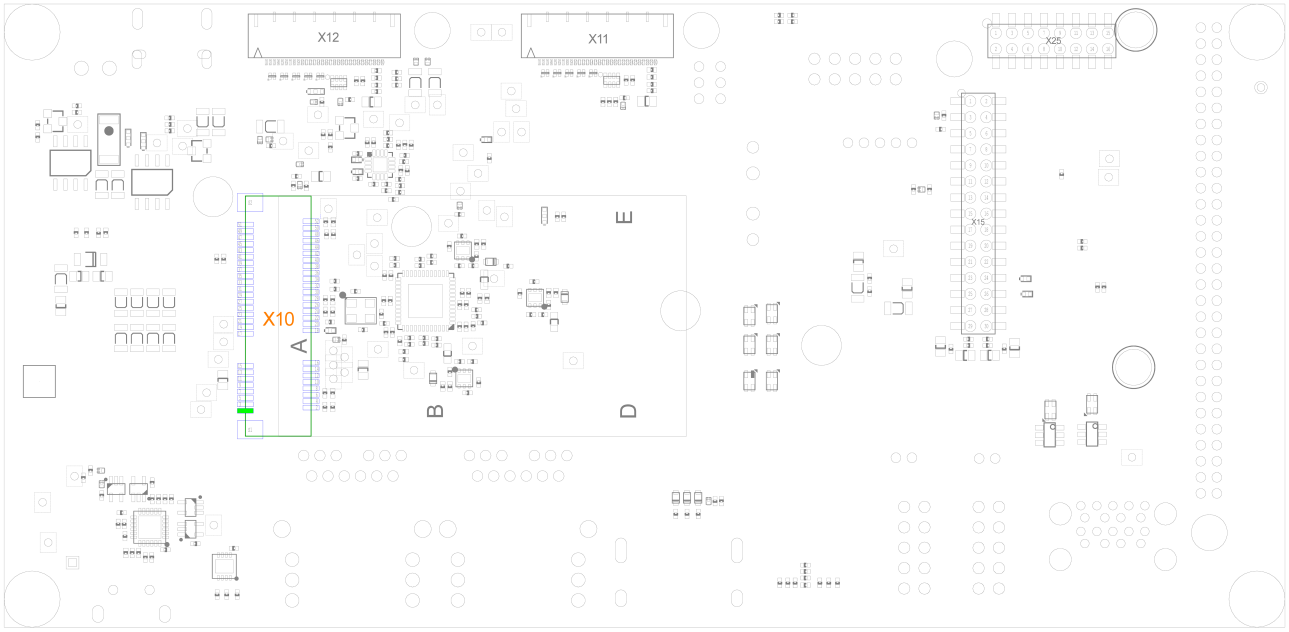
The phyBOARD-Pollux provides a standard microSDHC card slot at X7 for use with SD/MMC interface cards. It allows for a fast, easy connection to peripheral devices like microSD and MMC cards. Power to the SD interface is supplied by inserting the appropriate card into the SD/MMC connector. It also features card detection, a lock mechanism, and a smooth extraction function by pushing the card in and out.

21.3.9.1 SD / MM Card Design Considerations

Series resistors might be required to adapt the drive strength of the card. SD interface should be routed with an impedance of 50 Ohms to a ground plane. The trace length between CLK, CMD, and DATA lanes should be matched and kept as short as possible. Avoid Vias and take care of the signal current return path.

21.3.10 PCIe (X10)

FIGURE 25: PCIe Connector (X10)



The 1-lane PCI Express interface provides PCIe Gen. 3.0 functionality, which supports up to 8 GT/s operations. Various control signals are implemented with GPIOs. The PCIe interface is brought out at the Mini PCIe connector X10 shown above.

The table below shows in-depth information, such as pin assignment and signals used to implement special features of the Mini PCIe interface.

TABLE 48: X10 Pin Assignment

Interface Pin #	Signal name	Signal Type	Signal Level	Description
1	X_GPIO1_IO10/PCIe_nWAKE	O	3.3 V	nWAKE
2	VCC_3V3_SW	PWR_O	3.3 V	3.3 V Supply
3	X_SD1_DATA0/GPIO2_IO02/PCIe_COEX1	O	3.3 V	COEX1
4	GND	-	-	Ground
5	X_SD1_DATA1/GPIO2_IO03/PCIe_COEX2	O	3.3 V	COEX2
6	VCC_1V5_MPCI	PWR_O	1.5 V	1.5 V Supply
7	X_GPIO1_IO11/PCIe_nCLKREQ	I	3.3 V	Inverted Clock Request
8	NC	-	-	accessible at TP10
9	GND	-	-	Ground
10	NC	-	-	accessible at TP11
11	X_PCIE_REF_PAD_CLK_N	PCIe_O	-	100 MHz Reference Clock Negative Lane
12	NC	-	-	accessible at TP12

Interface Pin #	Signal name	Signal Type	Signal Level	Description
13	X_PCIE_REF_PAD_CLK_P	PCIe_O	-	100 MHz Reference Clock Positive Lane
14	NC	-	-	accessible at TP13
15	GND	-	-	Ground
16	NC	-	-	accessible at TP14
17	NC	-	-	accessible at TP18
18	GND	-	-	Ground
19	NC	-	-	accessible at TP19
20	X_GPIO1_IO14/PCIe_nW_DISABLE	O	3.3 V	nW_DISABLE
21	GND	-	-	Ground
22	X_GPIO1_IO08/PCIe_nPERST	O	3.3 V	nPERST
23	X_PCIE_RXN_N	PCIe_I	-	SOM receives Negative Lane
24	VCC_3V3_SW	PWR_O	3.3 V	3.3 V Supply

Interface Pin #	Signal name	Signal Type	Signal Level	Description
25	X_PCIE_RXN_P	PCIe_I	-	SOM Receive Positive Lane
26	GND	-	-	Ground
27	GND	-	-	Ground
28	VCC_1V5_MPCI	PWR_O	1.5 V	1.5 V Supply
29	GND	-	-	Ground
30	X_I2C2_SCL	OD-BI-PU	3.3 V	I^2C Clock
31	X_PCIE_TXN_N	PCIe_O	-	SOM Transmit Negative Lane
32	X_I2C2_SDA	OD-BI-PU	3.3 V	I^2C Data
33	X_PCIE_TXN_P	PCIe_O	-	SOM Transmit Positive Lane
34	GND	-	-	Ground
35	GND	-	-	Ground
36	USB_HUB_DN4_D-	USB_I/O	-	USB 2.0 Negative Lane

Interface Pin #	Signal name	Signal Type	Signal Level	Description
37	GND	-	-	Ground
38	USB_HUB_DN4_D+	USB_I/O	-	USB 2.0 Positive Lane
39	VCC_3V3_SW	PWR_O	3.3 V	3.3 V Supply
40	GND	-	-	Ground
41	VCC_3V3_SW	PWR_O	3.3 V	3.3 V Supply
42	nLED_WWAN	I	-	accessible at TP15
43	GND	-	-	Ground
44	nLED_WLAN	I	-	accessible at TP16
45	NC	-	-	-
46	nLED_WPAN	I	-	accessible at TP17
47	NC	-	-	-
48	VCC_1V5_MPCI	PWR_O	1.5 V	1.5 V Supply

Interface Pin #	Signal name	Signal Type	Signal Level	Description
49	NC	-	-	-
50	GND	-	-	Ground
51	NC	-	-	-
52	VCC_3V3_SW	PWR_O	3.3 V	3.3 V Supply
S1	GND	-	-	Ground
S2	GND	-	-	Ground

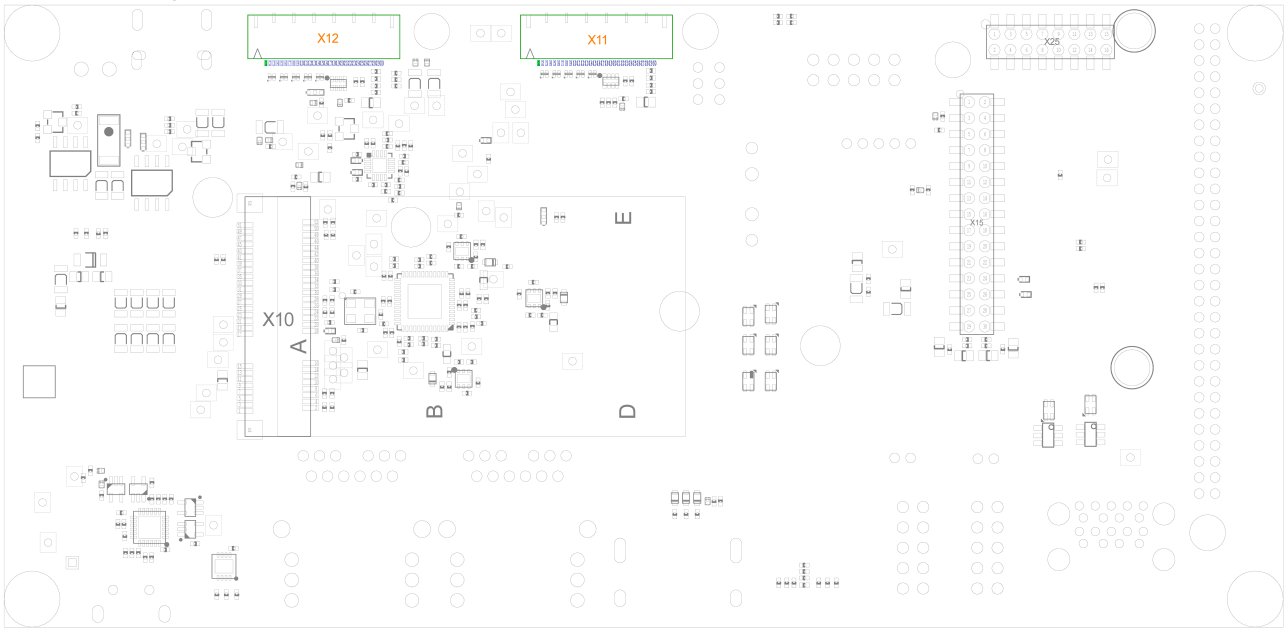
21.3.10.1 PCIe Design Considerations

100nF AC-Coupling capacitors are placed at the output of the phyCORE-i.MX 8M Plus in series to the TX- and CLK-Lanes. No further TX coupling capacitors are needed. The differential impedance should be 85 Ohm for all lanes.

21.3.11 Camera Connectivity

21.3.11.1 phyCAM-M MIPI CSI Camera Connectors

FIGURE 26: phyCAM-M MIPI CSI-2 Camera Connectors (X11 and X12)



The phyCORE-i.MX 8M Plus on the phyBOARD-Pollux offers 2 independent interfaces to connect digital camera boards with the MIPI CSI-2 interface. The 4-lane MIPI CSI-2 interfaces are brought out as phyCAM-M camera interfaces at connectors X10 and X11. The pin assignments of connectors X11 and X12 are shown below.

The phyCAM-M camera connectors fit the phyCAM-M product family with different colors and monochrome sensors. Suitable camera modules are e.g. VM-016-COL-M (1 MPix) or VM-017-BW-M (5 Mpix), which can be delivered with a complete objective. Contact the PHYTEC Sales Team for advice on how to tailor a camera module to your application.

The suitable cable can be found in the table below.

TABLE 49: phyCAM-M MIPI Cable Options

PHYTEC Art-No.	Description
WF271	phyCAM-M cable 150 mm

TABLE 50: CSI-1 (X11) Pin Assignment

Interface Pin #	Signal name	Signal Type	Signal Level	Description
1	GND	-	-	Ground
2	X_MIPI_CSI1_D0_P	MIPI CSI-2	-	MIPI-CSI-2 Data 0 Positive Lane
3	X_MIPI_CSI1_D0_N	MIPI CSI-2	-	MIPI-CSI-2 Data 0 Negative Lane
4	GND	-	-	Ground
5	X_MIPI_CSI1_D1_P	MIPI CSI-2	-	MIPI-CSI-2 Data 1 Positive Lane
6	X_MIPI_CSI1_D1_N	MIPI CSI-2	-	MIPI-CSI-2 Data 1 Negative Lane
7	GND	-	-	Ground
8	X_MIPI_CSI1_CLK_P	MIPI CSI-2	-	MIPI-CSI-2 Clock Positive Lane
9	X_MIPI_CSI1_CLK_N	MIPI CSI-2	-	MIPI-CSI-2 Clock Negative Lane
10	GND	-	-	Ground
11	X_MIPI_CSI1_D2_P	MIPI CSI-2	-	MIPI-CSI-2 Data 2 Positive Lane
12	X_MIPI_CSI1_D2_N	MIPI CSI-2	-	MIPI-CSI-2 Data 2 Negative Lane

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Interface Pin #	Signal name	Signal Type	Signal Level	Description
13	GND	-	-	Ground
14	X_MIPI_CSI1_D3_P	MIPI CSI-2	-	MIPI-CSI-2 Data 3 Positive Lane
15	X_MIPI_CSI1_D3_N	MIPI CSI-2	-	MIPI-CSI-2 Data 3 Negative Lane
16	GND	-	-	Ground
17	X_GPIO1_IO05/CSI1_CTRL4	OD-BI-PU	3.3 V	CSI2_CTRL4
18	X_GPIO1_IO03/CSI1_CTRL3	OD-BI-PU	3.3 V	CSI2_CTRL3
19	X_GPIO1_IO01/CSI1_CTRL2	OD-BI-PU	3.3 V	CSI2_CTRL2
20	X_GPIO1_IO00/CSI1_CTRL1	OD-BI-PU	3.3 V	CSI2_CTRL1
21	GND	-	-	Ground
22	X_I2C3_SCL	OD-BI-PU	3.3 V	I^2C Clock
23	X_I2C3_SDA	OD-BI-PU	3.3 V	DI^2C data
24	CSI1_ADDR	O	3.3 V	Choose the I2C address of the Camera

Interface Pin #	Signal name	Signal Type	Signal Level	Description
25	CSI1_nRESET	O	3.3 V	Hard reset for camera
26	CSI1_VCC_SELECT	OD-I-PU	3.3 V	Interface voltage selection open = 3.3 V GND = 5 V
27	GND	-	-	Ground
28	VCC_CSI1_OUT	PWR_O	3.3 V / 5 V	Supply of Cameras
29	VCC_CSI1_OUT	PWR_O	3.3 V / 5 V	Supply of Cameras
30	VCC_CSI1_OUT	PWR_O	3.3 V / 5 V	Supply of Cameras

TABLE 51: CSI-2 (X12) Pin Assignment

Interface Pin #	Signal name	Signal Type	Signal Level	Description
1	GND	-	-	Ground
2	X_MIPI_CSI2_D0_P	MIPI CSI-2	-	MIPI-CSI-2 Data 0 Positive Lane
3	X_MIPI_CSI2_D0_N	MIPI CSI-2	-	MIPI-CSI-2 Data 0 Negative Lane
4	GND	-	-	Ground
5	X_MIPI_CSI2_D1_P	MIPI CSI-2	-	MIPI-CSI-2 Data 1 Positive Lane
6	X_MIPI_CSI2_D1_N	MIPI CSI-2	-	MIPI-CSI-2 Data 1 Negative Lane
7	GND	-	-	Ground
8	X_MIPI_CSI2_CLK_P	MIPI CSI-2	-	MIPI-CSI-2 Clock Positive Lane
9	X_MIPI_CSI2_CLK_N	MIPI CSI-2	-	MIPI-CSI-2 Clock Negative Lane
10	GND	-	-	Ground
11	X_MIPI_CSI2_D2_P	MIPI CSI-2	-	MIPI-CSI-2 Data 2 Positive Lane
12	X_MIPI_CSI2_D2_N	MIPI CSI-2	-	MIPI-CSI-2 Data 2 Negative Lane

Interface Pin #	Signal name	Signal Type	Signal Level	Description
13	GND	-	-	Ground
14	X_MIPI_CSI2_D3_P	MIPI CSI-2	-	MIPI-CSI-2 Data 3 Positive Lane
15	X_MIPI_CSI2_D3_N	MIPI CSI-2	-	MIPI-CSI-2 Data 3 Negative Lane
16	GND	-	-	Ground
17	X_SAI1_RXD1/ GPIO4_IO03/ CSI2_CTRL3-4	OD-BI-PU	3.3 V	CSI2_CTRL4 GPIO4_IO03 shared with CSI2_CTRL3 via J18. Default not connected
18	X_SAI1_RXD1/ GPIO4_IO03/ CSI2_CTRL3-4	OD-BI-PU	3.3 V	CSI2_CTRL3 GPIO4_IO03 shared with CSI2_CTRL4 via J18. Default routes to CSI2_CTRL3
19	X_GPIO1_IO07/ CSI2_CTRL2	OD-BI-PU	3.3 V	CSI2_CTRL2
20	X_GPIO1_IO06/ CSI2_CTRL1	OD-BI-PU	3.3 V	CSI2_CTRL1
21	GND	-	-	Ground
22	X_I2C2_SCL	OD-BI-PU	3.3 V	I^2C Clock

Interface Pin #	Signal name	Signal Type	Signal Level	Description
23	X_I2C2_SDA	OD-BI-PU	3.3 V	I^2C Data
24	CSI2_ADDR	O	3.3 V	Choose the I2C address of the Camera
25	CSI2_nRESET	O	3.3 V	Hard reset for camera
26	CSI2_VCC_SELECT	OD-I-PU	3.3 V	Interface voltage selection open = 3.3 V GND = 5 V
27	GND	-	-	Ground
28	VCC_CSI2_OUT	PWR_O	3.3 V / 5 V	Supply of Cameras
29	VCC_CSI2_OUT	PWR_O	3.3 V / 5 V	Supply of Cameras
30	VCC_CSI2_OUT	PWR_O	3.3 V / 5 V	Supply of Cameras

21.3.11.2 Camera Design Considerations

Regarding camera connections when designing a customer carrier board:

1. The differential impedance should be 100 Ohms for all lanes to a Ground-Plane. Lanes should be matched.
2. phyCAM-M interfaces offer 3.3 V or 5 V supply voltages (selected by interface pin 26). Both voltages should be provided by the board to guarantee full compatibility with the phyCAM-M interface.
3. Each phyCAM interface needs a different I^2C address if connected to the same I^2C Bus. Place a Pull-up resistor at pin 24 to select the secondary address.

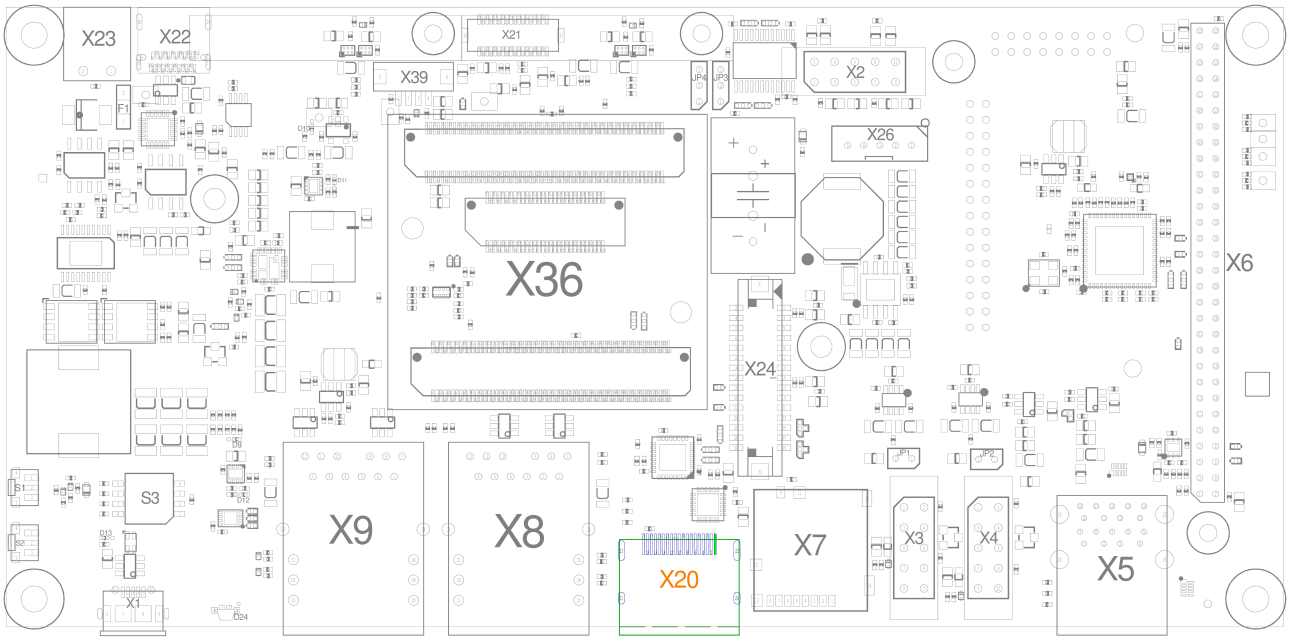
General information and design guidelines for PHYTEC camera interfaces can be found here:

- German: L-867Bd.A9 phyCAM Basis-Spezifikation und Design-In Guide
- English: L-867Be.A9 phyCAM Basis Specification and Design-In Guide

Specific information for each PHYTEC camera module can be found on that module's download page: PHYTEC Embedded Vision (DE) or PHYTEC Embedded Vision (EN)

21.3.12 HDMI (X20)

FIGURE 27: HDMI Connector (X20)



The phyBOARD-Pollux provides a High-Definition Multimedia Interface (HDMI), which is compliant with HDMI 2.0a. It supports a maximum resolution of 1920x1080p60, 1280x720p60, 720x480p60, and 640x480p60. Please refer to the i.MX 8M Plus Applications Processor Reference Manual for more information.

The HDMI interface is brought out at a standard HDMI type A connector (X20) on the phyBOARD-Pollux and comprises the following signal groups:

- Three pairs of data signals
- One pair of clock signals
- The Display Data Channel (DDC)
- The Consumer Electronics Control (CEC)
- The Hot Plug Detect (HPD) signal
- Audio Return Channel (ARC)

All signals are routed from the phyCORE-Connector to the HDMI receptacle through ESD Protection Diodes.

TABLE 52: X32 Pin Assignment

Interface Pin #	Signal name	Signal Type	Signal Level	Description
1	X_HDMI_TX2_P	HDMI_O	-	HDMI Data 2 Positive Lane
2	GND	-	-	Ground
3	X_HDMI_TX2_N	HDMI_O	-	HDMI Data 2 Negative Lane
4	X_HDMI_TX1_P	HDMI_O	-	HDMI Data 1 Positive Lane
5	GND	-	-	Ground
6	X_HDMI_TX1_N	HDMI_O	-	HDMI Data 1 Negative Lane
7	X_HDMI_TX0_P	HDMI_O	-	HDMI Data 0 Positive Lane
8	GND	-	-	Ground
9	X_HDMI_TX0_N	HDMI_O	-	HDMI Data 0 Negative Lane
10	X_HDMI_TXC_P	HDMI_O	-	HDMI Clock Positive Lane
11	GND	-	-	Ground
12	X_HDMI_TXC_N	HDMI_O	-	HDMI Clock Negative Lane

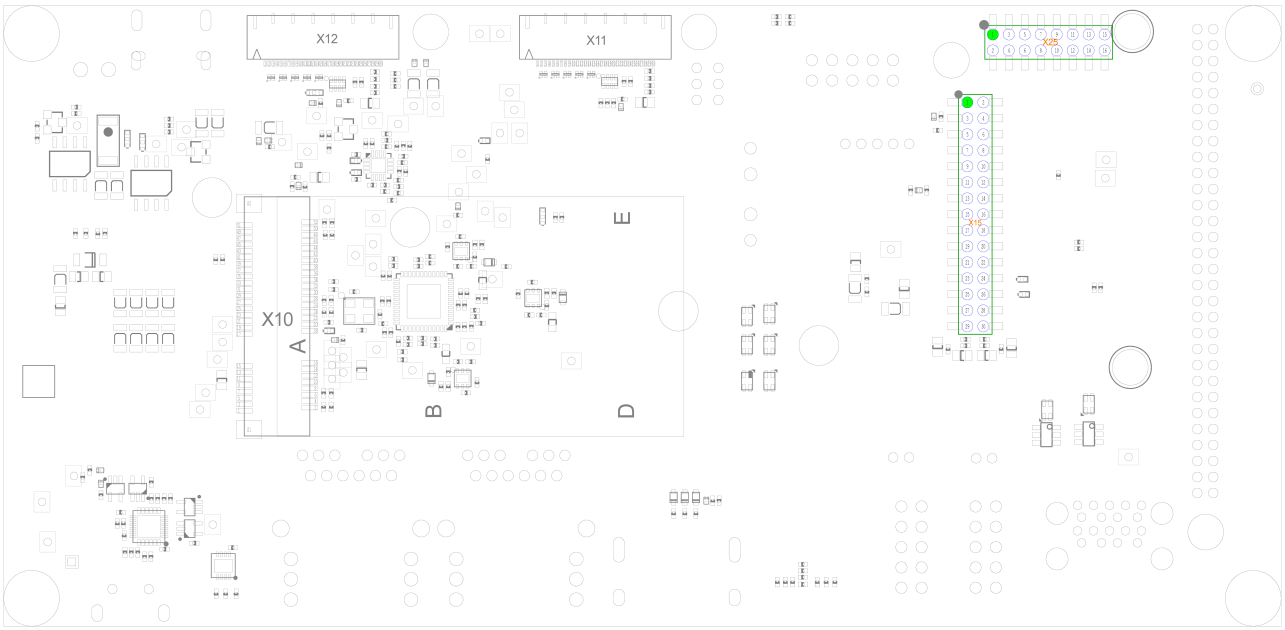
Interface Pin #	Signal name	Signal Type	Signal Level	Description
13	X_HDMI_CEC	OD-BI-PU	VDD_CEC	Consumer Electronics Control
14	X_EARC_P_UTIL	-	-	Audio Return Channel Positive Lane / Utility Pin
15	X_HDMI_DDC_SCL	OD-BI-PU	5 V	I^2C Clock
16	X_HDMI_DDC_SDA	OD-BI-PU	5 V	I^2C Data
17	GND	-	-	Ground
18	VCC_5V_HDMI_OUT	PWR_O	5 V	5 V Supply for HDMI Device
19	X_EARC_N_HPD	-	5 V	Audio Return Channel Negative Lane / Hot Plug detect
20	SHIELD_1	-	-	Shield connected to Ground over 100 nF and 150 pF parallel to 1 MOhm
21	SHIELD_2	-	-	
22	SHIELD_3	-	-	
23	SHIELD_4	-	-	

21.3.12.1 HDMI Design Considerations

The differential impedance should be 100 Ohms for all lanes to a Ground-Plane. Lanes should be matched. The DDC lanes need pull-up resistors between 1.5k and 2k to 5V through a diode. The CEC lane needs a 27k pull-up resistor connected to 3.3V through a diode. This prevents leaking current in a power-off state.

21.3.13 Audio/Video (SAI2/LVDS0)

FIGURE 28: Audio/Video Connectors (X15/X25)



The phyCORE-i.MX 8M Plus offers one LVDS display interface, which supports two output channels. The Audio/Video (A/V) connectors X15 and X25 provide an easy way to add typical A/V functions and features to the phyBOARD-Pollux. Standard interfaces such as 4-lane LVDS, I^2S, I^2C, and USB, as well as different supply voltages, are available at the two A/V female dual entry connectors. A special feature of these connectors is their connectivity from the top or bottom.

The A/V connector is intended to be used with phyBOARD Expansion Boards and to add specific audio/video connectivity with custom expansion boards. A/V connector X25 makes all signals for display connectivity available, while X15 provides signals for audio and touch screen connectivity as well as an I^2C bus and additional control signals. The tables below show the pin assignment of connectors X15 and X25.

TABLE 53: X25 Pin Assignment

Interface Pin #	Signal name	Signal Type	Signal Level	Description
1	GND	-	-	Ground
2	X_LVDS0_D2_P	LVDS_O	-	LVDS Data 2 Positive Lane
3	X_LVDS0_CLK_P	LVDS_O	-	LVDS Clock Positive Lane
4	X_LVDS0_D2_N	LVDS_O	-	LVDS Data 2 Negative Lane
5	X_LVDS0_CLK_N	LVDS_O	-	LVDS Clock Negative Lane
6	GND	-	-	Ground
7	GND	-	-	Ground
8	X_LVDS0_D3_P	LVDS_O	-	LVDS Data 3 Positive Lane
9	X_LVDS0_D1_P	LVDS_O	-	LVDS Data 1 Positive Lane
10	X_LVDS0_D3_N	LVDS_O	-	LVDS Data 3 Negative Lane
11	X_LVDS0_D1_N	LVDS_O	-	LVDS Data 1 Negative Lane
12	GND	-	-	Ground

Interface Pin #	Signal name	Signal Type	Signal Level	Description
13	GND	-	-	Ground
14	X_LVDS0_D0_P	LVDS_O	-	MIPI DSI Data 0 Positive Lane
15	VCC_IN_AV	PWR_O	12 V to 24 V	Input Supply Voltage of phyBOARD Pollux
16	X_LVDS0_D0_N	LVDS_O	-	MIPI DSI Data 0 Negative Lane

TABLE 54: X15 Pin Assignment

Interface Pin #	Signal name	Signal Type	Signal Level	Description
1	USB_HUB_DN3_D+_AV_CON	USB_I/O	-	USB 2.0 Data positive
2	USB_HUB_DN3_D-_AV_CON	USB_I/O	-	USB 2.0 Data negative
3	X_nRESET	OD-BI-PU	3.3 V	Global Board Reset
4	GND	-	-	Ground
5	X_SAI1_RXD0/GPIO4_IO02	I/O	3.3 V	SAI RXD/GPIO
6	X_SAI3_TXFS/GPIO4_IO31	I/O	3.3 V	SAI TXFS/GPIO
7	X_SAI3_TXC/GPIO5_IO00	I/O	3.3 V	SAI TXC/GPIO
8	X_SAI3_TXD/GPIO5_IO01	I/O	3.3 V	SAI TXD/Backlight EN
9	X_SAI3_MCLK/PWM4_OUT	I/O	3.3 V	SAI MCLK/Backlight PWM
10	X_SAI3_RXFS/GPIO4_IO28	I/O	3.3 V	SAI RXFS/GPIO
11	GND	-	-	Ground
12	X_SAI5_RXFS/GPIO3_IO19	I/O	3.3 V	SAI RXC/GPIO

Interface Pin #	Signal name	Signal Type	Signal Level	Description
13	X_SAI2_TXD0	I/O	3.3 V	
14	GND	-	-	Ground
15	X_SAI2_TXFS	I/O	3.3 V	SAI TXFS
16	X_SAI2_TXC	I/O	3.3 V	SAI TXC
17	X_SAI2_RXC	I/O	3.3 V	SAI TXC
18	X_SAI2_RXFS	I/O	3.3 V	SAI RXFS
19	X_SAI2_MCLK	I/O	3.3 V	SAI MCLK
20	X_SAI2_RXD0	I/O	3.3 V	SAI RXD0
21	GND	-	-	Ground
22	X_I2C4_SDA	OD-BI-PU	3.3 V	I^2C Data
23	X_UART3_RXD	I/O	3.3 V	UART RXD/GPIO Depending on J27. Default not connected.
24	X_I2C4_SCL	OD-BI-PU	3.3 V	I^2C Clock

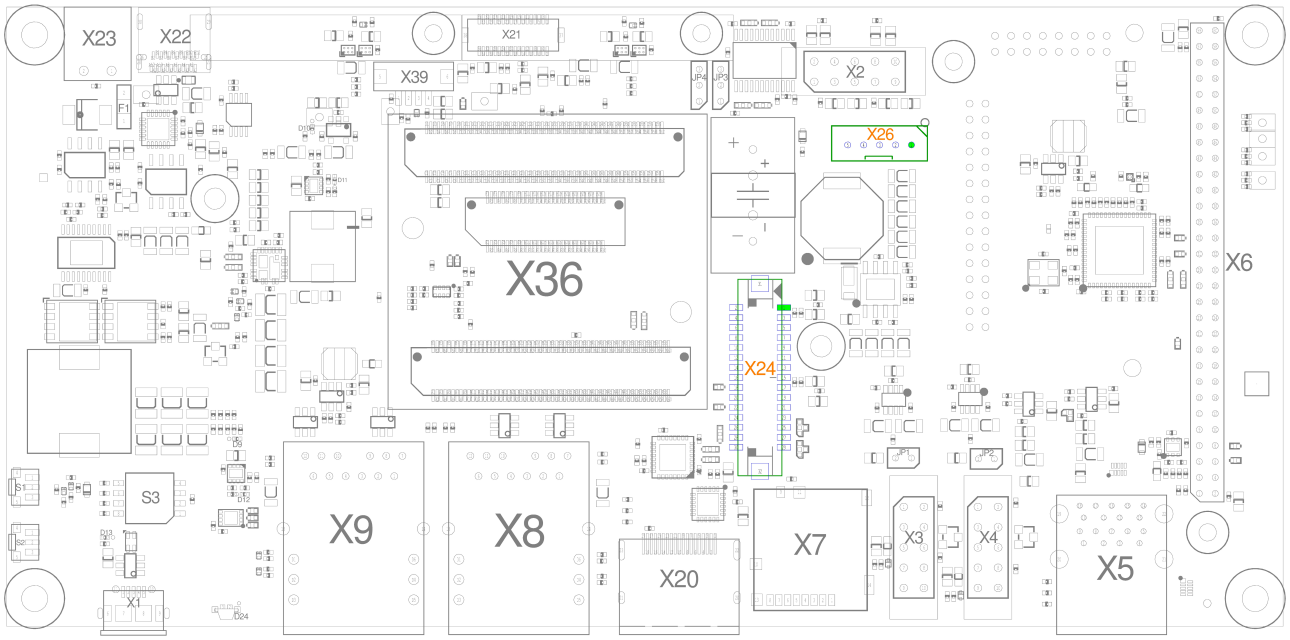
Interface Pin #	Signal name	Signal Type	Signal Level	Description
25	X_UART3_TXD	I/O	3.3 V	UART TXD/GPIO Depending on J26. Default not connected.
26	GND	-	-	Ground
27	VCC_5V	PWR_O	5 V	5 V Supply
28	VCC_3V3	PWR_O	3.3 V	3.3 V Supply
29	VCC_5V	PWR_O	5 V	5 V Supply
30	VCC_3V3	PWR_O	3.3 V	3.3 V Supply

21.3.13.1 Audio/Video Design Considerations

The differential impedance of LVDS0 lanes should be 100 Ohm and 50 Ohm to a Ground-Plane for all lanes. Lanes should be matched. The audio signals should have a single-ended impedance of 50 Ohms to a ground plane.

21.3.14 LVDS1 (X24/X26)

FIGURE 29: LVDS1 Connectors (X24/X26)



The phyCORE-i.MX 8M Plus offers one LVDS display interface, which supports two output channels. The video connectors X24 and X26 provide an easy way to connect a display to the phyBOARD-Pollux. The pinout of both connectors fits to the Glyn LVDS Display Family with different display sizes and display resolutions. In addition to the Glyn LVDS signals, there are USB and I^2C for touch brought out at X24, too.

The connectors are intended to be used with PHYTEC KLCD-AC163. The tables below show the pin assignment of connectors X24 and X26.

TABLE 55: X26 Pin Assignment

Interface Pin #	Signal name	Signal Type	Signal Level	Description
1	N.C.	-	-	not connected
2	N.C.	-	-	not connected
3	VCC_3V3_LVDS1	PWR_O	3.3 V	3.3 V supply
4	GND	-	-	Ground
5	X_LVDS1_CLK_N	LVDS_O	-	LVDS Clock Negative Lane
6	X_LVDS1_CLK_P	LVDS_O	-	LVDS Clock Positive Lane
7	VCC_3V3_LVDS1	PWR_O	3.3 V	3.3 V supply
8	GND	-	-	Ground
9	X_LVDS1_D0_N	LVDS_O	-	LVDS Data 0 Negative Lane
10	X_LVDS1_D0_P	LVDS_O	-	LVDS Data 0 Positive Lane
11	X_LVDS1_D1_N	LVDS_O	-	LVDS Data 1 Negative Lane
12	X_LVDS1_D1_P	LVDS_O	-	LVDS Data 1 Positive Lane

Interface Pin #	Signal name	Signal Type	Signal Level	Description
13	X_LVDS1_D2_N	LVDS_O	-	LVDS Data 2 Negative Lane
14	X_LVDS1_D2_P	LVDS_O	-	LVDS Data 2 Positive Lane
15	X_LVDS1_D3_N	LVDS_O	-	LVDS Data 3 Negative Lane
16	X_LVDS1_D3_P	LVDS_O	-	LVDS Data 3 Positive Lane
17	VCC_5V_LVDS1	PWR_O	5 V	5 V supply
18	N.C.	-	-	Default: not connected Can be tied to GND if J28 is mounted.
19	USB_HUB_DN3_D-_LVDS1	USB_I/O	-	Default: not connected USB 2.0 Data negative shared X15 depending on jumper setting J17.
20	USB_HUB_DN3_D+_LVDS1	USB_I/O	-	Default: not connected USB 2.0 Data positive shared X15 depending on jumper setting J16.
21	N.C.	-	-	not connected

Interface Pin #	Signal name	Signal Type	Signal Level	Description
22	N.C.	-	-	Default: not connected Can be tied to GND if J29 is mounted.
23	N.C.	-	-	not connected
24	N.C.	-	-	not connected
25	N.C.	-	-	not connected
26	N.C.	-	-	not connected
27	X_I2C4_SCL	-	-	Default: not connected Can be connected to X_I2C4_SCL or tied to GND or VCC_3V3_LVDS1 if J38 is mounted.
28	GND	-	-	Default tied to GND. Can be tied to VCC_3V3_LVDS1 if J4 is set to 2+3.
29	X_I2C4_SDA	-	-	Default: not connected Can be connected to X_I2C4_SDA or tied to GND or VCC_3V3_LVDS1 if J39 is mounted.
30	N.C.	-	-	not connected

Interface Pin #	Signal name	Signal Type	Signal Level	Description
31	GND	-	-	Terminal Pin
32	GND	-	-	Terminal Pin

TABLE 56: X24 Pin Assignment

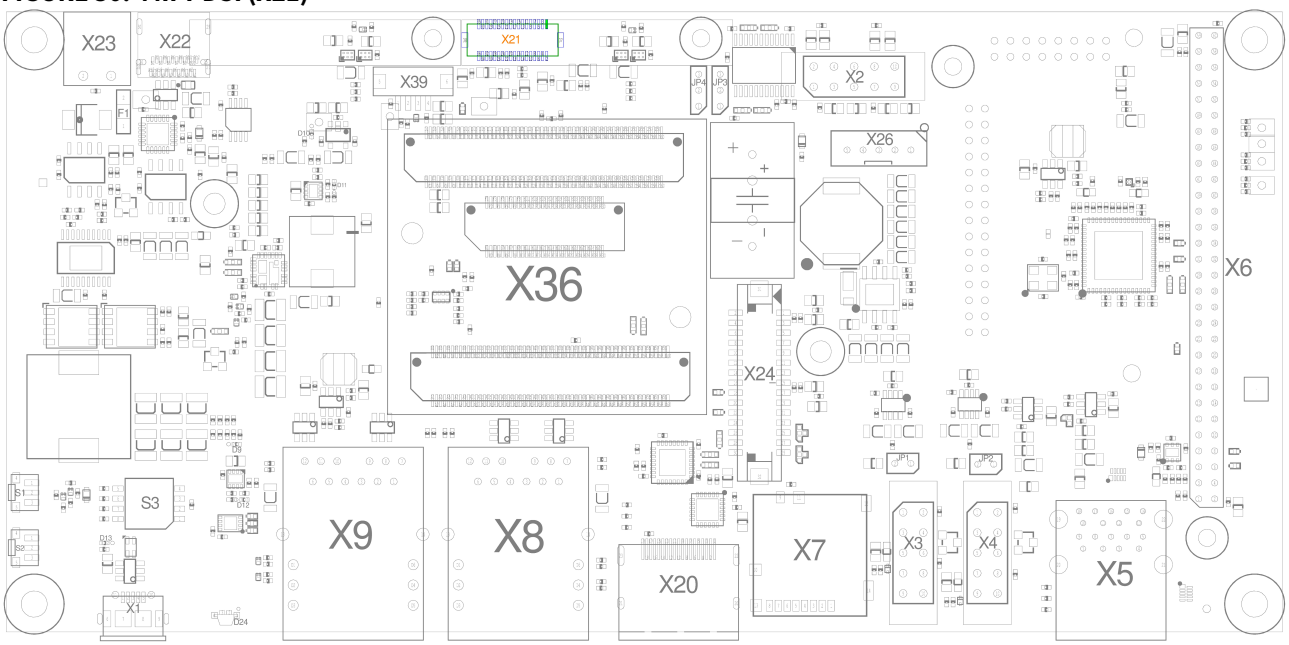
Interface Pin #	Signal name	Signal Type	Signal Level	Description
1	VCC_12V_LVDS1	PWR_O	12 V	12 V supply for display backlight. Default to a 12 V voltage regulator to provide current for the backlight. If VCC_IN is 12 V, VCC_IN can be connected directly to VCC_12V_LVDS1, and lower the BOM cost by removing the 12 V voltage regulator.
2	X_SPDIF_TX/PWM3_OUT	I/O	3.3 V	PWM output
3	GND	-	-	Ground
4	GND	-	-	Ground
5	X_SD2_WP/GPIO2_IO20/ LVDS1_BL_EN	I/O	3.3 V	Backlight enable

21.3.14.1 LVDS Design Considerations

The differential impedance of LVDS0 lanes should be 100 Ohm and 50 Ohm to a Ground-Plane for all lanes. Lanes should be matched.

21.3.15 MIPI-DSI (X21)

FIGURE 30: MIPI-DSI (X21)



The phyCORE-i.MX 8M Plus offers one MIPI-DSI display interface. MIPI-DSI has 4 channels, supporting one display with a resolution of up to 1920 x 1080 at 60Hz.

The following table shows the pin assignment of connector X21 (Hirose DF12(4.0)-36DP-0.5V(86)).

TABLE 57: X21 Pin Assignment

Interface Pin #	Signal name	Signal Type	Signal Level	Description
1	GND	-	-	Ground
2	GND	-	-	Ground
3	X_MIPI_DSI1_D0_P	DSI_O	-	MIPI DSI Data 0 Positive Lane
4	VCC_IN_MIPI_DSI	PWR_O	12 V to 24 V	internally connected to VCC_IN
5	X_MIPI_DSI1_D0_N	DSI_O	-	MIPI DSI Data 0 Negative Lane
6	VCC_IN_MIPI_DSI	PWR_O	12 V to 24 V	internally connected to VCC_IN
7	GND	-	-	Ground
8	GND	-	-	Ground
9	X_MIPI_DSI1_D1_P	DSI_O	-	MIPI DSI Data 1 Positive Lane
10	VCC_IN_MIPI_DSI	PWR_O	12 V to 24 V	internally connected to VCC_IN
11	X_MIPI_DSI1_D1_N	DSI_O	-	MIPI DSI Data 1 Negative Lane
12	VCC_IN_MIPI_DSI	PWR_O	12 V to 24 V	internally connected to VCC_IN

Interface Pin #	Signal name	Signal Type	Signal Level	Description
13	GND	-	-	Ground
14	GND	-	-	Ground
15	X_MIPI_DSI1_CLK_P	DSI_O	-	MIPI DSI Clock Positive Lane
16	VCC_5V_MIPI_DSI	PWR_O	5 V	5 V supply
17	X_MIPI_DSI1_CLK_N	DSI_O	-	MIPI DSI Clock Negative Lane
18	VCC_5V_MIPI_DSI	PWR_O	5 V	5 V supply
19	GND	-	-	Ground
20	GND	-	-	Ground
21	X_MIPI_DSI1_D2_P	DSI_O	-	MIPI DSI Data 2 Positive Lane
22	VCC_3V3_MIPI_DSI	PWR_O	3.3 V	3.3 V supply
23	X_MIPI_DSI1_D2_N	DSI_O	-	MIPI DSI Data 2 Negative Lane
24	VCC_3V3_MIPI_DSI	PWR_O	3.3 V	3.3 V supply

Interface Pin #	Signal name	Signal Type	Signal Level	Description
25	GND	-	-	Ground
26	GND	-	-	Ground
27	X_MIPI_DSI1_D3_P	DSI_O	-	MIPI DSI Data 3 Positive Lane
28	X_I2C4_SCL	OD-BI-PU	3.3 V	I^2C Clock
29	X_MIPI_DSI1_D3_N	DSI_O	-	MIPI DSI Data 3 Negative Lane
30	X_I2C4_SDA	OD-BI-PU	3.3 V	I^2C Data
31	GND	-	-	Ground
32	GND	-	-	Ground
33	MIPI_DSI1_GPIO0	I/O	3.3 V	Connected to TP53
34	X_SPDIF_RX/ PWM2_OUT/MIPI-DSI	I/O	3.3 V	PWM output
35	MIPI_DSI1_GPIO1	I/O	3.3 V	Connected to TP54
36	X_nRESET	OD-BI-PU	3.3 V	Global Board Reset

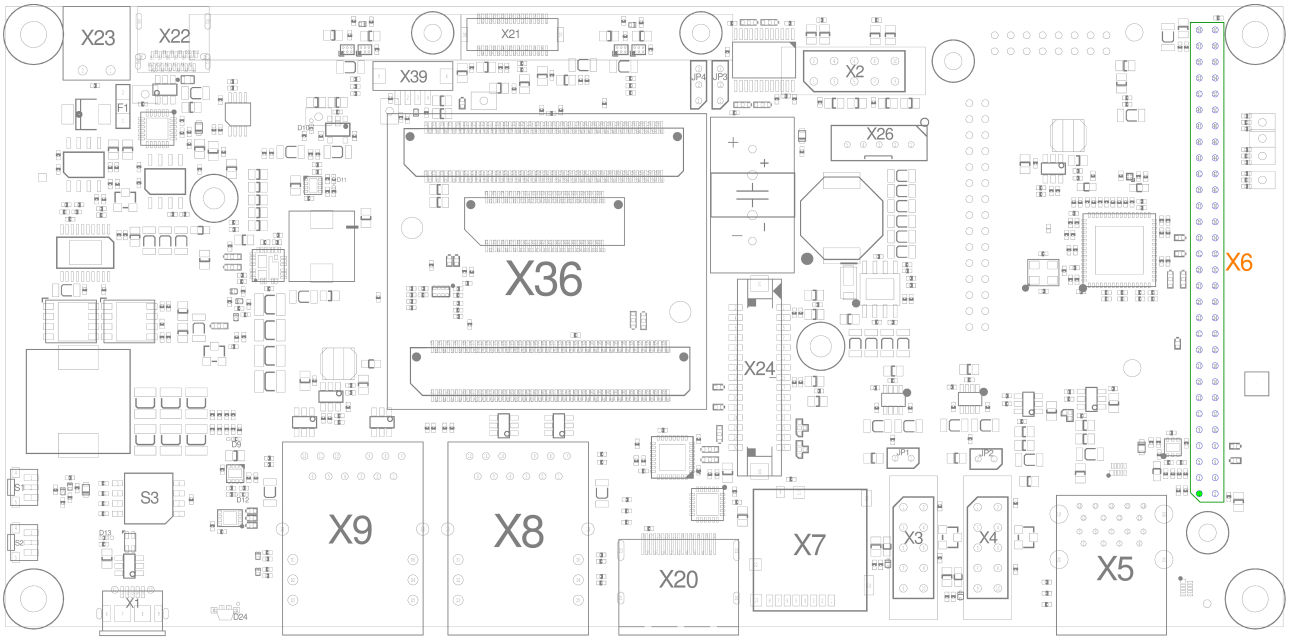
Interface Pin #	Signal name	Signal Type	Signal Level	Description
37	GND	-	-	Terminal Pin
38	GND	-	-	Terminal Pin

21.3.15.1 MIPI-DSI Design Considerations

The differential impedance of MIPI-DSI1 lanes should be 100 Ohm and 50 Ohm to a Ground-Plane for all lanes. Lanes should be matched.

21.3.16 Expansion Connector (X6)

FIGURE 31: Expansion Connector (X6)



The expansion connector X6 provides an easy way to add other functions and features to the phyBOARD-Pollux. Standard interfaces such as SPI, USB, JTAG, UART, SDIO, and I2C are available at the expansion connector. The expansion connector is intended to be used with a phyBOARD Evaluation Adapter. The expansion connector can also add specific functions with custom expansion boards. Information on the Evaluation Adapter for the expansion connector can be found in the Application Guide for phyBOARD Expansion Boards (L-793e).

The pinout of the expansion connector is shown in the table below:

TABLE 58: X6 Expansion Pinout

Interface Pin #	Signal name	Signal Type	Signal Level	Description
1	VCC_3V3_SW	PWR_O	3.3 V	3.3 V supply
2	VCC_5V_SW	PWR_O	5 V	5 V supply
3	VCC_1V8_EXP_CON	PWR_O	1.8 V	1.8 V supply
4	GND	-	-	Ground
5	X_UART3_TXD	I/O	3.3 V	Default connected to X_UART3_TXD via J47
6	X_SD1_STROBE/ UART3_CTS_B	I/O	3.3 V	MOSI
7	X_SD1_RESET_B/ UART3_RTS_B	I/O	3.3 V	MISO
8	X_UART3_RXD	I/O	3.3 V	Default connected to X_UART3_RXD via J46
9	GND	-	-	Ground
10	X_CLKOUT1	O	3.3 V	Monitor output clock
11	X_I2C2_SDA	OD-BI-PU	3.3 V	I^2C Data

Interface Pin #	Signal name	Signal Type	Signal Level	Description
12	X_CLKOUT2	O	3.3 V	Monitor output clock
13	X_I2C2_SCL	OD-BI-PU	3.3 V	I^2C Clock
14	GND	-	-	Ground
15	X_JTAG_TMS	I	3.3 V	JTAG TMS
16	JTAG_TRST	I	3.3 V	JTAG TRST Default connected to Global Board Reset X_nRESET via J35
17	X_JTAG_TDI	I	3.3 V	JTAG TDI
18	X_JTAG_TDO	O	3.3 V	JTAG TDO
19	GND	-	-	Ground
20	X_JTAG_TCK	I	3.3 V	JTAG TCK
21	USB_HUB_DN2_D+	USB_I/O	-	USB 2.0 Data positive
22	USB_HUB_DN2_D-	USB_I/O	-	USB 2.0 Data Negative
23	X_nRESET	OD-BI-PU	3.3 V	Global Board Reset

Interface Pin #	Signal name	Signal Type	Signal Level	Description
24	GND	-	-	Ground
25	X_SD1_CMD/ GPIO2_IO01	I/O	3.3 V	Refer to the i.MX 8M Plus Datasheet for all muxing options
26	X_SD1_DATA0/ GPIO2_IO02/EXP_CON	I/O	3.3 V	Refer to the i.MX 8M Plus Datasheet for all muxing options
27	X_SD1_CLK/GPIO2_IO00	I/O	3.3 V	Refer to the i.MX 8M Plus Datasheet for all muxing options
28	X_SD1_DATA1/ GPIO2_IO03/EXP_CON	I/O	3.3 V	Refer to the i.MX 8M Plus Datasheet for all muxing options
29	GND	-	-	Ground
30	X_SD1_DATA2/ GPIO2_IO04	I/O	3.3 V	Refer to the i.MX 8M Plus Datasheet for all muxing options
31	X_UART3_RXD	I/O	3.3 V	Default connected to X_UART3_RXD via J34
32	X_SD1_DATA3/ GPIO2_IO05	I/O	3.3 V	Refer to the i.MX 8M Plus Datasheet for all muxing options
33	X_UART3_TXD	I/O	3.3 V	Default connected to X_UART3_TXD via J33

Interface Pin #	Signal name	Signal Type	Signal Level	Description
34	GND	-	-	Ground
35	X_SD1_DATA4/ GPIO2_IO06	I/O	3.3 V	Refer to the i.MX 8M Plus Datasheet for all muxing options
36	X_SD1_DATA5/ GPIO2_IO07	I/O	3.3 V	Refer to the i.MX 8M Plus Datasheet for all muxing options
37	USB_HUB_nPWRCTL2	O	3.3 V	PWRCTL2/BATEN2 output of Ti TUSB8042A USB hub belonging to USB_HUB_DN2 and USB_HUB_nOVERCUR2
38	X_SD1_DATA6/ GPIO2_IO08	I/O	3.3 V	Refer to the i.MX 8M Plus Datasheet for all muxing options
39	USB_HUB_nOVERCUR2	OD-I-PU	3.3 V	nOVERCUR2 input of Ti TUSB8042A USB hub belonging to USB_HUB_DN2 and USB_HUB_nPWRCTL2
40	X_EARC_AUX	-	-	-
41	GND	-	-	Ground
42	X_SPDIF_EXT_CLK/ PWM1_OUT/GPIO5_IO05	I/O	3.3 V	Refer to the i.MX 8M Plus Datasheet for all muxing options
43	X_ECSPI2_SCLK	I/O	3.3 V	Refer to the i.MX 8M Plus Datasheet for all muxing options

Interface Pin #	Signal name	Signal Type	Signal Level	Description
44	X_SD1_DATA7/ GPIO2_IO09	I/O	3.3 V	Refer to the i.MX 8M Plus Datasheet for all muxing options
45	X_ECSPI2_MOSI	I/O	3.3 V	Refer to the i.MX 8M Plus Datasheet for all muxing options
46	GND	-	-	Ground
47	X_ECSPI2_MISO	I/O	3.3 V	Refer to the i.MX 8M Plus Datasheet for all muxing options
48	X_ONOFF	I	1.8 V	ONOFF input of phyCORE i.MX 8M Plus
49	X_ECSPI2_SS0	I/O	3.3 V	Refer to the i.MX 8M Plus Datasheet for all muxing options
50	X_PMIC_ON_REQ	O	1.8 V	The CPU uses PMIC_ON_REQ to start the PMIC power-on sequence by driving it high. During power down, the CPU keeps PMIC_ON_REQ low until X_ONOFF is triggered or the system is powered on again
51	GND	-	-	Ground
52	X_GPIO1_IO02/ PMIC_WDOG	I	3.3 V	PMIC_WDOG input of phyCORE i.MX 8M Plus PMIC can be used to power off phyCORE i.MX8 M Plus from any power state
53	X_ETH1_GPIO0	I/O	1.8 V	GPIO_0 pin of phyCORE i.MX 8M Plus Ethernet-PHY Ti DP83867

Interface Pin #	Signal name	Signal Type	Signal Level	Description
54	X_nTEMP_ALERT	I/OD	3.3 V	ALERT output of phyCORE i.MX 8M Plus temperature sensors, if ALERT is enabled
55	X_ETH1_GPIO1	I/O	1.8 V	GPIO_1 pin of phyCORE i.MX 8M Plus Ethernet-PHY Ti DP83867
56	GND	-	-	Ground
57	VCC_IN	PWR_O	12 V to 24 V	Input Supply Voltage of phyBOARD
58	ETH0_LED_1	O	1.8 V	LED_1 pin of phyBOARD-Pollux Ethernet-PHY Ti DP83867
59	GND	-	-	Ground
60	VCC_5V_MAIN	PWR_O	5 V	5 V Supply (always on)

21.3.17 Fan (X39)

If heatsinking is required for the phyCORE-i.MX 8M Plus, a PWM-controlled fan, can be connected to the phyBOARD-Pollux. The fan's supply voltage is 5 V, and the PWM signal is brought out as open-drain. The frequency generator signal, which can be used to monitor fan rotation, is connected to test pad TP55 and comes with a pull-up resistor to 3.3 V.

A Hirose DF13-4P-1.25V (75) socket is used as a connector with the following pinout:

TABLE 59: X39 Fan Pinout

Interface Pin #	Signal Name	Signal Type	Signal Level	Description
1	VCC_5V_SW	PWR_O	5 V	5 V Supply
2	GND	-	-	Ground
3	FAN_FG	OD-PU	3.3 V	Frequency Generator 'speedo'-signal of a PWM Fan. Connected to TP55
4	X_SPDIF_RX/PWM2_OUT/FAN_CON	OD-PU	5 V	Inverted PWM Output. An external pull-up resistor is mounted to tie to VCC_5V_SW

21.3.18 on-board Functionalities

21.3.18.1 Trusted Platform Module (TPM) (U24)

The phyBOARD-Pollux is equipped with a Trusted Platform Module (TPM) (Infineon TPM SLB 9670). The TPM is a chip developed, produced, tested, and certified according to the TCG specification that enhances the board with additional security functions. These security functions include the generation and secure storage (in the hardware) of keys for the authentication and identification of communication participants (SSH, server, cloud, etc.) and data, which can also be encrypted.

The TPM is connected to the phyCORE-i.MX 8M Plus through the ECSPI1 interface. GPIO1 and GPIO2 of the TPM can be configured by J43 and J44. Default GPIO1 is not connected, and GPIO2 is tied to Ground.

Note

PHYTEC has a specialized Embedded Security Team that supports customers who would like to plan and implement their individual security concepts. Contact PHYTEC for more information.

21.3.18.2 Multicolor (RGB) LED (D24)

The phyBOARD-Pollux provides one multicolor (RGB) LED (D24) (see phyBOARD-Pollux Components (Top)). The LEDs are connected to an LED driver (NXP PCA9533/01) controlled by the I2C2 bus.

21.3.18.3 EEPROM (U16)

The phyBOARD-Pollux provides a 2 kbit EEPROM (ST M24C02-RMC6TG) for general use. It is controlled by the I2C2 bus. The EEPROM's write protection pin is connected to TP41. Write protection can be enabled by mounting a R39 pull-up resistor. In this case, the EEPROM can be written if TP41 is tied to Ground only. The EEPROM I^2C address can be fully customized by jumpers J30, J31, and J32. The default address is 0x51.

21.3.18.4 Global Board Reset (X_nRESET)

The X_nRESET signal (X_POR_B at phyCORE-i.MX 8M Plus) is used to hold all devices with an external reset pin in the reset state. X_nRESET will be released after all board voltages are powered up, and allow the phyCORE-i.MX 8M Plus to boot. X_nRESET is brought out at several connectors, like the Expansion Connector (X6).

X_nRESET Design Considerations

Note that there is a 10 kOhms pull-up resistor on phyCORE-i.MX 8M Plus VDD_IO voltage. It is recommended to use this signal as an open drain.

21.3.18.5 on-board Power Supplies

The phyBOARD-Pollux provides supply voltages on several connectors to power external devices. Be sure not to exceed the maximum permissible current that can be drawn from each power domain.

TABLE 60: Onboard Power Supplies

Voltage Domain	Max. recommended additional current
VCC_12V_LVDS1	500 mA
VCC_5V_MAIN, VCC_5V_SW, VCC_5V_MIPI_DSI, VCC_5V_AV, VCC_5V_LVDS1, VCC_5V_CAN1, VCC_5V_CAN2	600 mA
VCC_3V3_SW, VCC_3V3_MIPI_DSI, VCC_3V3_LVDS1, VCC_3V3_AV	800 mA
VCC_1V8_EXP_CON	200 mA

In addition to these currents, phyBOARD-Pollux delivers current for USB_VBUS of X5 (2x 900 mA), phyCAM-M Interfaces (2x 1500 mA 3.3 V or 5 V depending on VCC_SELECT pin), and HDMI connector (150 mA).

Warning

Drawing current may result in heating of the voltage regulators' components and may require additional heat sinking.

21.3.18.6 on-board Measurement of SOM Power Consumption

FIGURE 32: TP34 (Top Side)

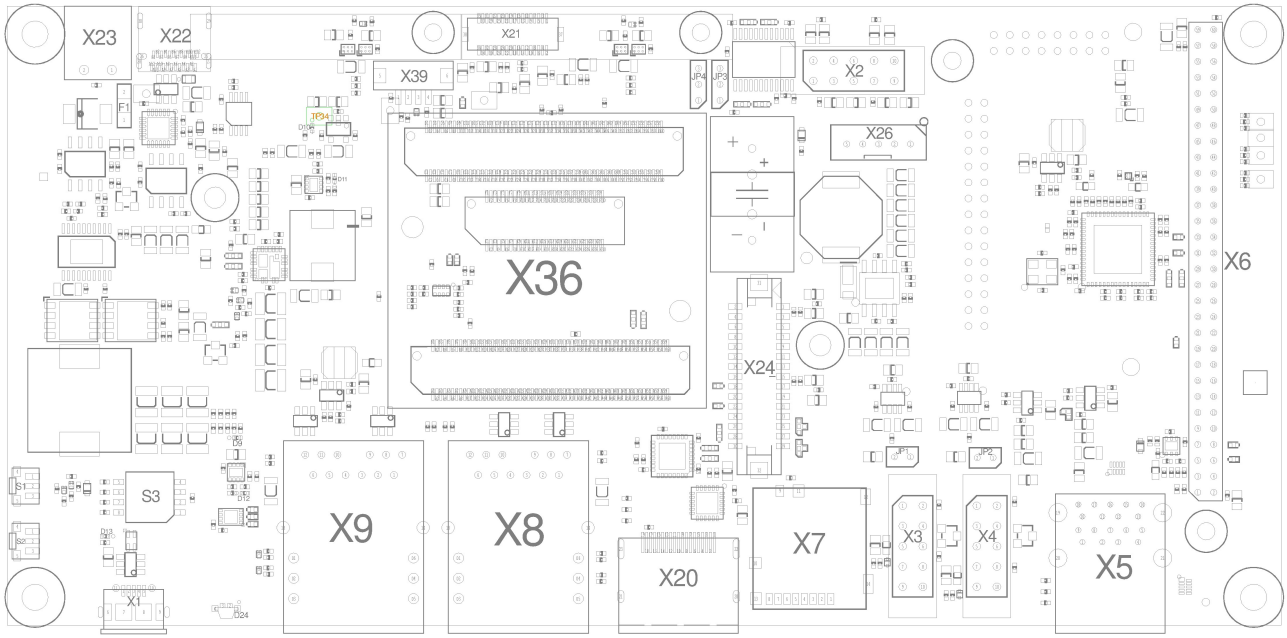
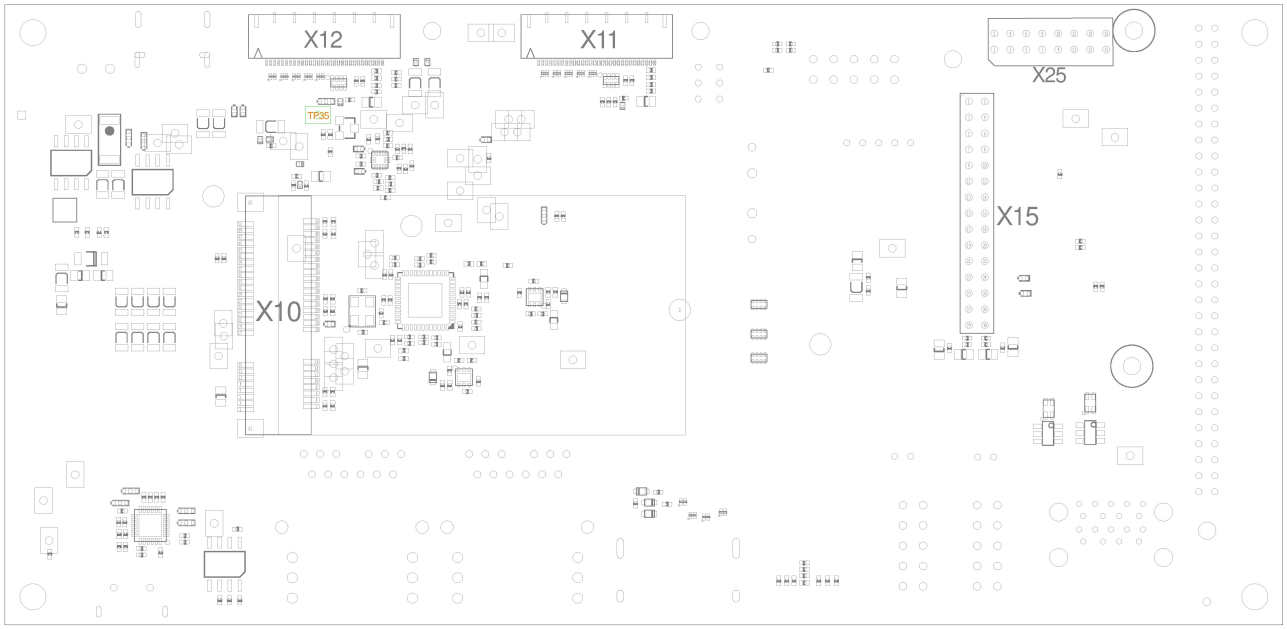


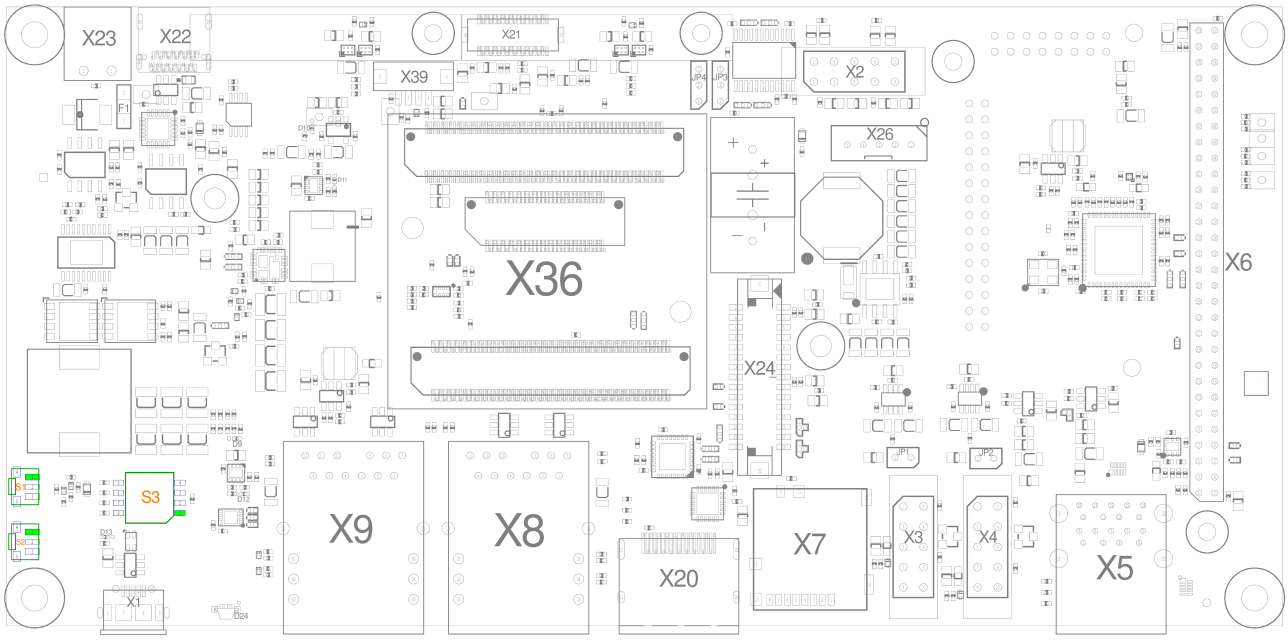
FIGURE 33: TP35 (Bottom Side)



The current consumption of the main supply voltage (VCC_3V3_SOM) for powering the phyCORE-module (VIN_3V3) can be measured on board to determine the power consumption of the SOM. A current sense amplifier translates the supply current into a proportional voltage, which can be measured at TP34 (on PCB top side) and TP35 (on PCB bottom side). The proportional factor is 5 mA/mV. For example, measuring 200 mV at TP34/TP35, the current consumption of the 3.3 V supply voltage is 200 mV * 5 mA/mV = 1000 mA (= 3.3 Watts).

21.3.19 Switches

FIGURE 34: phyBOARD-Pollux Switch Locations



21.3.19.1 System Reset Button (S1)

The phyBOARD-Pollux is equipped with a system reset button at S1. Pressing this button will tie the X_PMIC_RST_B pin (X36 Pin C11) of the phyCORE-i.MX 8M Plus low, causing the module to reset with a complete power cycle.

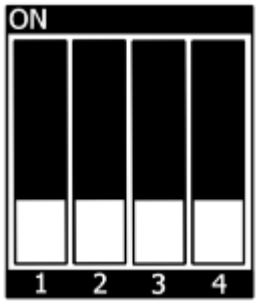
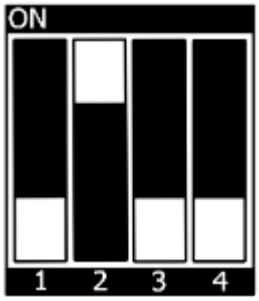
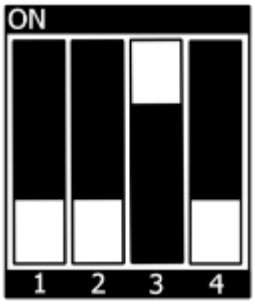
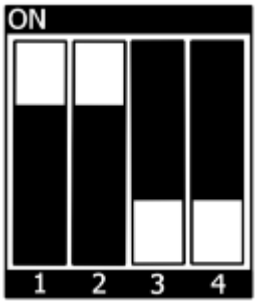
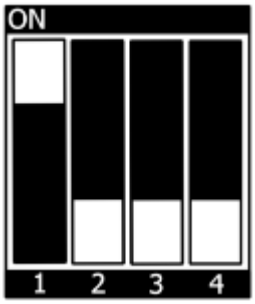
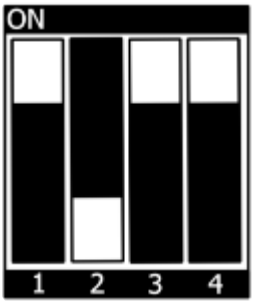
21.3.19.2 System ON/OFF Button (S2)

The phyBOARD-Pollux is equipped with an ON/OFF button at S2, which is connected to X_ONOFF of phyCORE-iMX 8M Plus. For more information, refer to the *i.XM 8M Plus Reference Manual*.

21.3.19.3 Boot Switch (S3)

The phyBOARD-Pollux features a boot switch with four individually switchable ports to select the phyCORE-i.MX 8M Plus default bootsource. Descriptions of the various boot modes can be found in Boot Mode Selection. The figures below show a visual representation of each S3 switch setting:

TABLE 61: Boot Configuration Options (S3)

	
eMMC	**Internal Fuses**
	
SPI NOR	**USB Serial Download**
	
SD Card	**Test Mode**

Boot Mode Design Considerations

Bootpin voltages have to be valid when X_POR_B (X_nRESET at phyBOARD-Pollux) is released.

22 Additional System Level Hardware Information

22.1 I2C Connectivity

The I2C1 interface of the i.MX 8M Plus is only available on the phyCORE module and is not connected to the phyBOARD-Pollux. The table below provides a list of the connectors and pins with I2C connectivity and on-board devices. The I^2C addresses are hexadecimal in 7-bit representation which is the default Linux representation.

TABLE 62: I2C2 Connectivity

I2C2 Interface	Location or Address
phyCAM-M CSI2 Connector (X12)	SDA pin 23, SCL pin 22
Mini PCIe Connector (X10)	SDA pin 30, SCL pin 32
Expansion Connector (X6)	SDA pin 11, SCL pin 13
STUSB4500 (U22)	0x28
TUSB8042A (U3)	0x44
PCA9533D/01 (U21)	0x62
M24C02-RMC6TG (U16)	0x51

TABLE 63: I2C3 Connectivity

I2C3 Interface	Location or Address
phyCAM-M CSI2 Connector (X11)	SDA pin 23, SCL pin 22

TABLE 64: I2C4 Connectivity

I2C4 Interface	Location or Address
A/V Connector (X15)	SDA pin 22, SCL pin 24
Display Connector (X24)	SDA pin 29, SCL pin 27
MIPI DSI Connector (X21)	SDA pin 30, SCL pin 28

To avoid any conflicts when connecting external I2C devices to the phyBOARD-Pollux, the addresses of the on-board I2C devices must be considered. The table below lists the addresses already in use. The default address is printed in bold. The I^2C addresses are hexadecimal in 7-bit representation, which is the default Linux representation.

TABLE 65: Reserved I2C Addresses

Bus	Connector	Prod. No.	Addresses
I2C2	phyCAM-M CSI2 Connector (X12)	VM-016-xxx-M	**0x10**, 0x18
		VM-x17-xxx-M	**0x36**, 0x37
		VM-017-xxx-L	**0x36**, 0x37, **0x18**
		VZ-018	**0x3D**, 0x38

23 Revision History

TABLE 66: Revision History

Date	Version #	Changes in this manual
26.01.2021	L-1009e.A0	Preliminary Manual Describes the phyCORE-i.MX 8M Plus SOM Version: 1549.0 Describes the phyBOARD-Pollux PCB Version: 1552.0
28.07.2021	L-1009e.A1	Manual update SOM Version: 1549.2 PCB Version: 1552.1
24.06.2022	L-1009e.A2	Manual Update: DSC Variant SOM: 1561.0 PDF Version
26.08.2026	L-1009e.A3	Manual update PCB Version: 1552.3 • Changes to X15 and X23

24 Contact Information

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