Hardware Manual - phyCORE-i.MX 8M Mini/ phyBOARD-Polis (1518.6/1532.4) (L-862e.A4)

A Product of PHYTEC Technology Holding Company

Hardware Manual - phyCORE-i.MX 8M Mini/phyBOARD-Polis (1518.6/1532.4) (L-862e.A4)	
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Information on this Manual

This hardware manual describes the PCL-069 System on Module, referred to as phyCORE®-i.MX 8M Mini, and the PBA-C-15, referred to as phyBOARD®-Polis. This manual also specifies the phyCORE-i.MX 8M Mini and phyBOARD-Polis' design and function. Precise specifications for the NXP® Semiconductor i.MX 8M Mini microcontrollers can be found in the i.MX 8M Mini Microcontroller Data Sheet/Reference Manual.

Design Considerations

The schematics shown in this hardware manual are believed to be correct. However, correctness can not be guaranteed. The schematics have been pulled from PHYTEC's designs that have been built, tested, and is known to work. The schematics have been re-formatted to fit better in this hardware manual.

Many hardware examples and suggestions are given in the following pages. Designing the phyCORE System on Module onto a Carrier Board is generally straightforward. However, before committing to a particular active component selection when designing a carrier board, it is wise to check out the software driver support for those components. A particular device may be supported in, say, for example, Linux but not in Windows Embedded Compact 7. Your overall project may go smoother if you pick components that are already supported in your target OS. The premade selections for our reference designs, for example our Single Board Computers, are typically focused on using components that are well supported under Linux.

Specific details may need to be considered when designing a customer-specific carrier board. For design information on carrier board components, please check the ***Design Considerations*** in each component section of phyCORE-i.MX 8M Mini on the phyBOARD-Polis. Be aware that not all components need to be considered when designing your own carrier board.

Preface

As a member of PHYTEC's phyCORE® product family, the phyCORE-i.MX 8M Mini is one of a series of PHYTEC System on Modules (SOMs) that can be populated with different controllers, various types of memory (RAM, NAND flash, eMMC), and many other features. This, in turn, offers increased kinds of functions and configurations. PHYTEC supports a variety of 8/16/32/64 bit controllers in two ways:

1. As the basis for Rapid Development Kits which serve as a reference and evaluation platform.
2. As insert-ready, fully functional phyCORE® OEM modules, which can be embedded directly into the user's peripheral hardware design.

Implementation of an OEM-able SOM subassembly as the "core" of your embedded design allows for increased focus on hardware peripherals and firmware without expending resources to "reinvent" microcontroller circuitry. Furthermore, much of the value of the phyCORE® module lies in its layout and test.

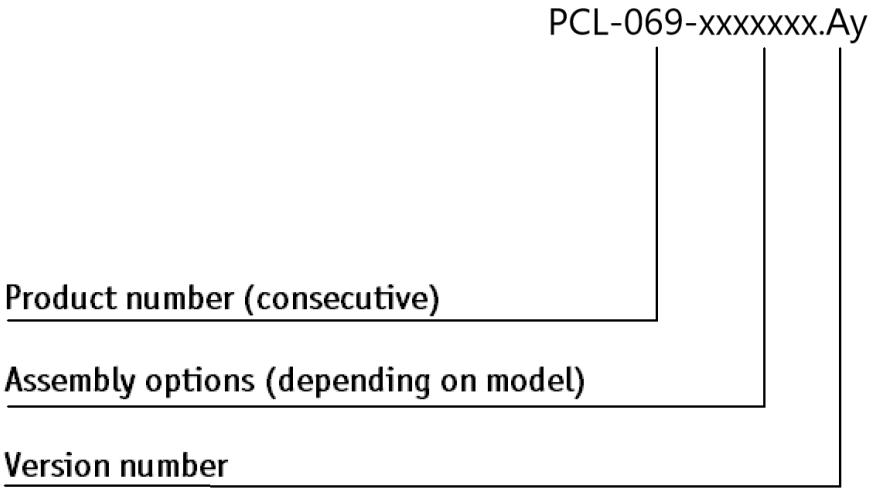
Production-ready Board Support Packages (BSPs) and Design Services for our hardware will further reduce development time and risk and allows for increased focus on product expertise. Take advantage of PHYTEC products to shorten time-to-market, reduce development costs, and avoid substantial design issues and risks. With this new innovative full system solution, new ideas can be brought to market in the most timely and cost-efficient manner.

For more information go to:

http://www.phytec.de/de/leistungen/entwicklungsunterstuetzung.html
or
http://www.phytec.eu/europe/oem-integration/evaluation-start-up.html

Ordering Information

The part numbering of the phyCORE has the following structure:



Product Specific Information and Technical Support

In order to receive product-specific information on all future changes and updates, we recommend registering at: http://www.phytec.de/de/support/registrierung.html or http://www.phytec.eu/europe/support/registration.html

For technical support and additional information concerning your product, please visit the support section of our website which provides product-specific information, such as errata sheets, application notes, FAQs, etc.
https://www.phytec.de/produkt/system-on-modules/phycore-imx-8m-mini-nano/
or
https://www.phytec.eu/product-eu/system-on-modules/phycore-imx-8m-mini-nano/

Note

Assembly Options include a choice of Controller, RAM (Size/Type), Size of NAND Flash, interfaces available, vanishing, temperature range, as well as other features. Please contact our sales team to get more information on the ordering options available.

Declaration of Electro Magnetic Conformity of the PHYTEC



phyCORE®-i.MX 8M Mini

PHYTEC System on Module (henceforth products) are designed for installation in electrical appliances or as dedicated Evaluation Boards (i.e.: for use as a test and prototype platform for hardware/software development) in laboratory environments.

Warning

PHYTEC products lacking protective enclosures are subject to damage by ESD and, therefore, must be unpacked, handled, or operated in environments in which sufficient precautionary measures have been taken with respect to ESD dangers. Only appropriately trained personnel such as qualified electricians, technicians, and engineers should handle and/or operate these products. Moreover, PHYTEC products should not be operated without protection circuitry if connections to the product's pin header rows are longer than 3 m.

PHYTEC products fulfill the norms of the European Union’s Directive for Electro Magnetic Conformity in accordance with the descriptions and rules of usage indicated in this hardware manual (particularly with respect to the pin header row connectors, power connector, and serial interface to a host-PC).

Tip

Implementation of PHYTEC products into target devices, as well as user modifications and extensions of PHYTEC products, is subject to renewed establishment of conformity to and certification of Electro Magnetic Directives. Users should ensure conformance following any modifications to the products as well as the implementation of the products into target systems.

Product Change Management and Information Regarding Parts Populated on the SOM / SBC

With the purchase of a PHYTEC SOM / SBC you will, in addition to our hardware and software possibilities, receive free obsolescence maintenance service for the hardware we provide. Our PCM (Product Change Management) team of developers is continuously processing all incoming PCN's (Product Change Notifications) from vendors and distributors concerning parts that are used in our products. Possible impacts on the functionality of our products due to changes in functionality or obsolesce of certain parts are constantly being evaluated in order to take the right measures either in purchasing decisions or within our hardware/software design.

Our general philosophy here is: **We never discontinue a product as long as there is a demand for it.**

Therefore, we have established a set of methods to fulfill our philosophy:

Avoidance strategies:

- Avoid changes by evaluating the longevity of parts during the design-in phase.
- Ensure the availability of equivalent second source parts.
- Stay in close contact with part vendors to be aware of roadmap strategies.

Change management in the rare event of an obsolete and non-replaceable part:

- Ensure long-term availability by stocking parts through last-time buy management according to product forecasts.
- Offer long-term frame contracts to customers.

Change management in case of functional changes:

- Avoid impacts on product functionality by choosing equivalent replacement parts.
- Avoid impacts on product functionality by compensating for changes through hardware redesign or backward-compatible software maintenance.
- Provide early change notifications concerning functional, relevant changes to our products.

We refrain from providing detailed part-specific information within this manual, which can be subject to continuous changes, due to part maintenance for our products.
In order to receive reliable, up-to-date, and detailed information concerning parts used for our product, please contact our support team through the contact information given within this manual.

PHYTEC Documentation

PHYTEC will provide a variety of hardware and software documentation for all of our products. This includes any or all of the following:

- **Quickstart Guide**: A short guide on how to set up and boot a phyCORE board along with brief information on building a BSP, the device tree, and accessing peripherals.
- **Hardware Manual**: A detailed description of the System on Module and accompanying carrier board.
- **Yocto Guide**: A comprehensive guide for the Yocto version the phyCORE uses. This guide contains an overview of Yocto; an introduction, installing and customizing the PHYTEC BSP; how to work with programs like Poky and Bitbake; and much more.

- **BSP Manual**: A manual specific to the BSP version of the phyCORE. Information such as how to build the BSP, booting, updating software, device tree, and accessing peripherals can be found here.
- **Development Environment Guide**: This guide shows how to work with the Virtual Machine (VM) Host PHYTEC has developed and prepared to run various Development Environments. There are detailed step-by-step instructions for Eclipse and Qt Creator, which are included in the VM. There are instructions for running demo projects for these programs on a phyCORE product as well. Information on how to build a Linux host PC yourself is also a part of this guide.
- **Pin Muxing Table**: phyCORE SOMs have an accompanying pin table (in Excel format). This table will show the complete default signal path, from processor to carrier board. The default device tree muxing option will also be included. This gives a developer all the information needed in one location to make muxing changes and design options when developing a specialized carrier board or adapting a PHYTEC phyCORE SOM to an application.

On top of these standard manuals and guides, PHYTEC will also provide Product Change Notifications, Application Notes, and Technical Notes. These will be done on a case-by-case basis. Most of the documentation can be found on the applicable download page of our products.

Tip

After finishing the Quickstart Guide, we recommend working through the Development Environment Guide. This will give you a comprehensive overview of the features and functions of both the SOM and carrier board.

These manuals and more can be found in the download section of phyCORE-i.MX 8M Mini Product page.

Conventions, Abbreviations, and Acronyms

This hardware manual describes the PCL-069 System on Module, referred to as phyCORE®-i.MX 8M Mini, and the PB-02820-xxxxx.Ax, referred to as phyBOARD®-Polis. The manual specifies the phyCORE-i.MX 8M Mini and phyBOARD-Polis' design and function. Precise specifications for the NXP® Semiconductor i.MX 8M Mini microcontrollers can be found in the*i.MX 8M Mini Microcontroller Data Sheet/Reference Manual*.

Tip

Due to part maintenance for our products (which are subject to continuous changes), we refrain from providing detailed, part-specific information within this manual. Please read the section Product Change Management and Information Regarding Parts Populated on the SOM / SBC within the Preface for more information.

Tip

The BSP delivered with the phyCORE-i.MX 8M Mini includes drivers and/or software for controlling all components such as interfaces, memory, etc. Programming close to hardware at register level is not necessary in most cases. For this reason, this manual contains no detailed description of the controller's registers or information relevant to software development. Please refer to the *NXP i.MX 8M Mini Reference Manual*, if such information is needed to connect customer-designed applications.

Conventions

The conventions used in this manual are as follows:

- Signals that are preceded by an "n", "/", or “#” character (e.g.: nRD, /RD, or #RD), or that have a dash on top of the signal name (e.g.: RD) are designated as active low signals. That is, their active state is when they are driven low, or are driving low.
- A "0" indicates a logic zero or low-level signal, while a "1" represents a logic one or high-level signal.
- The hex numbers given for addresses of I^2C devices always represent the 7 MSB of the address byte. The correct value of the LSB which depends on the desired command (read (1), or write (0)) must be added to get the complete address byte. E.g. given address in this manual 0x41 => complete address byte = 0x83 to read from the device and 0x82 to write to the device
- Tables that describe jumper settings show the default position in **bold, blue text.**

Types of Signals

Different types of signals are brought out at the phyCORE-Connector. The following table lists the abbreviations used to specify the type of signal.

1 Signal Types

Signal Type	Description	Abbreviation
Power	Supply voltage input	PWR_I
Ref-Voltage	Reference voltage output	REF_O

Signal Type	Description	Abbreviation
Input	Digital input	I
Input-Pullup	Input with pull up	I-PU
Output	Digital output	O
IO	Bidirectional input/output	I/O
OC-Bidir	Open collector input/output with pull up	OC-BI
OC-Output	Open collector output without pull up requires an external pull up	OC
OD-Bidir PU	Open-drain input/output with pull up	OD-BI
OD-Output	Open-drain output without pull up requires an external pull up	OD
OD-Output-Pullup	Open-drain output with pull up	OD-PU
5V Input PD	5 V tolerant input with pull-down	5V_PD
USB IO	Differential line pairs 90 Ohm USB level bidirectional input/output	USB_I/O
ETHERNET Input	Differential line pairs 100 Ohm Ethernet level input	ETH_I
ETHERNET Output	Differential line pairs 100 Ohm Ethernet level output	ETH_O
ETHERNET IO	Differential line pairs 100 Ohm Ethernet level bidirectional input/output	ETH_I/O
PCIe Input	Differential line pairs 85 Ohm PCIe level input	PCIe_I
PCIe Output	Differential line pairs 85 Ohm PCIe level output	PCIe_O
MIPI CSI-2 Input	Differential line pairs 100 Ohm MIPI CSI-2 level input	CSI2_I
MIPI DSI-2 Output	Differential line pairs 100 Ohm MIPI DSI-2 level input	DSI2_O
CAN FD IO	Differential line pairs 120 Ohm CAN FD level bidirectional input/output	CAN_I/O

Signal Type	Description	Abbreviation
CAN FD IO	Differential line pairs 120 Ohm CAN FD level bidirectional input/output	CAN_I/O
Wireless	Wireless signal input/output	WL_I/O

Abbreviations and Acronyms

Many acronyms and abbreviations are used throughout this manual. Use the table below to navigate any unfamiliar terms used in this document.

2 Abbreviations and Acronyms Used in this Manual

Abbreviation	Definition
BGA	Ball Grid Array
BSP	Board Support Package (software delivered with the Development Kit including an operating system (Windows or Linux) preinstalled on the module and development tools)
CB	Carrier board; used in reference to the phyCORE development kit carrier board
EMI	Electromagnetic Interference
GPI	General-purpose input
GPIO	General-purpose input and output
GPO	General-purpose output
IRAM	Internal RAM; the internal static RAM on the NXP® Semiconductor i.MX 8M microcontroller
J	Solder jumper; these types of jumpers require solder equipment to remove and place
JP	Solderless jumper; these types of jumpers can be removed and placed by hand with no special tools
OEM	Original Equipment Manufacturers

Abbreviation	Definition
PCB	Printed circuit board
PCM	Product Change Management
PCN	Product Change Notification
PMIC	Power management IC
RTC	Real-time clock
SBC	Single Board Computer
SMT	Surface mount technology
SOM	System on Module; used in reference to the PCL-066 /phyCORE®-i.MX 8M module
Sx	User button Sx (e.g. S1, S2, etc.) used in reference to the available user buttons, or DIP-Switches on the carrier board
Sx_y	Switch y of DIP-Switch Sx; used in reference to the DIP-Switch on the carrier board
VM	Virtual Machine

phyCORE-i.MX 8M Mini Introduction

The phyCORE-i.MX 8M Mini belongs to PHYTEC's phyCORE System on Module family. The phyCORE SOMs represent the continuous development of PHYTEC System on Module technology. Like its mini-, micro-, and nanoMODUL predecessors, phyCORE boards integrate all core elements of a microcontroller system on a sub-miniature board and are designed in a manner that ensures their easy expansion and embedding in peripheral hardware developments.

Independent research indicates approximately 70 % of all EMI (Electro-Magnetic Interference) problems are caused by insufficient supply voltage grounding of electronic components in high-frequency environments. The phyCORE board design features an increased pin package, which allows for the dedication of approximately 37 % of all connector pins on the phyCORE boards to Ground. This improves EMI and EMC characteristics and makes it easier to design complex applications meeting EMI and EMC guidelines using phyCORE boards, even in high-noise environments.

phyCORE boards achieve their small size through modern SMT and multi-layer design. Due to the complexity of our modules, 0201-packaged SMT components and laser-drilled microvias are used on the boards, providing phyCORE users with access to this cutting-edge miniaturization technology for integration into their own design.

The phyCORE-i.MX 8M Mini is a sub-miniature (37 mm x 40 mm) soldered System on Module populated with the NXP® Semiconductor i.MX 8M Mini microcontroller. Its universal design enables its insertion in a wide range of embedded applications. All controller signals and ports extend from the controller to a 1,27mm pitch BGA Ball. Each signal ball has an associated GND pin which ensures the GND reference for each signal. The ball packages are placed in lines. There is enough space between lines to ensure the possibility of easy routing out of the package. Signal balls for a high-speed signal like HDMI are placed on the outer lines, making it easy to route to the top layer of the carrier board. The SOM is designed to support carrier boards with as few as 6 layers to reduce PCB costs. For proper EMC characteristics, it is necessary to place the processor caps directly under the SOM. This required a hole in the carrier board.

The descriptions in this manual are based on the NXP® Semiconductor i.MX 8M Mini. Descriptions of compatible microcontroller derivative functions are not included, as such functions are not relevant for the basic functioning of the phyCORE-i.MX 8M Mini.

phyCORE-i.MX 8M Mini Features

The phyCORE-i.MX 8M Mini offers the following features:

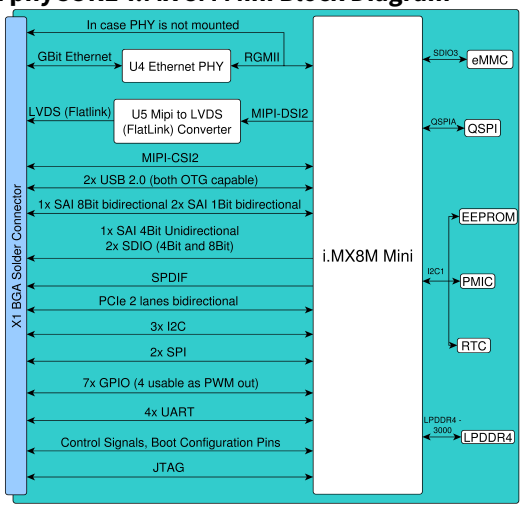
- Insert-ready, sub-miniature (37 mm x 40 mm) System on Module (SOM) sub-assembly in low EMI design, achieved through advanced SMD technology
- Mounted using BGA Technology
- Populated with the NXP® Semiconductor i.MX 8M Mini microcontroller (BGA486 packaging)
- 1.6 GHz core clock frequency (up to 1.8 GHz)
- Boot from different memory devices (eMMC standard)
- Single supply voltage of +3.3 V with onboard power management
- All controller-required supplies are generated onboard
- Improved interference safety achieved through multi-layer PCB technology and dedicated ground pins
- 2 GB (up to 4 GB)[1]) LPDDR4 RAM
- 4 GB (up to 256 GB[1]) onboard eMMC
- 4 kB[1] I^2C EEPROM
- 2x High-Speed USB 2.0 OTG interfaces
- 1x 10/100/1000 MBit Ethernet interface (if Ethernet transceiver is mounted)[2]
- One RGMII interface at TTL level (if Ethernet transceiver is not mounted)[2]
- Three I^2C interfaces

- Two SPI interfaces
- One PCIe interface
- Four UART interfaces
- Four PWM outputs
- One LVDS interface (if MIPI-DSI to LVDS converter is mounted)[2]
- One MIPI DSI interface (if MIPI-DSI to LVDS converter is not mounted)[2]
- One MIPI CSI camera interface
- One 4-Bit SD-Card interface
- One 8-Bit SDIO interface
- SAI audio interface
- Internal RTC
- Available for different temperature grades (Product Temperature Grades)

1. The maximum memory size listed as of the printing of this manual.
   Please contact PHYTEC for more information about additional or new module configurations available.
2. Please refer to the order options described in the Preface
   or contact PHYTEC for more information about additional module configurations.

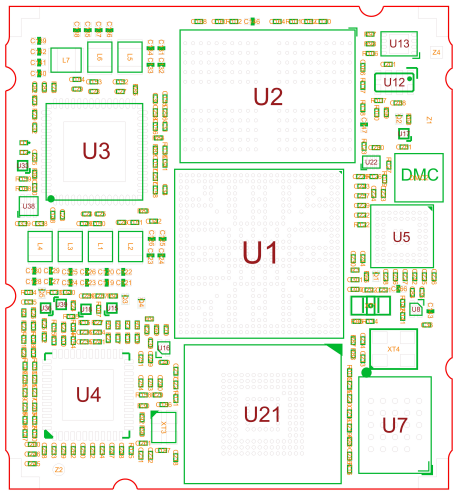
phyCORE-i.MX 8M Mini Block Diagram

1 phyCORE-i.MX 8M Mini Block Diagram

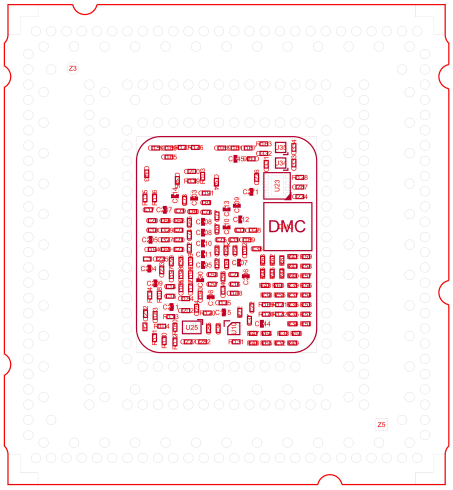


phyCORE-i.MX 8M Mini Component Placement

2 phyCORE-i.MX 8M Mini Component Placement (Top)



3 phyCORE-i.MX 8M Mini Component Placement (Bottom)



phyCORE-i.MX 8M Mini Minimal Operating Requirements

We recommend connecting all available VDD_3V3 input pins to the power supply system on a custom carrier board housing the phyCORE-i.MX 8M Mini and, at minimum, the matching number of GND pins neighboring the VDD_3V3 input pins. In addition, proper implementation of the phyCORE-i.MX 8M Mini module into a target application also requires connecting all GND pins.
Refer to Power for more information.

Pin Description

Module connections **must** not exceed their expressed maximum voltage or current. Maximum signal input values are indicated in the corresponding controller manuals/datasheets. As damage from improper connections varies according to use and application, the user must take appropriate safety measures to ensure that the module connections are protected from overloading through connected peripherals.

All controller signals extend to BGA Signal Balls (1.27 mm) which allows the phyCORE-i.MX 8M Mini to be soldered into any target application like a "big chip".

PHYTEC provides a complete pinout table for the phyCORE-i.MX 8M Mini Connector X1. This table contains a complete signal path for the phyCORE-i.MX 8M Mini and the carrier board phyBOARD-Polis, including signal names, pin muxing paths, and descriptions specific to each pin. It also provides the appropriate voltage domain, signal type (ST), and a functional grouping of the signals. The signal type also includes information about the signal direction. A table describing the signal types can be found with the pinout table.

https://www.phytec.de/produkt/system-on-modules/phycore-imx-8m-mini-nano-phyboard-polis-download/#pin-description

Warning

- The NXP® Semiconductor i.MX 8M Mini is a multi-voltage-operated microcontroller and, as such, special attention should be paid to the interface voltage levels to avoid unintentional damage to the microcontroller and other onboard components. Please refer to the *NXP Semiconductor NXP i.MX 8M Mini Reference Manual* for details on the functions and features of controller signals and port pins.
- As some of the signals which are brought out on the phyCORE-Connector are used to configure the boot mode for specific boot options, please make sure that these signals are not driven by any device on the baseboard during reset. The signals which may affect the boot configuration are shown in the table phyCORE-Connector Boot Configuration Pins.
- It is necessary to avoid voltages at the IO pins of the phyCORE-i.MX 8M Mini which are sourced from the supply voltage of peripheral devices attached to the SOM during power-up or power–down. These voltages can cause a current flow into the controller, especially if peripheral devices attached to the interfaces of the i.MX 8M Mini are supposed to be powered while the phyCORE-i.MX 8M Mini is in suspend mode or turned off. To avoid this, bus switches either supplied by VDD_3V3_S on the phyCORE side or having their output enabled to the SOM controlled by the X_PGOOD_OD signal (see External Logic Supply Voltage) must be used.

Tips

- Most of the controller pins have multiple multiplexed functions. As most of these pins are connected directly to the phyCORE-Connector, the alternative functions are available by using the i.MX 8M Mini's pin muxing options. Signal names and descriptions in the accompanying table, however, are in regard to the specification of the phyCORE-i.MX 8M Mini and the functions defined. Please refer to the *i.MX 8M Reference Manual* or the schematic to get to know about alternative functions. In order to utilize a specific pin's alternative function, the corresponding registers must be configured within the appropriate driver of the BSP.
- In case a design requires specific logic levels at its signals, special attention has to be paid to the settings of i.MX 8M Mini's internal pull resistors. It is good design practice to never rely on the SoC-internal pull resistors.

- The following tables describe the full set of signals available at the phyCORE-Connector according to the phyCORE-i.MX 8M Mini specification. However, the availability of some interfaces is order-specific (e.g. Camera_0). Thus, some signals might not be available on your module.
- As the phyCORE-i.MX 8M Mini is delivered with the carrier board phyBOARD-Polis, the pin muxing might be changed within the appropriate BSP in order to support all features of the carrier board. If so, information on the differences from the pinout given in the following tables can be found in the carrier board's documentation.

Errata information

Existing issues may be solved by referring to the following chapters in *NXP Mask Set Errata for Mask 0N87W, Rev. 1, 09/2021*:

- ERR050080: IO: Degradation of internal IO pullup/pulldown current capability for IO’s continuously driven in a 3.3V operating mode

It is good design practice to never rely on the SoC-internal pull resistors.

Unused Signals

It is recommended to handle unused signals according to the table below:

3 Abbreviations and Acronyms Used in this Manual

Interface	Signals	Recommendation
MIPI-CSI	X_MIPI_CSI_CLK_N X_MIPI_CSI_CLK_P X_MIPI_CSI_DATA0_N X_MIPI_CSI_DATA0_P X_MIPI_CSI_DATA1_N X_MIPI_CSI_DATA1_P X_MIPI_CSI_DATA2_N X_MIPI_CSI_DATA2_P X_MIPI_CSI_DATA3_N X_MIPI_CSI_DATA3_P	Connect to GND
MIPI-DSI/FlatLink-LVDS	X_FLATLINK_D0_N/MIPI_DSI_DATA0_N X_FLATLINK_D0_P/MIPI_DSI_DATA0_P X_FLATLINK_D1_N/MIPI_DSI_DATA1_N X_FLATLINK_D1_P/MIPI_DSI_DATA1_P X_FLATLINK_D2_N/MIPI_DSI_CLK_N X_FLATLINK_D2_P/MIPI_DSI_CLK_P X_FLATLINK_D3_N/MIPI_DSI_DATA2_N X_FLATLINK_D3_P/MIPI_DSI_DATA2_P X_FLATLINK_CLK_N/MIPI_DSI_DATA3_N X_FLATLINK_CLK_P/MIPI_DSI_DATA3_P	Leave unconnected
PCIe	X_PCIe_CLK_N X_PCIe_CLK_P X_PCIe_TXN_N X_PCIe_TXN_P X_PCIe_RXN_N X_PCIe_RXN_P	Leave unconnected
USB1	USB1_VBUS X_USB1_DN X_USB1_DP X_USB1_ID	Leave unconnected
USB2	USB2_VBUS X_USB2_DN X_USB2_DP X_USB2_ID	Leave unconnected

Interface	Signals	Recommendation
ETHERNET	X_ETH_A_P X_ETH_A_N X_ETH_B_P X_ETH_B_N X_ETH_C_P X_ETH_C_N X_ETH_D_P X_ETH_D_N	Leave unconnected
GPIO	All remaining single-ended signals	Leave unconnected

Power

The phyCORE-i.MX 8M Mini operates off of a single power supply voltage. The following sections discuss the primary power pins on the phyCORE-i.MX 8M Mini Connector X1 in detail.

Primary System Power (VDD_3V3)

The phyCORE-i.MX 8M Mini operates with a single primary voltage supply. Onboard switching and low dropout regulators generate the 2.5 V, 1.8 V, 1.2 V, 1.1 V, 0.9 V, and 0.8 V voltage rails required by the i.MX 8M Mini CPU and onboard components from the input voltage VDD_3V3.

For proper operation, the phyCORE-i.MX 8M Mini must be supplied with a voltage source of 3.3 V +4.5 %-4 % with 2 A load at the VDD pins on the phyCORE-i.MX 8M Mini Connector X1.

In order to perform a full power cycle of the phyCORE-i.MX 8M Mini, including the SNVS domain of the PMIC and the CPU, the voltage input rail VDD_3V3 has to remain below 0,3 V for at least 600 ms.

Note

It is recommended to choose a slightly higher value than 3.3 V for VDD_3V3 in order to account for series resistance of 3.3 V load switching components on the SoM. The PHYTEC phyBOARD-Polis for example supplies VDD_3V3 with 3.366 V ±3.5 %.

VDD_3V3: X1 → A75, A76, A77, A78

Connect all VDD_3V3 input pins to your power supply and, at the very least, the matching number of GND pins.

Corresponding GND: X1 → B36, B37, B38, B39, B40, B41

Please refer to the section Pin Description for information on additional GND pins located at the phyCORE-i.MX 8M Mini Connector X1.

Warning

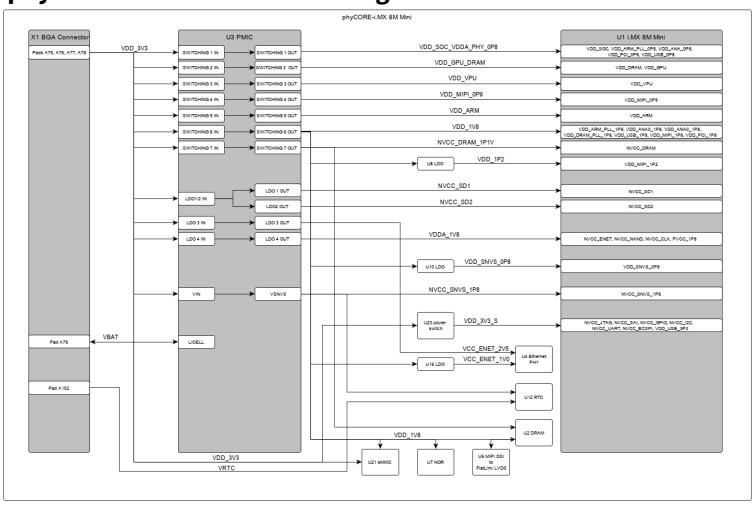
As a general design rule, PHYTEC recommends connecting all GND pins neighboring signals which are being used in the application circuitry. For maximum EMI performance, all GND pins should be connected to a solid ground plane.

Power Management IC (PMIC)(U3)

The phyCORE-i.MX 8M Mini provides an onboard Power Management IC (PMIC) at position U3 to generate different voltages required by the microcontroller and the onboard components. The Powering Scheme figure presents a graphical depiction of the powering scheme. The PMIC supports many functions like on-chip RTC and different power management functionalities like dynamic voltage control, different low power modes, and regulator supervision. It is connected to the i.MX 8M Mini via the onboard I^2C bus (I2C1) (I2C Interface). The I^2C address of the PMIC is 0x08.

Power Domains

4 phyCORE-i.MX 8M Mini Powering Scheme



External voltages:

- VDD_3V3: SOM input supply voltage
- VDD_BAT: Backup supply (connected to VBAT)

Internally generated voltages:

4 Internally Generated Voltages

VDD_SOC_VDDA_PHY_0P8	i.MX 8M Mini SOC logic and PHY supply (VDD_SOC1-12, VDD_ARM_PLL_0P8, VDD_ANA_0P8_1-2, VDD_PCI_0P8, VDD_USB_0P8) (0.8 V)
VDD_GPU_DRAM	i.MX 8M Mini 3D GPU and DRAM supply (VDD_GPU1-5, VDD_DRAM1-6, VDD_DRAM_PLL_0P8) (0.8/0.9 V)
VDD_VPU	i.MX 8M Mini MIPI PLL, logic (VDD_MIPI_0P9) (0.9 V)
VDD_MIPI_0P9	i.MX 8M Mini MIPI PLL, logic (VDD_MIPI_0P9) (0.9 V)
VDD_ARM	i.MX 8M Mini Mini ARM supply (VDD_ARM1-14) (0.8/0.9 V)
NVCC_DRAM_1P1V	DRAM supply (NVCC_DRAM1-13) (1.1 V)

VDD_1V8	i.MX 8M Mini general 1.8 V supply (VDD_ARM_PLL_1P8, VDD_ANA0_1P8_1-2, VDD_ANA1_1P8_1-2, VDD_DRAM_PLL_1P8, VDD_USB_1P8, VDD_MIPI_1P8, VDD_PCI_1P8) (1.8)
NVCC_SD2	i.MX 8M Mini SDIO2 supply (NVCC_SD2) (1.8/3.3 V)
VDDA_1V8	i.MX 8M Mini 1.8 V analog supply (VCC_24M_XTAL_1P8. PVCC0_1P8, VCC2_1P8, NVCC_ENET, NVCC_NAND, NVCC_CLK) (1.8 V)
NVCC_SNVS_1P8	i.MX 8M Mini SNVS GPIO driver supply /NVCC_SNVS_1P8) (1.8 V)
VCC_ENET_2V5	i.MX 8M Mini Ethernet PHY supply (U4) (2.5 V)
NVCC_SD1	i.MX 8M Mini SDIO1 supply (NVCC_SD1) (3.3 V PHYTEC default setting, 1.8 V possible through software adjustment)
VDD_3V3_S	i.MX 8M Mini general 3.3 V supply (NVCC_JTAG, NVCC_SAI1-3, NVCC_SAI5, NVCC_GPIO1, NVCC_I2C, NVCC_UART, NVCC_ECSPI, VCC_USB_3P3) (3.3 V)

External Logic Supply Voltage

The voltage level of the phyCORE's logic circuitry is VDD_3V3_S (3.3 V) which is derived from the SOM main input voltage, VDD_3V3. In order to follow the mandatory power-up and power-down sequencing for the i.MX 8M Mini, external devices have to be supplied by the I/O supply voltage VDD_3V3_S which is brought out at pin E14 of the phyCORE-Connector. The use of VDD_3V3_S ensures that external components are only supplied when the supply voltages of the i.MX 8M Mini are stable.

Warning

The current draw for VDD_3V3_S must not exceed 500 mA. Consequently, this voltage should only be used as a reference or supply voltage for level shifters. VDD_3V3_S cannot be used to supply high-powered applications. If devices with higher power consumption are connected to the phyCORE-i.MX 8M Mini, their supply voltage should be switched on and off by use of the X_PGOOD signal. This way, the power-up and power-down sequencing will be considered even if the devices are not supplied directly by VDD_3V3_S.

Tip

If used to control or supply bus switches on the phyCORE side, VDD_3V3_S separates the supply voltages generated on the phyCORE-i.MX 8M Mini and the supply voltages used on the carrier board/custom application. This way, voltages at the IO pins of the phyCORE-i.MX 8M Mini which are sourced from the supply voltage of peripheral devices attached to the SOM are avoided.

These voltages can cause a current flow into the controller, especially if peripheral devices attached to the interfaces of the i.MX 8M Mini are supposed to be powered while the phyCORE-i.MX 8M Mini is in suspend mode or turned off. The bus switches can be supplied by VDD_3V3_S on the phyCORE side, or the bus switches' output enabled to the SOM can be controlled by X_PGOOD to prevent these voltages from occurring.
The use of level shifters supplied with VDD_3V3_S allows the signals to be converted according to the needs of the custom target hardware. Alternatively, signals can be connected to an open drain circuitry with a pull-up resistor attached to VDD_3V3_S.

Backup Power (VBAT)

At pin A79 (Signal VBAT) of the phyCORE-i.MX 8M Mini, a secondary 3.3 V voltage source may be attached to the SOM. The PMIC (U3) will use this secondary source to generate NVCC_SNVS_1P8 in case VDD_3V3 falls below a value of approx. 2.8 V.

On-Board RTC and RTC Backup Power (VRTC)

At pin A102 (Signal VRTC) of the phyCORE-i.MX 8M Mini, a secondary voltage source may be attached to the SOM in order to buffer the onboard RTC U12, while the SOM input voltage is not present. This manual describes only one of the available RTC active power states, which is used in conjunction with the phyBOARD-POLIS and the phyCORE-i.MX 8M Mini. The RTC RV-3028-C7 will enter its backup mode as soon as it detects the voltage level at Pin VRTC to be higher than the SOM input voltage VDD_3V3.

For further details on the functionalities of the RTC RV-3028-C7 please refer to *Micro Crystal Switzerland Application Manual RV-3028-C7.*

Warning

In its backup power state, the RTC will cease to communicate over I2C1 if the voltage level at the Pin VRTC is higher than the SOM input voltage VDD_3V3. In order to avoid unnecessary problems, the recommended voltage difference between VDD_3V3 and VRTC is approx. 300 mV.

Reset

Pin C43 on the phyCORE-Connector is designated as an open-drain reset input with a pull-up resistor, that triggers a hard reset of the module. The external reset signal is connected to the enable signal of the voltage supervisor U41, which triggers a watchdog event in the PMIC resulting in a hard reset of the module. For debouncing purposes, the U41 delays the signal by 8,804 ms.

For PCB versions 1518.0, 1518.1a and 1518.2 additional precautions have to be taken regarding the undervoltage detection of the phyCORE-i.MX 8M Mini. X_nPOR_IN must be held on a logical low level, as long as VDD_3V3 is below 3.135 V. If this is not considered in the design of a baseboard, there is a small chance that the SoM could enter an unspecified mode of operation. PCB version 1518.3 and higher will not require this feature any longer, yet it is good engineering practice, to monitor all voltage rails at all times.

The PMIC reset output signal POR_B is made available at the phyCORE-Connector through a buffer as the open drain signal X_nPOR_OUT_OD. X_nPOR_OUT_OD is not connected to a pull-up resistor on the module. This leaves the user the freedom to choose the voltage domain used on the target hardware.

In case of a hard reset, regardless if it was triggered internally or externally, the PMIC holds the POR_B signal low until the module voltages are at stabilized levels. The POR_B signal is released approximately 11 ms after the last module voltage is correctly generated.

In order to perform a full power cycle of the phyCORE-i.MX 8M Mini, including the SNVS domain of the PMIC and the CPU, the voltage input rail VDD_3V3 has to remain below 0,3 V for at least 600 ms.

5 phyCORE-Connector Reset Pins

SOM Connector Pin / phyBOARD-Polis Carrier Board Connector Pin	SOM Signal Name	SOM Voltage Domain	Signal Level	Signal Type	Description
C43	X_nRESET_IN	VDD_3V3	3.3 V	I-PU	SoM reset input. Transition to low level will power cycle the SoM. Signal is pulled up to SoM input voltage rail.
C47	X_nPOR_IN	VDD_3V3	3.3 V	I-PU	Power-on reset input. May be used to prolong reset state of CPU and other attached devices.

SOM Connector Pin / phyBOARD-Polis Carrier Board Connector Pin	SOM Signal Name	SOM Voltage Domain	Signal Level	Signal Type	Description
E19	X_nPOR_OUT_OD	VDD_3V3	Up to 3.3 V	OD	Power-on reset output. Requires an external pull-up resistor. Voltage range up to 3,3 V

System Boot Configuration

i.MX 8M Mini System Boot Settings

Most features of the i.MX 8M Mini microcontroller are configured and/or programmed during the initialization routine. Essential boot features however are latched into i.MX 8M Mini registers from pre-configured pull-resistors following power-on reset (POR_B) de-assertion.

The latched-in information includes:

- Boot mode selection
- Boot device selection
- Detailed boot device configuration

The internal ROM code is the first code executed during the initialization process of the i.MX 8M Mini after POR de-assertion. The ROM code detects the boot mode through pins X_BOOT_MODE0 and X_BOOT_MODE1, while the boot device is selected and configured by determining the state of the eFUSEs and/or the corresponding GPIO pins (BOOT_CFGx[14:12]).

Boot Mode Selection

The i.MX 8M Mini boot mode is determined by the logical levels of the pins X_BOOT_MODE0 and X_BOOT_MODE1 approx. 31 µs after POR_B de-assertion. X_BOOT_MODE0 and X_BOOT_MODE1 are brought out at the phyCORE-Connector pins C15 and C16. Possible settings and the resulting boot configuration of the i.MX 8M Mini are described in the following table:

6 phyCORE-i.MX 8M Mini Boot Modes

X_ BOOT_MODE1	X_ BOOT_MODE0	Boot Source
0	0	Fuse boot
0	1	Serial downloader
1	0	Internal boot
1	1	Reserved

The BOOT_MODE[1:0] lines have 10 kΩ pull-up and pull-down resistors populated on the module. The default boot mode on the phyCORE-i.MX 8M Mini is set to internal boot mode, hence leaving the two pins unconnected will result in the unavailability of the remaining boot mode settings. The default boot device of phyCORE-i.MX 8M Mini is eMMC at SDIO3. Once in serial downloader boot, the ROM code polls the USB1 interface, initiates the download of the code into the internal RAM, and triggers its execution from there. In serial downloader boot mode the BOOT_CFG pins are ignored. Please refer to the *NXP i.MX 8M Mini Reference Manual* for more detailed information.

In fuse boot and internal boot mode, the ROM code finds the bootloader in permanent memories, such as eMMC or SD-Cards, and executes it. The boot device selection and the required interface configuration are accomplished with the help of the eFUSEs and/or the corresponding GPIO input.

Boot Device Selection and Configuration

In fuse boot and internal boot mode, the ROM code uses the BOOT_CFG pin states and eFUSEs to determine the boot device and its detailed configuration.

During development, it is advisable to set the Boot Source to “Internal boot” so that choosing and configuring the boot device using GPIO pin inputs is available. The BOOT_CFG pins are sampled shortly after POR de-assertion and, if the BT_FUSE_SEL fuse is not blown, override the values of the corresponding eFUSEs BOOT_CFGx[14:0].

The Boot Configuration Pins table lists the eFUSEs BOOT_CFGx[14:0] and the corresponding input pins. On the phyCORE-i.MX 8M Mini, the BOOT_CFG GPIOs have 10 kΩ pull-up and pull-down resistors pre-installed to configure eFUSEs BOOT_CFGx[14:0] in accordance with the module features.

The specific boot configuration settings, set by the on-board configuration resistors, can be changed by modifying the resistors on the module or overwritten by connecting a configuration resistor (e.g. 1 kΩ) to the configuration signal. Choosing to not pull the boot configuration pins to a high or low level will lead to the configuration (other than the default configuration setting) being unavailable. If only the default boot option will be used no further boot resistors are necessary.

Furthermore, accidental pull resistances must be considered when designing base hardware for the phyCORE-i.MX 8M Mini. Any IC or passive component that forces a high or low level at one of the designated boot mode or boot configuration pins needs to be gated away during boot mode or boot configuration latch-in. A bus switch, buffer, or transistor circuit may yield the required results.

Please consider that any change of the default boot configuration can also influence other boot modes, which might result in faulty boot behavior. Please refer to the *NXP i.MX 8M Mini Reference Manual* for further information about the eFUSEs and the impact of the settings at the boot configuration pins.

The following table shows the phyCORE-i.MX 8M Mini default boot device configuration setting:

7 phyCORE-Connector Boot Configuration Default Setting

Memory Device	BOOT_CFG [14]	BOOT_CFG [13]	BOOT_CFG [12]	BOOT_CFG [11]	BOOT_CFG [10]	BOOT_CFG [9]	BOOT_CFG [8]	BOOT_CFG [7]	BOOT_CFG [6]	BOOT_CFG [5]	BOOT_CFG [4]	BOOT_CFG [3]	BOOT_CFG [2]	BOOT_CFG [1]	BOOT_CFG [0]
eMMC U21	0	1	0	1	0	1	0	0	1	0	1	0	1	1	0

Memory Device	BOOT_CFG [14]	BOOT_CFG [13]	BOOT_CFG [12]	BOOT_CFG [11]	BOOT_CFG [10]	BOOT_CFG [9]	BOOT_CFG [8]	BOOT_CFG [7]	BOOT_CFG [6]	BOOT_CFG [5]	BOOT_CFG [4]	BOOT_CFG [3]	BOOT_CFG [2]	BOOT_CFG [1]	BOOT_CFG [0]
Setting	010 - eMMC			10 - SDIO3		1 - Power Cycle enabled	0 - SD loopback clock source SEL through SD pad	0 - Regular boot	101 - 4-Bit DDR (MMC 4.4)			01 - High		1 - uSDHC IO voltage = 1,8 V	0 - uSDHC IO voltage manufacturer mode = 3,3 V

The following table shows an excerpt from the complete boot configuration table in the *NXP i.MX 8M Mini Reference Manual*, edited to represent the phyCORE-i.MX 8M Mini's available boot configuration settings:

8 phyCORE-i.MX 8M Mini Possible Boot Configuration Settings

Memory Device	BOOT_CFG [14]	BOOT_CFG [13]	BOOT_CFG [12]	BOOT_CFG [11]	BOOT_CFG [10]	BOOT_CFG [9]	BOOT_CFG [8]	BOOT_CFG [7]	BOOT_CFG [6]	BOOT_CFG [5]	BOOT_CFG [4]	BOOT_CFG [3]	BOOT_CFG [2]	BOOT_CFG [1]	BOOT_CFG [0]
SPI-NOR	1	1	0	000 - eCSPI1 001 - eCSPI2 010 - eCSPI3			SPI addressing: 0 - 3 bytes 1 - 2 bytes	Chip Select: 00 - CS#0 01 - CS#1 10 - CS#2 11 - CS#3	Reserved						

Memory Device	BOOT_CFG [14]	BOOT_CFG [13]	BOOT_CFG [12]	BOOT_CFG [11]	BOOT_CFG [10]	BOOT_CFG [9]	BOOT_CFG [8]	BOOT_CFG [7]	BOOT_CFG [6]	BOOT_CFG [5]	BOOT_CFG [4]	BOOT_CFG [3]	BOOT_CFG [2]	BOOT_CFG [1]	BOOT_CFG [0]
QSPI-NOR (FlexSPI)	1	0	0	0 - FLASH auto probe disabled 1- FLASH auto probe enabled	FLASH TYPE: 000 - Device supports 3 Byte read by default 001 - Device supports 4 Byte read by default			Hold time before reading from device: 0 – 500 us 1 – 1 ms 2 – 3 ms 3 – 10 ms		SPI FLASH Auto Probe Type: 0 – QuadSPI NOR		0 - FlexSPI FLASH dummy cycle auto-probe 0001 to 1111 - Set number of FlexSPI FLASH dummy cycles manually to chosen value			

Memory Device	BOOT_CFG [14]	BOOT_CFG [13]	BOOT_CFG [12]	BOOT_CFG [11]	BOOT_CFG [10]	BOOT_CFG [9]	BOOT_CFG [8]	BOOT_CFG [7]	BOOT_CFG [6]	BOOT_CFG [5]	BOOT_CFG [4]	BOOT_CFG [3]	BOOT_CFG [2]	BOOT_CFG [1]	BOOT_CFG [0]
eMMC	0	1	0	Port select: 00 - SDIO1 01 - SDIO2 10 - SDIO3		Power cycle: 0 – disabled 1 – enabled	SD loopback clock source SEL (SDR50 and SDR104 only): 0 - Through SD pad 1 - Direct	Fast boot: 0 - Regular 1 - Fast boot	Bus width: 000 - 1-Bit 001 - 4-Bit 010 - 8-Bit 101 - 4-Bit DDR (MMC 4.4) 110 - 8-Bit DDR (MMC 4.4) Remaining values are reserved			Speed: 00 - Normal 01 - High 10 - Reserved for HS200 11 - Reserved		USDHC IO voltage selection; normal mode: 0 - 3.3V 1 - 1.8V	USDHC IO voltage selection; manufacturer mode: 0 - 3.3V 1 - 1.8V

Memory Device	BOOT_CFG [14]	BOOT_CFG [13]	BOOT_CFG [12]	BOOT_CFG [11]	BOOT_CFG [10]	BOOT_CFG [9]	BOOT_CFG [8]	BOOT_CFG [7]	BOOT_CFG [6]	BOOT_CFG [5]	BOOT_CFG [4]	BOOT_CFG [3]	BOOT_CFG [2]	BOOT_CFG [1]	BOOT_CFG [0]
SD-Card	0	0	1	Port select: 00 - SDIO1 01 - SDIO2		Power cycle: 0 – disabled 1 – enabled	SD loopback clock source SEL (SDR50 and SDR104 only): 0 - Through SD pad 1 - Direct	Fast boot: 0 - Regular 1 - Fast boot	Reserved		Bus width: 000 - 1-Bit 001 - 4-Bit	Speed: 000 - Normal/ SDR12 001 - High/SDR25 010 - SDR50 011 - SDR104 101 - Reserved for DDR50 Others - Reserved			Reserved

The following table shows the properties of BOOT_CFG[14:0] during reset and during runtime and their location on the phyCORE-Connector, as well as their signal names.

9 phyCORE-Connector Boot Configuration Pins

Configuration Pin	SOM Connector Pin / phyBOARD-Polis Carrier Board Connector Pin	SOM Signal Name	SOM Voltage Domain	Signal Level	Signal Type	Description
BOOT_CFG[0]	A81	X_SAI1_RXD0 / BOOT_CFG[0]	VDD_3V3_S	3.3 V	I/O	Boot configuration pin 0 during reset SAI receive data 0 during runtime
BOOT_CFG[1]	A82	X_SAI1_RXD1 / BOOT_CFG[1]	VDD_3V3_S	3.3 V	I/O	Boot configuration pin 1 during reset SAI receive data 1 during runtime
BOOT_CFG[2]	A85	X_SAI1_RXD2 / BOOT_CFG[2]	VDD_3V3_S	3.3 V	I/O	Boot configuration pin 2 during reset SAI receive data 2 during runtime
BOOT_CFG[3]	A86	X_SAI1_RXD3 / BOOT_CFG[3]	VDD_3V3_S	3.3 V	I/O	Boot configuration pin 3 during reset SAI receive data 3 during runtime
BOOT_CFG[4]	A87	X_SAI1_RXD4 / BOOT_CFG[4]	VDD_3V3_S	3.3 V	I/O	Boot configuration pin 4 during reset SAI receive data 4 during runtime

Configuration Pin	SOM Connector Pin / phyBOARD-Polis Carrier Board Connector Pin	SOM Signal Name	SOM Voltage Domain	Signal Level	Signal Type	Description
BOOT_CFG[5]	A88	X_SAI1_RXD5 / BOOT_CFG[5]	VDD_3V3_S	3.3 V	I/O	Boot configuration pin 5 during reset SAI receive data 5 during runtime
BOOT_CFG[6]	A89	X_SAI1_RXD6 / BOOT_CFG[6]	VDD_3V3_S	3.3 V	I/O	Boot configuration pin 6 during reset SAI receive data 6 during runtime
BOOT_CFG[7]	A90	X_SAI1_RXD7 / BOOT_CFG[7]	VDD_3V3_S	3.3 V	I/O	Boot configuration pin 7 during reset SAI receive data 7 during runtime
BOOT_CFG[8]	A94	X_SAI1_TXD0 / BOOT_CFG[8]	VDD_3V3_S	3.3 V	I/O	Boot configuration pin 8 during reset SAI transmit data 0 during runtime
BOOT_CFG[9]	A95	X_SAI1_TXD1 / BOOT_CFG[9]	VDD_3V3_S	3.3 V	I/O	Boot configuration pin 9 during reset SAI transmit data 1 during runtime

Configuration Pin	SOM Connector Pin / phyBOARD-Polis Carrier Board Connector Pin	SOM Signal Name	SOM Voltage Domain	Signal Level	Signal Type	Description
BOOT_CFG[10]	A96	X_SAI1_TXD2 / BOOT_CFG[10]	VDD_3V3_S	3.3 V	I/O	Boot configuration pin 10 during reset SAI transmit data 2 during runtime
BOOT_CFG[11]	A97	X_SAI1_TXD3 / BOOT_CFG[11]	VDD_3V3_S	3.3 V	I/O	Boot configuration pin 11 during reset SAI transmit data 3 during runtime
BOOT_CFG[12]	A98	X_SAI1_TXD4 / BOOT_CFG[12]	VDD_3V3_S	3.3 V	I/O	Boot configuration pin 11 during reset SAI transmit data 4 during runtime
BOOT_CFG[13]	A99	X_SAI1_TXD5 / BOOT_CFG[13]	VDD_3V3_S	3.3 V	I/O	Boot configuration pin 13 during reset SAI transmit data 5 during runtime
BOOT_CFG[14]	A100	X_SAI1_TXD6 / BOOT_CFG[14]	VDD_3V3_S	3.3 V	I/O	Boot configuration pin 14 during reset SAI transmit data 6 during runtime

i.MX 8M Nano System Boot Settings

The i.MX 8M Nano uses a boot process different from the i.MX 8M Mini. Boot devices with fixed configuration may be selected through the use of 6 Boot Mode pins, 2 of which are shared with the i.MX 8M Mini. The phyCORE-i.MX 8M Nano is pre-configured with the default Boot Mode setting eMMC boot.

10 phyCORE-i.MX 8M Nano Possible Boot Configuration Settings

Device	BOOT_MODE5	BOOT_MODE4	BOOT_MODE3	BOOT_MODE2	BOOT_MODE1	BOOT_MODE0
QSPI (FlexSPI)	0	0	0	1	1	0
eMMC	0	0	0	0	1	0
SD-Card	0	0	0	0	1	1
Serial download	0	0	0	0	0	1
Fuse boot	0	0	0	0	0	0

System Memory

The phyCORE-i.MX 8M Mini provides four types of onboard memory:

- One bank LPDDR4 RAM: 2 GB LPDDR4 RAM (up to 4 GB)[3]
- eMMC: 8 GB (up to 32 GB)
- Quad SPI-NOR: 32 MB (up to 256 MB)[3]
- I²C-EEPROM: 4 kB[3]

The following sections detail each memory type used on the phyCORE-i.MX 8M Mini.

3. The maximum memory size listed is as of the printing of this manual. Please contact PHYTEC for more information about additional, or new module configurations available.

LPDDR4-RAM (U2)

The RAM memory of the phyCORE-i.MX 8M Mini is comprised of one 32-bit wide bank with two 16-bit wide LPDDR4-RAM chips in one integrated circuit. The chips are connected to the DDR interface called the DDR Controller (DDRC) of the i.MX 8M Mini microcontroller.

Typically, the LPDDR4-RAM initialization is performed by a boot loader or operating system following a power-on reset and must not be changed at a later point by any application code. When writing custom code independent of an operating system or boot loader, the RAM must be initialized by accessing the appropriate RAM configuration registers on the i.MX 8M Mini controller. Refer to the *NXP i.MX 8M Mini Reference Manual* for accessing and configuring these registers.

QUAD SPI-NOR (U7)

The Quad NOR flash memory at U7 is connected to the Flexible Serial Peripheral Interface A (FlexSPI A). The connected flash device uses the provided Chip Select 0 signal (QSPIA_SS0). The NOR flash device is powered by the 1.8 V supply voltage VDD_1V8. No further voltages are required to program the device.

As of the printing of this manual, these NOR flash devices generally have a life expectancy of at least 100,000 erase cycles per sector and a data retention rate of typically 20 years. Any parts that are footprint (TBGA-24 5x5) and functionally compatible may be used with the phyCORE-i.MX 8M Mini.

For more information about the NOR Flash, please refer to the *NXP i.MX 8M Mini Reference Manual.*

eMMC Flash Memory (U21)

The managed NAND (eMMC) flash device is powered by the supply voltages VDD_1V8 (1.8 V) and VDD_3V3_S (3.3 V). No further voltages are required for programming the device. The eMMC memory is connected to the SDIO3 interface of the i.MX 8M Mini. Any parts that are footprint (BGA153) and functionally compatible may be used with the phyCORE-i.MX 8M Mini.

For more information about the eMMC, please refer to the *NXP i.MX 8M Mini Reference Manual*.

I²C EEPROM (U13)

The phyCORE-i.MX 8M Mini is populated with a 4 kB I²C[4] EEPROM at U13. This memory can be used to store configuration data or other general-purpose data. This device is accessed through I²C port 1 of the i.MX 8M Mini. The control registers for I²C port 1 are mapped between addresses 0x021A 8000 and 0x021A BFFF. Please see the NXP i.MX 8M Mini Reference Manual for detailed information on the registers.

The three lower address bits are fixed to zero which means that the EEPROM can be accessed at I²C address 0x51.

4. See the manufacturer's datasheet for interfacing and operation.

EEPROM Write Control

The Write Control (WC) signal of the EEPROM is permanently fixed to GND over resistor R106, so the EEPROM is not always write-protected.

Serial Interfaces

The phyCORE-i.MX 8M Mini provides numerous dedicated serial interfaces, some of which are equipped with a transceiver to allow direct connection to external devices:

- 2x SDIO interfaces (4 and 8-Bit)
- 4x High-speed UART interfaces.
- 2x High-Speed USB OTG interfaces extended directly from the i.MX 8M Mini USB 2.0 PHY
- 1x 10/100/1000 Mbit Ethernet interface
- 4x independent I^2C interfaces
- 2x Serial Peripheral Interfaces (SPI), extending from the first and second SPI modules (eCSPI1 and eCSPI2) of the i.MX 8M Mini. A third interface can be implemented through the use of GPIOs. See *NXP i.MX 8M Mini Reference Manual* muxing options.
- 4x Serial Audio Interfaces (SAI), originating from the i.MX 8M Mini I^2S module.
- 1x PCI Express Gen. 2, extending directly from the i.MX 8M Mini PCIe PHY
- 1x MIPI CSI-2 interface with 4 data lanes and 1 clock lane
- 1x SPDIF interface

The following sections detail each of these serial interfaces.

SDIO Interfaces

The SDIO interfaces are part of the ultra Secured Digital Host Controller and can be used to connect external SD-Cards, eMMC, or any other device requiring an SDIO interface (examples include WiFI, I/O expansion).
The phyCORE-i.MX 8M Mini features two SDIO interfaces (4 and 8-Bit). On the phyCORE-i.MX 8M Mini, the interface signals extend from the controller's first and second Ultra Secured Digital Host Controller (uSDHC1/uSDHC2) to the phyCORE-Connector.

uSDHC2 provides dedicated card-detect, write-protect and power enable signals. For uSDHC2 to function a pull-up resistor (eg. 10k) from X_SD2_PWR_EN to the SOM input voltage VDD_3V3 is required. This enables the uSDHC2 interface by powering the corresponding domain in the i.MX 8M Mini. This feature may be used to limit access to the CPU through an openly available SD-Card slot, or for similar purposes.

uSDHC1 card-detect and write-protect functions may be implemented by using GPIOs of the i.MX 8M Mini. Refer to the *NXP i.MX 8M Mini Reference Manual.* For more information about SD-Cards, please refer to the manufacturer's user manual.

The tables below show the locations of the various interface signals on the phyCORE-Connector. The Ultra Secure Digital Host Controller is fully compatible with SD/SDIO 3.0 (200MHz SDR signaling for up to 100 MB/s) and MMC 5.1 (HS400 DDR for up to 400 MB/s). uSDHC1 and uSDHC3 both provide 8-Bit interfaces, and uSDHC2 provides a 4-Bit interface. Refer to the *NXP i.MX 8M Mini Reference Manual* for more information.

11 SDIO1 Interface Signal Locations

SOM Connector Pin / phyBOARD-Polis Carrier Board Connector Pin	SOM Signal Name	SOM Voltage Domain	Signal Level	Signal Type	Description
A9	X_SD1_DATA1	NVCC_SD1	3,3 V	I/O	SD1 data 1 input and output
A10	X_SD1_DATA0	NVCC_SD1	3,3 V	I/O	SD1 data 0 input and output
A11	X_SD1_DATA7	NVCC_SD1	3,3 V	I/O	SD1 data 7 input and output
A12	X_SD1_DATA6	NVCC_SD1	3,3 V	I/O	SD1 data 6 input and output
A13	X_SD1_CLK	NVCC_SD1	3,3 V	O	SD1 clock output
A14	X_SD1_CMD	NVCC_SD1	3,3 V	O	SD1 command output
A15	X_SD1_DATA5	NVCC_SD1	3,3 V	I/O	SD1 data 5 input and output
A16	X_SD1_DATA4	NVCC_SD1	3,3 V	I/O	SD1 data 4 input and output
A17	X_SD1_DATA3	NVCC_SD1	3,3 V	I/O	SD1 data 3 input and output
A18	X_SD1_DATA2	NVCC_SD1	3,3 V	I/O	SD1 data 2 input and output

SOM Connector Pin / phyBOARD-Polis Carrier Board Connector Pin	SOM Signal Name	SOM Voltage Domain	Signal Level	Signal Type	Description
A19	X_SD1_RESET_B	NVCC_SD1	3,3 V	O	SD1 reset output
A20	X_SD1_STROBE	NVCC_SD1	3,3 V	O	SD1 strobe output

12 SDIO2 Interface Signal Locations

SOM Connector Pin / phyBOARD-Polis Carrier Board Connector Pin	SOM Signal Name	SOM Voltage Domain	Signal Level	Signal Type	Description
C18	X_SD2_RESET_B	NVCC_SD2	1,8 V/ 3,3 V	O	SD2 reset output
C19	X_SD2_WP	NVCC_SD2	1,8 V/ 3,3 V	O	SD2 write-protect output
C20	X_SD2_CD_B	NVCC_SD2	1,8 V/ 3,3 V	O	SD2 card detect
C21	X_SD2_DATA1	NVCC_SD2	1,8 V/ 3,3 V	I/O	SD2 data 1 input and output
C22	X_SD2_DATA0	NVCC_SD2	1,8 V/ 3,3 V	I/O	SD2 data 0 input and output
C23	X_SD2_CLK	NVCC_SD2	1,8 V/ 3,3 V	O	SD2 clock output
C24	X_SD2_CMD	NVCC_SD2	1,8 V/ 3,3 V	O	SD2 command output

SOM Connector Pin / phyBOARD-Polis Carrier Board Connector Pin	SOM Signal Name	SOM Voltage Domain	Signal Level	Signal Type	Description
C25	X_SD2_DATA3	NVCC_SD2	1,8 V/ 3,3 V	I/O	SD2 data 3 input and output
C26	X_SD2_DATA2	NVCC_SD2	1,8 V/ 3,3 V	I/O	SD2 data 2 input and output
E20	X_SD2_PWR_EN	VDD_3V3	3,3 V	I	SD2 power supply enable

Universal Asynchronous Interface

The phyCORE-i.MX 8M Mini provides four high-speed universal asynchronous interfaces. Hardware flow control (RTS and CTS signals) may be implemented through the use of additional GPIO signals. See muxing options in *NXP i.MX 8M Mini Reference Manual* for more information. Location of the signals on the phyCORE-Connector:

13 UART Signal Locations

SOM Connector Pin / phyBOARD-Polis Carrier Board Connector Pin	SOM Signal Name	SOM Voltage Domain	Signal Level	Signal Type	Description
C27	X_UART1_RXD	VDD_3V3_S	3,3 V	I/O	UART1 receive data
C28	X_UART1_TXD	VDD_3V3_S	3,3 V	I/O	UART1 transmit data
C29	X_UART2_RXD	VDD_3V3_S	3,3 V	I/O	UART2 receive data
C30	X_UART2_TXD	VDD_3V3_S	3,3 V	I/O	UART2 transmit data

SOM Connector Pin / phyBOARD-Polis Carrier Board Connector Pin	SOM Signal Name	SOM Voltage Domain	Signal Level	Signal Type	Description
C31	X_UART3_RXD	VDD_3V3_S	3,3 V	I/O	UART3 receive data
C32	X_UART3_TXD	VDD_3V3_S	3,3 V	I/O	UART3 transmit data
C33	X_UART4_RXD	VDD_3V3_S	3,3 V	I/O	UART4 receive data
C34	X_UART4_TXD	VDD_3V3_S	3,3 V	I/O	UART4 transmit data

USB OTG Interfaces

The phyCORE-i.MX 8M Mini provides two high-speed USB OTG interfaces, which use the i.MX 8M Mini's embedded High-Speed USB 2.0 PHY.

For the use of various USB functionalities, only an external USB Standard-A (for USB host), USB Standard-B (for USB devices), or USB Mini-AB (for USB OTG) connector is needed. The applicable interface signals (DN, DP, ID, and VBUS) are located on the phyCORE-Connector X1. The locations of the USB OTG interface signals on the phyCORE-Connector X1 can be found in the tables below.

If overcurrent and power-enable signals are needed for the USB host interface, the functionality can be easily implemented through the use of GPIOs.

Errata information

Existing issues may be solved by referring to the following chapters in *NXP Mask Set Errata for Mask 0N87W, Rev. 1, 09/2021*:

- ERR050101: USB: Endpoint conflict issue in device mode

14 USB1 OTG Signal Locations

SOM Connector Pin / phyBOARD-Polis Carrier Board Connector Pin	SOM Signal Name	SOM Voltage Domain	Signal Level	Signal Type	Description
A21	X_USB1_DN	VDD_3V3_S	DIFF	I/O	Negative USB1 data signal
A22	X_USB1_DP	VDD_3V3_S	DIFF	I/O	Positive USB1 data signal
A23	X_USB1_ID	VDD_3V3_S	3,3 V	I	USB1 OTG identification pin
E17	USB1_VBUS	VDD_3V3_S	1,4 V	I	USB1 voltage bus detection

15 USB2 OTG Signal Locations

SOM Connector Pin / phyBOARD-Polis Carrier Board Connector Pin	SOM Signal Name	SOM Voltage Domain	Signal Level	Signal Type	Description
A25	X_USB2_DN	VDD_3V3_S	DIFF	I/O	Negative USB2 data signal
A26	X_USB2_DP	VDD_3V3_S	DIFF	I/O	Positive USB2 data signal
A24	X_USB2_ID	VDD_3V3_S	3,3 V	I	USB2 OTG identification pin
E18	USB2_VBUS	VDD_3V3_S	Typ. 1,4 V	I	USB2 voltage bus detection

Ethernet Interface

Connection of the phyCORE-i.MX 8M Mini to the World Wide Web or a local area network (LAN) is possible using the onboard GbE PHY at U4. It is connected to the RGMII interface of the i.MX 8M Mini. The PHY operates with a data transmission speed of 10, 100, or 1000 Mbit/s. Alternatively, the RGMII interface which is available on the phyCORE-Connector can be used to connect an external PHY. In this case, the onboard GbE PHY (U4) must not be populated (see RGMII Interface).

Ethernet PHY (U4)

With an Ethernet PHY mounted at U4, the phyCORE-i.MX 8M Mini has been designed for use in 10/100/1000Base-T networks. The 10/100/1000Base-T interface with its LED signals extends to the phyCORE-i.MX 8M Mini Connector X1.

16 Ethernet Signal Locations

SOM Connector Pin / phyBOARD-Polis Carrier Board Connector Pin	SOM Signal Name	SOM Voltage Domain	Signal Level	Signal Type	Description
C7	X_ETH0_LED0_LINK	VCC_3V3	Typ. 3,3 V	OD	Ethernet link LED signal
C8	X_ETH0_LED2_ACT	VCC_3V3	Typ. 3,3 V	OD	Ethernet activity LED signal
A103	X_ETH_A_P	VCC_ENET_2V5	DIFF	ETH_I/O	Positive Ethernet A signal
A104	X_ETH_A_N	VCC_ENET_2V5	DIFF	ETH_I/O	Negative Ethernet A signal
A1	X_ETH_B_P	VCC_ENET_2V5	DIFF	ETH_I/O	Positive Ethernet B signal
A2	X_ETH_B_N	VCC_ENET_2V5	DIFF	ETH_I/O	Negative Ethernet B signal

SOM Connector Pin / phyBOARD-Polis Carrier Board Connector Pin	SOM Signal Name	SOM Voltage Domain	Signal Level	Signal Type	Description
A3	X_ETH_C_P	VCC_ENET_2V5	DIFF	ETH_I/O	Positive Ethernet C signal
A4	X_ETH_C_N	VCC_ENET_2V5	DIFF	ETH_I/O	Negative Ethernet C signal
A5	X_ETH_D_P	VCC_ENET_2V5	DIFF	ETH_I/O	Positive Ethernet D signal
A6	X_ETH_D_N	VCC_ENET_2V5	DIFF	ETH_I/O	Negative Ethernet D signal

The onboard GbE PHY supports HP Auto-MDIX technology, eliminating the need for a direct-connect LAN or a cross-over patch cable. It detects the TX and RX pins of the connected device and automatically configures the PHY TX and RX pins accordingly. The Ethernet PHY also features an auto-negotiation to automatically determine the best speed and duplex mode.

The Ethernet PHY is connected to the RGMII interface of the i.MX 8M Mini. Please refer to the *NXP i.MX 8M Mini Reference Manual* for more information about this interface.

In order to connect the module to an existing 10/100/1000Base-T network, some external circuitry is required. The required termination resistors on the analog signals (ETH0_A±, ETH0_B±, ETH0_C±, ETH0_D±) are integrated into the chip, so there is no need to connect external termination resistors to these signals.

Connection to external Ethernet magnetics should be done using very short signal traces. The A+/A-, B+/B-, C+/C-, and D+/D- signals should be routed as 100 Ohm differential pairs. The same applies to the signal lines after the transformer circuit. The carrier board layout should avoid any other signal lines crossing the Ethernet signals.

Ethernet PHY Reset

The Ethernet PHY at U4 can be reset via software. The reset input of the Ethernet PHY is connected to the Power-On Reset (POR) signal of the module and to the GPIO *RESET_ETHPHY* of the i.MX 8M Mini.

MAC Address

In a computer network such as a local area network (LAN), the MAC (Media Access Control) address is a unique computer hardware number. For a connection to the internet, a table is used to convert the assigned IP number to the hardware's MAC address. In order to guarantee that the MAC address is unique, all addresses are managed in a

central location. PHYTEC has acquired a pool of MAC addresses. The MAC address of the phyCORE-i.MX 8M Mini is located on the bar code sticker attached to the module. This number is a 12-digit HEX value.

RGMII Interface

In order to use an external Ethernet PHY instead of the onboard GbE PHY at U8, the RGMII interface (ENET) of the i.MX 8M Mini is brought out at phyCORE-i.MX 8M Mini Connector X1.

Errata information

Existing issues may be solved by referring to the following chapters in *NXP Mask Set Errata for Mask 0N87W, Rev. 1, 09/2021*:

- ERR011437: IOMUX: The read data is always zero when the ODE bit of ENET PHY IOs is set

Warning

The GbE PHY (U4) **must not** be populated on the module if the RGMII interface is used.

17 RGMII Interface Signal Locations

SOM Connector Pin / phyBOARD-Polis Carrier Board Connector Pin	SOM Signal Name	SOM Voltage Domain	Signal Level	Signal Type	Description
C1	X_ENET_RGMII_RX_CTL	VDDA_1V8	1,8 V	I	RGMII receive control signal
C2	X_ENET_RGMII_RXC	VDDA_1V8	1,8 V	I	RGMII receive clock signal
C3	X_ENET_RGMII_RD0	VDDA_1V8	1,8 V	I	RGMII receive data signal 0
C4	X_ENET_RGMII_RD1	VDDA_1V8	1,8 V	I	RGMII receive data signal 1
C5	X_ENET_RGMII_RD2	VDDA_1V8	1,8 V	I	RGMII receive data signal 2
C6	X_ENET_RGMII_RD3	VDDA_1V8	1,8 V	I	RGMII receive data signal 3

SOM Connector Pin / phyBOARD-Polis Carrier Board Connector Pin	SOM Signal Name	SOM Voltage Domain	Signal Level	Signal Type	Description
C65	X_ENET_MDIO	VDDA_1V8	1,8 V	O	RGMII Management Data Input Output
C66	X_ENET_MDC	VDDA_1V8	1,8 V	O	RGMII Management Data Clock
C67	X_ENET_RGMII_TX_CTL	VDDA_1V8	1,8 V	O	RGMII transmit control signal
C68	X_ENET_RGMII_TXC	VDDA_1V8	1,8 V	O	RGMII transmit clock signal
C69	X_ENET_RGMII_TD0	VDDA_1V8	1,8 V	O	RGMII transmit data signal 0
C70	X_ENET_RGMII_TD1	VDDA_1V8	1,8 V	O	RGMII transmit data signal 1
C71	X_ENET_RGMII_TD2	VDDA_1V8	1,8 V	O	RGMII transmit data signal 2
C72	X_ENET_RGMII_TD3	VDDA_1V8	1,8 V	O	RGMII transmit data signal 3

SPI Interfaces

The Serial Peripheral Interface (SPI) interface is a four-wire, bidirectional serial bus that provides a simple and efficient method for data exchange among devices. The phyCORE provides two SPI interfaces on the phyCORE-i.MX 8M Mini Connector X1.

Each SPI interface provides one chip-select signal. The enhanced Configurable SPI (eCSPI) of the i.MX 8M Mini has three separate modules (eCSPI1, eCSPI2, and eCSPI3) which support data rates of up to 20 Mbit/s. The interface signals of the first and second modules (eCSPI1, eCSPI2) are made available on the phyCORE-Connector. The third SPI module can be made available through the i.MX 8M Mini pin muxing options. Refer to the *NXP i.MX 8M Mini Reference Manual* for more detailed information. All modules are master/slave configurable. The following tables list the SPI signals on the phyCORE-i.MX 8M Mini Connector X1.

Errata information

Existing issues may be solved by referring to the following chapters in *NXP Mask Set Errata for Mask 0N87W, Rev. 1, 09/2021*:

- ERR009535: ECSPI: Burst completion by SS signal in slave mode is not functional
- ERR009606: ECSPI: In master mode, burst lengths of 32n+1 will transmit incorrect data
- ERR009165: ECSPI: TXFIFO empty flag glitch can cause the current FIFO transfer to be sent twice

18 SPI1 Interface Signal Locations

SOM Connector Pin / phyBOARD-Polis Carrier Board Connector Pin	SOM Signal Name	SOM Voltage Domain	Signal Level	Signal Type	Description
A53	X_ECSPI1_SS0	VDD_3V3_S	3,3 V	O	SPI1 chip select signal
A54	X_ECSPI1_MOSI	VDD_3V3_S	3,3 V	O	SPI1 master out, slave in signal
A55	X_ECSPI1_MISO	VDD_3V3_S	3,3 V	I	SPI1 master in, slave out signal
A56	X_ECSPI1_SCLK	VDD_3V3_S	3,3 V	O	SPI1 serial clock output signal

19 SPI2 Interface Signal Locations

SOM Connector Pin / phyBOARD-Polis Carrier Board Connector Pin	SOM Signal Name	SOM Voltage Domain	Signal Level	Signal Type	Description
A57	X_ECSPI2_SS0	VDD_3V3_S	3,3 V	O	SPI2 chip select signal
A58	X_ECSPI2_MOSI	VDD_3V3_S	3,3 V	O	SPI2 master out, slave in signal

SOM Connector Pin / phyBOARD-Polis Carrier Board Connector Pin	SOM Signal Name	SOM Voltage Domain	Signal Level	Signal Type	Description
A59	X_ECSPI2_MISO	VDD_3V3_S	3,3 V	I	SPI2 master in, slave out signal
A60	X_ECSPI2_SCLK	VDD_3V3_S	3,3 V	O	SPI2 serial clock output signal

I²C Interface

The Inter-Integrated Circuit (I²C) interface is a two-wire, bidirectional serial bus that provides a simple and efficient method for data exchange among devices. The i.MX 8M Mini contains four identical, independent Multimaster fast-mode I²C modules. The interface of three modules is available at the phyCORE-Connector. The first I²C module (I2C1) connects to the onboard EEPROM at U13 (I²C EEPROM), the PMIC at U3 (Power Management IC), the Real-Time Clock at U12, and the MIPI to LVDS converter at U5 LVDS (FlatLink). The MIPI to LVDS converter connects to the I2C1 interface through the level shifter U22. The voltage domain in this part of the bus is 1,8 V.

Tip

To ensure the proper functioning of the I²C interface, external pull resistors matching the load at the interface must be connected. There are no pull-up resistors mounted on the module. For detailed information on the voltage levels for the pull-up resistors, please refer to the *i.MX 8M Mini datasheet.*

Errata information

Existing issues may be solved by referring to the following chapters in *NXP Mask Set Errata for Mask 0N87W, Rev. 1, 09/2021*:

- ERR007805: I2C: When the I2C clock speed is configured for 400 kHz, the SCL low period violates the I2C spec of 1.3 uS min
- ERR050045: IOMUX: Setting ODE control bit of I2C IOs causes malfunction

The following tables list the I²C ports on the phyCORE-Connector, separated by interface:

20 I2C2 Interface Signal Locations

SOM Connector Pin / phyBOARD-Polis Carrier Board Connector Pin	SOM Signal Name	SOM Voltage Domain	Signal Level	Signal Type	Description
C39	X_I2C2_SCL	VDD_3V3_S	3,3 V	OD	I2C2 serial clock output signal
C40	X_I2C2_SDA	VDD_3V3_S	3,3 V	OD-BI	I2C2 serial data input-output

21 I2C3 Interface Signal Locations

SOM Connector Pin / phyBOARD-Polis Carrier Board Connector Pin	SOM Signal Name	SOM Voltage Domain	Signal Level	Signal Type	Description
A61	X_I2C3_SCL	VDD_3V3_S	3,3 V	OD	I2C3 serial clock output signal
A62	X_I2C3_SDA	VDD_3V3_S	3,3 V	OD-BI	I2C3 serial data input-output

22 I2C4 Interface Signal Locations

SOM Connector Pin / phyBOARD-Polis Carrier Board Connector Pin	SOM Signal Name	SOM Voltage Domain	Signal Level	Signal Type	Description
A63	X_I2C4_SCL	VDD_3V3_S	3,3 V	OD	I2C4 serial clock output signal
A64	X_I2C4_SDA	VDD_3V3_S	3,3 V	OD-BI	I2C4 serial data input-output

Onboard I2C Bus

The first I^2C module (I2C1) connects to the onboard EEPROM at U13 and the PMIC at U3. The following table shows the addresses of all I2C1 devices on the phyCORE-i.MX 8M Mini:

23 I2C1 Onboard Bus Addresses

Device	Address
EEPROM (section EEPROM)	0x51 0x59 (factory use only)
PMIC (section PMIC)	0x08
RTC	0x52
MIPI to LVDS converter	0x2D

Synchronous Audio Interface (SAI)

The phyCORE-i.MX 8M Mini features a Synchronous Audio Interface that supports full-duplex serial interfaces with frame synchronization such as I2S, AC97, and TDM. The interface is divided into four sub-interfaces: SAI1, SAI2, SAI3, and SAI5. All signals are routed directly to the phyCORE-i.MX 8M Mini Connector X1. All signals are part of the VDD_3V3_S voltage domain.

SAI1 provides 8-bit transmit and 8-bit receive functionality with receive, transmit, and master clock output. Frame synchronization is available for receive and transmit operations. The tables below show the signal locations for each SAI interface.

Errata information

Existing issues may be solved by referring to the following chapters in *NXP Mask Set Errata for Mask 0N87W, Rev. 1, 09/2021*:

- ERR050542: SAI: The Bit Count Timestamp Register (TBCTR, RBCTR) may return a live rather than latched Timestamp

24 SAI1 Signal Locations

SOM Connector Pin / phyBOARD-Polis Carrier Board Connector Pin	SOM Signal Name	SOM Voltage Domain	Signal Level	Signal Type	Description
A81	X_SAI1_RXD0/ BOOT_CFG[0]	VDD_3V3_S	3,3 V	I/O	SAI1 receive data 0 signal
A82	X_SAI1_RXD1/ BOOT_CFG[1]	VDD_3V3_S	3,3 V	I/O	SAI1 receive data 1 signal
A83	X_SAI1_RXFS	VDD_3V3_S	3,3 V	I/O	SAI1 receive frame synchronization signal
A84	X_SAI1_RXC	VDD_3V3_S	3,3 V	I/O	SAI1 receive bit clock signal
A85	X_SAI1_RXD2/ BOOT_CFG[2]	VDD_3V3_S	3,3 V	I/O	SAI1 receive data 2 signal
A86	X_SAI1_RXD3/ BOOT_CFG[3]	VDD_3V3_S	3,3 V	I/O	SAI1 receive data 3 signal
A87	X_SAI1_RXD4/ BOOT_CFG[4]	VDD_3V3_S	3,3 V	I/O	SAI1 receive data 4 signal
A88	X_SAI1_RXD5/ BOOT_CFG[5]	VDD_3V3_S	3,3 V	I/O	SAI1 receive data 5 signal
A89	X_SAI1_RXD6/ BOOT_CFG[6]	VDD_3V3_S	3,3 V	I/O	SAI1 receive data 6 signal
A90	X_SAI1_RXD7/ BOOT_CFG[7]	VDD_3V3_S	3,3 V	I/O	SAI1 receive data 7 signal
A91	X_SAI1_MCLK	VDD_3V3_S	3,3 V	I/O	SAI1 master clock signal

SOM Connector Pin / phyBOARD-Polis Carrier Board Connector Pin	SOM Signal Name	SOM Voltage Domain	Signal Level	Signal Type	Description
A92	X_SAI1_TXFS	VDD_3V3_S	3,3 V	I/O	SAI1 transmit frame synchronization signal
A93	X_SAI1_TXC	VDD_3V3_S	3,3 V	I/O	SAI1 transmit bit clock signal
A94	X_SAI1_TXD0/ BOOT_CFG[8]	VDD_3V3_S	3,3 V	I/O	SAI1 transmit data 0 signal
A95	X_SAI1_TXD1/ BOOT_CFG[9]	VDD_3V3_S	3,3 V	I/O	SAI1 transmit data 1 signal
A96	X_SAI1_TXD2/ BOOT_CFG[10]	VDD_3V3_S	3,3 V	I/O	SAI1 transmit data 2 signal
A97	X_SAI1_TXD3/ BOOT_CFG[11]	VDD_3V3_S	3,3 V	I/O	SAI1 transmit data 3 signal
A98	X_SAI1_TXD4/ BOOT_CFG[12]	VDD_3V3_S	3,3 V	I/O	SAI1 transmit data 4 signal
A99	X_SAI1_TXD5/ BOOT_CFG[13]	VDD_3V3_S	3,3 V	I/O	SAI1 transmit data 5 signal
A100	X_SAI1_TXD6/ BOOT_CFG[14]	VDD_3V3_S	3,3 V	I/O	SAI1 transmit data 6 signal
A101	X_SAI1_TXD7	VDD_3V3_S	3,3 V	I/O	SAI1 transmit data 7 signal

SAI2 provides 1-bit transmit and 1-bit receive functionality with receive, transmit, and master clock output. Frame synchronization is available for receive and transmit operations.

25 SAI2 Signal Locations

SOM Connector Pin / phyBOARD-Polis Carrier Board Connector Pin	SOM Signal Name	SOM Voltage Domain	Signal Level	Signal Type	Description
C58	X_SAI2_TXFS/ UART1_CTS_B	VDD_3V3_S	3,3 V	I/O	SAI2 transmit frame synchronization signal
C59	X_SAI2_MCLK	VDD_3V3_S	3,3 V	I/O	SAI2 master clock signal
C60	X_SAI2_RXD0/ UART1_RTS_B	VDD_3V3_S	3,3 V	I/O	SAI2 receive data 0 signal
C61	X_SAI2_TXC	VDD_3V3_S	3,3 V	I/O	SAI2 transmit bit clock signal
C62	X_SAI2_TXD0	VDD_3V3_S	3,3 V	I/O	SAI2 transmit data 0 signal
C63	X_SAI2_RXC/ UART1_RX	VDD_3V3_S	3,3 V	I/O	SAI2 receive bit clock signal
C64	X_SAI2_RXFS/ UART1_TX	VDD_3V3_S	3,3 V	I/O	SAI2 receive frame synchronization signal

SAI3 provides 1-bit transmit and 1-bit receive functionality with receive, transmit, and master clock output. Frame synchronization is available for receive and transmit operations.

26 SAI3 Signal Locations

SOM Connector Pin / phyBOARD-Polis Carrier Board Connector Pin	SOM Signal Name	SOM Voltage Domain	Signal Level	Signal Type	Description
A65	X_SAI3_TXFS/ UART2_RX	VDD_3V3_S	3,3 V	I/O	SAI3 transmit frame synchronization signal
A66	X_SAI3_MCLK	VDD_3V3_S	3,3 V	I/O	SAI3 master clock signal
A67	X_SAI3_TXD	VDD_3V3_S	3,3 V	I/O	SAI3 transmit data signal
A68	X_SAI3_RXD/ UART2_RTS_B	VDD_3V3_S	3,3 V	I/O	SAI3 receive data signal
A69	X_SAI3_TXC/ UART2_TX	VDD_3V3_S	3,3 V	I/O	SAI3 transmit bit clock signal
A70	X_SAI3_RXC/ UART2_CTS_B	VDD_3V3_S	3,3 V	I/O	SAI3 receive bit clock signal
A71	X_SAI3_RXFS	VDD_3V3_S	3,3 V	I/O	SAI3 receive frame synchronization signal

SAI5 provides 4-bit receive functionality with receive and master clock output. Frame synchronization is available for receive operations.

27 SAI5 Signal Locations

SOM Connector Pin / phyBOARD-Polis Carrier Board Connector Pin	SOM Signal Name	SOM Voltage Domain	Signal Level	Signal Type	Description
C51	X_SAI5_RXD3	VDD_3V3_S	3,3 V	I/O	SAI5 receive data 3 signal
C52	X_SAI5_RXD2	VDD_3V3_S	3,3 V	I/O	SAI5 receive data 2signal
C53	X_SAI5_RXD1	VDD_3V3_S	3,3 V	I/O	SAI5 receive data 1 signal
C54	X_SAI5_RXD0	VDD_3V3_S	3,3 V	I/O	SAI5 receive data 0 signal
C55	X_SAI5_MCLK	VDD_3V3_S	3,3 V	I/O	SAI5 master clock signal
C56	X_SAI5_RXC	VDD_3V3_S	3,3 V	I/O	SAI5 receive bit clock signal
C57	X_SAI5_RXFS	VDD_3V3_S	3,3 V	I/O	SAI5 receive frame synchronization signal

PCI Express Interface

The 1-lane PCI Express interface of the phyCORE-i.MX 8M Mini provides PCIe Gen. 2.0 functionality which supports 5 Gbit/s operations. Furthermore, the interface is fully backward compatible with the 2.5 Gbit/s Gen. 1.1 specification. Additional control signals which might be required (e.g. “present” and “wake”) can be implemented via the use of GPIOs. Please refer to the schematic of a suitable PHYTEC carrier board (e.g. phyBOARD-Polis) for a circuit example. The table below show the signal location for the PCIe interface.

Errata information

Existing issues may be solved by referring to the following chapters in *NXP Mask Set Errata for Mask 0N87W, Rev. 1, 09/2021*:

- ERR011193: PCIE: EP, PM_PME: L1 Exit Does Not Occur when PME Service Timeout Mechanism Expires

28 PCIe Interface Signal Locations

SOM Connector Pin / phyBOARD-Polis Carrier Board Connector Pin	SOM Signal Name	SOM Voltage Domain	Signal Level	Signal Type	Description
A27	X_PCIe_CLK_N	VDD_1V8	DIFF	O	PCIe negative clock signal
A28	X_PCIe_CLK_P	VDD_1V8	DIFF	O	PCIe positive clock signal
A29	X_PCIe_TXN_N	VDD_1V8	DIFF	O	PCIe negative transmit signal
A30	X_PCIe_TXN_P	VDD_1V8	DIFF	O	PCIe positive transmit signal
A31	X_PCIe_RXN_N	VDD_1V8	DIFF	I	PCIe negative receive signal
A32	X_PCIe_RXN_P	VDD_1V8	DIFF	I	PCIe positive receive signal

General Purpose I/Os

The following table lists all pins not used by any of the other interfaces described explicitly in this manual and which, therefore, can be used as GPIO without harming other features of the phyCORE-i.MX 8M Mini. In addition, most pins directly routed to the phyCORE-i.MX M Mini Connector X1 can be configured as GPIO due to the multiplexing functionality of the i.MX 8M Mini.

For more details on the possible GPIO settings, see the *NXP i.MX 8M Mini Reference Manual.*

29 GPIO Pin Locations

SOM Connector Pin / phyBOARD-Polis Carrier Board Connector Pin	SOM Signal Name	SOM Voltage Domain	Signal Level	Signal Type	Description
C36	X_PWM1/ GPIO1_IO01	VDD_3V3_S	3,3 V	I/O	GPIO01 00 with PWM ability
C49	X_GPIO1_IO08/ ETH_1588_EVENT_IN	VDD_3V3_S	3,3 V	I/O	GPIO01 08, also useable for IEEE 1588 protocol event out
C50	X_GPIO1_IO09/ ETH_1588_EVENT_OUT	VDD_3V3_S	3,3 V	I/O	GPIO01 09, also useable for IEEE 1588 protocol event in
C44	X_GPIO1_IO12	VDD_3V3_S	3,3 V	I/O	GPIO01 12
A80	X_PWM2/ GPIO1_IO13	VDD_3V3_S	3,3 V	I/O	GPIO01 13 with PWM ability
C46	X_PWM3/ GPIO1_IO14	VDD_3V3_S	3,3 V	I/O	GPIO01 14 with PWM ability
C45	X_PWM4/ GPIO1_IO15	VDD_3V3_S	3,3 V	I/O	GPIO01 15 with PWM ability

JTAG Interface

The phyCORE-i.MX 8M Mini is equipped with a JTAG interface for downloading program code into the external flash, internal controller RAM, or for any debugging programs that are executed. Location of the JTAG pins on the phyCORE-i.MX 8M Mini Connector X1:

30 JTAG Interface Signal Locations

SOM Connector Pin / phyBOARD-Polis Carrier Board Connector Pin	SOM Signal Name	SOM Voltage Domain	Signal Level	Signal Type	Description
C9	X_JTAG_TCK	VDD_3V3_S	3,3 V	I	JTAG clock signal
C10	X_JTAG_TMS	VDD_3V3_S	3,3 V	I	JTAG test mode select signal
C11	X_JTAG_TDO	VDD_3V3_S	3,3 V	O	JTAG data out signal
C12	X_JTAG_TDI	VDD_3V3_S	3,3 V	I	JTAG data in signal
C13	X_JTAG_MOD	VDD_3V3_S	3,3 V	I	JTAG mode signal
C14	X_JTAG_TRST_B	VDD_3V3_S	3,3 V	I	JTAG tap reset signal

Display Interfaces

In the industrial market, LVDS is the default display with the best long-time availability. MIPI is normally used for the consumer market. For this reason, PHYTEC has added a MIPI to LVDS converter as part of the SOM design. This allows an LVDS display to be used in industrial applications. Alternatively, phyCORE-i.MX 8M MINI can be ordered without the converter and a jumper in its place so that a MIPI display can be used.

Warning

It is not possible to use both an LVDS and MIPI display at the same time. Only one type of display can be used at any given time.

LVDS (Flatlink)

The LVDS interface of the phyCORE-i.MX 8M Mini, using an optional MIPI to LVDS converter, is converted from the i.MX 8M Mini's MIPI-DSI2 interface. The converter supports resolutions of up to 1920x1200 (WUXGA) at 60 frames per second with 24 bpp and reduced blanking. It is also suitable for resolutions of 1366x768 with 60 frames per second and 1280x800 at 60 frames per second, both 18 and 24 bpp. The LVDS interface is available only when U5 is mounted. Please refer to the *Texas Instruments SN65DSI83 datasheet* for more information.

Location of the LVDS signals on the phyCORE-i.MX 8M Mini Connector:

31 LVDS Interface Signal Locations

SOM Connector Pin / phyBOARD-Polis Carrier Board Connector Pin	SOM Signal Name	SOM Voltage Domain	Signal Level	Signal Type	Description
A43	X_FLATLINK_D0_N/ MIPI_DSI_DATA0_N	VDD_1V8	DIFF	O	Negative LVDS data 0 signal
A44	X_FLATLINK_D0_P/ MIPI_DSI_DATA0_P	VDD_1V8	DIFF	O	Positive LVDS data 0 signal
A45	X_FLATLINK_D1_N/ MIPI_DSI_DATA1_N	VDD_1V8	DIFF	O	Negative LVDS data 1 signal

SOM Connector Pin / phyBOARD-Polis Carrier Board Connector Pin	SOM Signal Name	SOM Voltage Domain	Signal Level	Signal Type	Description
A46	X_FLATLINK_D1_P/ MIPI_DSI_DATA1_P	VDD_1V8	DIFF	O	Positive LVDS data 1 signal
A47	X_FLATLINK_D2_N/ MIPI_DSI_CLK_N	VDD_1V8	DIFF	O	Negative LVDS data 2 signal
A48	X_FLATLINK_D2_P/ MIPI_DSI_CLK_P	VDD_1V8	DIFF	O	Positive LVDS data 2 signal
A49	X_FLATLINK_D3_N/ MIPI_DSI_DATA2_N	VDD_1V8	DIFF	O	Negative LVDS data 3 signal
A50	X_FLATLINK_D3_P/ MIPI_DSI_DATA2_P	VDD_1V8	DIFF	O	Positive LVDS data 3 signal
A51	X_FLATLINK_CLK_N/ MIPI_DSI_DATA3_N	VDD_1V8	DIFF	O	Negative LVDS clock signal
A52	X_FLATLINK_CLK_P/ MIPI_DSI_DATA3_P	VDD_1V8	DIFF	O	Positive LVDS clock signal

MIPI-Display Serial Interface 2 (MIPI-DSI2)

The i.MX 8M Mini's MIPI-DSI2 interface provides resolutions of up to 1920x1080 at 60 frames per second. It uses four data channels and one clock channel. The MIPI-DSI2 interface is only available if the MIPI to LVDS converter U5 is not mounted. The interface provides a maximum bit rate of 1,5 Gbit/s.

32 MIPI DSI-2 Interface Signal Locations

SOM Connector Pin / phyBOARD-Polis Carrier Board Connector Pin	SOM Signal Name	SOM Voltage Domain	Signal Level	Signal Type	Description
A43	X_FLATLINK_D0_N/ MIPI_DSI_DATA0_N	VDD_1V8	DIFF	O	Negative MIPI-DSI data 0 signal
A44	X_FLATLINK_D0_P/ MIPI_DSI_DATA0_P	VDD_1V8	DIFF	O	Positive MIPI-DSI data 0 signal
A45	X_FLATLINK_D1_N/ MIPI_DSI_DATA1_N	VDD_1V8	DIFF	O	Negative MIPI-DSI data 1 signal
A46	X_FLATLINK_D1_P/ MIPI_DSI_DATA1_P	VDD_1V8	DIFF	O	Positive MIPI-DSI data 1 signal
A47	X_FLATLINK_D2_N/ MIPI_DSI_CLK_N	VDD_1V8	DIFF	O	Negative MIPI-DSI clock signal
A48	X_FLATLINK_D2_P/ MIPI_DSI_CLK_P	VDD_1V8	DIFF	O	Positive MIPI-DSI clock signal

SOM Connector Pin / phyBOARD-Polis Carrier Board Connector Pin	SOM Signal Name	SOM Voltage Domain	Signal Level	Signal Type	Description
A49	X_FLATLINK_D3_N/ MIPI_DSI_DATA2_N	VDD_1V8	DIFF	O	Negative MIPI-DSI data 2 signal
A50	X_FLATLINK_D3_P/ MIPI_DSI_DATA2_P	VDD_1V8	DIFF	O	Positive MIPI-DSI data 2 signal
A51	X_FLATLINK_CLK_N/ MIPI_DSI_DATA3_N	VDD_1V8	DIFF	O	Negative MIPI-DSI data 3 signal
A52	X_FLATLINK_CLK_P/ MIPI_DSI_DATA3_P	VDD_1V8	DIFF	O	Positive MIPI-DSI data 3 signal

MIPI CSI-2 Camera Interface

The phyCORE-i.MX 8M Mini features a MIPI CSI-2 camera interface. It is routed directly to phyCORE-i.MX 8M Mini Connector X1. The interface provides a maximum bit rate of 1,5 Gbit/s. It uses four data channels and one clock channel. All signals, including control signals and an I^2C interface, to use the camera interfaces, according to PHYTEC's phyCAM-S standard, are available at the phyCORE-i.MX 8M Mini Connector.

The i.MX 8M Mini microcontroller is equipped with one MIPI camera interface. The following table shows the location of all MIPI CSI-2 interface signals on the phyCORE-Connector X1:

33 Camera Interface MIPI CSI-2 Signal Locations

SOM Connector Pin / phyBOARD-Polis Carrier Board Connector Pin	SOM Signal	SOM Voltage Domain	Signal Level	Signal Type	Description
A33	X_MIPI_CSI_DATA3_N	VDD_1V8	DIFF	I	Negative MIPI-CSI data 3 signal
A34	X_MIPI_CSI_DATA3_P	VDD_1V8	DIFF	I	Positive MIPI-CSI data 3 signal
A35	X_MIPI_CSI_DATA2_N	VDD_1V8	DIFF	I	Negative MIPI-CSI data 2 signal
A36	X_MIPI_CSI_DATA2_P	VDD_1V8	DIFF	I	Positive MIPI-CSI data 2 signal
A37	X_MIPI_CSI_CLK_N	VDD_1V8	DIFF	I	Negative MIPI-CSI clock signal
A38	X_MIPI_CSI_CLK_P	VDD_1V8	DIFF	I	Positive MIPI-CSI clock signal
A39	X_MIPI_CSI_DATA1_N	VDD_1V8	DIFF	I	Negative MIPI-CSI data 1 signal
A40	X_MIPI_CSI_DATA1_P	VDD_1V8	DIFF	I	Positive MIPI-CSI data 1 signal
A41	X_MIPI_CSI_DATA0_N	VDD_1V8	DIFF	I	Negative MIPI-CSI data 0 signal
A42	X_MIPI_CSI_DATA0_P	VDD_1V8	DIFF	I	Positive MIPI-CSI data 0 signal

SPDIF Interface

The phyCORE-i.MX 8M Mini features a SPDIF interface. It is routed directly to phyCORE-i.MX 8M Mini Connector X1.

Errata information

Existing issues may be solved by referring to the following chapters in *NXP Mask Set Errata for Mask 0N87W, Rev. 1, 09/2021*:

- ERR050448: SPDIF: SPDIF clock limitation

34 SPDIF Interface Signal Locations

SOM Connector Pin / phyBOARD-Polis Carrier Board Connector Pin	SOM Signal	SOM Voltage Domain	Signal Level	Signal Type	Description
A72	X_SPDIF_EXT_CLK	VDD_3V3_S	3,3 V	O	SPDIF clock signal
A73	X_SPDIF_TX	VDD_3V3_S	3,3 V	O	SPDIF transmit data signal
A74	X_SPDIF_RX	VDD_3V3_S	3,3 V	I	SPDIF receive data signal

35 I2C4 Interface Signal Locations

SOM Connector Pin / phyBOARD-Polis Carrier Board Connector Pin	SOM Signal Name	SOM Voltage Domain	Signal Level	Signal Type	Description
A72	X_SPDIF_EXT_CLK	VDD_3V3_S	3,3 V	O	I2C4 serial clock output signal
A73	X_SPDIF_TX	VDD_3V3_S	3,3 V	O	I2C4 serial data input-output
A74	X_SPDIF_RX	VDD_3V3_S	3,3 V	I	

CPU Core Frequency Scaling

The i.MX 8M Mini on the phyBOARD-Polis is able to scale the clock frequency and voltage. This is used to save power when the full performance of the CPU is not needed. Scaling the frequency and voltage is referred to as Dynamic Voltage and Frequency Scaling (DVFS).

The i.MX 8M Mini BSP supports the DVFS feature. The *Linux* kernel provides a DVFS framework that allows each CPU core to have a minimum/maximum frequency as well as the applicable voltage and a governor that regulates these values depending on the system load. Depending on the i.MX 8M Mini variant used, several different frequencies are supported. Further details on how to configure this governor can be found in the *phyCORE-i.MX 8M Mini BSP Manual*.

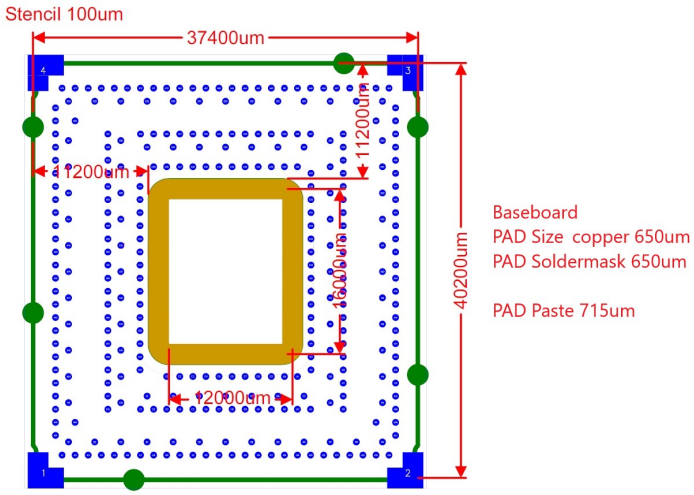
Technical Specifications

Warning

Due to changes in functionality and design that are currently being developed, there are several values that cannot be determined in time for the release of this manual. All values with "TBD (To Be Determined)" are currently being evaluated. These values will be added to future manual editions.

The module's profile is a maximum of 10 mm thick, with a maximal component height of 3.0 mm on the bottom (connector) side of the PCB and approximately 5.0 mm on the top (microcontroller) side. The board itself is approximately 1.4 mm thick.

5 phyCORE-i.MX 8M Mini Footprint



Tip

To facilitate the integration of the phyCORE-i.MX 8M Mini into your design, the footprint of the phyCORE-i.MX 8M Mini can be downloaded (see Integrating the phyCORE-i.MX 8M Mini).

Additional Specifications:

36 Technical Specifications

Dimensions:	37 mm x 40 mm
Weight:	0,008 kg
Storage temperature:	tbd
Operating temperature:	-40°C - +85°C
Humidity:	tbd

These specifications describe the standard configuration of the phyCORE-i.MX 8M Mini as of the printing of this manual.

phyCORE-i.MX 8M Mini Power Consumption

In order to illustrate the power consumption of the phyCORE-i.MX 8M Mini in various realistic load scenarios, multiple measurements were conducted. It is important to note, that these measurements are a sole depiction of the specific stresses, asserted to the SOM through the specified software applications. The given results may be utilized to dimension a power supply for the phyCORE-i.MX 8M Mini on custom hardware. Especially custom software may yield different results in power consumption compared to the values posted in the table below. It is vital that power consumption of the phyCORE-i.MX 8M Mini is evaluated when it is intended to be used with custom software.

The power consumption of the phyCORE-i.MX 8M Mini was measured at the 3.3 V SOM input voltage rail. The results below do not account for a possible current draw through the switched 3.3 V voltage rail VDD_3V3_S. The SOM is capable of drawing the measured current continuously. In case the ambient temperature varies greatly from the underlying test conditions for this measurement, a difference in power consumption may be observed.

In the applicable datasheet, the manufacturer of the i.MX 8M Mini CPU defines maximum current ratings for each voltage rail, which are designated as a guideline during the dimensioning of the on-module power supply and the resulting voltage rails. The mentioned absolute current ratings were considered in the design process of the phyCORE-i.MX 8M Mini's power infrastructure, yet does not represent realistic use cases for the SOM.

37 phyCORE-i.MX 8M Mini/Nano Power Consumption Test Cases

phyCORE-i.MX 8M Mini (PCL-069-1032311I)							
	Case 1	**Case 2**	**Case 3**	**Case 4**	**Case 5**	**Case 6**	**Case 7**
eMMC-Boot system idle DVFS ondemand	X	X	X	X	X	X	X
iperf3 client eth0 Gigabit		X	X	X	X	X	X
stressapptest -s 900 -M 1200 -m 8 -W							X
CPU-Load (4x dd from /dev/urandom to /dev/null)			X	X	X	X	

phyCORE-i.MX 8M Mini (PCL-069-1032311I)							
	Case 1	**Case 2**	**Case 3**	**Case 4**	**Case 5**	**Case 6**	**Case 7**
RAM-Load (memtester)				X	X	X	
GPU-Load (qt5-opengles2-test)					X		
VPU-Load (video 1080p)						X	
$T_{ambient}$ [°C]	22						
SOM input VDD_3V3 [V]	3,36						
Power Consumption [Watt]	2.2	2.5	2.9	3.3	3.6	3.8	4
CPU Thermal Zone 0 [°C] (Junction temperature CPU)	50	53	59	62	68	68	78

phyCORE-i.MX 8M Nano (PCL-069-0611010C)				
	Case 1	**Case 2**	**Case 3**	**Case 4**
eMMC-Boot system idle DVFS ondemand	X	X	X	X
iperf3 client eth0 Gigabit		X	X	X
stressapptest -s 900 -M 600 -m 8 -W		X		

phyCORE-i.MX 8M Nano (PCL-069-0611010C)				
	Case 1	**Case 2**	**Case 3**	**Case 4**
CPU-Load dd from /dev/urandom to /dev/null				X
RAM-Load (memtester)			X	
Tambient [°C]	22			
SOM input VDD_3V3 [V]	3.36			
Power Consumption [W]	1.31	2.29	1.85	2.07
CPU Thermal Zone 0 [°C] (Junction temperature CPU)	43	53	48	52

Tip

For further information and assistance regarding your application's power consumption, please contact PHYTEC sales.

Low-Power Modes

The i.MX 8M Mini offers various low-power modes. For further, more detailed information, on how to activate and utilize the different low-power modes please refer to the PHYTEC *phyCORE-i.MX 8M Mini BSP Manual and NXP i.MX 8M Mini Reference Manual*. The phyCORE-i.MX 8M Mini supports the following low-power modes:

Linux suspend to RAM via command "echo mem > /sys/power/state"

Product Temperature Grades

Warning

The right temperature grade of the module greatly depends on the use case. It is necessary to determine if the use case suits the temperature range of the chosen module (see below). If necessary, a heat spreader can be used for temperature compensation.

The feasible operating temperature of the SOM highly depends on the use case of your software application. Modern high-performance microcontrollers and other active parts, such as the ones described within this manual, are usually rated by qualifications based on tolerable junction or case temperatures. Therefore, making a general statement about minimum or maximum ambient temperature ratings for the described SOM is not possible.

However, the above-mentioned parts are available at different temperature qualification levels by the producers. We offer our SOMs in different configurations, making use of those temperature qualifications. To indicate which level of temperature qualification is used for active and passive parts of a SOM configuration, we have categorized our SOMs into three temperature grades.

The Product Temperature Grades table describes these grades in detail. These grades describe a set of components that, in combination, add up to a useful set of product options with different temperature grades. This enables us to make use of cost optimizations depending on the required temperature range.

In order to determine the right temperature grade and whether the minimum or maximum qualification levels are met within an application, the following conditions must be defined by considering the use case:

- Determined the processing load for the given software use case
- Maximum temperature ranges of components (Product Temperature Grades)
- Power consumption resulting from a baseload and the calculating power required (in consideration of peak loads as well as time periods for system cooldown)
- Surrounding temperatures and existing airflow in case the system is mounted into a housing
- Heat resistance of the heat dissipation paths within the system along with the considered usage of a heat spreader or a heat sink to optimize heat dissipation

38 Product Temperature Grades

Product Temp. Grade	Controller Temp Range (Junction Temp)	RAM (Case Temp)	Others (Ambient)
I	Industrial -40°C to +105°C / Automotive -40°C to+125°C	Industrial -40°C to +95°C	Industrial -40°C to +85°C
C	Commercial 0°C to +95°C	Consumer 0°C to +95°C	Consumer 0°C to +70°C

phyCORE-i.MX 8M Mini FTGA Mounting

The phyCORE i.MX 8M Mini uses Fused Tin Grid Array (FTGA) to mount to a carrier board (for example, phyBOARD-Polis). FTGA provides several advantages:

- An easy-to-produce design
- Permanent and robust mechanical connection to the carrier application
- Relaxed fit in regards to onboard circuitry
- Easy to design in any application
- Low profile
- Cost-efficient

For more information about FTGA soldering, please refer to the PHYTEC FTGA Soldering Guide (LAN-095e.A1 i.MX 8M Mini Fused Tin Grid Array (FTGA) Soldering Information).

Hints for Integrating and Handling the phyCORE-i.MX 8M Mini

Integrating the phyCORE-i.MX 8M Mini

Apart from this hardware manual, more information is available to facilitate the integration of the phyCORE-i.MX 8M Mini into customer applications.

1. The design of the phyBOARD-Polis can be used as a reference for any customer application.
2. Many answers to common questions can be found at: https://www.phytec.de/produkt/system-on-modules/phycore-imx-8m-mini-nano/ or https://www.phytec.eu/product-eu/system-on-modules/phycore-imx-8m-mini-nano/
3. The link “Carrier Board” within the category Dimensional Drawing leads to the layout data as shown in phyCORE-i.MX 8M Mini Footprint. It is available in different file formats. The use of this data allows the user to integrate the phyCORE-i.MX 8M Mini SOM as a single component of your design.
4. Different support packages are available for support in all stages of embedded development. Please visit http://www.phytec.de/de/support/support-pakete.html or https://www.phytec.eu/support/support-packages/ or contact our sales team for more details.
5. Many answers to common questions can be found at:
   https://www.phytec.de/produkt/system-on-modules/phycore-imx-8m-mini-nano/
   or
   https://www.phytec.eu/product-eu/system-on-modules/phycore-imx-8m-mini-nano/

Integrating the phyCORE into a Target Application

Successful integration in user target circuitry greatly depends on the adherence to the layout design rules for the GND connections of the phyCORE module. For maximum EMI performance, PHYTEC recommends, as a general design rule, connecting all GND pins to a solid ground plane. As a minimum, all GND pin neighboring signals which are being used in the application circuitry should be connected to GND.

Handling the phyCORE-i.MX 8M Mini

phyCORE Module Modifications

The removal of various components, such as the microcontroller or the standard quartz, is not advisable given the compact nature of the module. Should this nonetheless be necessary, please ensure that the board, as well as surrounding components and sockets, remain undamaged while desoldering. Overheating the board can cause the solder pads to loosen, rendering the module inoperable. If soldered components need to be removed, the use of a desoldering pump, desoldering braid, an infrared desoldering station, desoldering tweezers, hot air rework stations, or other desoldering methods is strongly recommended. Follow the instructions carefully for whatever method of removal is used.

Warning

The manufacturer guarantee is voided if any modifications to the module are performed, regardless of their nature.

phyCORE-i.MX 8M Mini on the phyBOARD-Polis

Hardware Overview

The phyBOARD-Polis for phyCORE-i.MX 8M Mini is a low-cost, feature-rich software development platform supporting the NXP Semiconductors i.MX 8M Mini microcontroller. Due to numerous standard interfaces, the phyBOARD-Polis can serve as the bedrock for any application. At the core of the phyBOARD-Polis is the PCL-069/ phyCORE-i.MX 8M Mini System On Module (SOM) containing the processor, DRAM, eMMC, power regulation, supervision, transceivers, and other core functions required to support the i.MX 8M Mini processor. Surrounding the SOM is the PB-02820-xxxxx.Ax/phyBOARD-Polis carrier board, adding power input, buttons, connectors, signal breakout, and Ethernet connectivity along with other peripherals.

The PCL-069 System On Module connects to the phyBOARD-Polis carrier board using a Ball Grid Array (BGA). The PCL-069 SOM is soldered directly onto the phyBOARD-Polis using PHYTEC's Direct Solder Connect technology. This solution offers an ultra-low-cost Single Board Computer for the i.MX 8M Mini processor, while maintaining most of the advantages of the SOM concept.

phyBOARD-Polis Concept

phyCORE carrier boards are designed and tested to be used in:

- series products
- evaluating, testing, and prototyping PHYTEC System on Modules in laboratory environments prior to their use in customer-designed applications.

PHYTEC phyCORE carrier boards are fully equipped with all mechanical and electrical components necessary for a fast, secure start-up. Subsequent communication to and programming of applicable PHYTEC System on Modules (SOM) is made easy.

This modular development platform concept includes the following components:

- The **phyCORE-i.MX 8M Mini** module populated with the i.MX 8M Mini microprocessor and all applicable SOM circuitry such as LPDDR 4 SDRAM, managed NAND, Ethernet transceiver, WiFi, and PMIC to name a few.
- The **phyBOARD-Polis** carrier board offers all essential components and connectors for a start-up including a power supply for 24 V input voltage, and interface connectors such as **USB micro-AB**, **USB A**, and **Ethernet RJ-45** which enable the use of the SOM's interfaces with standard cables.

The carrier board can also serve as a reference design for the development of custom target hardware in which the phyCORE SOM is deployed. Carrier board schematics are available under a Non-Disclosure Agreement (NDA). Reuse of carrier board circuitry enables users of PHYTEC SOMs to shorten time-to-market, reduce development costs, and avoid substantial design issues and risks.

SBCplus Concept

The SBCplus concept was developed to meet the many, small differences in customer requirements with little development effort. This greatly reduces the time to market. The core of the SBCplus concept is the SBC design library (a kind of construction set) that consists of a large number of function blocks (so-called "building blocks") that are continuously being refined and updated.

Recombining these function blocks allows PHYTEC to develop a customer-specific SBC within a short time. We are able to deliver production-ready custom Single Board Computers within a few weeks at very low costs. The already developed SBCs, such as the phyBOARD-Polis, each represent a combination of different customer wishes. This

means all necessary interfaces are already available on the standard versions, allowing PHYTEC SBCs to be integrated into a large number of applications without modification.

For any necessary detail adjustment, extension connectors are available which allow a wide variety of functions to be added.

Tip

For further information, please contact PHYTEC sales.

phyBOARD-Polis Features

The phyBOARD-Polis i.MX 8M Mini supports the following features:

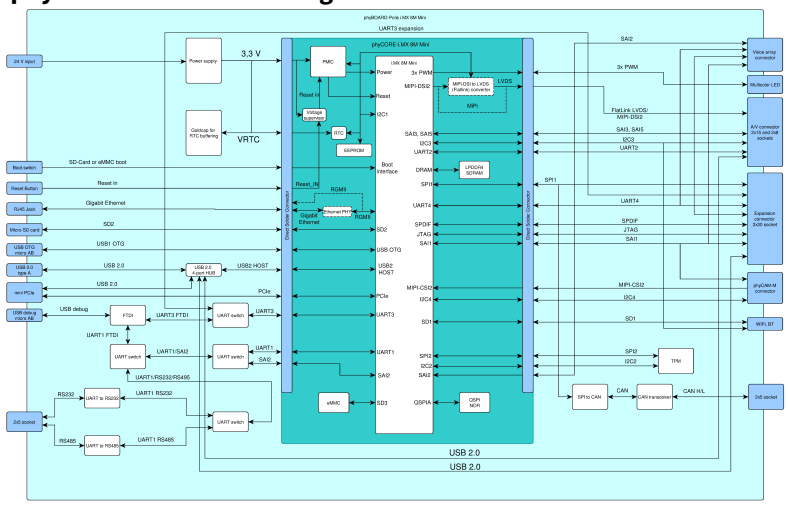
- Developed in accordance with PHYTEC's new SBCplus concept (SBCplus Concept)
- Populated with PHYTEC's phyCORE-i.MX 8M Mini SOM (via BGA mounting)
- Dimensions 100 mm × 100 mm
- Boot from eMMC or SD-Card
- Max. 1.6 GHz core clock frequency and up to four cores
- Wide input of voltage ranges (12 V – 24 V through external power module)
- 2GB RAM
- 8GB eMMC
- 4kB EEPROM
- 1x RJ45 jack for 10/100/1000 Mbps Ethernet
- 1x USB 2.0 host interface brought out to a USB Standard-A connector[5]
- 1x USB OTG interface available at a USB Micro-AB connector
- 1x Secure Digital / Multi-Media Memory Card interface brought out to a Micro-SD connector
- 1x LVDS interface brought out via an A/V connector
- 1x MIPI-DSI2 brought out via an A/V connector (if MIPI to LVDS converter is not mounted)
- 1x MIPI CSI-2 camera interface via the phyCAM-M connector
- 1x PCIe interface brought out to a Mini PCI Express connector
- RS-232 / RS-485 transceiver supporting UART4 including handshake signals with data rates of up to 1 Mbps (2×5 pin header 2.54 mm)
- Reset Button
- ON/OFF Button
- WiFi via the SD1 SDIO interface
- One multicolor LED
- SAI Audio brought out via A/V connector
- Voice array connector
- JTAG via evaluation adapter
- Expansion connector for different interfaces:
  - I^2C
  - SPI
  - UART
  - USB
  - SPDIF
- TPM via SPI or I^2C

Warning

5. There is no protective circuit for the USB interfaces brought out at the Mini PCI Express or the expansion connector.

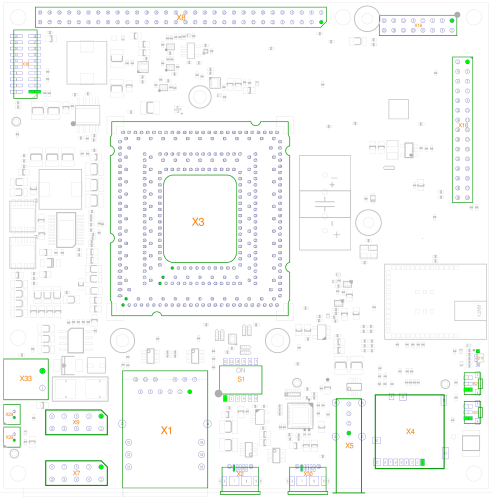
phyBOARD-Polis Block Diagram

6 phyBOARD-Polis Block Diagram

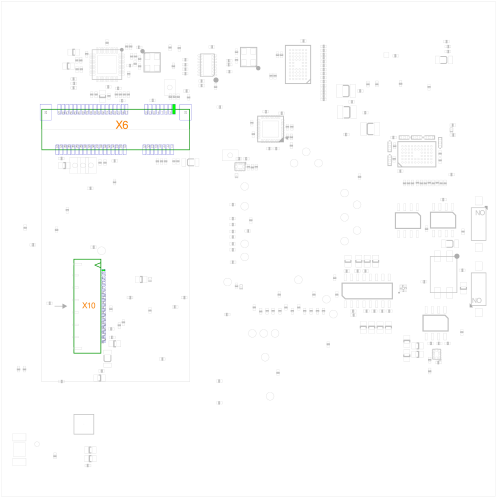


phyBOARD-Polis Component Placement

7 phyBOARD-Polis Components (Top)



8 phyBOARD-Polis Components (Bottom)



phyBOARD-Polis Component Overview

The phyBOARD-Polis features many different interfaces and is equipped with the components listed in table Connectors and Pin Headers. For a more detailed description of each component, refer to the appropriate section listed in the table below. phyBOARD-Polis Components (Top) and phyBOARD-Polis Components (Bottom) highlight the location of each component for easy identification.

Connectors and Pin Headers

This is a list of all available connectors on the phyBOARD-Polis.

39 phyBOARD-Polis Pin Headers and Connectors

Reference Designator	Description	Section
X1	Ethernet0 connector (RJ45 with speed and link LED)	Ethernet
X2	USB On-the-Go connector (USB Micro-AB)	USB OTG
X3	phyCORE connector	phyCORE-Connection
X4	Secure Digital / Multi-Media Card (Micro-slot)	SD /MM Card
X5	USB host connector (USB 2.0 Standard-A)	USB

Reference Designator	Description	Section
X6	PCI Express connector (Mini PCI Express)	PCIe
X7	CAN FD connector (2x5 pin header 2.54 mm pitch)	CAN FD
X8	Expansion connector (2×30 socket connector 2 mm pitch)	Expansion
X9	RS-232 with RTS and CTS, or RS-485 (UART3 2×5 pin header 2.54 mm pitch)	UART
X10	Camera phyCAM-M connector (30-pole Hirose FFC-connector, 0.5 mm pitch)	MIPI CSI-2
X16	A/V connector #1 (2×8 dual-entry connector 2 mm pitch)	A/V
X18	A/V connector #2 (2×15 dual-entry connector 2 mm pitch)	
X30	Debug FTDI (USB Debug)	USB Debug
X33	Power supply 12-24 V (2-pole Phoenix Contact Mini COMBICON base strip)	Power Supply
X38	Voice Array Connector	Voice Array

Warning

Module connections **must** not exceed their expressed maximum voltage or current. Maximum signal input values are indicated in the corresponding controller manuals/datasheets. As damage from improper connections varies according to use and application, the user must take appropriate safety measures to ensure that the module connections are protected from overloading through connected peripherals.

LEDs

The phyBOARD-Polis is populated with one LED, which is user-programmable. phyBOARD-Polis Components (Top) shows the location of the LED.

40 phyBOARD-Polis LED Description

LED	Color	Description	Section
D11	RGB	User-programmable RGB LED	Multicolor LED

Switches

The phyBOARD-Polis is populated with 3 switches. The tables below show their function:

41 phyBOARD-Polis S2/S3 Descriptions

Switch	Description	Section
S2	RESET	System Reset
S3	ON/OFF	System ON/OFF

Additionally, S1 is a 5-port dip switch bar populated for several functions:

- Boot Selection (see Multi-port Switch)
- SD-Card or WIFI Selection
- UART3 destination (A/V or FTDI) (see USB Debug)

Jumpers

The phyBOARD-Polis comes pre-configured with several solder jumpers (J). The jumpers enable the flexible configuration of a limited number of features for development purposes.

Warning

Due to the small footprint of the solder jumpers (J), PHYTEC does not recommend manual jumper modifications. This may also render the warranty invalid. Contact our sales team if you need jumper configurations different from the default configuration.

phyBOARD-Polis SBC Component Details

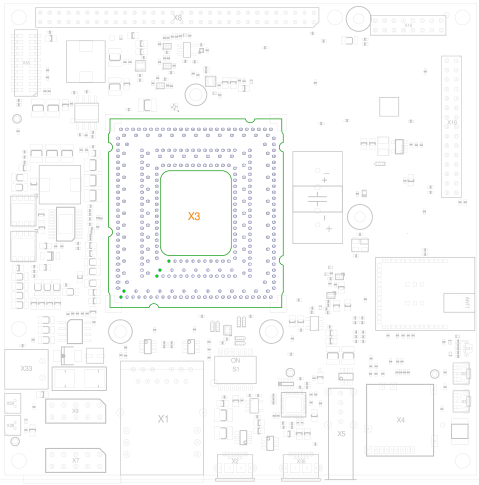
This section provides a more detailed look at the phyBOARD-Polis components. Each subsection details a particular connector/interface for configuring that interface.

Tip

Where possible, we also provide any useful information regarding design considerations for components. This can be used if you plan to design your own carrier board.

phyCORE-Connection (X3)

9 phyCORE Connector (X3)

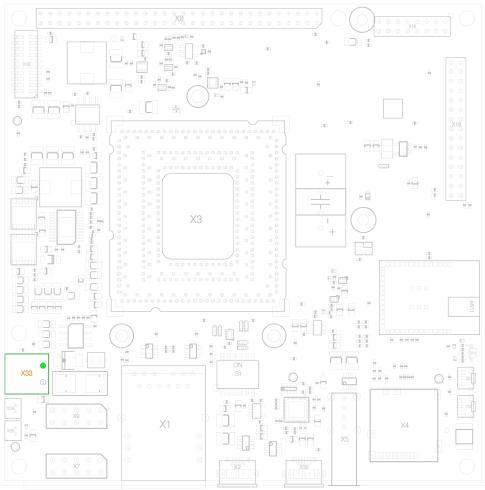


Power Supply (X33)

Warning

Do not change modules or jumper settings while the phyBOARD-Polis is supplied with power!

10 Power Supply Connector (X33)



The phyBOARD-Polis is available with one power supply connector, a 2-pole Combicon Phoenix connector suitable for a single supply voltage (X33).

The required current load capacity for all power supply solutions depends on the specific configuration of the phyCORE mounted on the phyBOARD-Polis, the particular interfaces enabled while executing software, as well as whether an optional expansion board is connected to the carrier board. The power input is protected against

overcurrent with a fuse (F1). A suppressor diode (D36) protects against polarity reversal. The pin assignment of the power input connector X33:

42 X33 Pin Assignment

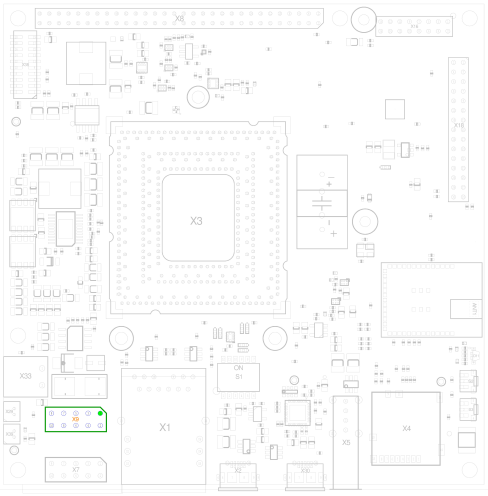
Interface Pin #	Signal	Description
1	VCC_IN_24V	24 V power supply
2	GND	Ground

Power Design Considerations

It is recommended to route high current rails, like the SOM supply voltage, as planes to keep series resistance at a minimum. The same thing should be applied to ground paths. For more information, see phyCORE-i.MX 8M Mini Power Consumption.

UART Connectivity (X8 and X9)

11 UART Connector (X9)



The phyCORE-i.MX 8M Mini features 4 UART interfaces. On the phyBOARD-Polis, TTL level UART2 is available at the A/V connector (X18) and TTL level UART4 is available at the expansion connector (X8). The availability of UART3 at the expansion connector depends on the state of the debug USB port and the configuration of switch S1 (Multi-port Switch) If a USB device is connected to the debug USB port (USB Debug), UART3 will only be available for the FTDI U66. The following is a detailed description of UART states and conditions:

- UART1:
  - U84 gives the option to use the UART1 default muxing option or the alternative muxing option SAI2_RXC and SAI2_RXFS for UART1 functionality. S1 (Multi-port Switch, pad 3) controls the configuration of U84.
  - U83 makes UART1 (default or alternative assignment) available for the FTDI U66 or the conversion to RS232/RS485. If a USB device is plugged into the debug USB port (USB Debug), U83 will route UART1 to U66. U83 output is twisted.
  - U85 gives the option to use the UART1 RS232/RS485 signal either for conversion to RS232 or RS485 via U78 or U77. S1 (pad 5) controls the configuration of U84. SAI2_RXD0 and SAI2_TXFS are used for handshake functionality.

- UART2: Available at connector X18
- UART3: U82 gives the option to route UART3 to U87 as debug UART or to route UART3 to the expansion connector X8. In case a USB device is plugged into the debug USB port (USB Debug), U83 will route UART1 to U87.
- UART4: Available at expansion connector X8 and voice array connector X38

Further information on the switch S1 can be found in the section Multi-port Switch. Further information on the expansion connector X8 can be found in the section Expansion Connector. The following table shows the signal mapping of the RS-232 and RS-485 level signals at connector X9:

43 X9 Pin Assignment

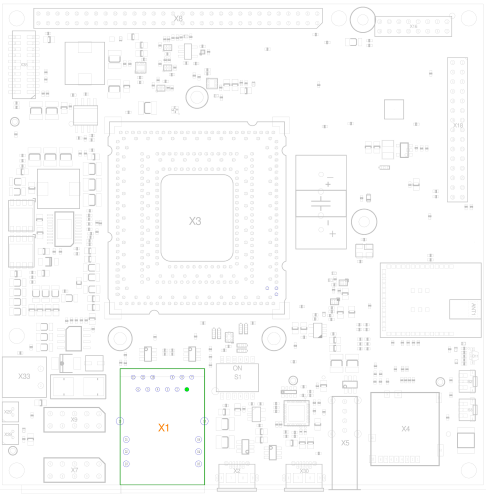
Interface Pin #	Signal	Pin #	Signal
1	NC	2	NC
3	UART1_RXD_RS232	4	UART1_RTS_RS232
5	UART1_TXD_RS232	6	UART1_CTS_RS232
7	UART1_RS485_A	8	UART1_RS485_B
9	GND	10	NC

UART Design Consideration

When designing a custom carrier board, remember the TTL level is 3.3 V. Route signals as single-ended 50 Ohm lines.

Ethernet Connectivity (X1)

12 Ethernet Connector (X1)



The phyBOARD-Polis is equipped with an RJ45 connector supporting a 10/100/1000Base-T network connection. The LEDs for LINK (green) and ACTIVITY (yellow) indications are integrated into the connector. The Ethernet transceiver

supports Auto MDI-X, eliminating the need for a direct connect LAN or cross-over cable. They detect the TX and RX pins of the connected device and automatically configure the PHY TX and RX pins accordingly.

The following table shows the pin assignment of the Ethernet0 connector X1:

44 X1 Pin Assignment

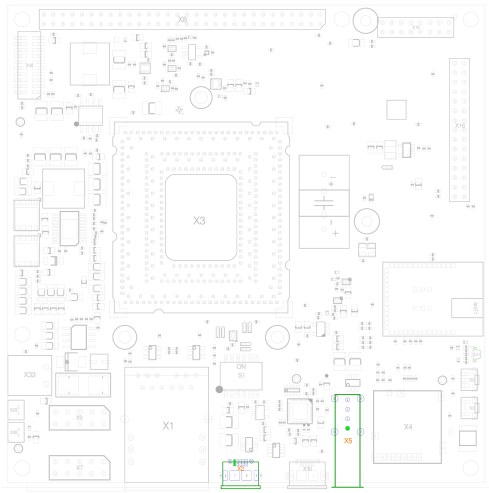
Interface Pin #	Signal name	Signal Type	Signal Level	Description
1	X_ETH_A_P	Ethernet	Analog	D1+
2	X_ETH_A_N	Ethernet	Analog	D1-
3	X_ETH_B_P	Ethernet	Analog	D2+
4	X_ETH_B_N	Ethernet	Analog	D2-
5	GND	-	-	MDCT1
6	GND	-	-	MDCT2
7	X_ETH_C_P	Ethernet	Analog	D3+
8	X_ETH_C_N	Ethernet	Analog	D3-
9	X_ETH_D_P	Ethernet	Analog	D4+
10	X_ETH_D_N	Ethernet	Analog	D4-
11	VCC_3V3	Ethernet	3.3 V	LED_GR_A
12	X_ETH0_LED0_LINK	Ethernet	Analog	LED_GR_C
13	VCC_3V3	Ethernet	3.3 V	LED_YE_A
14	X_ETH0_LED2_ACT	Ethernet	Analog	LED_YE_C

Ethernet Design Consideration

The data lanes should be routed with a differential impedance of 100 Ohm and kept as short as possible. The center taps of each pair's transformer have to be connected to GND through a 100nF capacitor. The LED pins are open-drain outputs of the SOM without a resistor, so they should be connected to the cathodes of the LEDs through a suitable resistor.

USB OTG and 2.0 Connectivity (X2 and X5)

13 USB OTG and 2.0 Connectors (X2 and X5)



The phyBOARD-Polis provides one USB 2.0 and one USB OTG interface.

USB1 is accessible at the USB Micro-AB connector X2 and is configured as USB OTG. USB OTG devices are capable of initiating a session, controlling the connection, and exchanging host and peripheral roles with each other. This interface is compliant with USB revision 2.0. USB2 is accessible at the Standard-A connector X5 and is configured as a USB host.

The following tables show the pin assignments of the USB OTG and USB 2.0 interface:

45 USB OTG - X2 Pin Assignment

Interface Pin #	Signal name	Signal Level	Signal Type	Description
1	USB_OTG1_VBUS	5 V	PWR_I	5 V USB supply voltage
2	X_USB1_DN	Diff	USB_I/O	Negative USB1 data signal
3	X_USB1_DP	Diff	USB_I/O	Positive USB1 data signal
4	X_USB1_ID	3,3 V	I	USB 1 identification signal
5	GND	-	-	Ground
6	SHIELD1	Shield	-	Shield connected to Ground over 2,2 nF parallel to 1 MOhm

Interface Pin #	Signal name	Signal Level	Signal Type	Description
7	SHIELD2	Shield	-	Shield connected to Ground over 2,2 nF parallel to 1 MOhm
8	SHIELD3	Shield	-	Shield connected to Ground over 2,2 nF parallel to 1 MOhm
9	SHIELD4	Shield	-	Shield connected to Ground over 2,2 nF parallel to 1 MOhm
10	SHIELD5	Shield	-	Shield connected to Ground over 2,2 nF parallel to 1 MOhm
11	SHIELD6	Shield	-	Shield connected to Ground over 2,2 nF parallel to 1 MOhm

46 USB 2.0 - X5 Pin Assignment

Interface Pin #	Signal name	Signal Level	Signal Type	Description
1	USB_HUB_VBUS1	5 V	PWR_I	5 V USB supply voltage
2	USB_HUB_DM1	Diff	USB_I/O	Negative USB HUB1 data signal
3	USB_HUB_DP1	Diff	USB_I/O	Positive USB HUB1 data signal
4	GND	-	-	Ground
S1	SHIELD1	Shield	-	Shield connected to Ground over 2,2 nF parallel to 1 MOhm
S2	SHIELD2	Shield	-	Shield connected to Ground over 2,2 nF parallel to 1 MOhm

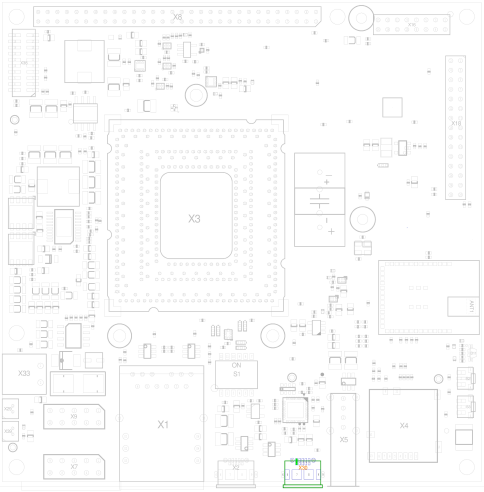
Interface Pin #	Signal name	Signal Level	Signal Type	Description
S3	SHIELD3	Shield	-	Shield connected to Ground over 2,2 nF parallel to 1 MOhm
S4	SHIELD4	Shield	-	Shield connected to Ground over 2,2 nF parallel to 1 MOhm

USB Design Consideration

The data lanes should be routed with a differential impedance of 90 Ohm and kept as short as possible.

USB Debug (X30)

14 USB Debug Connector (X30)



The phyBOARD-Polis offers a USB debug interface, that is accessible via the USB micro-AB connector X30. When a USB device is plugged into X30, UART3 will automatically be routed to the UART to USB converter U87. The following table shows the pin configuration of the debug USB micro-AB connector X30:

47 X30 Pin Assignment

Interface Pin #	Signal name	Signal Level	Signal Type	Description
1	VBUS_DEBUG_USB	5 V	PWR_I	5 V USB supply voltage
2	DEBUG_USB_DM	Diff	USB_I/O	Negative debug USB data signal

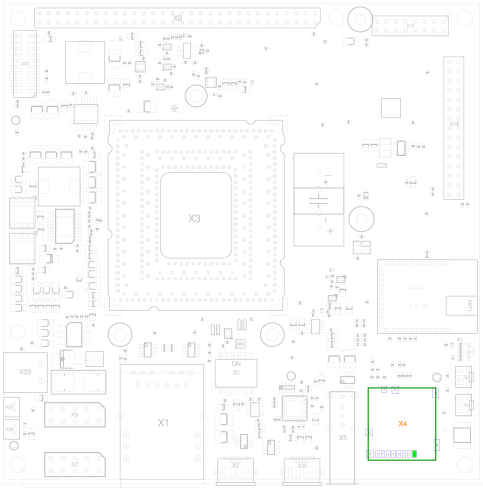
Interface Pin #	Signal name	Signal Level	Signal Type	Description
3	DEBUG_USB_DP	Diff	USB_I/O	Positive debug USB data signal
4	DEBUG_USB_ID	3,3 V	I	Debug USB identification signal (not connected)
5	GND	-	-	Ground
6	SHIELD1	Shield	-	Shield connected to Ground over 2,2 nF parallel to 1 MOhm
7	SHIELD2	Shield	-	Shield connected to Ground over 2,2 nF parallel to 1 MOhm
8	SHIELD3	Shield	-	Shield connected to Ground over 2,2 nF parallel to 1 MOhm
9	SHIELD4	Shield	-	Shield connected to Ground over 2,2 nF parallel to 1 MOhm
10	SHIELD5	Shield	-	Shield connected to Ground over 2,2 nF parallel to 1 MOhm
11	SHIELD6	Shield	-	Shield connected to Ground over 2,2 nF parallel to 1 MOhm

Debug Design Considerations

The UART data signals to the UART to USB converter should be routed as singled-ended signals with an impedance of 50 Ohm and kept as short as possible. The USB data lanes should be routed with a differential impedance of 90 Ohm and kept as short as possible.

Secure Digital Memory / MultiMedia Card (X4)

15 SD-Card / MM Card Connector (X4)



The phyBOARD-Polis provides a standard microSDHC card slot at X4 for use with SD/MMC interface cards. It allows for a fast, easy connection to peripheral devices like SD and MMC cards. Power to the SD interface is supplied by inserting the appropriate card into the SD/MMC connector. It also features card detection, a lock mechanism, and a smooth extraction function by pushing the card in and out.

DIP switch S1 provides a toggle between default and SD-Card boot. In order to boot from SD-Card, S1 (pads 1-12) must be switched ON (refer to Multi-port Switch for further information).

48 X4 Pin Assignment

Interface Pin #	Signal name	Signal Level	Signal Type	Description
1	X_SD2_DATA2	1,8 V/3,3 V	I/O	SD2 data 2
2	X_SD2_DATA3	1,8 V/3,3 V	I/O	SD2 data 3
3	X_SD2_CMD	1,8 V/3,3 V	O	SD2 command
4	VCC_3V3	3,3 V	PWR_I	3,3 V supply voltage
5	X_SD2_CLK	1,8 V/3,3 V	O	SD2 clock
6	GND			Ground
7	X_SD2_DATA0	1,8 V/3,3 V	I/O	SD2 data 0
8	X_SD2_DATA1	1,8 V/3,3 V	I/O	SD2 data 1

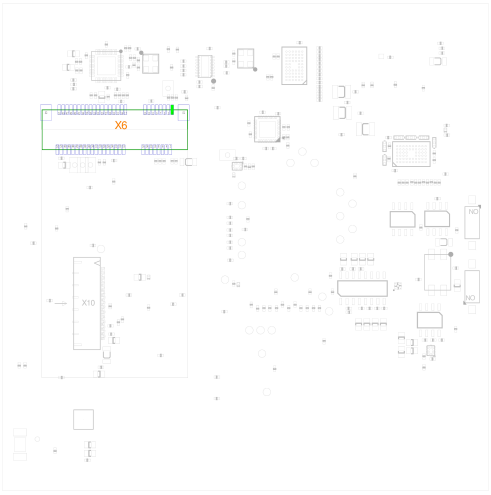
Interface Pin #	Signal name	Signal Level	Signal Type	Description
9	X_SD2_CD_B	1,8 V/3,3 V	I	SD2 card detect
10	GND	-	-	Ground
11	GND	-	-	Ground
12	GND	-	-	Ground
13	GND	-	-	Ground
14	GND	-	-	Ground

SD / MM Card Design Considerations

Series resistors in data and clock signals should be placed as close as possible to the signal source. For I/O signals this means two resistors in one electric net are recommended. The voltage of the SD2 signal lanes is NVCC_SD2 and can switch between 1.8 V and 3.3 V. The supply voltage of the SD-Card remains 3.3 V and should not be connected to NCVV_SD2. All signals should be routed as 50 Ohm single-ended lines.

PCIe Connectivity (X6)

16 PCIe Connector (X6)



The 1-lane PCI Express interface of the phyBOARD-Polis provides PCIe Gen. 2.0 functionality, which supports 5 Gbit/s operations. The interface is fully backward compatible with the Gen. 1.1, 2.5 Gbit/s specifications. Various control signals are implemented with GPIOs. The pin assignment of the Mini PCI Express connector is shown in the following table:

49 X6 Pin Assignment

Interface Pin #	Signal name	Signal Level	Signal Type	Description
1	X_SAI1_RXD5/ BOOT_CFG[5]	3,3 V	O	X_SAI1_RXD5/ BOOT_CFG[5] switches nWAKE High level only possible when nPOR_IN_DELAYED is not active (low)
2	VCC_3V3	3,3 V	PWR_I	Supply voltage 3,3 V
3	X_SAI1_TXD0/ BOOT_CFG[8]	3,3 V	IO	PCI express reserved
4	GND	-	-	Ground
5	X_SAI5_TXD7	3,3 V	IO	PCI express reserved
6	VCC_1V5	1,5 V	PWR_I	Supply voltage 1,5 V
7	X_PCIE2_CLKREQ_ B	-	-	PCI express clock request
8	NC	-	-	Not connected
9	GND	-	-	Ground
10	NC	-	-	Not connected
11	X_PCIe_CLK_N	Diff	PCIe_O	Negative PCIe clock signal
12	NC	-	-	Not connected
13	X_PCIe_CLK_P	Diff	PCIe_O	Positive PCIe clock signal
14	NC	-	-	Not connected

Interface Pin #	Signal name	Signal Level	Signal Type	Description
15	GND	-	-	Ground
16	NC	-	-	Not connected
17	NC	-	-	Not connected
18	GND	-	-	Ground
19	NC	-	-	Not connected
20	NC	-	-	Not connected
21	GND	-	-	Ground
22	miniPCIe_nPERST	3,3 V	O	PCI express reset
23	X_PCIE_RXN_N	Diff	PCIe_I	Negative PCIe receive signal
24	VCC_3V3	3,3 V	PWR_I	Supply voltage 3,3 V
25	X_PCIE_RXN_P	Diff	PCIe_I	Positive PCIe receive signal
26	GND	-	-	Ground
27	GND	-	-	Ground
28	VCC_1V5	1,5 V	PWR_I	Supply voltage 1,5 V
29	GND	-	-	Ground
30	X_I2C2_SCL	3,3 V	OD	I2C2 serial clock
31	X_PCIE_TXN_N	Diff	PCIe_O	Negative PCIe transmit signal

Interface Pin #	Signal name	Signal Level	Signal Type	Description
32	X_I2C2_SDA	3,3 V	OD-BI	I2C2 serial data signal
33	X_PCIE_TXN_P	Diff	PCIe_O	Positive PCIe transmit signal
34	GND	-	-	Ground
35	GND	-	-	Ground
36	USB_HUB_DM3	Diff	USB_I/O	Negative USB HUB 3 signal
37	GND	-	-	Ground
38	USB_HUB_DP3	Diff	USB_I/O	Positive USB HUB 3 signal
39	VCC_3V3	3,3 V	PWR_I	Supply voltage 3,3 V
40	GND	-	-	Ground
41	VCC_3V3	3,3 V	PWR_I	Supply voltage 3,3 V
42	TP1	-	-	Test pad 1
43	GND	-	-	Ground
44	TP2	-	-	Test pad 2
45	NC	-	-	Not connected
46	TP3	-	-	Test pad 3
47	NC	-	-	Not connected
48	VCC_1V5	1,5 V	PWR_I	Supply voltage 1,5 V

Interface Pin #	Signal name	Signal Level	Signal Type	Description
49	NC	-	-	Not connected
50	GND	-	-	Ground
51	NC	-	-	Not connected
52	VCC_3V3	3,3 V	PWR_I	Supply voltage 3,3 V
S1	GND	-	-	Ground
S2	GND	-	-	Ground

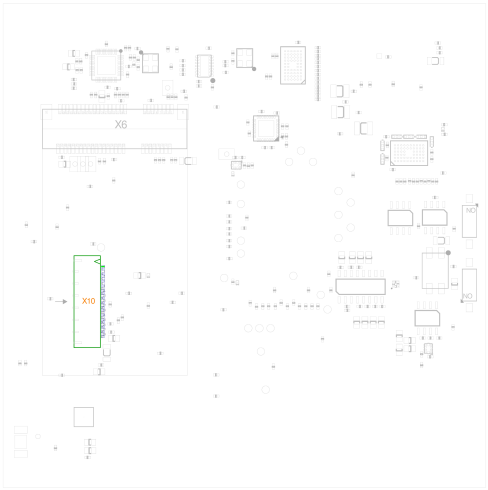
PCIe Design Considerations

100nF AC-Coupling capacitors are placed close to output pins of the i.MX 8M Mini on the PCL-069 in series to the TX-Lanes. No further TX coupling capacitors are needed. The differential impedance should be 85 Ohm.

Camera Connections

phyCAM-M MIPI CSI-2 Camera Connector (X10)

17 phyCAM-M MIPI CSI-2 Camera Connector (X10)



The phyCORE-i.MX 8M Mini on the phyBOARD-Polis offers one interface to connect to digital cameras with the MIPI CSI-2 interface. The signals of the Camera Serial Interface (CSI) are available as a multi-lane LVDS camera interface together with an I^2C interface to allow for a direct connection of appropriate camera modules. On the phyBOARD-Polis, the CMOS Camera Interface is brought out as a phyCAM-M camera interface at connector X10. Information on

the phyCAM-M standard and other possibilities can be found in the phyCAM manual: https://www.phytec.de/fileadmin/user_upload/downloads/Manuals/L-748e_10.pdf.

Pin assignment of the phyCAM-M MIPI CSI-2 connector X10:

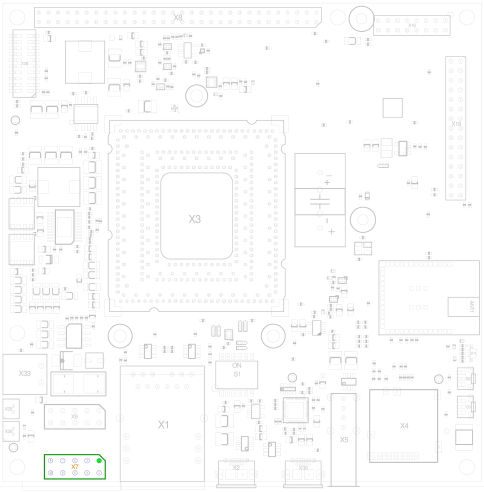
50 X10 Pin Assignment

Interface Pin #	Signal Name	Signal Level	Signal Type	Description
1	GND	-	-	Ground
2	X_MIPI_CSI_DATA0_P	Diff	CSI2_I	Positive MIPI CSI data 0 signal
3	X_MIPI_CSI_DATA0_N	Diff	CSI2_I	Negative MIPI CSI data 0 signal
4	GND	-	-	Ground
5	X_MIPI_CSI_DATA1_P	Diff	CSI2_I	Positive MIPI CSI data 1 signal
6	X_MIPI_CSI_DATA1_N	Diff	CSI2_I	Negative MIPI CSI data 1 signal
7	GND	-	-	Ground
8	X_MIPI_CSI_CLK_P	Diff	CSI2_I	Positive MIPI CSI clock signal
9	X_MIPI_CSI_CLK_N	Diff	CSI2_I	Negative MIPI CSI clock signal
10	GND	-	-	Ground
11	X_MIPI_CSI_DATA2_P	Diff	CSI2_I	Positive MIPI CSI data 2 signal
12	X_MIPI_CSI_DATA2_N	Diff	CSI2_I	Negative MIPI CSI data 2 signal
13	GND	-	-	Ground
14	X_MIPI_CSI_DATA3_P	Diff	CSI2_I	Positive MIPI CSI data 3 signal

Interface Pin #	Signal Name	Signal Level	Signal Type	Description
15	X_MIPI_CSI_DATA3_N	Diff	CSI2_I	Negative MIPI CSI data 3 signal
16	GND	-	-	Ground
17	X_SAI2_TXD0	3,3 V	IO	Multipurpose pin 4
18	X_SAI1_TXFS	3,3 V	IO	Multipurpose pin 3
19	X_SAI1_MCLK	3,3 V	IO	Multipurpose Pin 2 / Default = TRIGGER (IN)
20	X_SD2_RESET_B	1,8 V/ 3,3 V	OD	CSI reset signal
21	GND	-	-	Ground
22	X_I2C4_SCL	3,3 V	OD	I2C4 serial clock signal
23	X_I2C4_SDA	3,3 V	OD_BI	I2C4 serial data signal
24	CSI1_I2C_ADR	3,3 V	OD	I2C4 address select
25	CSI1_ nRESET	3,3 V		Camera reset signal
26	CSI1_VCC_SELECT	3,3 V		Set voltage on VCC pins
27	GND	-	-	Ground
28	VCC_CAM_CSI1	3,3 V/ 5 V	PWR_I	CSI supply voltage 3,3 V or 5 V
29	VCC_CAM_CSI1	3,3 V/ 5 V	PWR_I	CSI supply voltage 3,3 V or 5 V
30	VCC_CAM_CSI1	3,3 V/ 5 V	PWR_I	CSI supply voltage 3,3 V or 5 V

CAN FD (X7)

18 CAN FD (X7)



The CAN with Flexible Data-Rate (CAN FD) is an updated extension of the original CAN protocol. This enables extra data bytes and flexible bit rates. In general, the CAN FD offers 3 benefits to regular CAN:

1. Increased Data Length
   CAN FD supports up to 64 data bytes per data frame vs. 8 data bytes for regular CAN.
2. Increased Speed
   CAN FD supports dual bit rates: normal 1Mbit/S bit rate of a regular CAN and data bit rates up to 5Mbit/s, depending on network and transceiver types.
3. Improved Reliability
   CAN FD uses an improved cyclic redundancy check (CRC), lowering the risks of undetected errors.

Pin assignment of the CAN FD Connector X7:

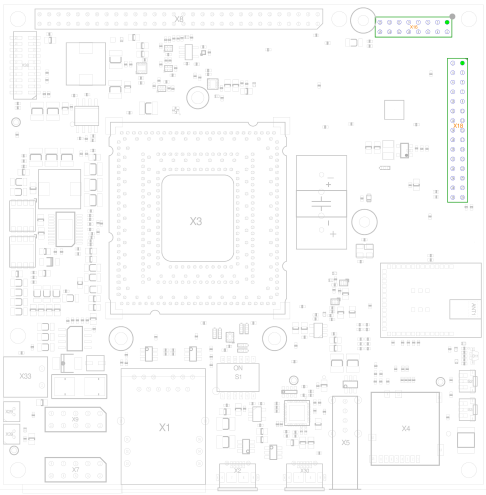
51 X7 Pin Assignment

Interface Pin #	Signal Name	Signal Level	Signal Type	Description
1	NC	-	-	-
2	GND	-	-	Ground
3	X_CAN_L	Diff	CAN_I/O	CAN FD low signal
4	X_CAN_H	Diff	CAN_I/O	CAN FD high signal
5	GND	-	-	Ground
6	NC	-	-	-
7	NC	-	-	-

Interface Pin #	Signal Name	Signal Level	Signal Type	Description
8	NC	-	-	-
9	NC	-	-	-
10	NC	-	-	-

Audio/Video Connectors (X16 and X18)

19 Audio/Video Connectors (X16 and X18)



The Audio/Video (A/V) connectors X16 and X18 provide an easy way to add typical A/V functions and features to the phyBOARD-Polis. Standard interfaces such as parallel display, I^2S, and I^2C as well as different supply voltages are available at the two 2 mm pitch dual inline sockets.

The A/V connector is intended for use with phyBOARD Expansion Boards[6] and to add specific audio/video connectivity with custom expansion boards. A/V connector X16 makes all data and clock signals for display connectivity available. X18 provides signals for audio and touch screen connectivity as well as an I^2C bus and additional control signals.

Pin assignments for A/V connectors X16 and X18:

52 X16 A/V Connector Pin Assignment

Interface Pin #	Signal Name	Signal Level	Signal Type	Description
1	GND	-	-	Ground
2	X_FLATLINK_D2_P/ MIPI_DSI_CLK_P	Diff	DSI2_O	Positive LVDS data 2 signal or Positive MIPI DSI clock signal

Interface Pin #	Signal Name	Signal Level	Signal Type	Description
3	X_FLATLINK_CLK_P / MIPI_DSI_DATA3_P	Diff	DSI2_O	Positive LVDS clock signal or Positive MIPI DSI data 3 signal
4	X_FLATLINK_D2_N/ MIPI_DSI_CLK_N	Diff	DSI2_O	Negative LVDS data 2 signal or Negative MIPI DSI clock signal
5	X_FLATLINK_CLK_N / MIPI_DSI_DATA3_N	Diff	DSI2_O	Negative LVDS clock signal or Negative MIPI DSI data 3 signal
6	GND	-	-	Ground
7	GND	-	-	Ground
8	X_FLATLINK_D3_P/ MIPI_DSI_DATA2_P	Diff	DSI2_O	Positive LVDS data 3 signal or Positive MIPI DSI data 2 signal
9	X_FLATLINK_D1_P/ MIPI_DSI_DATA1_P	Diff	DSI2_O	Positive LVDS data 1 signal or Positive MIPI DSI data 1 signal
10	X_FLATLINK_D3_N/ MIPI_DSI_DATA2_N	Diff	DSI2_O	Negative LVDS data 3 signal or Negative MIPI DSI data 2 signal
11	X_FLATLINK_D1_N/ MIPI_DSI_DATA1_N	Diff	DSI2_O	Negative LVDS data 1 signal or Negative MIPI DSI data 1 signal
12	GND	-	-	Ground
13	GND	-	-	Ground

Interface Pin #	Signal Name	Signal Level	Signal Type	Description
14	X_FLATLINK_D0_P/ MIPI_DSI_DATA0_P	Diff	DSI2_O	Positive LVDS data 0 signal or Positive MIPI DSI data 0 signal
15	VCC_IN_24V	24 V	PWR_I	24 V display supply voltage
16	X_FLATLINK_D0_N/ MIPI_DSI_DATA0_N	Diff	DSI2_O	Negative LVDS data 0 signal or Negative MIPI DSI data 0 signal

53 X18 A/V Connector Pin Assignment

Interface Pin #	Signal Name	Signal Level	Signal Type	Description
1	USB_HUB_DP2	Diff	USB_I/O	Positive USB HUB 2 signal
2	USB_HUB_DM2	Diff	USB_I/O	Negative USB HUB 2 signal
3	X_nPOR_OD	3,3 V	OD	Open drain Power-On Reset of SoM
4	GND	-	-	Ground
5	X_SAI3_RXD / UART2_RTS_B	3,3 V	IO	SAI3 receive data
6	X_SAI3_TXFS / UART2_RX	3,3 V	IO	SAI3 transmit frame synchronization signal
7	X_SAI3_TXC / UART2_TX	3,3 V	IO	SAI3 transmit bit clock signal
8	X_SAI3_TXD	3,3 V	IO	SAI3 transmit data
9	X_SAI3_MCLK	3,3 V	IO	SAI3 master clock signal

Interface Pin #	Signal Name	Signal Level	Signal Type	Description
10	X_SAI3_RXFS	3,3 V	IO	SAI3 receive bit clock signal
11	GND	-	-	Ground
12	X_SAI3_RXC / UART2_CTS_B	3,3 V	IO	SAI3 receive bit clock signal
13	X_SAI5_RXD3	3,3 V	IO	SAI5 receive data 3
14	GND	-	-	Ground
15	X_SAI5_RXFS	3,3 V	IO	SAI5 receive frame synchronization signal
16	X_SAI5_RXD2	3,3 V	IO	SAI5 receive data 2
17	X_SAI5_RXC	3,3 V	IO	SAI5 receive bit clock
18	X_SAI5_RXD1	3,3 V	IO	SAI5 receive data 1
19	X_SAI5_MCLK	3,3 V	IO	SAI5 master clock signal
20	X_SAI5_RXD0	3,3 V	IO	SAI5 receive data 0
21	GND	-	-	Ground
22	X_I2C3_SDA	3,3 V	OD-BI	I2C3 serial data
23	X_UART2_RXD	3,3 V	IO	UART2 receive data
24	X_I2C3_SCL	3,3 V	OD	I2C3 serial clock
25	X_UART2_TXD	3,3 V	IO	UART2 transmit data
26	GND	-	-	Ground

Interface Pin #	Signal Name	Signal Level	Signal Type	Description
27	VCC_5V	5 V	PWR_I	5 V supply voltage
28	VCC_3V3	3,3 V	PWR_I	3,3 V supply voltage
29	VCC_5V	5 V	PWR_I	5 V supply voltage
30	VCC_3V3	3,3 V	PWR_I	3,3 V supply voltage

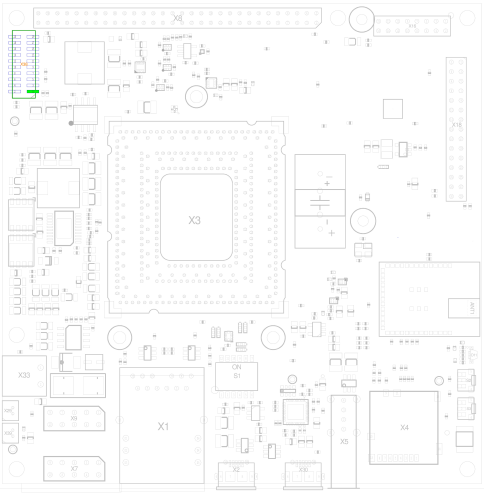
6 Please find additional information on phyBOARD Expansion Boards in the corresponding application guide . (L-793e).

A/V Design Consideration

All signals should be routed as short as possible and as 50 Ohm single-ended lines.

Voice Array Connector (X38)

20 Voice Array Connector (X38)



The phyBOARD-Polis offers a 2x9 socket as a voice array connector with UART, I2C, and I2S functionality. The following table shows the pin assignment of the voice array connector X38:

54 X38 Pin Assignment

Interface Pin #	Signal Name	Signal Level	Signal Type	Description
1	VCC_5V	5 V	PWR_I	5 V supply voltage
2	VCC_3V3	3,3 V	PWR_I	3,3 V supply voltage

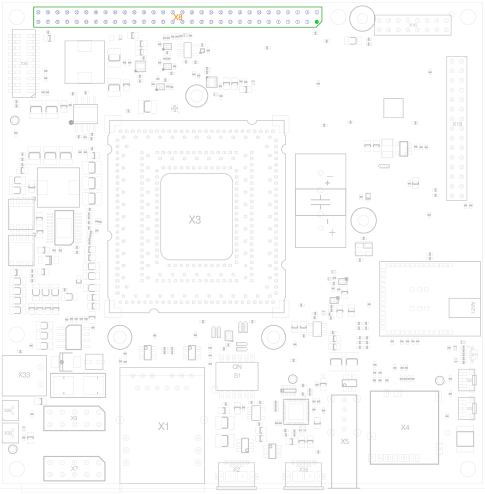
Interface Pin #	Signal Name	Signal Level	Signal Type	Description
3	X_UART4_TXD	3,3 V	O	UART4 transmit data
4	X_UART4_RXD	3,3 V	I	UART4 receive data
5	X_I2C3_SCL	3,3 V	O	I2C3 serial clock
6	X_I2C3_SDA	3,3 V	IO	I2C3 serial data
7	X_SAI1_MCLK	3,3 V	IO	SAI1 master clock
8	X_SAI1_RXC	3,3 V	IO	SAI1 receive bit clock
9	X_SAI1_RXD0/ BOOT_CFG[0]	3,3 V	IO	SAI1 receive data 0
10	X_SAI1_RXD1/ BOOT_CFG[1]	3,3 V	IO	SAI1 receive data 1
11	X_SAI1_RXD2/ BOOT_CFG[2]	3,3 V	IO	SAI1 receive data 2
12	X_SAI1_RXD3/ BOOT_CFG[3]	3,3 V	IO	SAI1 receive data 3
13	GND	-	-	Ground
14	GND	-	-	Ground
15	X_SAI2_MCLK	3,3 V	IO	SAI2 master clock
16	X_SAI2_TXC	3,3 V	IO	SAI2 transmit bit clock
17	X_SAI2_TXD0	3,3 V	IO	SAI2 transmit data 0
18	X_SAI1_RXD4/ BOOT_CFG[4]	3,3 V	IO	SAI1 receive data 4

Voice Array Design Considerations

All signals should be routed as short as possible and as 50 Ohm single-ended lines.

Expansion Connector (X8)

21 Expansion Connector (X8)



The expansion connector X8 provides an easy way to add other functions and features to the phyBOARD-Polis. Standard interfaces such as USB, SPDIF, JTAG, UART, SPI, and I^2C as well as different supply voltages and some GPIOs are available at the female expansion connector. The expansion connector is intended for use with phyBOARD Expansion Boards and to add specific functions with custom expansion boards. Information on the expansion boards available for the expansion connector can be found in the Application Guide for phyBOARD Expansion Boards (L-793e).

Pin assignment of the expansion connector X8:

55 X8 Expansion Connector Pin Assignment

Interface Pin #	Signal Name	Signal Level	Signal Type	Description
1	VCC_3V3	3,3 V	PWR_I	3,3 V supply voltage
2	VCC_5V	5 V	PWR_I	5 V supply voltage
3	VCC_1V5	1,5 V	PWR_I	1,5 V supply voltage
4	GND	-	-	Ground
5	X_ECSPI1_SS1	3,3 V	OD	SPI1 chip select
6	X_ECSPI1_MOSI	3,3 V	O	SPI1 master out slave in

Interface Pin #	Signal Name	Signal Level	Signal Type	Description
7	X_ECSPI1_MISO	3,3 V	I	SPI1 master in slave out
8	X_ECSPI1_SCLK	3,3 V	O	SPI1 serial clock
9	GND	-	-	Ground
10	X_UART3_RXD_EXP	3,3 V	I	UART3 receive data
11	X_I2C3_SDA	3,3 V	OD_BI	I2C3 serial data
12	X_UART3_TXD_EXP	3,3 V	O	UART3 transmit data
13	X_I2C3_SCL	3,3 V	OD	I2C3 serial clock
14	GND	-	-	Ground
15	X_JTAG_TMS	3,3 V	I	JTAG test mode select
16	X_JTAG_TRST_B	3,3 V	I	JTAG tap reset
17	X_JTAG_TDI	3,3 V	I	JTAG data in
18	X_JTAG_TDO	3,3 V	O	JTAG data out
19	GND	-	-	Ground
20	X_JTAG_TCK	3,3 V	I	JTAG clock
21	USB_HUB_DP4	Diff	USB_I/O	Positive USB HUB 4 signal
22	USB_HUB_DM4	Diff	USB_I/O	Negative USB HUB 4 signal
23	X_nRESET_IN	3,3 V	OD	Open drain SoM reset input

Interface Pin #	Signal Name	Signal Level	Signal Type	Description
24	GND	-	-	Ground
25	X_SPDIF_TX	3,3 V	O	SPDIF transmit data
26	X_SPDIF_RX	3,3 V	I	SPDIF receive data
27	X_SPDIF_EXT_CLK	3,3 V	O	SPDIF clock
28	X_nPOR_OD	3,3 V	OD	Open drain SoM Power-On Reset output
29	GND	-	-	Ground
30	X_TEST_MODE	3,3 V	I	Test Mode signal (boot signal for i.MX 8M Nano)
31	UART4_RXD	3,3 V	I	UART4 receive data
32	X_SAI1_TXD1 / BOOT_MODE_CFG[9]	3,3 V	I/O	SAI1 transmit data 1
33	UART4_TXD	3,3 V	O	UART4 transmit data
34	GND	-	-	Ground
35	X_SAI1_TXD2 / BOOT_MODE_CFG[10]	3,3 V	I/O	SAI1 transmit data 2
36	X_SAI1_TXD3 / BOOT_MODE_CFG[11]	3,3 V	I/O	SAI1 transmit data 3
37	X_SAI1_TXD4 / BOOT_MODE_CFG[12]	3,3 V	I/O	SAI1 transmit data 4

Interface Pin #	Signal Name	Signal Level	Signal Type	Description
38	X_SAI1_TXD5 / BOOT_MODE_CFG[13]	3,3 V	I/O	SAI1 transmit data 5
39	X_SAI1_TXD6 / BOOT_MODE_CFG[14]	3,3 V	I/O	SAI1 transmit data 6
40	X_CLKIN1	1,8 V	I	Serial clock 1 input
41	GND	-	-	Ground
42	X_CLKOUT1	1,8 V	O	Serial clock 1 output
43	X_POR_IN	3,3 V	I	SoM Power-On Reset input
44	X_ETH_JTAG_TDI	1,8 V	I	Ethernet JTAG data in
45	X_ ETH_JTAG_TMS	1,8 V	I	Ethernet JTAG test mode
46	GND	-	-	Ground
47	X_ ETH_JTAG_TDO	1,8 V	O	Ethernet JTAG data out
48	X_ ETH_JTAG_CLK	1,8 V	I	Ethernet JTAG clock
49	X_ ETH_GPIO1	1,8 V	I/O	Ethernet GPIO1
50	X_CLKIN2	1,8 V	I	Serial clock 2 input
51	GND	-	-	Ground
52	X_CLKOUT2	1,8 V	O	Serial clock 2 output

Interface Pin #	Signal Name	Signal Level	Signal Type	Description
53	USB_HUB_PRTPWR 4	5 V	I	USB HUB 4 power enable
54	USB_HUB_nOSC4	5 V	I	USB HUB 4 over current sense
55	X_RTC_INT	3,3 V	O	RTC interrupt output
56	GND	-	-	Ground
57	VCC_IN_24V	24 V	PWR_I	24 V board input voltage
58	nPOR_IN_DELAYED	3,3 V	O	SoM Power-On Reset delayed
59	GND	-	-	Ground
60	VCC_5V_REG	5 V	PWR_I	5 V supply voltage

Expansion Connector Design Consideration

All signals should be routed as short as possible and as 50 Ohm single-ended lines.

I²C Connectivity

The I²C interfaces of the i.MX 8M Mini are available at different connectors on the phyBOARD-Polis. The following table provides a list of the connectors and pins with I²C connectivity:

56 I2C Connectivity Interface Connections

Interface	Interface Pin #	Signal Name	Signal Level	Signal Type
X18	24	I2C3_SCL	3,3 V	O
X18	22	I2C3_SDA	3,3 V	I/O
X8	13	I2C3_SCL	3,3 V	O
X8	11	I2C3_SDA	3,3 V	I/O

Interface	Interface Pin #	Signal Name	Signal Level	Signal Type
X38	5	I2C3_SCL	3,3 V	O
X38	6	I2C3_SDA	3,3 V	I/O
X10	23	I2C4_SCL	3,3 V	O
X10	24	I2C4_SDA	3,3 V	I/O

Onboard Functionalities

Trusted Platform Module (TPM)

The phyBOARD-Polis is equipped with a Trusted Platform Module (TPM). The TPM is a chip developed, produced, tested, and certified according to the TCG specification that enhances the board with additional security functions. These security functions include the generation and secure storage (in the hardware) of keys for the authentication and identification of communication participants (SSH, server, cloud, etc.) and data, which can also be encrypted.

The TPM requires either an SPI or I^2C interface, depending on the mounted module. The TPM is connected to the SOM through the following interfaces:

57 Trusted Platform Module (TPM) Interface Connections

Pin #	Signal Name	Signal Level	Signal Type	Description
24	X_ECSPI2_MISO	3,3 V	I	SPI2 master in slave out
21	X_ECSPI2_MOSI	3,3 V	O	SPI2 master out slave in
20	X_ECSPI2_SS0	3,3 V	O	SPI2 chip select
19	X_ECSPI2_SCLK	3,3 V	O	SPI2 serial clock
29	X_I2C2_SDA	3,3 V	I/O	I2C2 serial data
30	X_I2C2_SCL	3,3 V	O	I2C2 serial clock
31	X_SD1_RESET_B/ GPIO2_IO10	3,3 V	I/O	TPM reset signal

Pin #	Signal Name	Signal Level	Signal Type	Description
32	X_SD1_STROBE/ GPIO2_IO11	3,3 V	I/O	TPM

Tip

For more information about your security needs, contact a PHYTEC salesperson.

WLAN and Bluetooth Transceiver Module

The phyBOARD-Polis is equipped with a WLAN and Bluetooth Transceiver Module that is capable of providing WLAN and Bluetooth functionality. The module requires a UART with handshake capability and a 4-bit SDIO interface. The module is connected to the SOM through the following interfaces:

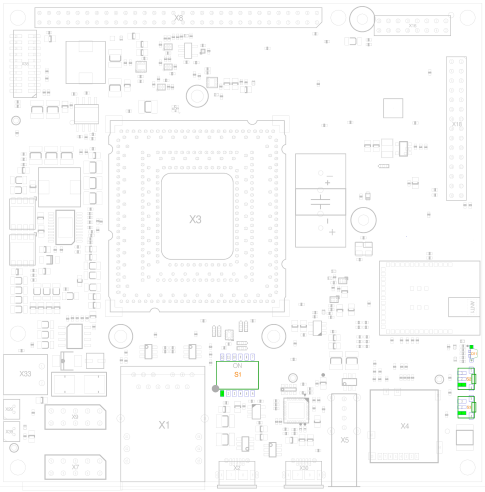
58 Wireless WLAN and Bluetooth Transceiver Module Interface Connections

Interface Pin #	Signal Name	Signal Level	Signal Type	Description
22	X_SD1_DATA0	3,3 V	I/O	SD1 data 0
23	X_SD1_DATA1	3,3 V	I/O	SD1 data 1
25	X_SD1_DATA2	3,3 V	I/O	SD1 data 2
26	X_SD1_CMD	3,3 V	O	SD1 command
27	X_SD1_DATA3	3,3 V	I/O	SD1 data 3
29	X_SD1_CLK	3,3 V	O	SD1 clock
31	X_SAI3_RXD/ UART2_RTS_B	3,3 V	I/O	UART2 request to send
32	X_SAI3_RXC/ UART2_CTS_B	3,3 V	I/O	UART2 clear to send
33	X_SAI3_TXC/ UART2_TX	3,3 V	I/O	UART2 transmit data
34	X_SAI3_TXFS/ UART2_RX	3,3 V	I/O	UART2 receive data

Interface Pin #	Signal Name	Signal Level	Signal Type	Description
21	X_SD1_DATA4	3,3 V	I/O	SD1 data 4
12	X_SD1_DATA5	3,3 V	I/O	SD1 data 5
39	X_SD1_DATA6	3,3 V	I/O	SD1 data 6
40	X_SD1_DATA7	3,3 V	I/O	SD1 data 7

LEDs and Switches

22 phyBOARD-Polis Switches and LED Locations



Multicolor (RGB) LED (D11)

The phyBOARD-Polis provides one multicolor (RGB) LED (D11). The table below shows the signals that control colors:

59 Multicolor LED Configuration

Color	Signal	Description
Red	X_GPIO1_IO00	PWM output for red LED
Green	X_PWM3/GPIO1_IO14	PWM3 output for red LED
Blue	X_PWM4/GPIO1_IO15	PWM4 output for red LED

LED Design Consideration

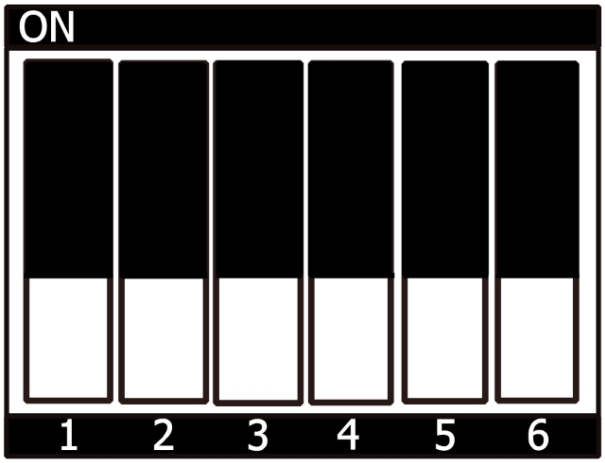
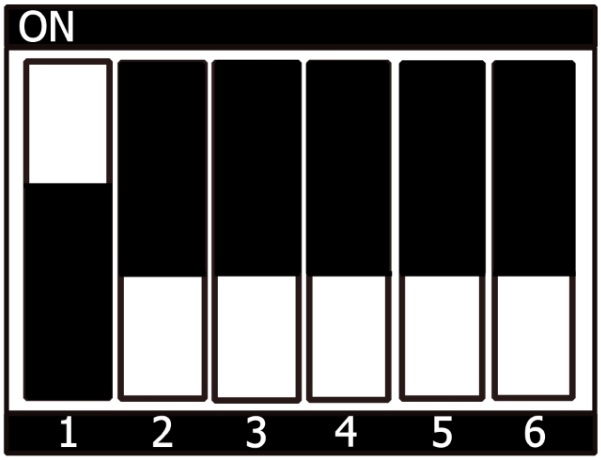
All signals should be routed as short as possible and as 50 Ohm single-ended lines.

Switches

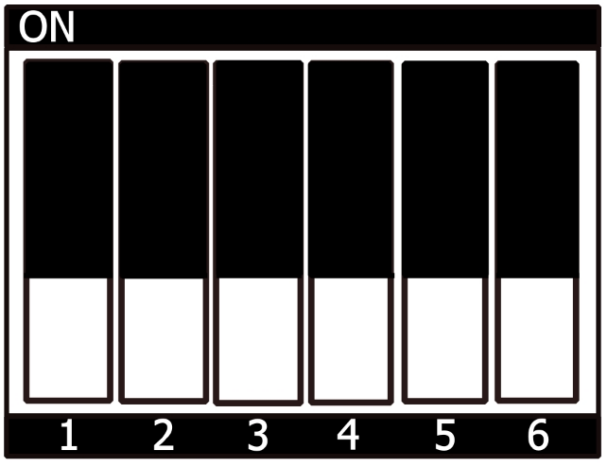
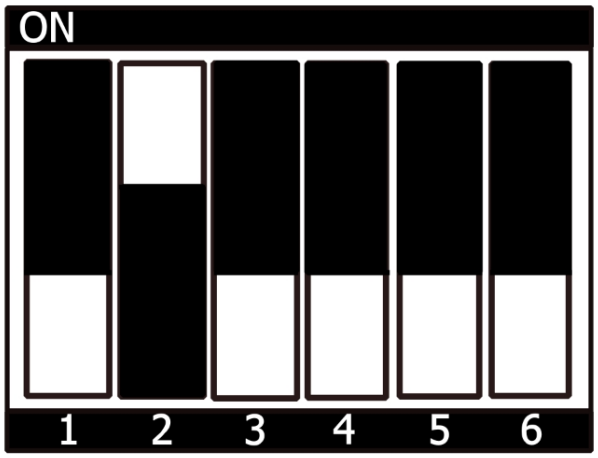
Multi-port Switch (S1)

The phyBOARD-Polis features a multi-port switch with six individually switchable ports. This switch controls the SOM boot mode, SOM boot configuration, UART functionality, and USB configuration when i.MX 8M NANO is mounted on the carrier board. The figures below show a visual representation of each S1 switch setting:

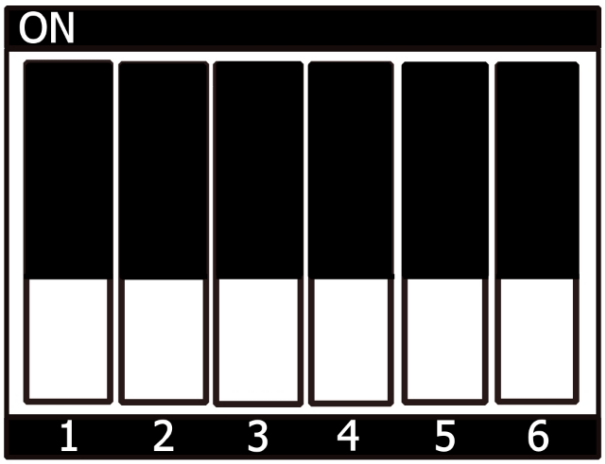
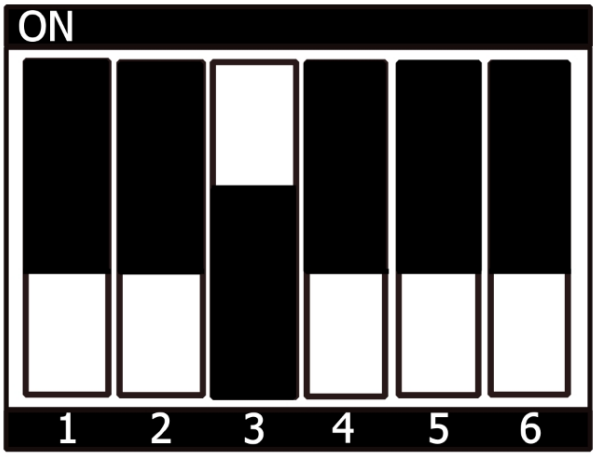
60 S1 - Switch 1

	
Default SOM Boot	***Alternate boot mode***

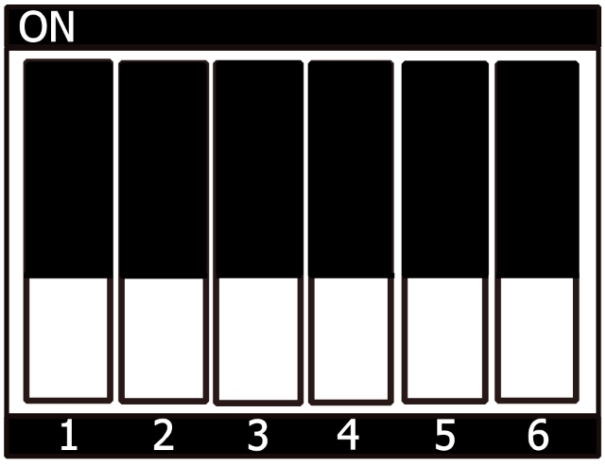
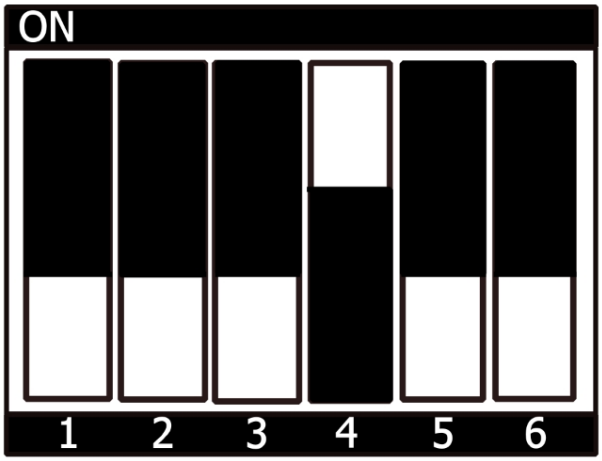
61 S1 - Switch 2

	
SD-Card boot	***QSPI boot***

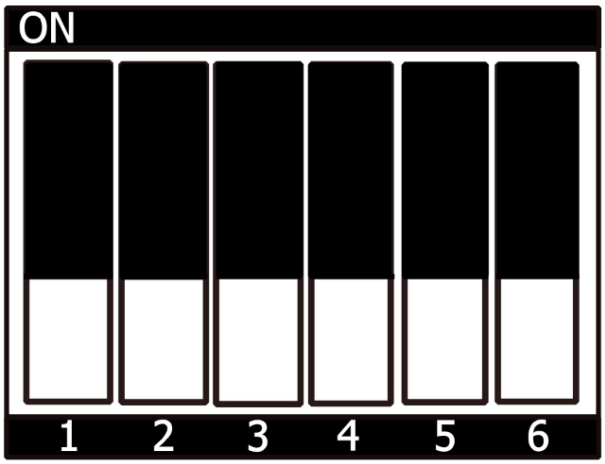
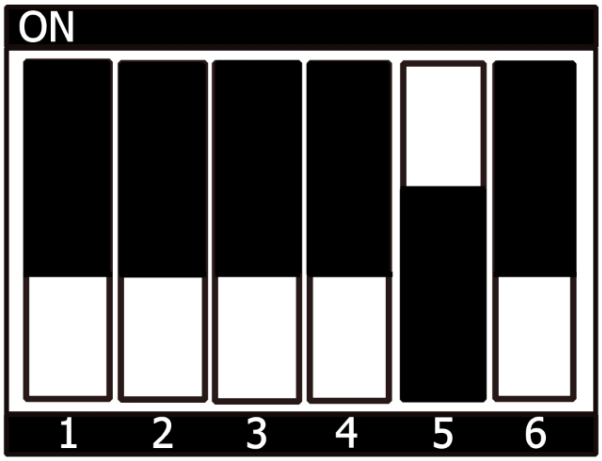
62 S1 - Switch 3

	
Internal boot (eMMC, SD-Card, and QSPI)	***Serial downloader (USB boot)***

63 S1 - Switch 4

	
UART1 to RS232	***UART1 to RS485***

64 S1 - Switch 5 (i.MX 8M NANO only)

	
USB NANO OTG port	***USB NANO HUB***

65 Boot Switch Configuration Options (S1)

Switch Nr.:	Off position	On position
1	Default SoM boot	Alternate boot mode (SD-Card and QSPI)
2	SD-Card boot	QSPI boot
3	Internal boot (eMMC, SD-Card, and QSPI)	Serial downloader (USB boot)
4	UART1 to RS232 conversion	UART1 to RS485 conversion
5	i.MX 8M NANO: USB interface connected to phyBOARD-POLIS USB HUB U2 and USB Type-A X5	i.MX 8M NANO: USB interface connected to phyBOARD-POLIS OTG port X2
6	Not connected	Not connected

Boot Mode Design Considerations

All signals should be routed as short as possible and as 50 Ohm single-ended lines.

System Reset Button (S2)

The phyBOARD-Polis is equipped with a system reset button at S2. Pressing this button will toggle the X_nRESET_IN pin (C43) of the phyCORE-i.MX 8M Mini low, causing the module to reset with a complete power cycle. For more information regarding a manual reset, refer to Reset.

System ON/OFF Button (S1)

The phyBOARD-Polis is equipped with an ON/OFF button at S3. For more information on the ON/OFF switch, refer to the *i.XM 8M Mini Reference Manual*.

Revision History

66 Revision History

Date	Version Numbers	Changes in this Manual
25.10.2019	Manual L-862e.A0	Preliminary Edition. Describes the phyCORE-i.MX 8M Mini SOM Version: 1518.1a Describes the phyBOARD-Polis PCB Version: 1532.0
03.07.2020	L-862e.A1	PCB Revision: 1532.1 Updated PCB Figures and content Section: Power Consumption Updated
21.04.2021	L-862e.A2	Added section: Unused Signals Updated section: System Boot Configuration • Updated section: i.MX 8M Mini System Boot Settings • Added section: i.MX 8M Nano System Boot Settings
05.07.2022	L-862e.A3	PDF Version available
21.03.2025	L-862e.A4	SoM Version: 1518.6 PCB Version: 1532.4 Updated: • Low Power Modes • Antenna Module • Manual Formatting

Contact Information

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