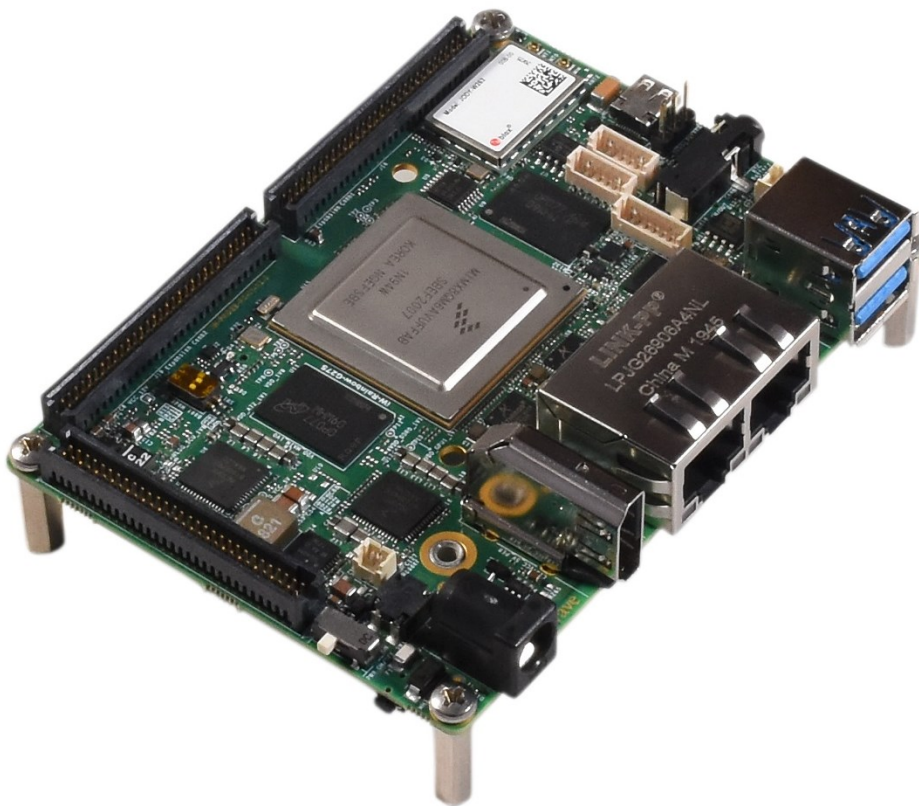


iW-RainboW-G27S

i.MX 8 QuadMax/QuadPlus

Pico ITX Single Board Computer

Hardware User Guide



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1. INTRODUCTION

1.1 Purpose

This document is the Hardware User Guide for the Pico ITX Single Board computer based on the NXP's i.MX 8 QM/QP (QuadMax/QuadPlus) Application processor. This board is fully supported by iWave Systems Technologies Pvt. Ltd. This Guide provides detailed information on the overall design and usage of the i.MX 8 QM/QP PICO ITX SBC from a Hardware Systems perspective.

1.2 Pico ITX SBC Overview

The Pico ITX is a versatile small form factor SBC (Single Board Computer) definition targeting application that requires low power, low costs, and high performance. The SBCs are used as building blocks for portable and stationary embedded systems. The core CPU and support circuits, including DRAM, boot flash, power sequencing, CPU power supplies, GBE and dual channel LVDS/MIPI display transmitter are concentrated on the Module.

NXP's i.MX 8 SoC based Pico ITX Single Board computer is rich with i.MX 8 features along with, eMMC, Dual Ethernet PHY, USB3.0 Hub, Wi-Fi & BT module and comes in compact 100mm x 72mm form factor.

1.3 List of Acronyms

The following acronyms will be used throughout this document.

Table 1: Acronyms & Abbreviations

Acronyms	Abbreviations
ARM	Advanced RISC Machine
BT	Bluetooth
CAN	Controller Area Network
CODEC	Coder-Decoder
CPU	Central Processing Unit
CSI	Camera Serial Interface
CTS	Clear to Send
DP	Display Port
DRAM	Dynamic Random-Access Memory
DSI	Display Serial Interface
eDP	Embedded Display Port
eMMC	Enhanced Multi Media Card
EMS	Electronics manufacturing services
ESAI	Enhanced Serial Audio Interface
FIFO	First In First Out
FLEXCAN	Flexible Control Area Network
FlexSPI	Flexible Serial Peripheral Interface

Acronyms	Abbreviations
GB	Giga Byte
Gbps	Gigabits per sec
GPIO	General Purpose Input Output
GPU	Graphics Processing Unit
HDCP	High-bandwidth Digital Content Protection
HDMI	High-Definition Multimedia Interface
I2C	Inter-Integrated Circuit
I2S	Inter-Integrated Sound
IC	Integrated Circuit
JTAG	Joint Test Action Group
LPDDR4	Low Power Double Data Rate4
MHz	Mega Hertz
MIPI	Mobile Industry Processor Interface
MLB	Media Local Bus
OTG	On-The-Go
PCB	Printed Circuit Board
PCIe	Peripheral Component Interconnect express
PMIC	Power management integrated circuits
RAM	Random Access Memory
RGMI	Reduced gigabit media-independent interface
RoHS	Restriction of Hazardous Substances
RTC	Real Time Clock
RTS	Request to Send
SAI	Serial Audio Interface
SATA	Serial Advanced Technology Attachment
SD	Secure Digital
SDIO	Secure Digital Input Output
SoC	System on Chip
SBC	Single Board Computer
SPDIF	The Sony/Philips Digital Interface
SPI	Serial Peripheral Interface
UART	Universal Asynchronous Receiver/Transmitter
USB	Universal Serial Bus
VPU	Video Processing Unit
Wi-Fi	Wireless Fidelity

1.4 Terminology Description

In this document, wherever Signal Type is mentioned, below terminology is used.

Table 2: Terminology

Terminology	Description
I	Input Signal
O	Output Signal
IO	Bidirectional Input/output Signal
CMOS	Complementary Metal Oxide Semiconductor Signal
HCSL	High speed Current Steering Logic
LVDS	Low Voltage Differential Signal
HDMI	High-Definition Multimedia Interface Differential Signal
DP	Display Port Differential Signal
GBE	Gigabit Ethernet Signal
PCIe	PCIe differential pair signals
SATA	Serial Advanced Technology Attachment differential pair signals
USB HS	Universal Serial Bus High Speed differential pair signals
USB SS	Universal Serial Bus Super Speed differential pair signals
MIPI	Mobile Industry Processor Interface differential pair signals
OD	Open Drain Signal
OC	Open Collector Signal
Power	Power Pin
PU	Pull Up
PD	Pull Down
NA	Not Applicable
NC	Not Connected

Note: Signal Type does not include internal pull-ups or pull-downs implemented by the chip vendors and only includes the pull-ups or pull-downs implemented On-SBC.

1.5 References

- iMX8QMAEC_Rev0.pdf
- iMX8QM_RM_Rev_F.pdf

1.6 Important Note

In this document, wherever i.MX 8 QM/QP CPU signal name is mentioned, it is followed as per below format for easy understanding.

- If CPU pin doesn't have multiplexing option or used for dedicated functionality then the signal name is mentioned as functionality name.

"Functionality Name"

Example: ENET1_RGMII_TXC

In this signal, ***ENET1_RGMII_TXC*** pad is used for same functionality.

- If CPU pin selected as GPIO function, then the signal name is mentioned as

"Functionality Description (GPIO Number)"

Example: BCONFIG_0(GPIO1_05)

In this signal, ***BCONFIG_0*** is the GPIO functionality and ***GPIO1_05*** is the GPIO number.

Note: The above naming is not applicable for other signals which are not connected to CPU.

2.2 i.MX 8 QM/QP PICO ITX SBC Features

i.MX 8 QM/QP PICO ITX SBC supports the following features.

CPU

- i.MX 8 QM/QP Processor¹:
 - i.MX 8 QuadMax : 2 x Cortex-A72, 4 x Cortex-A53 & 2 x Cortex-M4F
 - i.MX 8 QuadPlus : 1 x Cortex-A72, 4 x Cortex-A53 & 2 x Cortex-M4F

Power

- PF8100 PMIC x 2

Memory

- LPDDR4 - 4GB (Expandable up to 8GB)^{2,3}
- eMMC Flash – 16GB (Expandable up to 256GB)³
- Micro SD slot

Network & Communication

- Gigabit Ethernet PHY Transceiver with RJ45 Magjack Connector x 2
- USB 3.0 High Speed Hub through dual stack Type-A Connector
- USB3.0 Header (Optional)
- USB 2.0 OTG port through - micro AB Receptacle Connector
- Wi-Fi 1x1 802.11a/b/g/n/ac/ax in 2.4 GHz or 5 GHz⁴
- RS232 x 1
- CAN x 1

Audio/Video Features

- HDMI Output through HDMI (Type A) Connector⁵
- HDMI Input through micro HDMI (Type D) Connector
- 40Pin eDP Display Connector (Optional)⁴
- I2S Audio Codec
- 3.5mm Audio IN/OUT
- Line In Header (Optional)

Expansion Connector Interfaces

- Expansion Connector 1
 - 4 lane MIPI DSI x 1
 - 4 lane LVDS x 2
 - CAN/SPDIF x1 Port
 - DMA_I2C/USB2.0 x 1 Port
 - SPI x 1 Port
 - PWM x1 Port
- Expansion Connector 2
 - 4 lane MIPI CSI x 1
 - 4 lane LVDS x 2
 - LVDS I2C x 1 Port
 - MIPI CSI I2C x 1 Port
 - PWM x1 Port
 - SPI x 1 Port
 - M41 UART x 1 Port
- Expansion Connector 3
 - 4 lane MIPI CSI x 1
 - MIPI CSI I2C x 1 Port
 - 4 lane MIPI DSI x 1
 - DMA_I2C x 1 Port
 - SAI (Receive Mode) x1 Port
 - QSPI x 1 Port
 - CAN x 1 Port
 - M40 UART x 1 Port
 - UART x 1 Port

Miscellaneous Interfaces

- Debug UART Connector
- JTAG Header (Optional)
- TAMPER Header (Optional)
- External RTC Controller (Optional)
- RTC Battery Connector
- M.2 Connector Key B
 - PCIe x2
 - SATA x 1

- USB 3.1 x 1
- I2S x 1
- I2C x 1
- HSIC x 1(Optional)
- Nano SIM Connector

Power Supply:

- 12V, 2A input through External Adaptor

Temperature Support:

- -40°C to +85°C Industrial

Environment Specification

- RoHS2 and REACH Compliance

Form Factor:

- 100mm X 72mm (Pico ITX Specification)

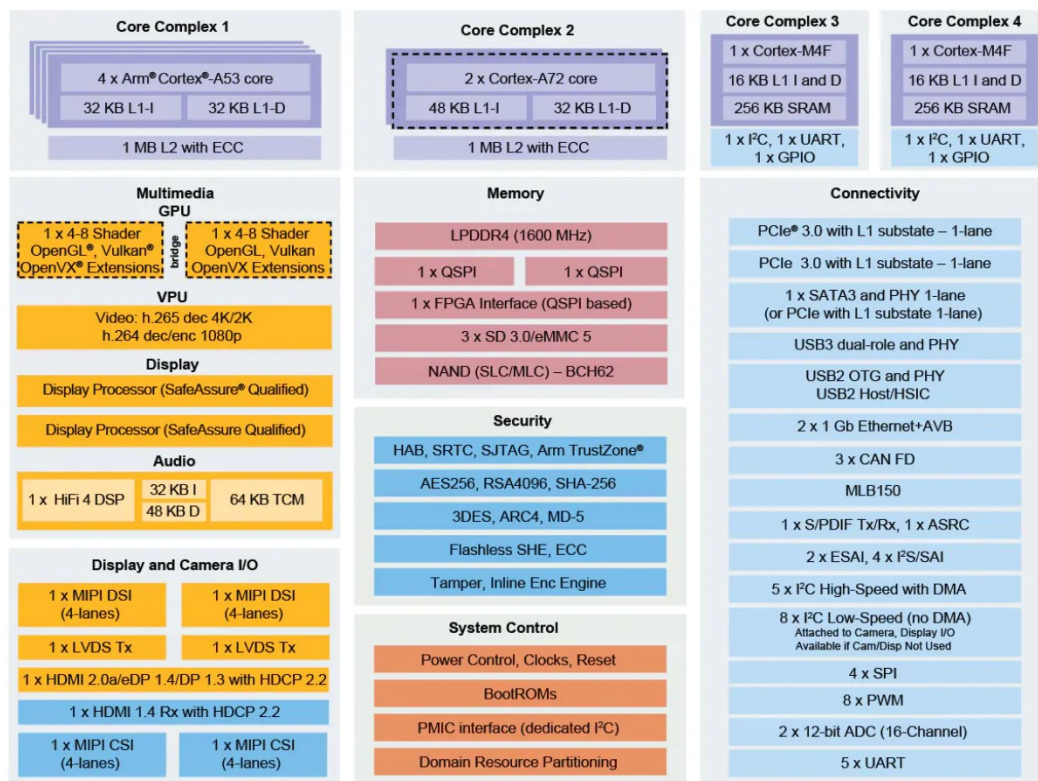
- ^{1.} *There are two configurations of i.MX 8 Processor, hence in this document i.MX 8 is used to represent either i.MX 8 QM or i.MX 8 QP based on the Part Number.*
- ^{2.} *The i.MX 8 can support up to 16GB RAM but considering available LPDDR4 configuration, it can support 8GB by using two 4GB chips. If 8GB (64Gb) chips are available then 16GB DDR can be supported.*
- ^{3.} *Memory Size will differ based on iWave's Product Part Number.*
- ^{4.} *802.11ax is supported only in JODY-W3 Module.*
- ^{5.} *The i.MX 8 support HDMI or eDP through same pins, hence any one can be supported at a time based on the SBC part Number.*

2.3 i.MX 8 CPU

iW-RainboW-G27S PICO ITX SBC can support i.MX 8 CPUs from NXP. The i.MX 8 Family consists of two processors: i.MX 8 Quad Max & iMX8 Quad Plus. The Major Difference between i.MX 8 CPUs are:

- i.MX 8 QuadMax : 2 x Cortex-A72, 4 x Cortex-A53 & 2 x Cortex-M4F
- i.MX 8 QuadPlus : 1 x Cortex-A72, 4 x Cortex-A53 & 2 x Cortex-M4F

The i.MX 8 QuadMax/QuadPlus processors support ARM Cortex-A72 Core @ 1.6 GHz, ARM Cortex-A53 Core @ 1.2 GHz, ARM Cortex-M4F Core @ 264 MHz, dual 32-core GPU subsystems, 4K, H.265 capable VPU, and dual failover-ready display controllers, 2x 4K displays, supporting multiple display output options, including MIPI-DSI, HDMI 2.0, eDP/DP, and LVDS. Memory interfaces supporting LPDDR4, DDR4, Quad SPI/Octal SPI (FlexSPI), eMMC 5.1, RAW NAND and SD 3.0, and a wide range of peripheral I/Os such as PCIe 3.0 provide wide flexibility.



Available on certain product families Note: Accessing muxable controller's full capabilities is dependent upon board component choices.

Figure 2: i.MX 8 Block Diagram

Note: The i.MX 8 QuadMax/QuadPlus processor offers numerous advanced features, please refer the latest i.MX 8 Datasheet & Reference Manual for Electrical characteristics and other information, which may be revised from time to time.

2.4 PF8100 PMIC

i.MX 8 QM/QP PICO ITX SBC uses two PF8100/PF8200 PMIC for SBC Power management. Both the PF8100 PMIC are programmed with custom Sequence code EQ and ES from NXP.

The PF8100 is a power management integrated circuit (PMIC) features seven high efficiency buck converters and four linear regulators for powering the processor, memory and miscellaneous peripherals. Built-in one-time programmable memory stores key start up configurations, drastically reducing external components typically used to set output voltage and sequence of external regulators. Regulator parameters are adjustable through high-speed 3.4 MHz I2C after start up offering flexibility for different system states. The PF8100 PMIC U6 (EQ) & U16 (ES) comes in 56pin 8x8 QFN Packages and are placed on the Top side of the SBC.

2.5 Boot Media Setting Switch

i.MX 8 QM/QP PICO ITX SBC supports two positions Boot Media Switch (SW1) which is physically located in the top of the PCB. This switch is used to select the boot media of i.MX 8 QM/QP. i.MX 8 QM/QP PICO ITX SBC supports two boot media options for booting i.MX 8 QM/QP as mentioned in the below table.

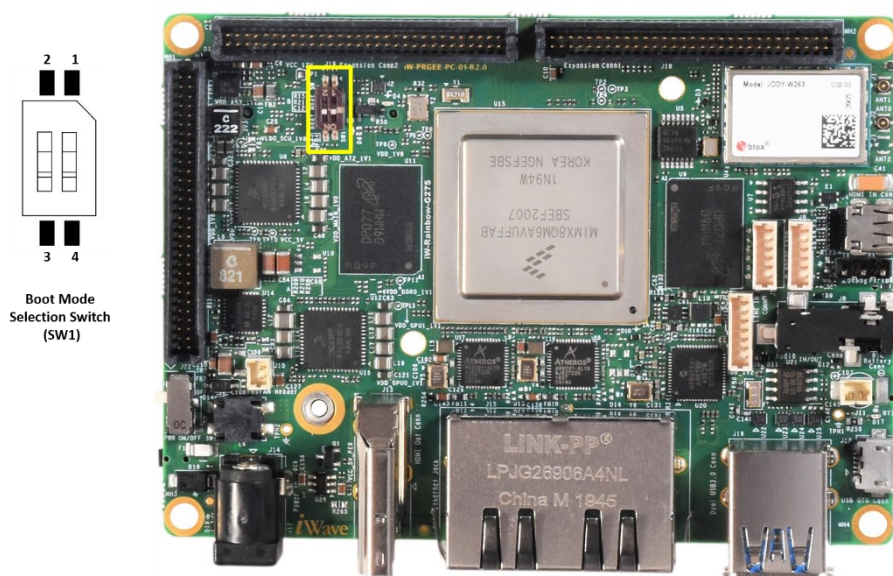


Figure 3: Boot Media Switch

Table 3: Boot Media Settings

Boot Media	SW1 (2 Position Switch)	
	POS1	POS2
Boot from Fuse	OFF	OFF
USB Serial Download	OFF	ON
eMMC	ON	OFF
uSD	ON	ON

2.6 Memory

2.6.1 LPDDR4 RAM

The i.MX 8 QM/QP PICO ITX SBC supports 4GB RAM using two 32bit 2GB LPDDR4 IC connected to DDR_CH0 and DDR_CH1 channels of CPU to support LPDDR4 up to 1.6 GHz. Both the LPDDR4 parts U11 and U9 are placed on Top side of the SBC. LPDDR4 memory size can be customised based on the requirement by contacting iWave support team.

2.6.2 eMMC Flash

The i.MX 8 QM/QP PICO ITX SBC supports 16GB eMMC as default boot and storage device. This is connected to eMMC0 version 5.1 controller of the i.MX 8 QM/QP CPU and operates at 1.8V (I/O supply) and 3.3V (NAND core supply) Voltage levels.

The eMMC flash (U39) memory is physically located on bottom side of the SBC. The memory size of the eMMC Flash can be customised based on the requirement by contacting iWave Support Team.

2.6.3 Micro SD Connector

The i.MX 8 QM/QP PICO ITX SBC supports Micro SD connector which can be used to connect Micro SD card as optional boot device as well as Mass storage device. Micro SD card connector (J21) is connected to the USDHC1 controller of the i.MX 8 CPU. The main power to Micro SD Card Connector is 3.3 Voltage. The i.MX 8 QM/QP PICO ITX SBC supports configurable I/O voltage levels for USDHC1 lines through LDO2OUT of PMIC1. The I/O voltage level of USDHC2 lines can be set 1.8V or 3.3V based on PMIC configuration. And the micro SD Connector is physically located on Bottom side of the i.MX 8 QM/QP PICO ITX SBC as shown below.

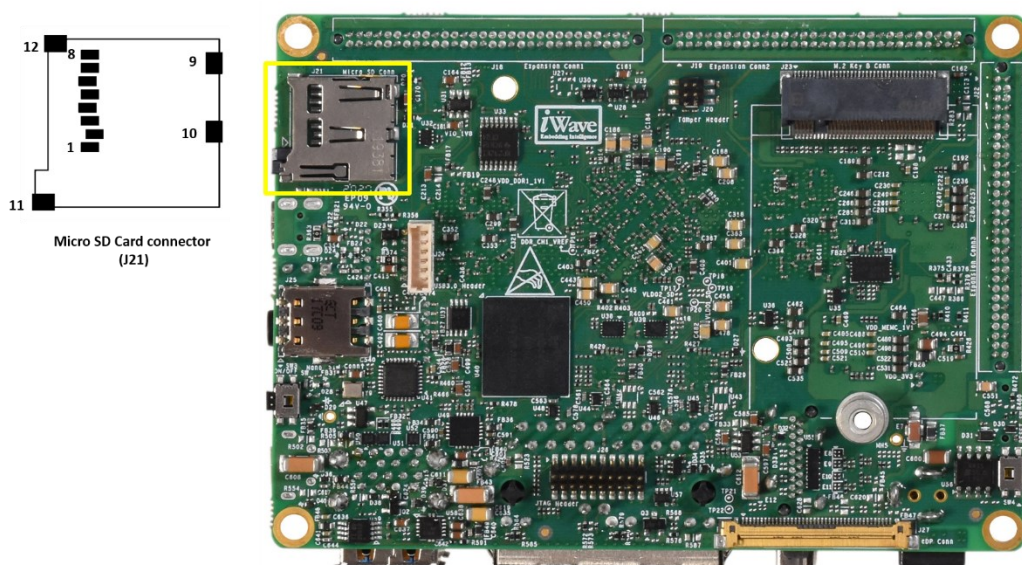


Figure 4: Micro SD Connector

2.7 Network & Communication

2.7.1 Wi-Fi and Bluetooth Interface

The i.MX 8 QM/QP PICO ITX SBC is integrated with u-blox's "JODY-W263" or "JODY-W374" based Wi-Fi & Bluetooth module. The JODY-W2/W3 series are compact modules based on the Marvell 88W8987 AEC-Q100 compliant chipset. They enable Wi-Fi, Bluetooth, and Bluetooth low energy communication. The JODY-W2 modules can be operated in the following modes:

- Wi-Fi 1x1 802.11a/b/g/n/ac in 2.4 GHz or 5 GHz
- Dual-mode Bluetooth 5, including audio, can be operated fully simultaneous with Wi-Fi

The JODY-W3 modules can be operated in the following modes:

- Wi-Fi6 802.11a/b/g/n/ac/ax in 2.4 GHz or 5 GHz
- Bluetooth/Bluetooth LE 5.1 including audio, can be operated fully simultaneous with Wi-Fi

The JODY-W2 undergoes extended automotive qualification according to ISO 16750-4 and is manufactured in line with ISO/TS 16949. Connection to a host processor is through SDIO, or High-Speed UART interfaces. The i.MX 8 QM/QP PICO ITX SBC uses processor's UART1 interface for Bluetooth and USDHC2 interface for Wi-Fi in a default configuration. In the i.MX 8 QM/QP PICO ITX SBC, antenna pins of JODY-W263 Bluetooth and Wi-Fi are connected to J1 and J2 connector respectively.

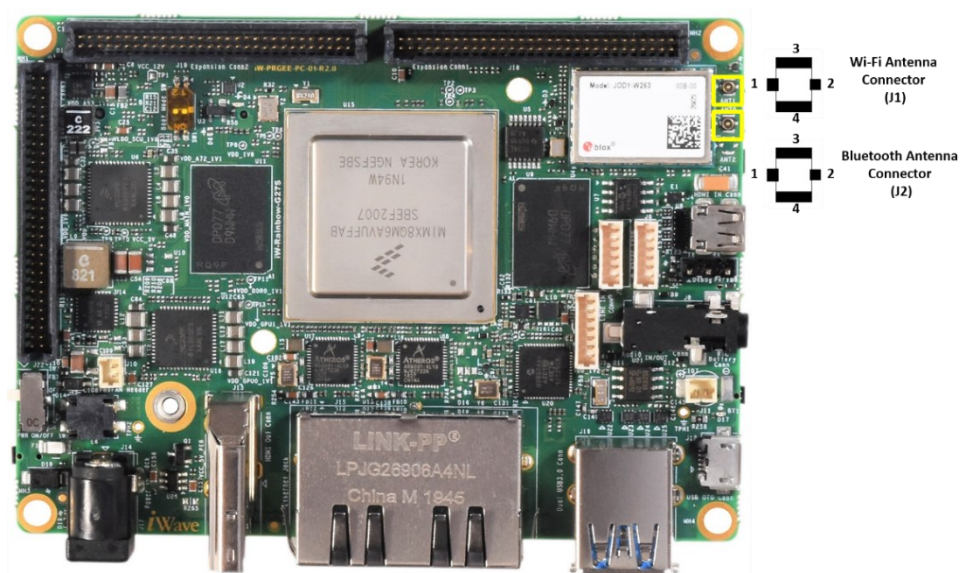


Figure 5: Wi-Fi and Bluetooth Antenna Connector

Connector Part Number - : RECE-20449-001E-01 from Taoglas Limited / MM4829-2702RA4 from Murata

Antenna Part Number - : FXP830.24.0100B from Taoglas Limited / 2042811100 from Molex

Note: Contact iWave support team if JODY-W3 Support is required.

2.7.2 Gigabit Ethernet Interface

The i.MX 8 QM/QP PICO ITX SBC supports Dual Ethernet Port interface through Dual external ethernet PHY from Atheros, Qualcomm which supports 10/100/1000Mbps Ethernet. The AR8031 integrates Atheros Green ETHOS® power saving technologies and significantly saves power not only during the work time, but also overtime. Atheros Green ETHOS® power savings include ultra-low power in cable unplugged mode or port power down mode, and automatic optimized power saving based on cable length. The AR8031 also supports IEEE 802.3az EEE standard (Energy Efficient Ethernet) and Atheros proprietary SmartEEE. The SmartEEE allows legacy MAC/SoC devices without 802.3az support to function as a complete 802.3az system. Further, the AR8031 supports Wake-on-LAN (WoL) feature to be able to help manage and regulate total system power requirements.

The Ethernet PHY's output signals GBE0 and GBE1 are directly connected to RJ45 Magjack (J15), Left & Right connector respectively. Also, it supports Speed (Yellow) and Link/Activity (Green) LED indications on RJ45 Magjack. The RJ45 Magjack combo connector is physically located at the top of the board as shown below.

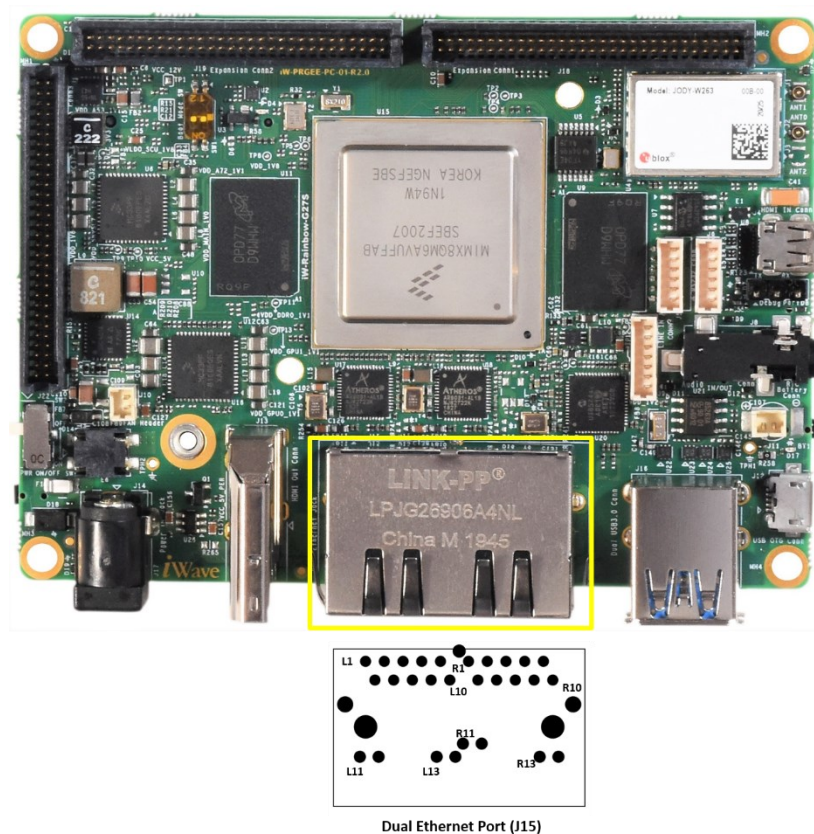


Figure 6: Dual RJ45 Magjack

2.7.3 USB3.0 Host Interface

The i.MX 8 QM/QP PICO ITX SBC supports Super Speed USB3.0 Host interface through USB3.0 hub USB5744-I/2G from Microchip along USB3.0 Hub. The channel 1 and channel 2 signals from USB5744-I/USB hub is directly connected to Bottom and Top port of Dual stack USB3.0 Type-A connector (J16) respectively.

The Dual stack USB3.0 Type-A connector is physically located at the top of the board as shown below.

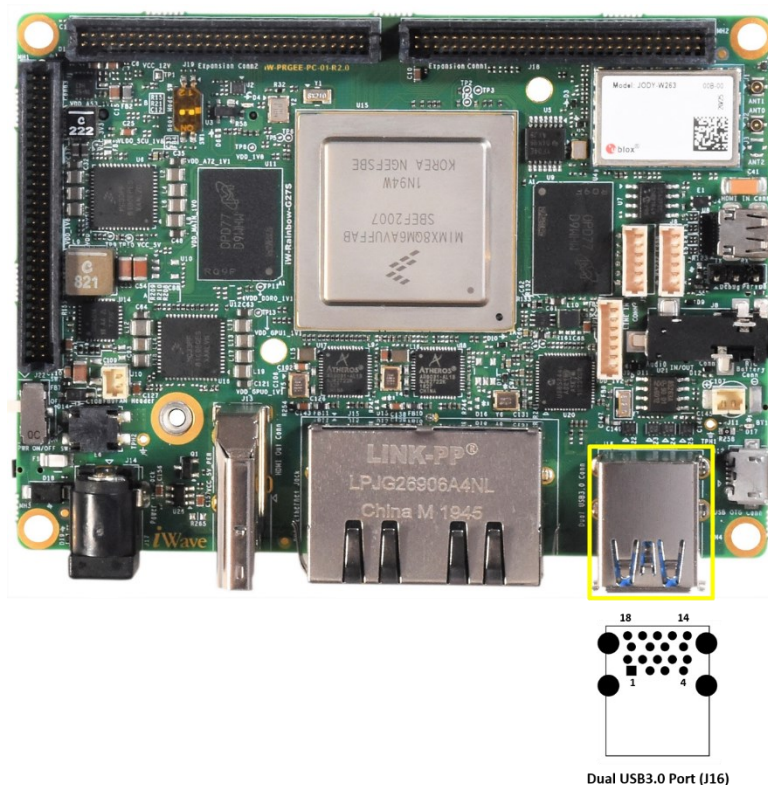


Figure 7: Dual Stack USB3.0 Type A connector

2.7.4 USB3.0 Header (Optional)

The i.MX 8 QM/QP PICO ITX SBC optionally supports one Super Speed USB3.0 Host interface through USB3.0 hub USB5744-I/2G from Microchip along USB3.0 Hub. The channel-4 signals from USB5744-I/USB hub are directly connected to 1.27mm Standard USB3.0 Header (J24).

Table 4: USB3.0 Header Pinout

Pin No	Pin Name	Signal Name	Signal Type/Termination	Description
1	VCC_5V	VCC_5V	O, 5V Power	5V Supply Voltage.
2	RXM	USB3_HUB4_RXM	IO, DIFF	USB 3.0 Receive Negative Pair.
3	RXP	USB3_HUB4_RXP	IO, DIFF	USB 3.0 Receive Positive Pair.
4	TXM	USB3_HUB4_TXM	IO, DIFF	USB 3.0 Transmit Negative Pair.
5	TXP	USB3_HUB4_TXP	IO, DIFF	USB 3.0 Transmit Positive Pair.
6	GND	GND	Power	Ground.

Number of Pins: 6

Connector Part number: 53047-0610 from Molex

Mating Connector: 0510210600 from Molex with crimping pins

Note: Contact iWave support team if USB3.0 Header Support is required.

2.7.5 USB2.0 OTG Interface

The i.MX 8 QM/QP PICO ITX SBC USB2.0 High Speed OTG interface through i.MX 8 CPU's USB0 interface. This USB2.0 Port0 signals of i.MX 8 QM/QP CPU is directly connected to USB2.0 MicroAB connector (J12). This port can be used as USB OTG functionality which supports USB host and USB device based on USB ID pin status. This USB2.0 OTG connector is physically located at the top of the board as shown below

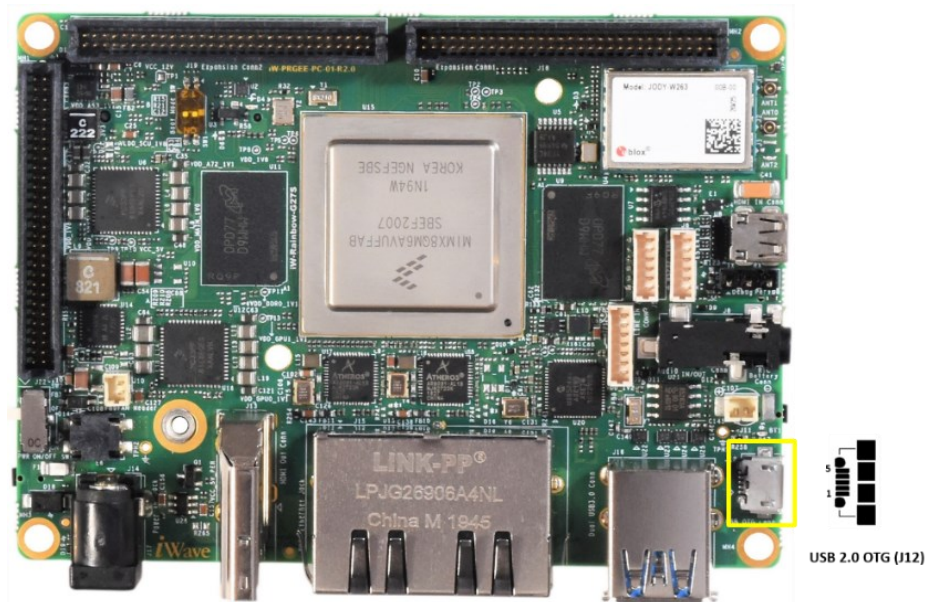


Figure 8: USB 2.0 OTG connector

The VBUS power of this USB2.0 connector is connected through current limit power switch which can be used to switch On/Off the power based on the device or Host and also limits the current above 500mA in host mode. The connected SBC detects the USB functionality through USB ID pin and controls the power using the USB0_EN_OC# pin of IMXQM/QP CPU. In Host mode, USB0_EN_OC# should drive high to enable the power to the connector and in device mode, USB0_EN_OC# should drive low to disable the power to the connector

2.7.6 CAN Interface

The i.MX 8 QM/QP PICO ITX SBC supports a Control Area Network (CAN) Port. CAN0 of the i.MX 8 QM/QP CPU is connected to MCP2562FD-E/SN CAN Transceiver and CANL & CANH of the transceiver are connected to J5 (CAN1) connector.

Number of Pins: 6

Connector Part number: 53047-0610 from Molex

Mating Connector: 0510210600 from Molex with crimping pins

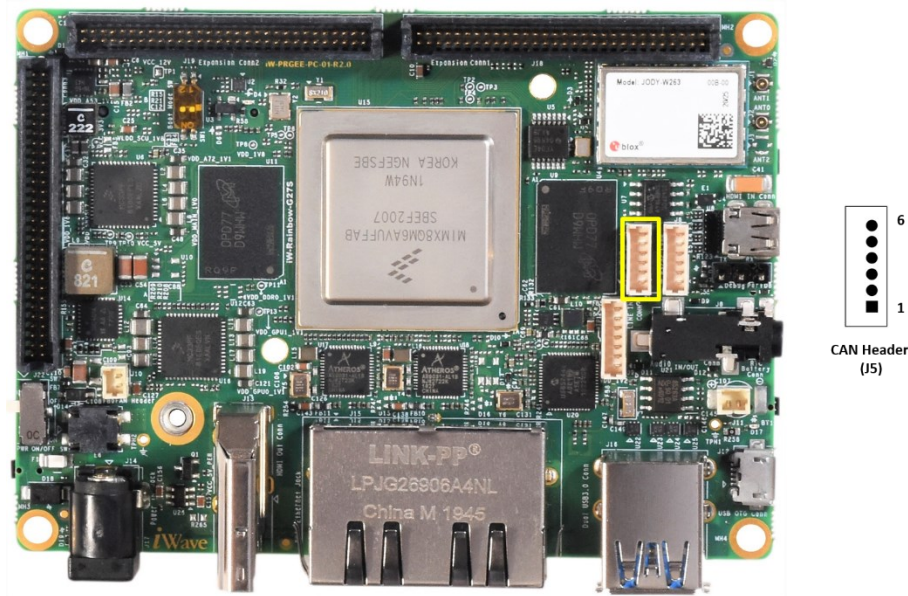


Table 5: CAN Header Pinout

Pin No	Pin Name	Signal Name	Signal Type/ Termination	Description
1	VCC_5V	VCC_5V	O, 5V Power	5V Supply Voltage.
2	NC	NC	NA	NC.
3	CANL	CAN0_LOW	IO, DIFF	CAN0 Low-Level Voltage I/O
4	GND	GND	Power	Ground.
5	CANH	CAN0_HIGH	IO, DIFF	CAN0 High-Level Voltage I/O
6	GND	GND	Power	Ground.

2.8 Serial Interface Features

2.8.1 Debug UART Interface

The i.MX 8 QM/QP PICO ITX SBC supports debug interface through i.MX 8 CPU's UART4 interface. The UART4 signals from i.MX 8 QM/QP CPU connector is connected to Debug UART header(J7) through a 1.8V to 3.3V level Translator. This Debug UART header can be used for Debug purpose, which is physically located at the top of the board as shown below.

Number of Pins: 3

Connector Part number: M20-9990345 from Harwin

USB to UART Cable: TTL-232R-RPI from FTDI

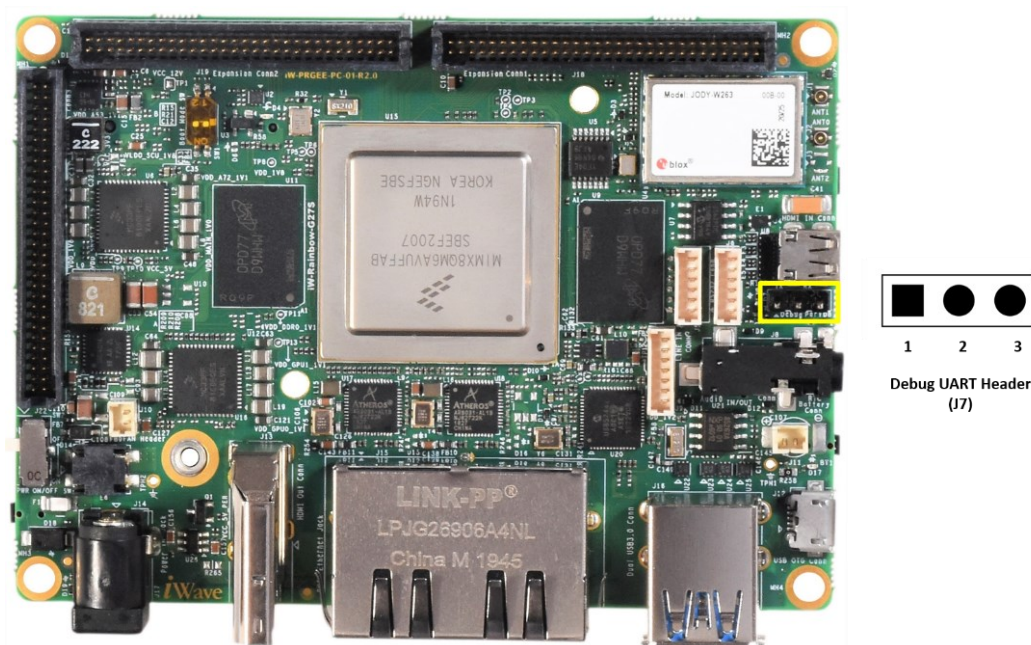


Figure 10: Debug UART Header

Table 6: Debug UART Header Pinout

Pin No	Pin Name	Signal Name	Signal Type/ Termination	Description
1	UART_TXD	UART4_TX	O, 3.3V CMOS	UART interface Transmit signal.
2	UART_RXD	UART4_RX	I, 3.3V CMOS	UART interface Receive signal.
3	GND	GND	Power	Ground.

2.8.2 RS232 Data UART Interface

The i.MX 8 QM/QP PICO ITX SBC supports RS232 Data Interface through i.MX 8 CPU's UART0 interface. This UART0 signals from i.MX 8 QM/QP CPU connector is connected to "MAX3232" RS-232 Line Driver and Receiver via 1.8V to 3.3V level Translator. The RS232 Signals from MAX3232 are connected to RS232 Header(J6), which is physically located at the top of the board as shown below.

Number of Pins: 6

Connector Part number: 53047-0610 from Molex

Mating Connector: 0510210600 from Molex with crimping pins

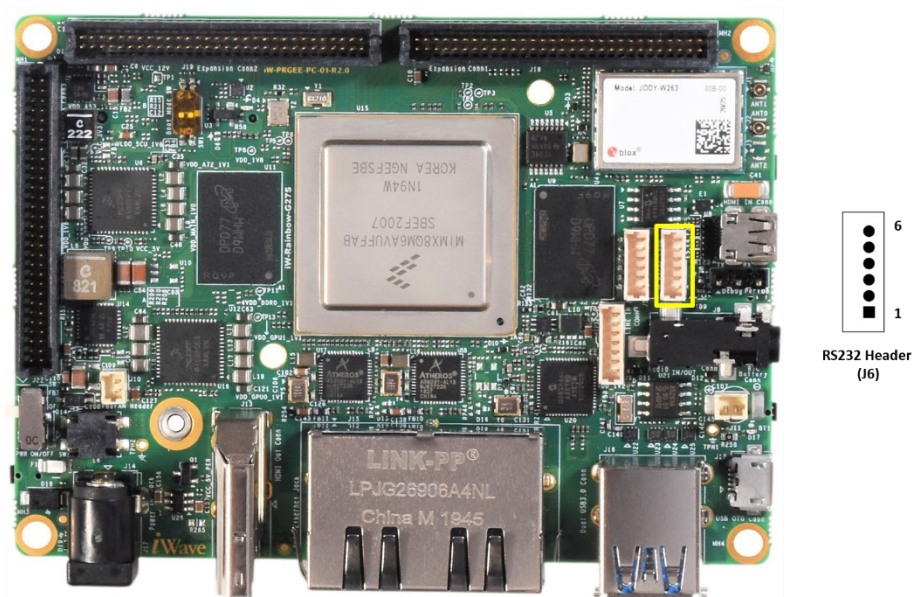


Figure 11: RS232 Data UART Header

Table 7: RS232 Data UART Header Pinout

Pin No	Pin Name	Signal Name	Signal Type/ Termination	Description
1	GND	GND	Power	Ground.
2	CTS	RS232_RTS	I, RS232	RS232 interface Ready to Send signal.
3	VCC	VCC_3V3	O, 3.3V Power	NC <i>Optional 3.3V Supply Voltage.</i>
4	TXD	RS232_RXD	I, RS232	RS232 interface Transmit signal.
5	RXD	RS232_TXD	O, RS232	RS232 interface Receive signal.
6	RTX	RS232_CTS	O, RS232	RS232 interface Clear to Send signal.

2.9 Audio/Video Features

2.9.1 HDMI Output Interface

i.MX 8 QM/QP PICO ITX SBC supports HDMI 2.0 audio/video out. HDMI Signals from the i.MX 8 QM/QP CPU is connected to Standard HDMI Type-A Flag connector with ESD protection circuitry. HDMI Output connector (J13) is physically located on top of the board as shown below

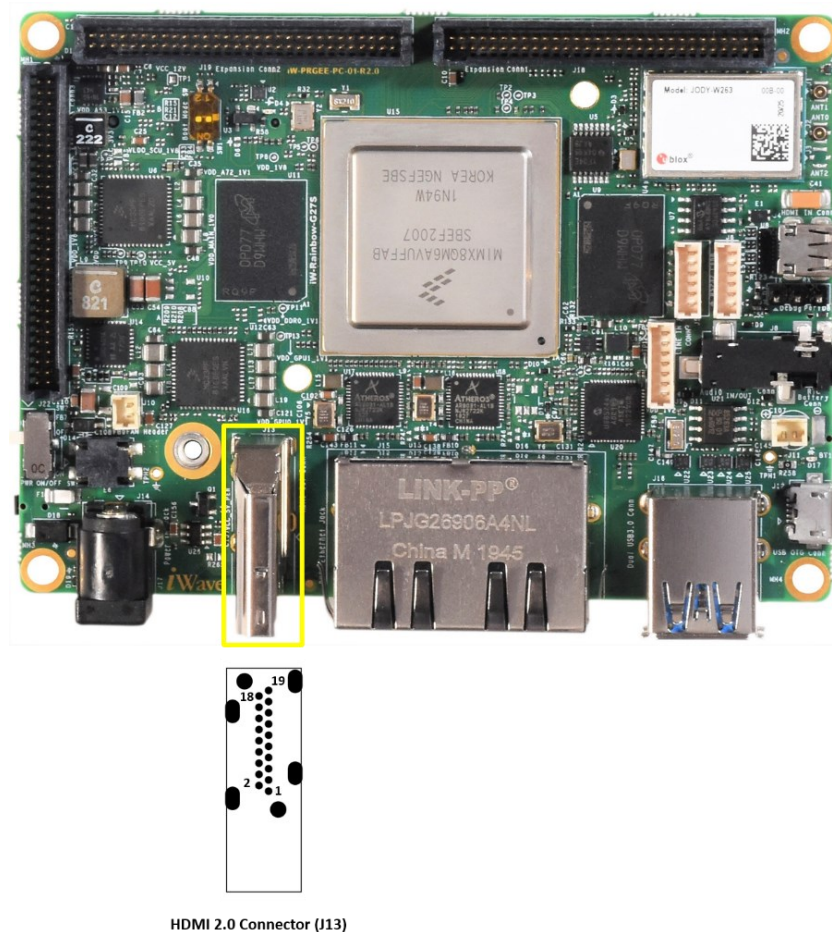


Figure 12: HDMI Output Connector

2.9.2 HDMI Input Interface

i.MX 8 QM/QP PICO ITX SBC supports optional HDMI Input video. The i.MX8 Processor supports HDMI-RX HDMI 2.0a with HDCP 2.2 and 1.4. The HDMI_RX Controller Supports up to 4K2K at 60Hz resolution and Compliant with HDCP2.2 (and backward compatible with HDCP1.4) with up to 600Mhz pixel clock and supports up to 8 (Status and Control Data Channel) SCDC slave addresses. HDMI Signals from the micro HDMI Type-D connector is connected to i.MX 8 QM/QP CPU with ESD protection circuitry. HDMI Input connector (J4) is physically located on top of the board as shown below

Note: Currently HDMI Receiver is not supported by NXP

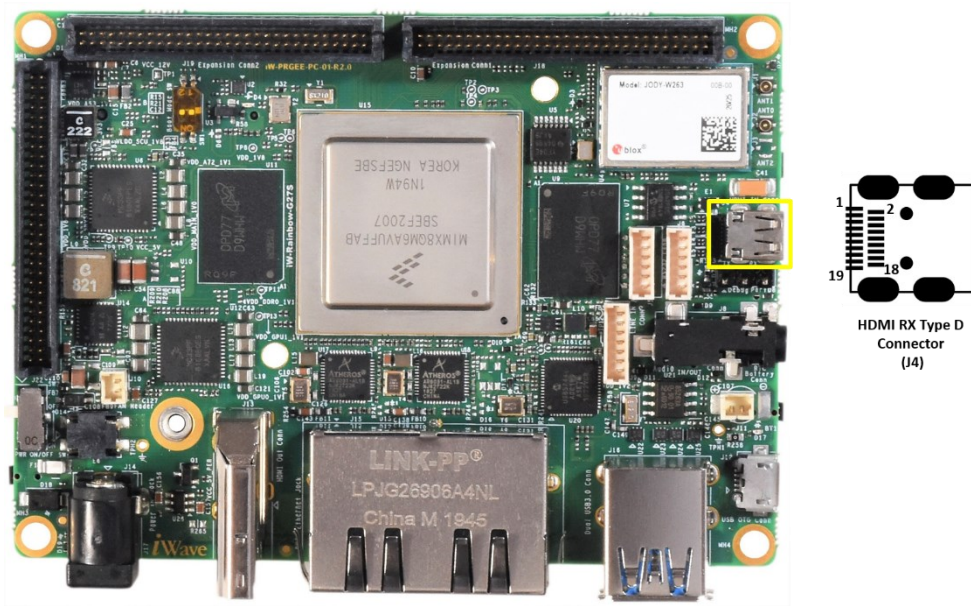


Figure 13: HDMI Input Connector

2.9.3 40 Pin Embedded Display Port (eDP) Interface (Optional)

i.MX 8 QM/QP PICO ITX SBC supports optional 40 pin eDP Display Connector. The i.MX 8 CPU Supports eDP specification, Version, 1.4. The eDP Signals from the i.MX 8 QM/QP CPU is connected to Standard 40 pin eDP connector with ESD protection circuitry. 40 pin eDP connector (J27) is physically located on bottom of the board as shown below. Either eDP or HDMI can be used at a time. Contact iWave support team, if eDP Display Interface support is required.

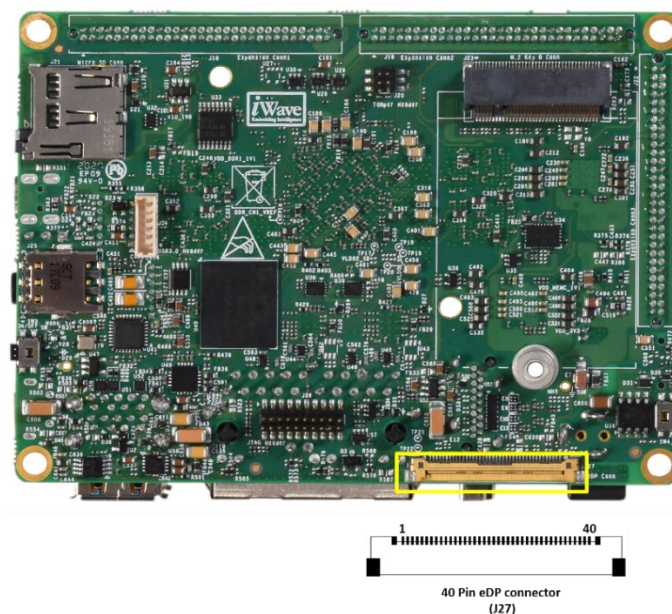


Figure 14: 40 pin eDP connector

Table 8: 40 Pin eDP connector Pinout

Pin No.	Pin Name	Signal Name	Signal Type/ Termination	Description
1	NC	-	-	NC.
2	H_GND	GND	Power	Ground.
3	LANE3_N	HDMI_TX0_CLK_N/EDP3_N	O, eDP	NC. <i>Note: Optionally connected to eDP Lane 3 Negative</i>
4	LANE3_P	HDMI_TX0_CLK_P/EDP3_P	O, eDP	NC. <i>Note: Optionally connected to eDP Lane 3 Positive</i>
5	H_GND	GND	Power	Ground.
6	LANE2_N	HDMI_TX0_DATA0_EDP2_N	O, eDP	NC. <i>Note: Optionally connected to eDP Lane 2 Negative</i>
7	LANE2_P	HDMI_TX0_DATA0_EDP2_P	O, eDP	NC. <i>Note: Optionally connected to eDP Lane 2 Positive</i>
8	H_GND	GND	Power	Ground.
9	LANE1_N	HDMI_TX0_DATA1_EDP1_N	O, eDP	NC. <i>Note: Optionally connected to eDP Lane 1 Negative</i>
10	LANE1_P	HDMI_TX0_DATA1_EDP1_P	O, eDP	NC. <i>Note: Optionally connected to eDP Lane 1 Positive</i>
11	H_GND	GND	Power	Ground.
12	LANE0_N	HDMI_TX0_DATA2_EDP0_N	O, eDP	NC. <i>Note: Optionally connected to eDP Lane 0 Negative</i>
13	LANE0_P	HDMI_TX0_DATA2_EDP0_P	O, eDP	NC. <i>Note: Optionally connected to eDP Lane 0 Positive</i>
14	H_GND	GND	Power	Ground.
15	DP_AUX_P	EDP_AUX_P	IO,0.1uF AC Couple	NC. <i>Note: Optionally connected to eDP AUX Positive</i>
16	DP_AUX_N	EDP_AUX_N	IO,0.1uF AC Couple	NC. <i>Note: Optionally connected to eDP AUX Negative</i>
17	H_GND	GND	Power	Ground.
18	LCD_VCC	VCC_3V3_EDP	O, 3.3V Power	3.3V Supply Voltage.
19	LCD_VCC	VCC_3V3_EDP	O, 3.3V Power	3.3V Supply Voltage.
20	LCD_VCC	VCC_3V3_EDP	O, 3.3V Power	3.3V Supply Voltage.
21	LCD_VCC	VCC_3V3_EDP	O, 3.3V Power	3.3V Supply Voltage.
22	LCD_SELF_TEST/NC	NC	NC	NC.
23	LCD_GND	GND	Power	Ground.
24	LCD_GND	GND	Power	Ground.
25	LCD_GND	GND	Power	Ground.
26	LCD_GND	GND	Power	Ground.
27	HPD	HDMI_TX_HPD	I, 5V CMOS	NC.

Pin No.	Pin Name	Signal Name	Signal Type/ Termination	Description
28	BL_GND	GND	Power	Ground.
29	BL_GND	GND	Power	Ground.
30	BL_GND	GND	Power	Ground.
31	BL_GND	GND	Power	Ground.
32	BL_ENABL	eDP_BL_ENABLE(GPIO1_19)	O, 3.3V CMOS	NC eDP Display Backlight enable Signal.
33	BL_PWM_DIM	eDP_PWM(GPIO1_22)	O, 3.3V CMOS	NC eDP Display PWM Signal.
34	NC/I2C_SCL	HDMI_TX0_TS_SCL	O, 3.3V CMOS 2.2K PU	NC Optional I2C clock.
35	NC/I2C_SDA	HDMI_TX0_TS_SDA	IO, 3.3V CMOS 2.2K PU	NC Optional I2C Data.
36	BL_PWR	VCC_12V_EDP	O, 12V Power	12V Supply Voltage.
37	BL_PWR	VCC_12V_EDP	O, 12V Power	12V Supply Voltage.
38	BL_PWR	VCC_12V_EDP	O, 12V Power	12V Supply Voltage.
39	BL_PWR	VCC_12V_EDP	O, 12V Power	12V Supply Voltage.
40	NC2/RESERVED	EDP_5V	O, 5V Power	Optional 5V Supply Voltage.

Note: Contact iWave support team if eDP Display Interface support is required.

2.9.4 I2S Audio Interface

The i.MX 8 QM/QP PICO ITX SBC supports Audio IN/OUT through CPU's SAI1 interface which can support I2S format. The four wire I2S signals from i.MX 8 QM/QP CPU is connected to I2S Audio Codec "SGTL5000" to support CTIA configuration Headphone Stereo output and Mono Mic input through Single 3.5mm audio Jack (J8). The Audio IN/OUT Jack is physically located at the top of the board as shown below.

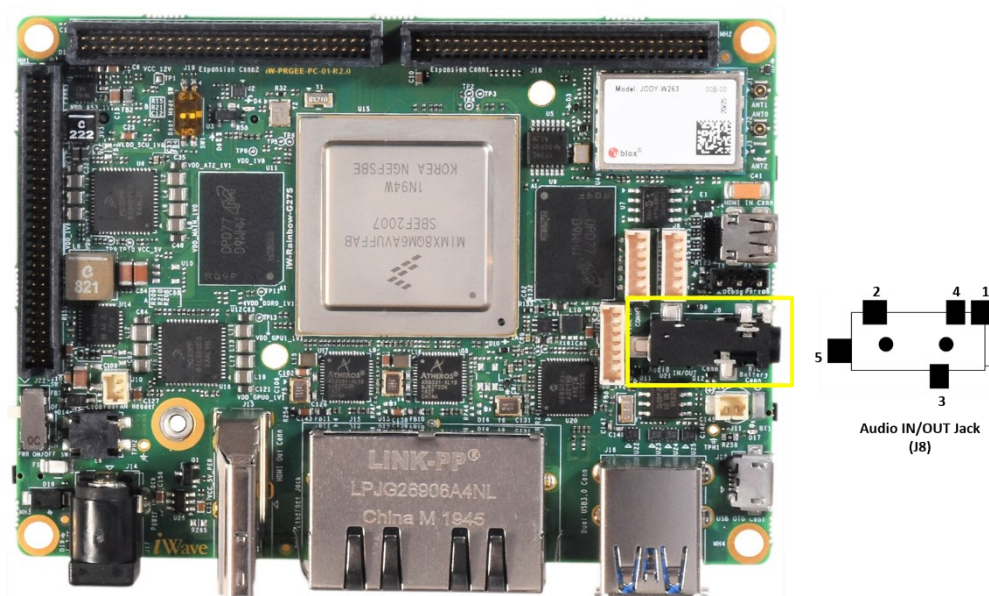


Figure 15: Audio IN/OUT Jack

2.9.5 Line Header (Optional)

The i.MX 8 QM/QP PICO ITX SBC Optionally supports Line In though I2S Audio Codec “SGTL5000” and. The Line In and Speaker Header(J9) is physically located at the top of the board as shown below.

Number of Pins: 7

Connector Part number: 53047-0710 from Molex

Mating Connector: 0510210700 from Molex with crimping pins

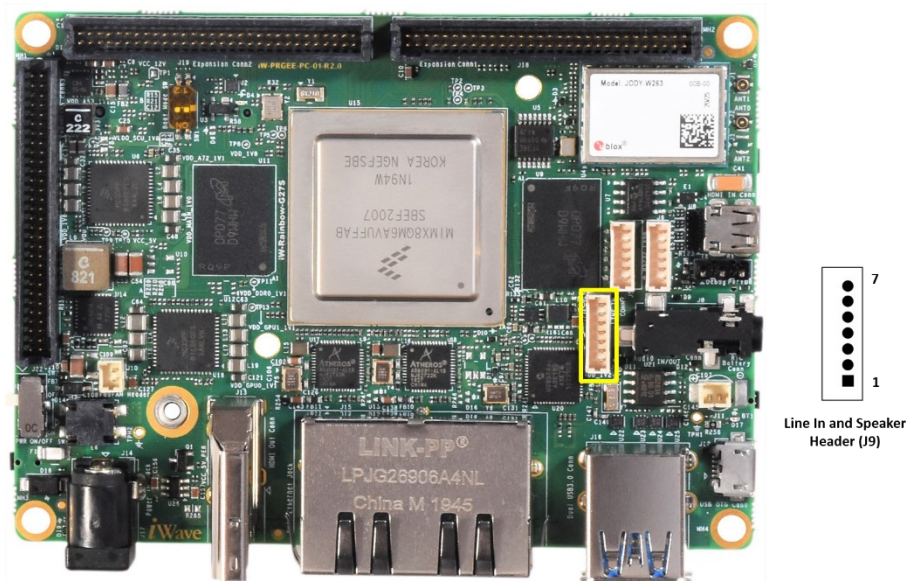


Figure 16: Line in Header

Table 9: Line in and Speaker Header Pinout

Pin No	Pin Name	Signal Name	Signal Type/ Termination	Description
1	LN_L	LINE_IN_L	I, Analog Audio	Line IN Left.
2	LN_R	LINE_IN_R	I, Analog Audio	Line IN Right.
3	GND	AGND	GND	Analog Ground.
4	NC	-	-	NC
5	NC	-	-	NC
6	NC	-	-	NC
7	NC	-	-	NC

Note: Contact iWave support team if Line in Header support is required.

2.10 M.2 Key B Connector

The i.MX 8 QM/QP Pico ITX SBC supports M.2 B key socket is the Next Generation Form Factor (NGFF) which is designed to support multiple modules and make the M.2 more suitable in application like solid-state storage, WWAN. The M.2 Key-B Connector (J23) which is placed at the bottom side of the board.

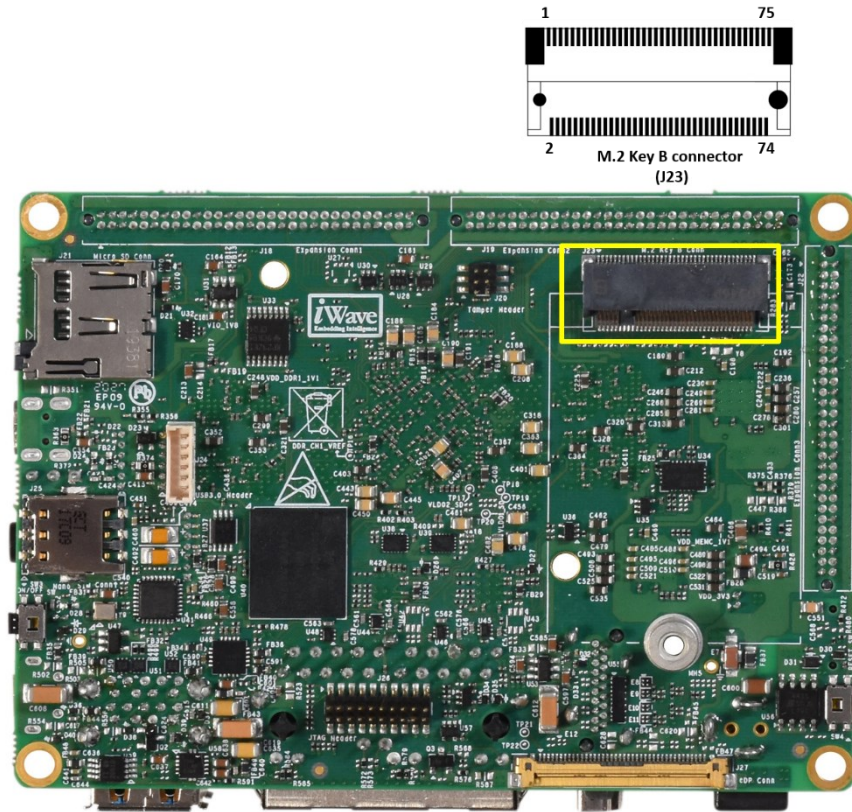


Figure 17: M.2 Key B Connector

The M.2 Key B Connector supports PCIe x2, SATA, USB 2.0 and 3.0, audio, UIM, HSIC, I2C and SMBus. The PCIe Lane 0 and SATA Lane , PCIe lane 1 and USB3.0 pins are muxed in the M.2 Key B connector side. In order to support the PCIe x2 , SATA and USB3.0 the “FUSB340” 2:1 Mux is used.

The Signal “SATA_SEL(GPIO0_04)” which selects between PCIe lane 0 or SATA. By Default, SATA is selected, to use the PCI Lane 0 make the SATA_SEL(GPIO0_04) Low.

Similarly, the Signal “USBSS_SEL(GPIO2_24)” which selects between PCIe lane 1 or USB3.0. By Default, USB3.0 is selected, to use the PCI Lane 1 make the USBSS_SEL(GPIO2_24) Low.

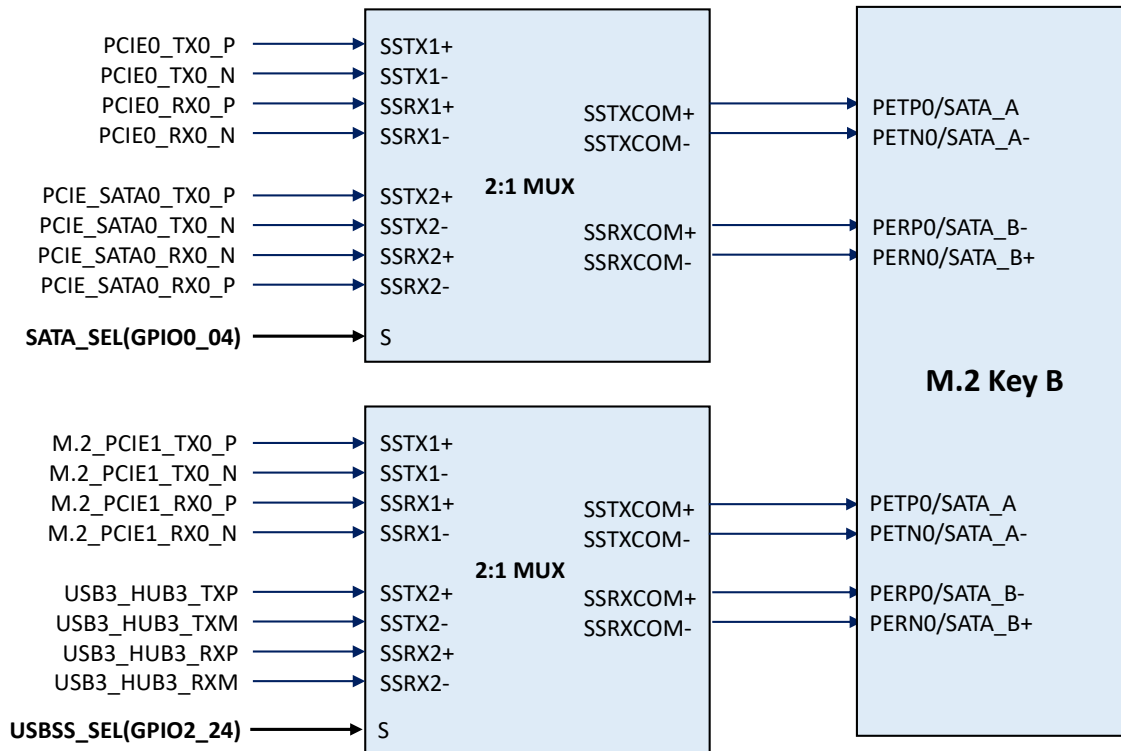


Figure 18: M.2 Key B Connector Pin Muxing

The i.MX 8 QM/QP Pico ITX SBC supports a Nano SIM connector to support the WWAN M.2 Modules. The nano SIM connector(J25) is physically located on the bottom of the board.

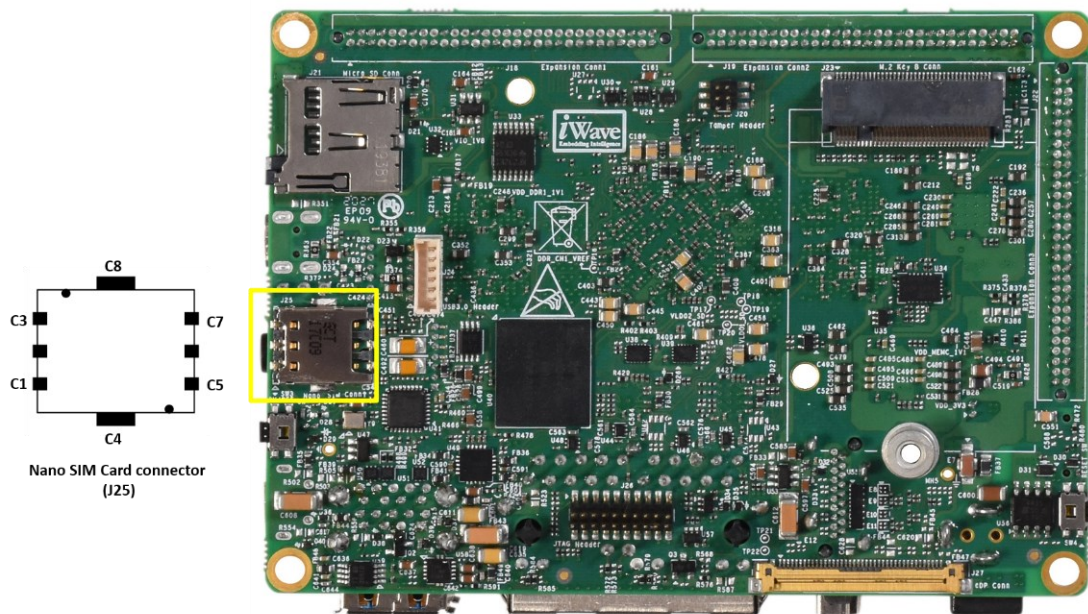


Figure 19: Nano SIM Connector

Table 10: M.2 Connector Pinout

Pin No	Pin Name	Signal Name	Signal Type/ Termination	Description
1	CONFIG_3	M.2_CONFIG_3(GPIO0_03)	I, 1.8V CMOS 10K PU	M.2 Configuration Pin 3.
2	VCC_3V3	VCC_3V3	O, 3.3V Power	3.3V Supply Voltage.
3	GND	GND	Power	Ground.
4	VCC_3V3	VCC_3V3	O, 3.3V Power	3.3V Supply Voltage.
5	GND	GND	Power	Ground.
6	FULL_CARD_POWER_OFF# (O)(0/1.8V_3.3V)	M.2_PWR_OFF#(GPIO3_28)	O, 1.8V CMOS	M.2 Full card Power off Signal.
7	USB_D+	M.2_USB_D+	IO, USB	USB2.0 Port0 Data Plus.
8	W_DISABLE1# (O)(0/3.3V)	M.2_W_DISABLE1#(GPIO3_26)	O, 3.3V CMOS	M.2 Wireless Disable Signal
9	USB_D-	M.2_USB_D-	IO, USB	USB2.0 Port0 Data Minus.
10	GPIO9(LED1#/DAS_DSS#) (I/O)(0/3.3V)	M.2_LED	IO, 3.3V CMOS	SATA Activity Signal. Optionally connected LED
11	GND	GND	Power	Ground.
12	B1	NC	NC	NC.
13	B2	NC	NC	NC.
14	B3	NC	NC	NC.
15	B4	NC	NC	NC.
16	B5	NC	NC	NC.
17	B6	NC	NC	NC.
18	B7	NC	NC	NC.
19	B8	NC	NC	NC.
20	GPIO5(AUDIO0/I2S_CLK(I/O)(0/1.8V)	AUD_SAI0_TXC(GPIO3_06)	IO, 1.8V CMOS/ 33E Series	Serial Audio Interface Channel0 Clock
21	CONFIG_0	M.2_CONFIG_0(GPIO0_19)	I, 1.8V CMOS 10K PU	M.2 Configuration Pin 0.
22	GPIO6_(AUDIO1/I2S_RX) (I/O)(0/1.8V)	AUD_SAI0_RXD(GPIO3_04)	I, 1.8V CMOS	Serial Audio Interface Channel0 Data Input
23	GPIO11(WOWWAN#/HSI_C_DATA(1.2V))(I/O) (0/1.8V)	M.2_GPIO11(GPIO2_22)/ USB_HSIC0_DATA	IO, 1.8V CMOS	General Purpose Input Output. <i>Note: Optionally connected to USB_HSIC0_DATA</i>
24	GPIO7(AUDIO2/I2S_TX) (I/O)(0/1.8V)	AUD_SAI0_TXD(GPIO3_03)	O, 1.8V CMOS	Serial Audio Interface Channel0 Data Output
25	DPR (O) (0/1.8V)	M.2_DPR(GPIO5_23)	O, 1.8V CMOS	M.2 Dynamic Power Reduction Signal.
26	GPIO10_(W_DISABLE_2#/HSIC_STROBE(1.2V)) (I/O)(0/1.8V)	M.2_DEVSLP(GPIO2_04)/ USB_HSIC0_STROBE	IO, 1.8V CMOS	General Purpose Input Output. <i>Note: Optionally connected to USB_HSIC0_STROBE</i>

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Pin No	Pin Name	Signal Name	Signal Type/ Termination	Description
27	GND	GND	Power	Ground.
28	GPIO8(AUDIO3/I2S_WS)(I/O)(0/1.8V)	AUD_SAI0_TXFS(SPI2_CS1)	IO, 1.8V CMOS	Serial Audio Interface Channel0 Left Right Clock
29	PERN1/USB30_RX-/SSIC_RX-	PERN1/USB3.1-RX-	I,PCIe/USB_SS	USB 3.0 Receive Negative Pair. <i>Note: PCIe Port 1 Receive pair Negative.</i>
30	UIM-RESET (I)	M2_UIM_RST	O, SIM	SIM Card Reset Signal.
31	PERP1/USB30_RX+/SSIC_RX+	PERP1/USB3.1-RX+	I,PCIe/USB_SS	USB 3.0 Receive Positive Pair. <i>Note: PCIe Port 1 Receive pair Positive.</i>
32	UIM-CLK (I)	M2_UIM_CLK	I, SIM	SIM Card Clock Signal.
33	GND	GND	Power	Ground.
34	UIM-DATA (I/O)	M2_UIM_DAT	IO, SIM	SIM Card Data IO Signal.
35	PETN1/USB3.1-TX-/SSIC-TXN	PETN1/USB3.1-TX-	O,PCIe/USB_SS	USB 3.0 Transmit Negative Pair. <i>Note: PCIe Port 1 Transmit pair Negative.</i>
36	UIM-PWR (I)	M2_UIM_PWR	O, SIM Power	SIM Card Power.
37	PETP1/USB3.1-TX+/SSIC-TXP	PETP1/USB3.1-TX+	O,PCIe/USB_SS	USB 3.0 Transmit Positive Pair. <i>Note: PCIe Port 1 Transmit pair Positive.</i>
38	DEVSLP (O)	M.2_DEVSLP(GPIO3_27)	O, 1.8V CMOS	M.2 Device Sleep Pin
39	GND	GND	Power	Ground.
40	GPIO0(SMB_CLK/GNSS_SCL/SIM_DET2)(I/O)(0/1.8V)	DMA_I2C1_SCL	O, 1.8V CMOS	I2C CLK.
41	PERN0/SATA_B+	PERN0/SATA-B+	I,PCIe/SATA	SATA Receive Lane Positive. <i>Note: PCIe Port 0 Transmit pair negative.</i>
42	GPIO1(SMB_DATA/GNSS_SDA/UIM_DAT2)(I/O)(0/1.8V)	DMA_I2C1_SDA	IO, 1.8V CMOS	I2C Data.
43	PERP0/SATA_B-	PERP0/SATA-B-	I,PCIe/SATA	SATA Receive Lane Negative. <i>Note: PCIe Port 0 Transmit pair Positive.</i>
44	GPIO2_(ALERT#/GNSS_IRQ/UIM_CLK2)(I)/(0/1.8V)	GPIO_SMBUS_ALERT (GPIO0_16)	IO, 1.8V CMOS	General Purpose Input Output.
45	GND	GND	Power	Ground.
46	GPIO3(SYSCLK/GNSS_0/UIM_RST2) (I/O)(0/1.8V)	M.2_GPIO3(GPIO3_02)	IO, 1.8V CMOS	General Purpose Input Output.

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Pin No	Pin Name	Signal Name	Signal Type/ Termination	Description
47	PETN0/SATA_A-	PETN0/SATA-A-	O,PCIe/SATA	SATA Transmit Lane Negative. <i>Note: PCIe Port 0 Transmit pair Positive.</i>
48	GPIO4(TX_BLK/GNSS_1/ UIM_PWR2)(I/O)(0/1.8V)	M.2_GPIO4(GPIO3_1 4)	IO, 1.8V CMOS	General Purpose Input Output.
49	PETP0/SATA_A+	PETP0/SATA-A+	O,PCIe/SATA	SATA Transmit Lane Positive. <i>Note: PCIe Port 0 Transmit pair Negative.</i>
50	PERST# (O)(0/3.3V)	PCIE_RST_B(GPIO4_2 9)	O, 3.3V CMOS	PCIe Resets Signal.
51	GND	GND	Power	Ground.
52	CLKREQ# (I/O)(0/3.3V)	M.2_CLKREQ(GPIO5_00)	IO, 3.3V CMOS	M.2 Clock Request Pin
53	REFCLKN	M2_PCIE1_REFCLK_N	O,PCIe	PCIe Channel-A Clock Positive. <i>Note: From External Oscillator.</i>
54	PEWAKE# (I/O)(0/3.3V)	PCIE_WAKE_B(GPIO4_28)	O, 3.3V CMOS	PCIe Wake Signal
55	REFCLKP	M2_PCIE1_REFCLK_P	O,PCIe	PCIe Channel-A Clock Negative. <i>Note: From External Oscillator.</i>
56	MFG_DATA	HDMI_TX0_TS_SDA	IO, 3.3V CMOS	NC. <i>Optionally connected I2C Data.</i>
57	GND	GND	Power	Ground.
58	MFG_CLOCK	HDMI_TX0_TS_SCL	O, 3.3V CMOS	NC. <i>Optionally connected I2C Clock.</i>
59	ANTCTL0 (I)(0/1.8 V)	NC	NC	NC.
60	COEX3 (I/O)(0/1.8V)	M.2_COEX3(GPIO0_00)	IO, 1.8V CMOS	General Purpose Input Output.
61	ANTCTL1 (I)(0/1.8 V)	NC	NC	NC.
62	COEX_TXD (O)(0/1.8V)	UART3_TX	O, 1.8V CMOS	NC. <i>Optionally connected UART3 TX.</i>
63	ANTCTL2 (I)(0/1.8 V)	NC	NC	NC.
64	COEX_RXD (I)(0/1.8V)	UART3_RX	I, 1.8V CMOS	NC. <i>Optionally connected UART3 RX.</i>
65	ANTCTL3 (I)(0/1.8 V)	NC	NC	NC.
66	SIM_DETECT (I)	M.2_SIM_DETECT	NC	NC
67	RESET# (O)(0/1.8V)	M.2_RESET(GPIO3_23)		M.2 Reset Signal
68	SUSCLK(32KHZ) (O)(0/3.3V)	M.2_SUSCLK		<i>Note: Optionally connected 32.768kHz Clock output</i>
69	CONFIG_1	M.2_CONFIG_1(GPIO3_24)	I, 1.8V CMOS 10K PU	M.2 Configuration Pin 1.

Pin No	Pin Name	Signal Name	Signal Type/ Termination	Description
70	VCC_3V3	VCC_3V3	O, 3.3V Power	3.3V Supply Voltage.
71	GND	GND	Power	Ground.
72	VCC_3V3	VCC_3V3	O, 3.3V Power	3.3V Supply Voltage.
73	GND	GND	Power	Ground.
74	VCC_3V3	VCC_3V3	O, 3.3V Power	3.3V Supply Voltage.
75	CONFIG_2	M.2_CONFIG_2(GPIO 1_31)	I, 1.8V CMOS 10K PU	M.2 Configuration Pin 2.

The i.MX 8 QM/QP Pico ITX SBC can support M.2 NGFF Key B 4G Modules, SATA Module, and NVMe PCIe x2 Modules
Below are the steps for Inserting an M.2 Key B Module to the i.MX 8 QM/QP Pico ITX SBC M.2 Connector

Step 1: Move the Module against housing Chamber.

Step 2: Rotate the Module to 25 Degree and insert until the bottom of the module surface reaches the ramp.

Step 3: Rotate the Module to horizontal Position by hand

Step 4: Fix the module with M3 x4 Screw

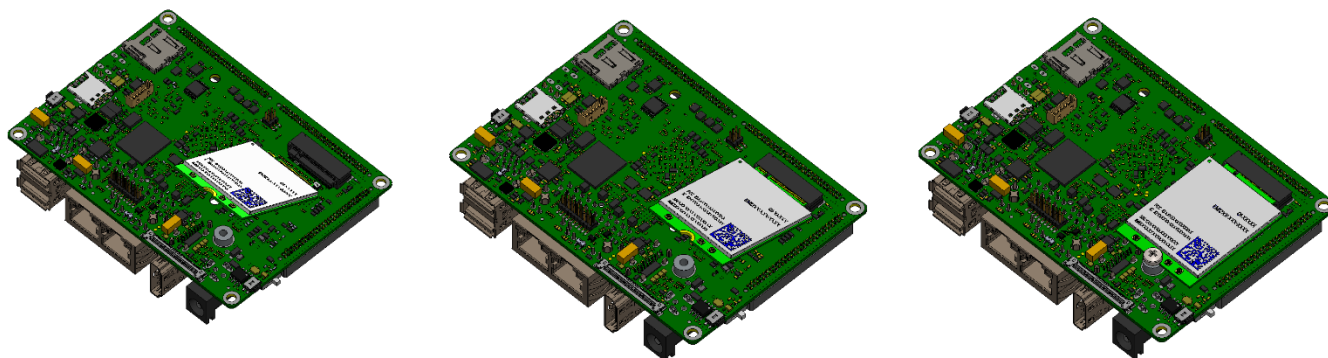


Figure 20: M.2 Module Insertion Guide

2.11 Expansion Connector 1

The interfaces which are available at 60 Pin Expansion connector1 are explained in the following sections. This Expansion Connector1 (J18) is physically located at the top of the SBC as shown below.

Number of Pins -60

Connector Part TFC-130-01-L-D-A from Samtec

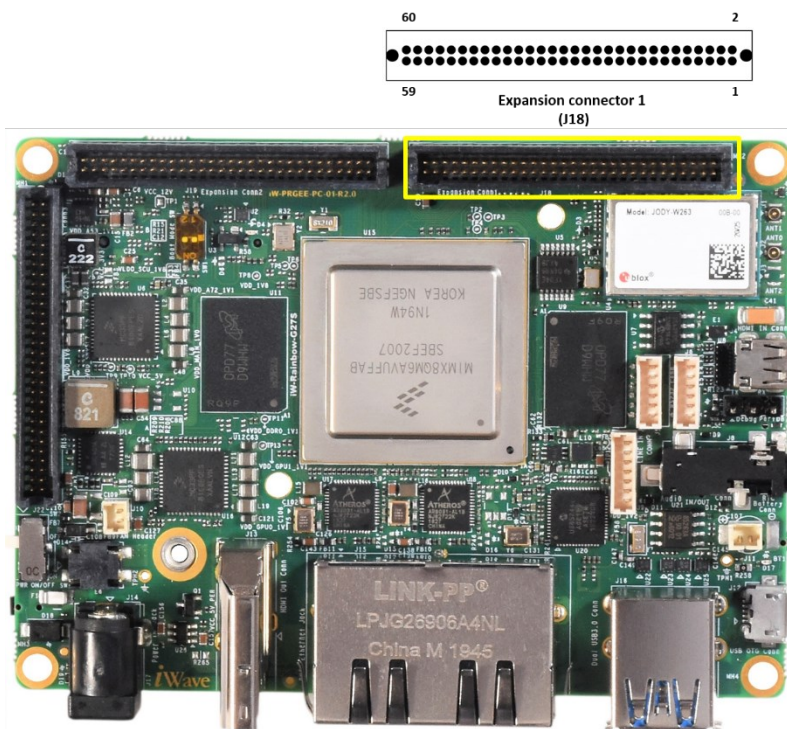


Figure 21: Expansion Connector 1

Table 11: Expansion Connector 1 Pinouts

Signal	Pin No	Pin No	Signal
MIPI_DSI0_DATA3_P	1	2	GND
MIPI_DSI0_DATA3_N	3	4	LVDS1_CH0_TX2_P
GND	5	6	LVDS1_CH0_TX2_N
MIPI_DSI0_DATA1_P	7	8	GND
MIPI_DSI0_DATA1_N	9	10	LVDS1_CH0_TX3_P
GND	11	12	LVDS1_CH0_TX3_N
MIPI_DSI0_CLK_P	13	14	GND
MIPI_DSI0_CLK_N	15	16	LVDS1_CH0_TX0_P
GND	17	18	LVDS1_CH0_TX0_N
MIPI_DSI0_DATA0_P	19	20	GND
MIPI_DSI0_DATA0_N	21	22	LVDS1_CH0_TX1_P
GND	23	24	LVDS1_CH0_TX1_N
MIPI_DSI0_DATA2_P	25	26	GND
MIPI_DSI0_DATA2_N	27	28	LVDS1_CH0_CLK_P
GND	29	30	LVDS1_CH0_CLK_N

Signal	Pin No	Pin No	Signal
LVDS1_CH1_TX3_N	31	32	SCL_USB_DP
LVDS1_CH1_TX3_P	33	34	SDA_USB_DM
GND	35	36	LCD1_BL_PWM(GPIO1_10)
LVDS1_CH1_TX2_N	37	38	LCD1_BKLT_EN(GPIO1_15)
LVDS1_CH1_TX2_P	39	40	CAN_SPDIF_RX
GND	41	42	CAN_SPDIF_TX
LVDS1_CH1_TX1_N	43	44	CAN_SPDIF_PD
LVDS1_CH1_TX1_P	45	46	SPI3_CS0
GND	47	48	SPI3_CS1
LVDS1_CH1_TX0_N	49	50	SPI3_MOSI
LVDS1_CH1_TX0_P	51	52	SPI3_MISO
GND	53	54	SPI3_SCLK
LVDS1_CH1_CLK_N	55	56	GND
LVDS1_CH1_CLK_P	57	58	VCC_5V
GND	59	60	VCC_12V

2.11.1 LVDS Interface

The i.MX 8 Processor's two four lane LVDS channels from LVDS1 interface are connected to Board Expansion connector. Processor has LVDS Display Bridge (LDB) connects to an External LVDS Display Interface. The purpose of the LDB is to support flow of synchronous RGB data to external display devices through the LVDS interface.

For more details on Expansion Connector LVDS pinouts, refer below table:

Exp. Pin No	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
LVDS1 Channel0				
28	LVDS1_CH0_CLK_P	LVDS1_CH0_CLK_P/BM36	O, LVDS	LVDS1 Channel0 Clock positive.
30	LVDS1_CH0_CLK_N	LVDS1_CH0_CLK_N/BK36	O, LVDS	LVDS1 Channel0 Clock negative.
4	LVDS1_CH0_TX2_P	LVDS1_CH0_TX2_P/BN39	O, LVDS	LVDS1 Channel0 Transmit Lane 2 positive.
6	LVDS1_CH0_TX2_N	LVDS1_CH0_TX2_N/BL39	O, LVDS	LVDS1 Channel0 Transmit Lane 2 negative.
10	LVDS1_CH0_TX3_P	LVDS1_CH0_TX3_P/BM40	O, LVDS	LVDS1 Channel0 Transmit Lane 3 positive.
12	LVDS1_CH0_TX3_N	LVDS1_CH0_TX3_N/BK40	O, LVDS	LVDS1 Channel0 Transmit Lane 3 negative.
16	LVDS1_CH0_TX0_P	LVDS1_CH0_TX0_P/BN37	O, LVDS	LVDS1 Channel0 Transmit Lane 0 positive.
18	LVDS1_CH0_TX0_N	LVDS1_CH0_TX0_N/BL37	O, LVDS	LVDS1 Channel0 Transmit Lane 0 negative.
22	LVDS1_CH0_TX1_P	LVDS1_CH0_TX1_P/BM38	O, LVDS	LVDS1 Channel0 Transmit Lane 1 positive.

Exp. Pin No	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
24	LVDS1_CH0_TX1_N	LVDS1_CH0_TX1_N/BK38	O, LVDS	LVDS1 Channel0 Transmit Lane 1 negative.
LVDS1 Channel1				
55	LVDS1_CH1_CLK_N	LVDS1_CH1_CLK_N/BK34	O, LVDS	LVDS1 Channel1 Clock negative.
57	LVDS1_CH1_CLK_P	LVDS1_CH1_CLK_P/BM34	O, LVDS	LVDS1 Channel1 Clock positive.
49	LVDS1_CH1_TX0_N	LVDS1_CH1_TX0_N/BL33	O, LVDS	LVDS1 Channel1 Transmit Lane 0 negative.
51	LVDS1_CH1_TX0_P	LVDS1_CH1_TX0_P/BN33	O, LVDS	LVDS1 Channel1 Transmit Lane 0 positive.
43	LVDS1_CH1_TX1_N	LVDS1_CH1_TX1_N/BK32	O, LVDS	LVDS1 Channel1 Transmit Lane 1 negative.
45	LVDS1_CH1_TX1_P	LVDS1_CH1_TX1_P/BM32	O, LVDS	LVDS1 Channel1 Transmit Lane 1 positive.
37	LVDS1_CH1_TX2_N	LVDS1_CH1_TX2_N/BL31	O, LVDS	LVDS1 Channel1 Transmit Lane 2 negative.
39	LVDS1_CH1_TX2_P	LVDS1_CH1_TX2_P/BN31	O, LVDS	LVDS1 Channel1 Transmit Lane 2 positive.
31	LVDS1_CH1_TX3_N	LVDS1_CH1_TX3_N/BK30	O, LVDS	LVDS1 Channel1 Transmit Lane 3 negative.
33	LVDS1_CH1_TX3_P	LVDS1_CH1_TX3_P/BM30	O, LVDS	LVDS1 Channel1 Transmit Lane 3 positive.
36	LCD1_BL_PWM(GPIO1_10)	LVDS1_GPIO00/BD34	O, 1.8V CMOS	LCD PWM controller Signal.
38	LCD1_BKLT_EN(GPIO1_15)	LVDS1_I2C1_SD A/ BN35	O, 1.8V CMOS	LCD Backlight Enable Signal.

2.11.2 MIPI DSI0 Display interface

The i.MX 8 CPU MIPI_DSI standard controller is a flexible, high-performance, and easy-to-use digital core that implements all protocol functions defined in the MIPI DSI Specification. The MIPI DSI controller provides an interface that allows communication with MIPI DSI-compliant peripherals. The MIPI DSI D-PHY is a high frequency, low power, low-cost, source-synchronous, physical layer supporting the MIPI Alliance standard for D-PHY.

For more details on MIPI DSI 0 Display Interface pinouts, refer below table:

Pin No.	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
19	MIPI_DSI0_DATA0_P	MIPI_DSI0_DATA0_P/BK28	O, MIPI	MIPI DSI0 differential data lane 0 positive
21	MIPI_DSI0_DATA0_N	MIPI_DSI0_DATA0_N/ BM28	O, MIPI	MIPI DSI0 differential data lane 0 negatives
7	MIPI_DSI0_DATA1_P	MIPI_DSI0_DATA1_P/BK26	O, MIPI	MIPI DSI0 differential data lane 1 positive

Pin No.	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
9	MIPI_DSI0_DATA1_N	MIPI_DSI0_DATA1_N/ BM26	O, MIPI	MIPI DSI0 differential data lane 1 negative
25	MIPI_DSI0_DATA2_P	MIPI_DSI0_DATA2_P /BL29	O, MIPI	MIPI DSI0 differential data lane 2 positive.
27	MIPI_DSI0_DATA2_N	MIPI_DSI0_DATA2_N/ BN29	O, MIPI	MIPI DSI0 differential data lane 2 negative.
1	MIPI_DSI0_DATA3_P	MIPI_DSI0_DATA3_P /BL25	O, MIPI	MIPI DSI0 differential data lane 3 positive
3	MIPI_DSI0_DATA3_N	MIPI_DSI0_DATA3_N/BN25	O, MIPI	MIPI DSI0 differential data lane 3 negative
13	MIPI_DSI0_CLK_P	MIPI_DSI0_CLK_P /BL27	O, MIPI	MIPI DSI0 differential Clock positive
15	MIPI_DSI0_CLK_N	MIPI_DSI0_CLK_N /BN27	O, MIPI	MIPI DSI0 differential Clock negative

2.11.3 SPI Interface

The i.MX 8 CPU supports low power Serial Peripheral Interface (SPI) module that supports an efficient interface to an SPI bus as a master and/or a slave with maximum clock speed of 40MHz.

For more details on SPI pinouts, refer below table:

Pin No.	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
46	SPI3_CS0	SPI3_CS0/BG5	IO, 1.8V CMOS	SPI0 Chip Select 0
48	SPI3_CS1	SPI3_CS1/BD8	IO, 1.8V CMOS	SPI0 Chip Select 1
54	SPI3_SCLK	SPI3_SCLK/BF6	IO, 1.8V CMOS/ 33E Series	SPI0 Clock
52	SPI3_MISO	SPI3_MISO/ BE5	I, 1.8V CMOS	SPI0 Master IN Slave Out
50	SPI3_MOSI	SPI3_MOSI/ BF2	O, 1.8V CMOS	SPI0 Master Out Slave In

2.11.4 CAN Interface

The Flexible Controller Area Network (FLEXCAN) module is a communication controller implementing the CAN protocol according to the CAN 2.0B protocol specification. CAN1 of CPU is connected to expansion connector.

For more details on Expansion Connector CAN pinouts, refer below table:

Exp. Pin No	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
40	FLEXCAN1_RX	FLEXCAN1_RX/ E5	I, 1.8V CMOS	CAN Receiver. <i>Note: Optionally connected to SPDIF Receiver Signal</i>
42	FLEXCAN1_TX	FLEXCAN1_TX/ G7	O, 1.8V CMOS	CAN Transmitter. <i>Note: Optionally connected to SPDIF Transmitter Signal</i>

Exp. Pin No	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
44	CAN1_PD(GPIO1_30)	MIPI_CSI1_GPIO 0_00/BN15	IO, 1.8V CMOS	CAN Power Down <i>Note: Optionally connected to SPDIF ETX Clock</i>

Note: Contact iWave support team if SPDIF support is required.

2.11.5 DMA I2C2. Interface

For more details on Expansion Connector-1, DMA I2C pinouts, refer below table:

Exp. Pin No	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
32	DMA_I2C2_SCL	GPT1_CLK/DMA .I2C2.SCL/BA53	O, 1.8V CMOS/2.2K PU	I2C clock. <i>Note: Optionally connected to USB Positive Signal from USB Hub, channel 4.</i>
34	DMA_I2C2_SDA	GPT1_CAPTURE /DMA.I2C2.SDA /AY50	IO, 1.8V CMOS/2.2K PU	I2C Data. <i>Note: Optionally connected to USB Negative Signal from USB Hub, channel 4.</i>

Note: Contact iWave support team if USB support is required.

2.11.6 GPIOs

Refer GPIO Column under “i.MX 8 Pin Multiplexing on Expansion Connector” for details on GPIO options available from Expansion connector 1.

2.12 Expansion Connector 2

The interfaces which are available at 60 Pin Expansion connector 2 are explained in the following sections. This Expansion Connector2 (J19) is physically located at the top of the SBC as shown below.

Number of Pins -60

Connector Part TFC-130-01-L-D-A from Samtec

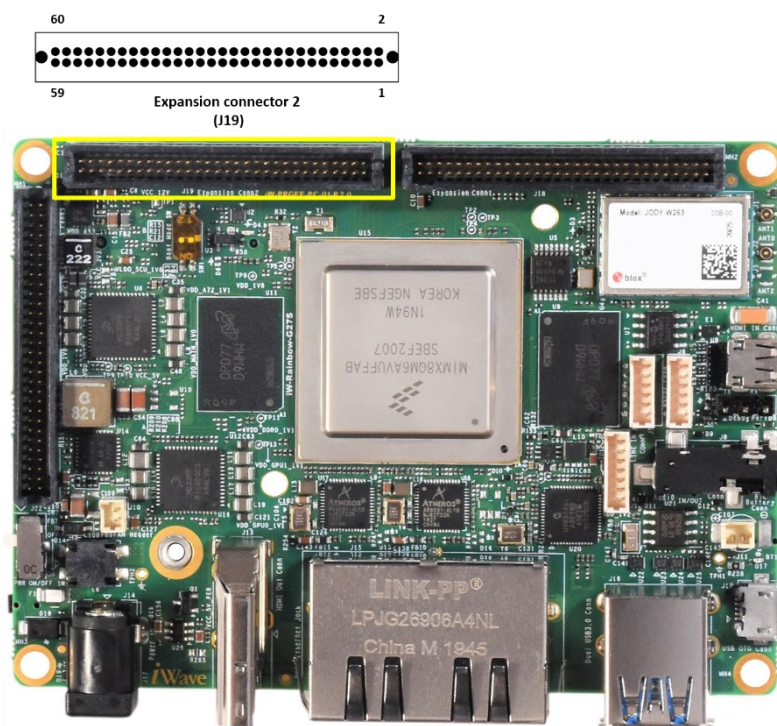


Figure 22: Expansion Connector 2

Table 12: Expansion Connector 2 Pinouts

Signal	Pin No	Pin No	Signal
MIPI_CSIO_DATA3_P	1	2	GND
MIPI_CSIO_DATA3_N	3	4	LVDS0_CH0_CLK_P
GND	5	6	LVDS0_CH0_CLK_N
MIPI_CSIO_DATA1_P	7	8	GND
MIPI_CSIO_DATA1_N	9	10	LVDS0_CH0_TX0_P
GND	11	12	LVDS0_CH0_TX0_N
MIPI_CSIO_CLK_P	13	14	GND
MIPI_CSIO_CLK_N	15	16	LVDS0_CH0_TX1_P
GND	17	18	LVDS0_CH0_TX1_N
MIPI_CSIO_DATA0_P	19	20	GND
MIPI_CSIO_DATA0_N	21	22	LVDS0_CH0_TX2_P
GND	23	24	LVDS0_CH0_TX2_N
MIPI_CSIO_DATA2_P	25	26	GND
MIPI_CSIO_DATA2_N	27	28	LVDS0_CH0_TX3_P
LVDS0_I2C0_SCL	29	30	LVDS0_CH0_TX3_N

Signal	Pin No	Pin No	Signal
LVDS0_I2C0_SDA	31	32	GND
LCD0_BL_PWM(GPIO1_04)	33	34	LVDS0_CH1_TX3_P
LCD0_1_EN(GPIO1_08)	35	36	LVDS0_CH1_TX3_N
MIPI_CSI0_I2C0_SCL	37	38	GND
MIPI_CSI0_I2C0_SDA	39	40	LVDS0_CH1_TX2_P
MIPI_CSI0_MCLK_OUT	41	42	LVDS0_CH1_TX2_N
SPI2_SCLK	43	44	GND
SPI2_CS0	45	46	LVDS0_CH1_TX1_P
SPI2_MISO	47	48	LVDS0_CH1_TX1_N
SPI2_MOSI	49	50	GND
M41_UART_RX_SCL(GPIO0_10)	51	52	LVDS0_CH1_TX0_P
M41_UART_TX_SDA(GPIO0_11)	53	54	LVDS0_CH1_TX0_N
GND	55	56	GND
VCC_5V	57	58	LVDS0_CH1_CLK_P
VCC_12V	59	60	LVDS0_CH1_CLK_N

2.12.1 LVDS Interface

The i.MX 8 Processor's two lane LVDS channels from LVDS0 interface are connected to Board Expansion connector. Processor has LVDS Display Bridge (LDB) connects to an External LVDS Display Interface. The purpose of the LDB is to support flow of synchronous RGB data to external display devices through the LVDS interface.

For more details on Expansion Connector LVDS pinouts, refer below table:

Exp. Pin No	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
LVDS1 Channel0				
4	LVDS0_CH0_CLK_P	LVDS0_CH0_CLK_P/BN41	O, LVDS	LVDS0 Channel0 Clock positive.
6	LVDS0_CH0_CLK_N	LVDS0_CH0_CLK_N/BL41	O, LVDS	LVDS0 Channel0 Clock negative.
10	LVDS0_CH0_TX0_P	LVDS0_CH0_TX0_P/BM42	O, LVDS	LVDS0 Channel0 Transmit Lane 0 positive.
12	LVDS0_CH0_TX0_N	LVDS0_CH0_TX0_N/BK42	O, LVDS	LVDS0 Channel0 Transmit Lane 0 negative.
16	LVDS0_CH0_TX1_P	LVDS0_CH0_TX1_P/BN43	O, LVDS	LVDS0 Channel0 Transmit Lane 1 positive.
18	LVDS0_CH0_TX1_N	LVDS0_CH0_TX1_N/BL43	O, LVDS	LVDS0 Channel0 Transmit Lane 1 negative.
22	LVDS0_CH0_TX2_P	LVDS0_CH0_TX2_P/BM44	O, LVDS	LVDS0 Channel0 Transmit Lane 2 positive.
24	LVDS0_CH0_TX2_N	LVDS0_CH0_TX2_N/BK44	O, LVDS	LVDS0 Channel0 Transmit Lane 2 negative.
28	LVDS0_CH0_TX3_P	LVDS0_CH0_TX3_P/BN45	O, LVDS	LVDS0 Channel0 Transmit Lane 3 positive.

Exp. Pin No	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
30	LVDS0_CH0_TX3_N	LVDS0_CH0_TX3_N/BL45	O, LVDS	LVDS0 Channel0 Transmit Lane 3 negative.
LVDS1 Channel1				
34	LVDS0_CH1_TX3_P	LVDS0_CH1_TX3_P/BH38	O, LVDS	LVDS0 Channel1 Clock positive.
36	LVDS0_CH1_TX3_N	LVDS0_CH1_TX3_N/BG37	O, LVDS	LVDS0 Channel1 Clock negative.
40	LVDS0_CH1_TX2_P	LVDS0_CH1_TX2_P/BH40	O, LVDS	LVDS0 Channel1 Transmit Lane 0 positive.
42	LVDS0_CH1_TX2_N	LVDS0_CH1_TX2_N/BG39	O, LVDS	LVDS0 Channel1 Transmit Lane 0 negative.
46	LVDS0_CH1_TX1_P	LVDS0_CH1_TX1_P/BH42	O, LVDS	LVDS0 Channel1 Transmit Lane 1 positive.
48	LVDS0_CH1_TX1_N	LVDS0_CH1_TX1_N/BG41	O, LVDS	LVDS0 Channel1 Transmit Lane 1 negative.
52	LVDS0_CH1_TX0_P	LVDS0_CH1_TX0_P/BH44	O, LVDS	LVDS0 Channel1 Transmit Lane 2 positive.
54	LVDS0_CH1_TX0_N	LVDS0_CH1_TX0_N/BG43	O, LVDS	LVDS0 Channel1 Transmit Lane 2 negative.
58	LVDS0_CH1_CLK_P	LVDS0_CH1_CLK_P/BH46	O, LVDS	LVDS0 Channel1 Transmit Lane 3 positive..
60	LVDS0_CH1_CLK_N	LVDS0_CH1_CLK_N/BH45	O, LVDS	LVDS0 Channel1 Transmit Lane 3 negative.
29	LVDS0_I2C0_SCL	LVDS0_I2C0_SCL/BD38	O, 1.8V CMOS/2.2K PU	LVDS Display I2C clock.
31	LVDS0_I2C0_SDA	LVDS0_I2C0_SDA/BD36	IO, 1.8V CMOS/2.2K PU	LVDS Display I2C Data.
33	LCD0_BL_PWM(GPIO1_04)	LVDS0_GPIO00/BE39	O, 1.8V CMOS	LCD Pulse width modulation signal.
35	LCD0_1_EN(GPIO1_08)	LVDS0_I2C1_SCL/BE37	O, 1.8V CMOS	LCD enable signal.

2.12.2 MIPI CSI Camera

The i.MX 8 CPU supports two 4-lane camera interfaces, the CSI-2 Rx Controller Core implements all three layers defined by the CSI-2 Specification: Pixel to Byte Packing, Low Level Protocol, and Lane Management. The D-PHY interface of the CSI-2 Rx Controller Core supports PHY Protocol Interface (PPI) compatible MIPI D-PHYs. The Local Interface is an easy to use pixel-based interface that supports 1 to 4 virtual channels and all data types. The Local interface runs at the User Interface clock rate for all implementations.

The CSI-2 Rx Controller Core takes care of all packet formatting details and transmission over the MIPI bus. The i.MX 8 Pico ITX SBC supports four lane MIPI CSI camera interface via Expansion connector 2 along with the other controlling signals.

For more details on MIPI CSI0 Interface pinouts, refer below table:

Exp. Pin No	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
37	MIPI_CSI0_I2C0_SCL	MIPI_CSI0_I2C0_SCL/ BH24	O, 1.8V CMOS/ 2.2K PU	MIPI CSI0 I2C Clock.
39	MIPI_CSI0_I2C0_SDA	MIPI_CSI0_I2C0 _SDA /BN19	IO, 1.8V CMOS/ 2.2K PU	MIPI CSI0 I2C Data.
41	MIPI_CSI0_MCLK_OUT	MIPI_CSI0_MCLK _OUT /BJ23	O, 1.8V CMOS	Master Clock for Camera.
13	MIPI_CSI0_CLK_P	MIPI_CSI0_CLK _P /BF20	I, MIPI	MIPI CSI0 differential Clock positive.
15	MIPI_CSI0_CLK_N	MIPI_CSI0_CLK _N /BE21	I, MIPI	MIPI CSI0 differential Clock negative.
19	MIPI_CSI0_DATA0_P	MIPI_CSI0_ DATA0_P/ BF22	I, MIPI	MIPI CSI0 differential data lane 0 positive.
21	MIPI_CSI0_DATA0_N	MIPI_CSI0_DATA0 _N/BE23	I, MIPI	MIPI CSI0 differential data lane 0 negative.
7	MIPI_CSI0_DATA1_P	MIPI_CSI0_DATA1 _P/BE19	I, MIPI	MIPI CSI0 differential data lane 1 positive.
9	MIPI_CSI0_DATA1_N	MIPI_CSI0_DATA1 _N/BF18	I, MIPI	MIPI CSI0 differential data lane 1 negative.
25	MIPI_CSI0_DATA2_P	MIPI_CSI0_DATA2_P/BF24	I, MIPI	MIPI CSI0 differential data lane 2 positive.
27	MIPI_CSI0_DATA2_N	MIPI_CSI0_DLN2_M/BE25	I, MIPI	MIPI CSI0 differential data lane 2 negative.
1	MIPI_CSI0_DATA3_P	MIPI_CSI0_DLN3_P/BF16	I, MIPI	MIPI CS0 differential data lane 3 positive.
3	MIPI_CSI0_DATA3_N	MIPI_CSI0_DLN3_M/BE17	I, MIPI	MIPI CSI0 differential data lane 3 negative.

2.12.3 SPI Interface

The i.MX 8 CPU supports low power Serial Peripheral Interface (SPI) module that supports an efficient interface to an SPI bus as a master and/or a slave with maximum clock speed of 40MHz.

For more details on SPI pinouts, refer below table:

Pin No.	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
43	SPI2_SCLK	SPI2_SCK/AW5	O, 1.8V CMOS	SPI2 Clock
45	SPI2_CS0	SPI2_CS0/AW1	O, 1.8V CMOS/ 33E Series	SPI2 Chip Select 1
47	SPI2_MISO	SPI2_SDI/AY4	I, 1.8V CMOS	SPI2 Master IN Slave Out
49	SPI2_MOSI	SPI2_SDO/BA1	O, 1.8V CMOS	SPI2 Master Out Slave In

2.12.4 M41 UART Interface

The integrated Cortex-M4 Microcontroller offloads real-time tasks from the main OS for hard real-time & low power mode. The M41 UART Interface UART Interface signals are connected to Expansion connector 2.

For more details on M41 UART pinouts, refer below table:

Exp. Pin No	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
51	M41_UART_RX_SCL(GPIO0_10)	M41_I2C0_SCL/LSIO.GPIO0.IO10/ AR45	I, 1.8V CMOS	M41 UART Receiver.
53	M41_UART_TX_SDA(GPIO0_11)	M41_I2C0_SDA/LSIO.GPIO0.IO11/ AU49	O, 1.8V CMOS	M41 UART Transmitter

2.12.5 GPIOs

Refer GPIO Column under “i.MX 8 Pin Multiplexing on Expansion Connector” for details on GPIO options available from Expansion connector 2.

2.13 Expansion Connector 3

The interfaces which are available at 60 Pin Expansion connector 3 are explained in the following sections. This Expansion Connector3 (J22) is physically located at the top of the SBC as shown below.

Number of Pins -60

Connector Part TFC-130-01-L-D-A from Samtec

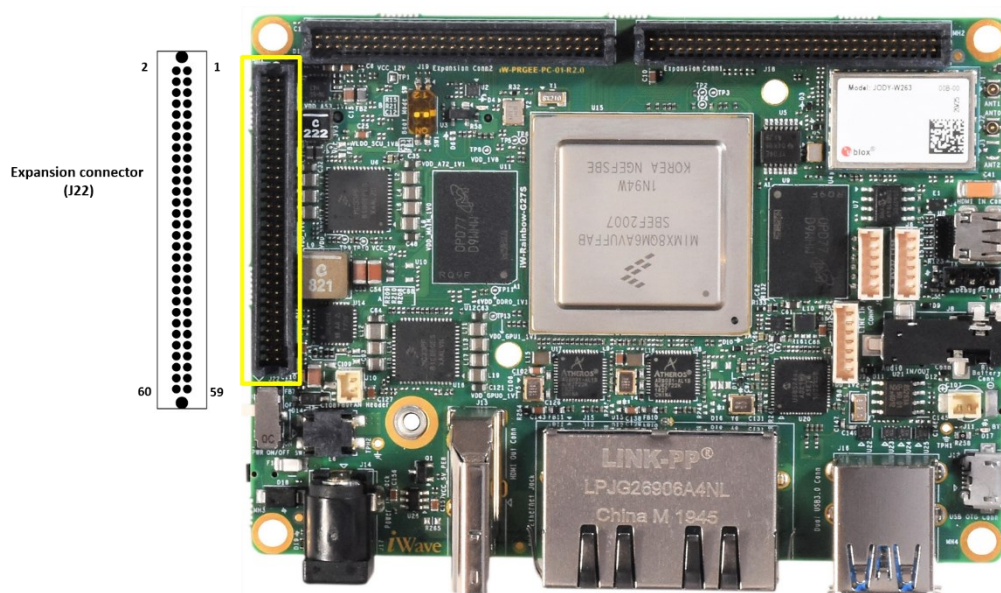


Figure 23: Expansion Connector 3

Table 13: Expansion Connector 3 Pinouts

Signal	Pin No	Pin No	Signal
LVDS1_I2C0_SCL	1	2	GND
LVDS1_I2C0_SDA	3	4	MIPI_CSI1_DATA3_N
TP_INT(GPIO0_01)	5	6	MIPI_CSI1_DATA3_P
UART3_RX_GPIO	7	8	GND
UART3_TX_GPIO	9	10	MIPI_CSI1_DATA1_N
DMA_I2C1_SCL	11	12	MIPI_CSI1_DATA1_P
DMA_I2C1_SDA	13	14	GND
FLEXCAN2_RX	15	16	MIPI_CSI1_CLK_N
FLEXCAN2_TX	17	18	MIPI_CSI1_CLK_P
M40_UART_RX_SCL(GPIO0_06)	19	20	GND
M40_UART_TX_SDA(GPIO0_07)	21	22	MIPI_CSI1_DATA0_N
QSPI1A_DATA3	23	24	MIPI_CSI1_DATA0_P
QSPI1A_DATA2	25	26	GND
QSPI1A_DATA1	27	28	MIPI_CSI1_DATA2_N
QSPI1A_DATA0	29	30	MIPI_CSI1_DATA2_P
QSPI1A_SS0	31	32	GND
QSPI1A_SS1	33	34	MIPI_DSI1_DATA3_N

Signal	Pin No	Pin No	Signal
QSPI1A_SCLK	35	36	MIPI_DSI1_DATA3_P
QSPI1A_RESET(GPIO4_22)	37	38	GND
SAI2_RXC(GPIO2_07)	39	40	MIPI_DSI1_DATA1_N
SAI2_RXD(GPIO2_08)	41	42	MIPI_DSI1_DATA1_P
SAI2_RXFS(GPIO2_09)	43	44	GND
CPU_RST_OUT_3V3	45	46	MIPI_DSI1_CLK_N
MIPI_CSI1_I2C0_SCL	47	48	MIPI_DSI1_CLK_P
MIPI_CSI1_I2C0_SDA	49	50	GND
MIPI_CSI1_MCLK_OUT	51	52	MIPI_DSI1_DATA0_N
CAM_RESET_OUT(GPIO1_28)	53	54	MIPI_DSI1_DATA0_P
GND	55	56	GND
VCC_5V	57	58	MIPI_DSI1_DATA2_N
VCC_3V3	59	60	MIPI_DSI1_DATA2_P

2.13.1 MIPI DSI 1 Display Interface

The i.MX 8 CPU MIPI_DSI standard controller is a flexible, high-performance, and easy-to-use digital core that implements all protocol functions defined in the MIPI DSI Specification. The MIPI DSI controller provides an interface that allows communication with MIPI DSI-compliant peripherals. The MIPI DSI D-PHY is a high frequency, low power, low-cost, source-synchronous, physical layer supporting the MIPI Alliance standard for D-PHY.

For more details on MIPI DSI 1 pinouts, refer below table:

Exp. Pin No	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
48	MIPI_DSI1_CLK_P	MIPI_DSI1_CLK_P/BG31	O, MIPI	MIPI DSI1 differential Clock positive
46	MIPI_DSI1_CLK_N	MIPI_DSI1_CLK_N/BH30	O, MIPI	MIPI DSI1 differential Clock negative
54	MIPI_DSI1_DATA0_P	MIPI_DSI1_DATA0_P/BG33	O, MIPI	MIPI DSI1 differential data lane 0 positive
52	MIPI_DSI1_DATA0_N	MIPI_DSI1_DATA0_N/BH32	O, MIPI	MIPI DSI1 differential data Lane 0 negative
42	MIPI_DSI1_DATA1_P	MIPI_DSI1_DATA1_P/BG29	O, MIPI	MIPI DSI1 differential data lane 1 positive
40	MIPI_DSI1_DATA1_N	MIPI_DSI1_DATA1_N/BH28	O, MIPI	MIPI DSI1 differential data lane 1 negative
60	MIPI_DSI1_DATA2_P	MIPI_DSI1_DATA2_P/BG35	O, MIPI	MIPI DSI1 differential data lane 2 positive
58	MIPI_DSI1_DATA2_N	MIPI_DSI1_DATA2_N/BH34	O, MIPI	MIPI DSI1 differential data lane 2 negative
36	MIPI_DSI1_DATA3_P	MIPI_DSI1_DATA3_P/BG27	O, MIPI	MIPI DSI1 differential data lane 3 positive
34	MIPI_DSI1_DATA3_N	MIPI_DSI1_DATA3_N/BH26	O, MIPI	MIPI DSI1 differential data lane 3 negative
1	LVDS1_I2C0_SCL	LVDS1_I2C0_SCL/	O, 1.8V	I2C clock Signal.

Exp. Pin No	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
		BL35	CMOS/2.2K PU	
3	LVDS1_I2C0_SDA	LVDS1_I2C0_SDA/ BE33	IO, 1.8V CMOS/2.2K PU	I2C Data Signal.
5	TP_INT(GPIO0_01)	SIM0_RST/ LSIO.GPIO0.IO01/AP48	O, 1.8V CMOS/2.2K PU	Touch Panel Interrupt Signal.

2.13.2 MIPI CSI Camera

The i.MX 8 CPU supports two 4-lane camera interfaces, the CSI-2 Rx Controller Core implements all three layers defined by the CSI-2 Specification: Pixel to Byte Packing, Low Level Protocol, and Lane Management. The D-PHY interface of the CSI-2 Rx Controller Core supports PHY Protocol Interface (PPI) compatible MIPI D-PHYs. The Local Interface is an easy to use pixel-based interface that supports 1 to 4 virtual channels and all data types. The Local interface runs at the User Interface clock rate for all implementations. The CSI-2 Rx Controller Core takes care of all packet formatting details and transmission over the MIPI bus. The i.MX 8 Pico ITX SBC supports four lane MIPI CSI camera interface via Expansion connector 3 along with the other controlling signals.

For more details on MIPI CSI1 Expansion Connector 3 pinouts, refer below table:

Exp. Pin No	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
47	MIPI_CSI1_I2C0_SCL	MIPI_CSI1_I2C0_SCL/BN17	O, 1.8V CMOS/ 2.2K PU	MIPI CSI1 I2C Clock.
49	MIPI_CSI1_I2C0_SDA	MIPI_CSI1_I2C0_SDA/BE15	IO, 1.8V CMOS/ 2.2K PU	MIPI CSI1 I2C Data.
51	MIPI_CSI1_MCLK_OUT	MIPI_CSI1_MCLK_OUT/ BN23	O, 1.8V CMOS	Master Clock for Camera.
18	MIPI_CSI1_CLK_P	MIPI_CSI1_CLK_P/BJ17	I, MIPI	MIPI CSI1 differential clock positive.
16	MIPI_CSI1_CLK_N	MIPI_CSI1_CLK_N/BH16	I, MIPI	MIPI CSI1 differential clock negative.
24	MIPI_CSI1_DATA0_P	MIPI_CSI1_DATA0_P/BH18	I, MIPI	MIPI CSI1 differential data lane 0 positive.
22	MIPI_CSI1_DATA0_N	MIPI_CSI1_DATA0_N/BJ19	I, MIPI	MIPI CSI1 differential data lane 0 negative.
12	MIPI_CSI1_DATA1_P	MIPI_CSI1_DATA1_P/BJ15	I, MIPI	MIPI CSI1 differential data lane 1 positive.
10	MIPI_CSI1_DATA1_N	MIPI_CSI1_DATA1_N/BH14	I, MIPI	MIPI CSI1 differential data lane 1 negative.
30	MIPI_CSI1_DATA2_P	MIPI_CSI1_DATA2_P/BJ21	I, MIPI	MIPI CSI1 differential data lane 2 positive.
28	MIPI_CSI1_DATA2_N	MIPI_CSI1_DATA2_N/BH20	I, MIPI	MIPI CSI1 differential data lane 2 negative.
6	MIPI_CSI1_DATA3_P	MIPI_CSI1_DATA3_P/BJ13	I, MIPI	MIPI CSI1 differential data lane 3 positive.

Exp. Pin No	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
4	MIPI_CSI1_DATA3_N	MIPI_CSI1_ DATA3_N/BH12	I, MIPI	MIPI CSI1 differential data lane 3 negative.

2.13.3 CAN Interface

The Flexible Controller Area Network (FLEXCAN) module is a communication controller implementing the CAN protocol according to the CAN 2.0B protocol specification. FLEXCAN2 of CPU are connected to Expansion connector3.

For more details on Expansion Connector CAN pinouts, refer below table:

Exp. Pin No	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
15	FLEXCAN2_RX	FLEXCAN2_RX/C 3	I, 1.8V CMOS	CAN Receiver.
17	FLEXCAN2_TX	FLEXCAN2_TX/E 7	O, 1.8V CMOS	CAN Transmitter.

2.13.4 UART Interface

The i.MX 8 CPU's UART3 connected to Expansion connector3.

For more details on UART3 pinouts, refer below table:

Exp. Pin No	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
7	UART3_RX_GPIO	M41_GPIO0_00 /DMA.UART3.R X/AP44 Or LVDS0_I2C1_SD A/ BE35	I, 1.8V CMOS	UART3 Receiver. <i>Note : Optionally connected LCD enable GPIO..</i>
9	UART3_TX_GPIO	M41_GPIO0_01 /DMA.UART3.TX /AU47 Or LVDS1_I2C1_SC L/ BD32	O, 1.8V CMOS	UART3 Transmitter <i>Note : Optionally connected LCD enable GPIO.</i>

Note: Contact iWave support team if GPIO support is required

2.13.5 DMA I2C2. Interface

For more details on Expansion Connector-1, DMA I2C pinouts, refer below table:

Exp. Pin No	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
11	DMA_I2C1_SCL	GPT0_CLK/DMA .I2C1.SCL/ AY52	O, 1.8V CMOS/2.2K PU	I2C clock.
13	DMA_I2C1_SDA	GPT0_CAPTURE /DMA.I2C1.SDA / AV52	IO, 1.8V CMOS/2.2K PU	I2C Data.

2.13.6 M41 UART Interface

The integrated Cortex-M4 Microcontroller offloads real-time tasks from the main OS for hard real-time & low power mode. The M41 UART Interface UART Interface signals are connected to Expansion connector 3.

For more details on M40 UART pinouts, refer below table:

Exp. Pin No	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
19	M40_UART_RX_SCL(G PIO0_06)	M40_I2C0_SCL/ AM44	I, 1.8V CMOS	M40 UART Receiver.
21	M40_UART_TX_SDA(G PIO0_07)	M40_I2C0_SDA/ AU51	O, 1.8V CMOS	M40 UART Transmitter

2.13.7 QSPI Interface.

The i.MX 8 CPU supports low power Quad Serial Peripheral Interface (QSPI) module that supports an efficient interface to an QSPI bus as a master and/or a slave with maximum clock speed of 200MHz.

For more details on SPI pinouts, refer below table:

Pin No.	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
23	QSPI1A_DATA3	QSPI1A_DATA3 /LSIO.GPIO4.IO23/E11	IO, 1.8V CMOS	QSPI Data 3.
25	QSPI1A_DATA2	QSPI1A_DATA2 /LSIO.GPIO4.IO24/E13	IO, 1.8V CMOS	QSPI Data 2.
27	QSPI1A_DATA1	QSPI1A_DATA1 /LSIO.GPIO4.IO25/D14	IO, 1.8V CMOS	QSPI Data 1.
29	QSPI1A_DATA0	QSPI1A_DATA0 /LSIO.GPIO4.IO26/D12	IO, 1.8V CMOS	QSPI Data 0.
31	QSPI1A_SS0	QSPI1A_SS0_B /LSIO.GPIO4.IO19 /J11	O, 1.8V CMOS	QSPI Chip select 0.
33	QSPI1A_SS1	QSPI1A_SS1_B /LSIO.GPIO4.IO20/G11	IO, 1.8V CMOS	QSPI Chip select 1.
35	QSPI1A_SCLK	QSPI1A_SCLK /LSIO.GPIO4.IO21/F10	O, 1.8V CMOS/ 33E Series	QSPI Clock.
37	QSPI1A_RESET(GPIO4_22)	QSPI1A_DQS /LSIO.GPIO4.IO22/H12	O, 1.8V CMOS	QSPI Reset.

2.13.8 SAI Interface

The i.MX 8 CPU supports SAI2 Receive Mode module. For more details on SPI pinouts, refer below table:

Exp. Pin No	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
39	SAI2_RXC(GPIO2_07)	ESAI1_SCKT/AY10	IO, 1.8V CMOS	SAI Receive Clock
41	SAI2_RXD(GPIO2_08)	ESAI1_TX0/BF10	I, 1.8V CMOS	SAI Receive signal.
43	SAI2_RXFS(GPIO2_09)	ESAI1_TX1/BA11	IO, 1.8V CMOS	Receive Frame Sync signal

2.13.9 GPIOs

Refer GPIO Column under “i.MX 8 Pin Multiplexing on Expansion Connector” for details on GPIO options available from Expansion connector 3.

2.14 Other Features

2.14.1 Fan Header

The i.MX 8 QM/QP Pico ITX SBC supports a Fan Header to connect cooling Fan if required. This Fan Header (J10) is physically located at the top of the board as shown below.

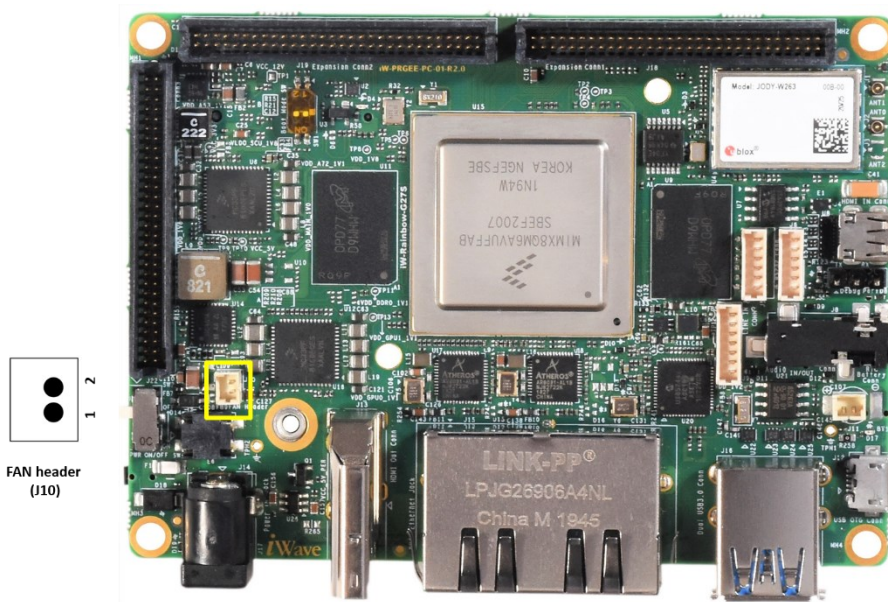


Figure 24: Fan Header

- Number of Pins - 2
- Connector Part - 10114829-10102LF from Amphenol ICC (FCI)
- Mating Connector - 10114826-00002LF from Amphenol ICC (FCI)
- Compatible FAN (Example) - MR3010H05B-RSR from Mechatronics Fan Group.

Table 14: FAN Header Pin Assignment

Pin No	Signal Name	Signal Type/ Termination	Description
1	VCC_5V	O, Power	+5V Power output to FAN. <i>Note: Optionally connected to 12V Power.</i>
2	GND	Power	Ground.

Note: Contact iWave support team if 12V Power Support is required for FAN Header support is required.

2.14.2 RTC Controller with RTC Battery Header

The i.MX 8 QM/QP Pico ITX SBC uses PF8100 PMIC, which supports external RTC cell. The SBC supports 2 pin connector for backup battery or coin cell connection. In SBC power off condition, PF8100 controller will take power from RTC battery/coin cell power and continues to keep the current time.

An Optional RTC Controller “PCF85263AT/AJ” is also supported in the The i.MX 8 QM/QP Pico ITX SBC. This external RTC Controller is connected to the .MX8 QM/QP CPU through DMA_I2C2 Interface and operates at 1.8V voltage level. The 2pin RTC(J11) battery connector is physically located on top side of the SBC as shown below.

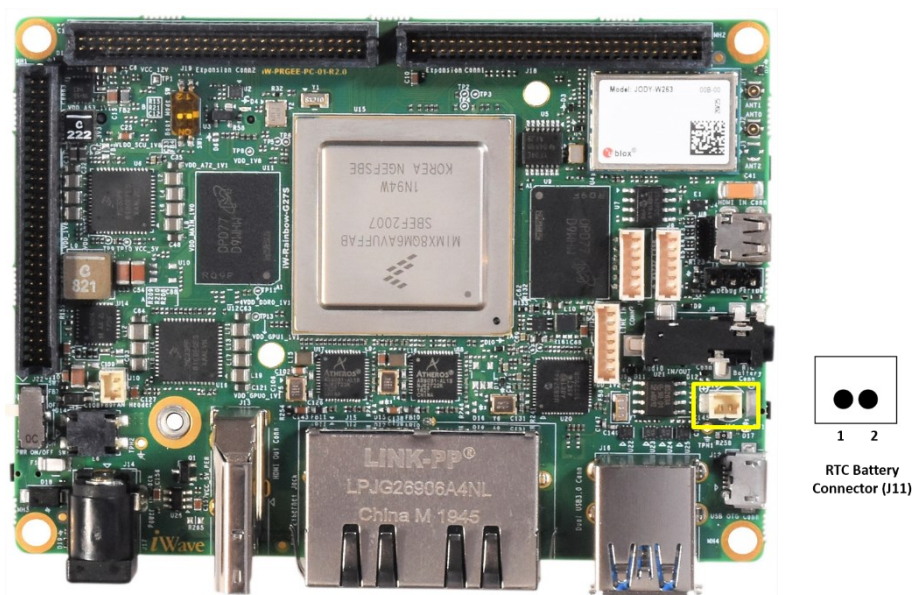


Figure 25: RTC Battery Header

- Number of Pins - 2
- Connector Part - 10114829-10102LF from Amphenol ICC (FCI)
- Mating Connector - 10114826-00002LF from Amphenol ICC (FCI)
- Mating Connector Crimp Contact - DF13-2630SCFA

Table 15: RTC Battery Header Pin Assignment

Pin No	Signal Name	Signal Type/ Termination	Description
1	VRTC_3V0	I, Power	+3V Power Input to RTC Controller
2	GND	Power	Ground.

Note: Contact iWave support team if External RTC Controller support is required.

2.14.3 JTAG Header

The i.MX 8 QM/QP Pico ITX SBC supports one JTAG interface and/or UART interface for CPU debug purpose over a customized 20-pin connector (J24). Even though this JTAG connector pinout is fully compatible with “ARM JTAG 20” connector, the physical dimension of connector is made smaller because of space constraint. i.MX 8 CPU’s JTAG pins are 1.8V tolerant and so 1.8V reference power is provided to pin 1 of the connectors to allow JTAG tool to automatically configure the logic signals for the right voltage.

The i.MX 8 CPU’s SCU_UART0 can be taken out from J24 header and via using 1.8V voltage level FTDI’s UART to USB smart cable (TTL-232RG-VREG1V8-WE) UART can be directly connected to Host PC for debugging.

JTAG Header (J26) is physically located on bottom side of the board.

Number of Pins - 20

Connector Part - 62132021021 from Wruth Electronics.

Mating Connector - LPPB102CFFN-RC from Sullins Connector Solutions

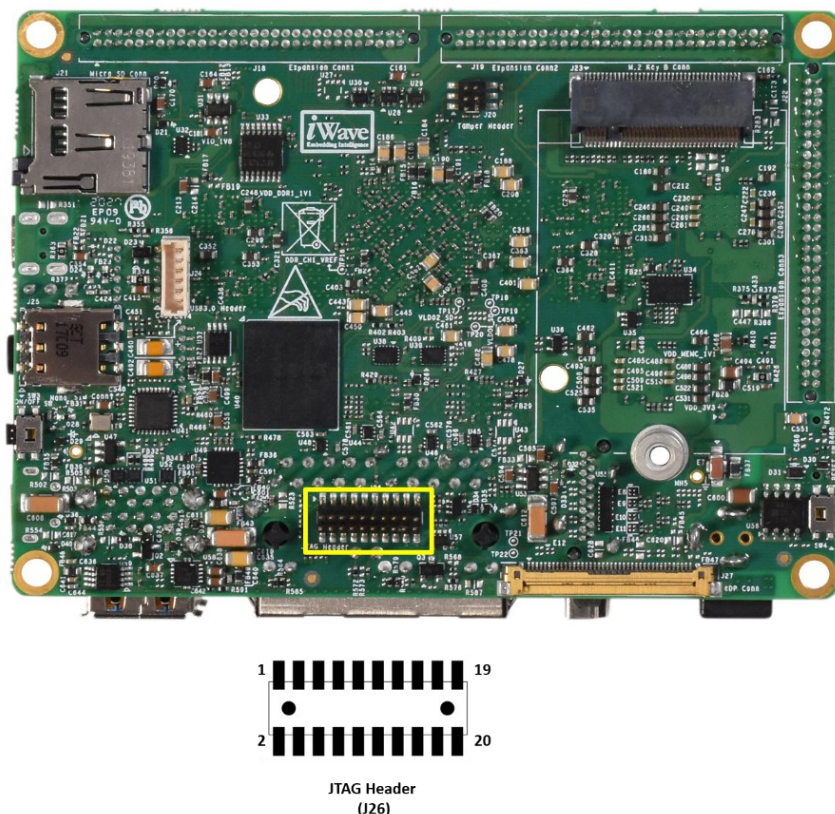


Figure 26: JTAG Header

Table 16: JTAG Header Pin Assignment

Pin No	Signal Name	Signal Type/ Termination	Description
1	VREF	O, 1.8V Power	VTREF Voltage Reference.
2	VSUPPLY	O, 1.8V Power	Supply Voltage.
3	JTAG_TRSTB	I, 1.8V CMOS/ 10K PU	JTAG test reset signal.
4	GND	Power	Ground. <i>Note: Optionally connected to SCU_UART0_TX</i>
5	JTAG_TDI	I, 1.8V CMOS/ 10K PU	JTAG test data input.
6	GND	Power	Ground. <i>Note: Optionally connected to SCU_UART0_RX</i>
7	JTAG_TMS	I, 1.8V CMOS/ 10K PU	JTAG test mode select.

8	GND	Power	Ground.
9	JTAG_TCK	I, 1.8V CMOS/ 10K PD	JTAG test Clock.
10	GND	Power	Ground.
11	-	-	Only pull down is provided.
12	GND	Power	Ground.
13	JTAG_TDO	O, 1.8V CMOS	JTAG test data output.
14	GND	Power	Ground.
15	JTAG_RESETB	I, 1.8V CMOS/ 10K PU	Reset input.
16	GND	Power	Ground.
17	-	-	Only pull up is provided.
18	GND	Power	Ground.
19	-	-	Only pull down is provided.
20	GND	Power	Ground.

Note: Contact iWave support team if SCU UART support is required.

2.14.4 Tamper Header

The i.MX 8 QM/QP Pico ITX SBC supports one Tamper Header for CPU protection purpose. The Tamper Header (J20) is physically located on bottom side of the board.

Number of Pins	-4
Connector Part	- 62130621021 from Wurth Electronics.
Mating Connector	- LPPB032CFFN-RC from Sullins Connector Solutions

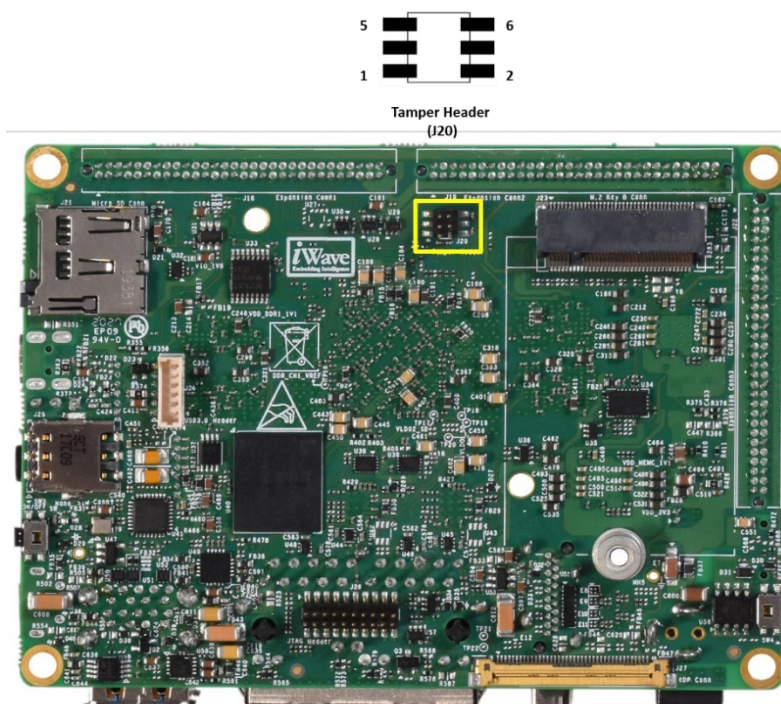


Figure 27: Tamper Header

Table 17: Tamper Header Pin Assignment

Pin No	Signal Name	Signal Type/ Termination	Description
1	SNVS_TAMPER_IN0	I, 1.8V Power	SNVS Tamper Input 0.
2	SNVS_TAMPER_OUT0	O, 1.8V Power	SNVS Tamper Output 0.
3	VDD_SNVS	O, 3V Power	VDD_SNVS Voltage Reference. <i>Note: Optionally Connected to 1.8V Power.</i>
4	GND	Power	Ground.
5	SNVS_TAMPER_IN1	I, 1.8V Power	SNVS Tamper Input 1.
6	SNVS_TAMPER_OUT1	Power	SNVS Tamper Output 1.

Note: Contact iWave support team 1.8Vto Tamper Header is required.

2.14.5 Power ON/OFF Switch

The i.MX 8 QM/QP Pico ITX SBC has power ON/OFF switch (SW2) to control the Main power Input ON/OFF functionality. The Power ON/OFF switch is physically located at the top of the board as shown below.

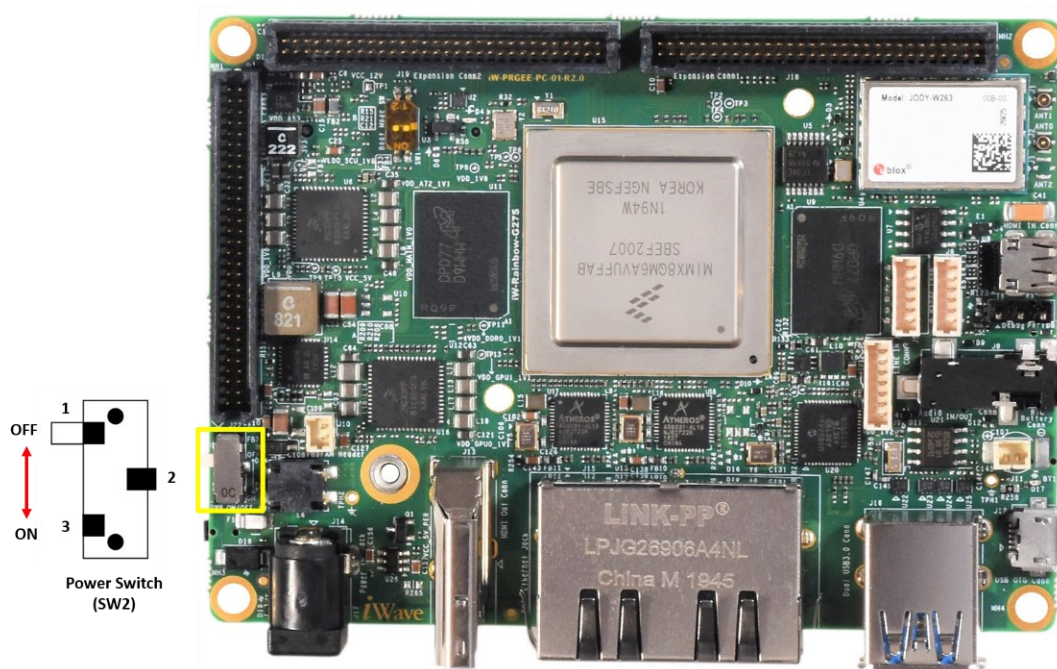


Figure 28: Power ON/OFF Switch

2.14.6 Reset Switch

The i.MX 8 QM/QP Pico ITX SBC supports Push button switch (SW1) to reset the i.MX 8 QM/QP CPU. Reset signal is directly connected from Reset Push button switch. This Reset Push button switch (SW4) is physically located at the bottom of the board as shown below.

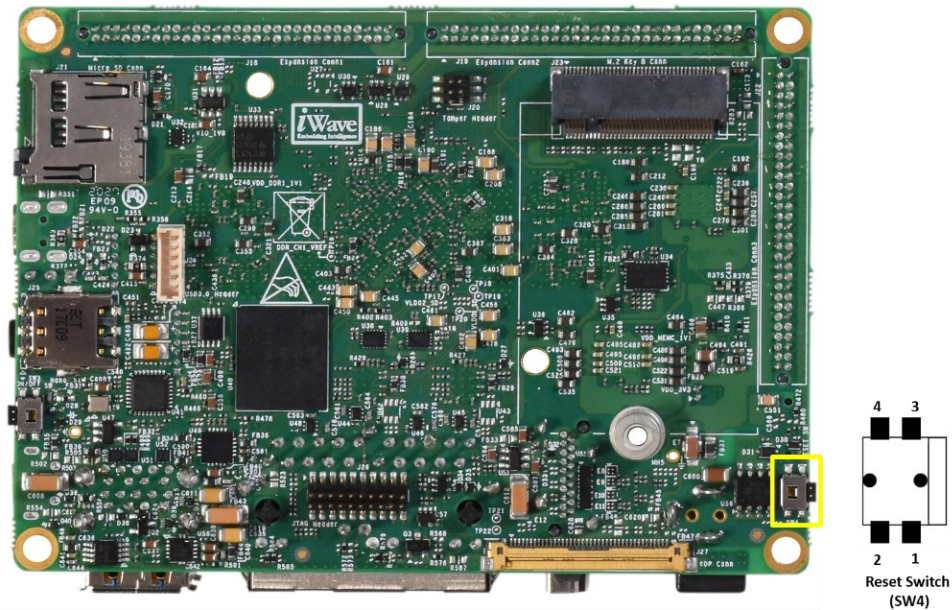


Figure 29: Reset Switch

2.14.7 CPU ON/OFF Switch

The i.MX 8 QM/QP Pico ITX SBC supports Push button switch (SW1) for ON OFF the i.MX 8 QM/QP CPU. ON/OFF is directly connected from ON/OFF Push button switch. This ON/OFF Push button switch (SW3) is physically located at the bottom of the board as shown below.

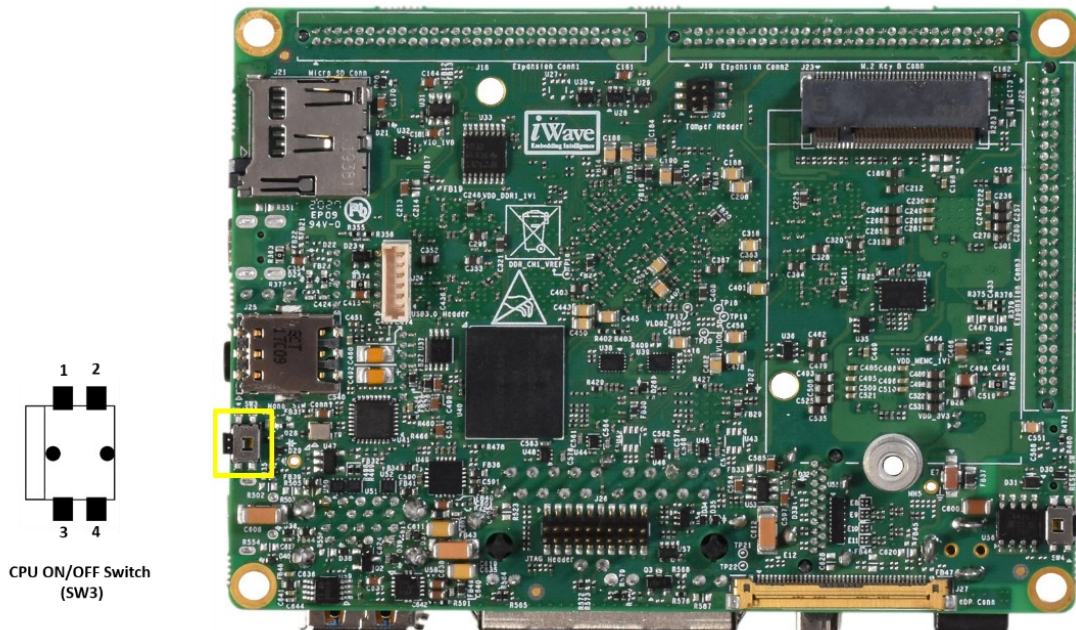


Figure 30: CPU ON/OFF Switch

2.15 i.MX 8 Pin Multiplexing on Expansion Connectors

The i.MX 8 QM/QP CPU IO pins have many alternate functions and can be configured to any one of the alternate functions based on the requirement, also most of the i.MX 8 CPU's IO pins can be configured as GPIO if required. The below table provides the details of i.MX 8 QM/QP CPU pin connections to the Expansion Connector and with selected pin function highlighted and available alternate functions. This table has been prepared by referring NXP's i.MX 8 Hardware User's Manual.

Important Note: It is strongly recommended to use the pin function same as selected in the Pico ITX SBC for iWave's BSP reusability.

Table 18: i.MX 8 QM/QP CPU IOMUX for Expansion Connector 1 interfaces

Interface/ Function	Expansion Connector Pin Number	i.MX 8 CPU Pin Number	Function 0	Function 1	Function 2	Function 3	GPIO	Default State
LVDS1 Channel0	30	BK36	LVDS1_CH0_CLK_N					LVDS1_CH0_CLK_N
	28	BM36	LVDS1_CH0_CLK_P					LVDS1_CH0_CLK_P
	18	BL37	LVDS1_CH0_TX0_N					LVDS1_CH0_TX0_N
	16	BN37	LVDS1_CH0_TX0_P					LVDS1_CH0_TX0_P
	24	BK38	LVDS1_CH0_TX1_N					LVDS1_CH0_TX1_N
	22	BM38	LVDS1_CH0_TX1_P					LVDS1_CH0_TX1_P
	6	BL39	LVDS1_CH0_TX2_N					LVDS1_CH0_TX2_N
	4	BN39	LVDS1_CH0_TX2_P					LVDS1_CH0_TX2_P
	12	BK40	LVDS1_CH0_TX3_N					LVDS1_CH0_TX3_N
	10	BM40	LVDS1_CH0_TX3_P					LVDS1_CH0_TX3_P
LVDS1 Channel1	55	BK34	LVDS1_CH1_CLK_N					LVDS1_CH1_CLK_N
	57	BM34	LVDS1_CH1_CLK_P					LVDS1_CH1_CLK_P
	49	BL33	LVDS1_CH1_TX0_N					LVDS1_CH1_TX0_N
	51	BN33	LVDS1_CH1_TX0_P					LVDS1_CH1_TX0_P
	43	BK32	LVDS1_CH1_TX1_N					LVDS1_CH1_TX1_N
	45	BM32	LVDS1_CH1_TX1_P					LVDS1_CH1_TX1_P
	37	BL31	LVDS1_CH1_TX2_N					LVDS1_CH1_TX2_N
	39	BN31	LVDS1_CH1_TX2_P					LVDS1_CH1_TX2_P
	31	BK30	LVDS1_CH1_TX3_N					LVDS1_CH1_TX3_N
	33	BM30	LVDS1_CH1_TX3_P					LVDS1_CH1_TX3_P
	36	BD34	LVDS1.GPIO0.IO00	LVDS1.PWM0.OUT		LSIO.GPIO1.IO10	GPIO1_10	LVDS1.PWM0.OUT

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Interface/ Function	Expansion Connector Pin Number	i.MX 8 CPU Pin Number	Function 0	Function 1	Function 2	Function 3	GPIO	Default State
	38	BN35	LVDS1.I2C1.SDA	DMA.UART3.RX		LSIO.GPIO1.IO15	GPIO1_15	LSIO.GPIO1.IO15
MIPI DSI0	15	BN27	MIPI_DSI0.CKN					MIPI_DSI0.CKN
	13	BL27	MIPI_DSI0.CKP					MIPI_DSI0.CKP
	21	BM28	MIPI_DSI0.DN0					MIPI_DSI0.DN0
	19	BK28	MIPI_DSI0.DP0					MIPI_DSI0.DP0
	9	BM26	MIPI_DSI0.DN1					MIPI_DSI0.DN1
	7	BK26	MIPI_DSI0.DP1					MIPI_DSI0.DP1
	27	BN29	MIPI_DSI0.DN2					MIPI_DSI0.DN2
	25	BL29	MIPI_DSI0.DP2					MIPI_DSI0.DP2
	3	BN25	MIPI_DSI0.DN3					MIPI_DSI0.DN3
	1	BL25	MIPI_DSI0.DP3					MIPI_DSI0.DP3
	32	BA53	GPT1_CLK	DMA.I2C2.SCL	LSIO.KPP0.COL7	LSIO.GPIO0.IO17	GPIO0_17	DMA.I2C2.SCL
	34	AY50	GPT1_CAPTURE	DMA.I2C2.SDA	LSIO.KPP0.ROW4	LSIO.GPIO0.IO18	GPIO0_18	DMA.I2C2.SDA
CAN1 1/SPDIF	40	E5	DMA.FLEXCAN1.RX			LSIO.GPIO3.IO31	GPIO3_31	DMA.FLEXCAN1.RX
		BC7	AUD.SPDIF0.RX	AUD.MQS.R	AUD.ACM.MCLK_IN1	LSIO.GPIO2.IO14	GPIO2_14	
	42	G7	DMA.FLEXCAN1.TX			LSIO.GPIO4.IO00	GPIO4_00	DMA.FLEXCAN1.TX
		BC9	AUD.SPDIF0.TX	AUD.MQS.L	AUD.ACM.MCLK_OUT1	LSIO.GPIO2.IO15	GPIO2_15	
	44	BN15	MIPI_CSI1.GPIO0.IO00	DMA.UART4.RX		LSIO.GPIO1.IO30	GPIO1_30	LSIO.GPIO1.IO30
		BD6	AUD.SPDIF0.EXT_CLK	DMA.DMA0.REQ_IN0		LSIO.GPIO2.IO16	GPIO2_16	
SPI3	54	BF6	DMA.SPI3.SCK			LSIO.GPIO2.IO17	GPIO2_17	DMA.SPI3.SCK
	52	BE5	DMA.SPI3.SDI	DMA.FTM.CH1		LSIO.GPIO2.IO19	GPIO2_19	DMA.SPI3.SDI
	50	BF2	DMA.SPI3.SDO	DMA.FTM.CH0		LSIO.GPIO2.IO18	GPIO2_18	DMA.SPI3.SDO
	46	BG5	DMA.SPI3.CS0	DMA.FTM.CH2		LSIO.GPIO2.IO20	GPIO2_20	DMA.SPI3.CS0
	48	BD8	DMA.SPI3.CS1			LSIO.GPIO2.IO21	GPIO2_21	DMA.SPI3.CS1

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Table 19: i.MX 8 QM/QP CPU IOMUX for Expansion Connector 2 interfaces

Interface/ Function	Expansion Connector Pin Number	i.MX 8 CPU Pin Number	Function 0	Function 1	Function 2	Function 3	GPIO	Default State
LVDS0 Channel0	6	BL41	LVDS0_CH0_CLK_N					LVDS0_CH0_CLK_N
	4	BN41	LVDS0_CH0_CLK_P					LVDS0_CH0_CLK_P
	12	BK42	LVDS0_CH0_TX0_N					LVDS0_CH0_TX0_N
	10	BM42	LVDS0_CH0_TX0_P					LVDS0_CH0_TX0_P
	18	BL43	LVDS0_CH0_TX1_N					LVDS0_CH0_TX1_N
	16	BN43	LVDS0_CH0_TX1_P					LVDS0_CH0_TX1_P
	24	BK44	LVDS0_CH0_TX2_N					LVDS0_CH0_TX2_N
	22	BM44	LVDS0_CH0_TX2_P					LVDS0_CH0_TX2_P
	30	BL45	LVDS0_CH0_TX3_N					LVDS0_CH0_TX3_N
	28	BN45	LVDS0_CH0_TX3_P					LVDS0_CH0_TX3_P
LVDS0 Channel1	60	BG45	LVDS0_CH1_CLK_N					LVDS0_CH1_CLK_N
	58	BH46	LVDS0_CH1_CLK_P					LVDS0_CH1_CLK_P
	54	BG43	LVDS0_CH1_TX0_N					LVDS0_CH1_TX0_N
	52	BH44	LVDS0_CH1_TX0_P					LVDS0_CH1_TX0_P
	48	BG41	LVDS0_CH1_TX1_N					LVDS0_CH1_TX1_N
	46	BH42	LVDS0_CH1_TX1_P					LVDS0_CH1_TX1_P
	42	BG39	LVDS0_CH1_TX2_N					LVDS0_CH1_TX2_N
	40	BH40	LVDS0_CH1_TX2_P					LVDS0_CH1_TX2_P
	36	BG37	LVDS0_CH1_TX3_N					LVDS0_CH1_TX3_N
	34	BH38	LVDS0_CH1_TX3_P					LVDS0_CH1_TX3_P
LVDS0 Control	29	BD38	LVDS0_I2C0_SCL	LVDS0.GPIO0.IO02		LSIO.GPIO1.IO06	GPIO1_06	LVDS0_I2C0_SCL
	31	BD36	LVDS0_I2C0_SDA	LVDS0.GPIO0.IO03		LSIO.GPIO1.IO07	GPIO1_07	LVDS0_I2C0_SDA
	33	BE39	LVDS0.GPIO0.IO00	LVDS0.PWM0.OUT		LSIO.GPIO1.IO04	GPIO1_04	LVDS0.PWM0.OUT
	35	BE37	LVDS0_I2C1_SCL	DMA.UART2.TX		LSIO.GPIO1.IO08	GPIO1_08	LSIO.GPIO1.IO08
SPI2	43	AW5	DMA.SPI2.SCK				GPIO3_07	LSIO.GPIO3.IO07
	45	AW1	DMA.SPI2.CS0				GPIO3_10	LSIO.GPIO3.IO10
	47	AY4	DMA.SPI2.SDI				GPIO3_09	LSIO.GPIO3.IO09
	49	BA1	DMA.SPI2.SDO				GPIO3_08	LSIO.GPIO3.IO08
MIPI CSIO	15	BE21	MIPI_CSIO.CKN					MIPI_CSIO.CKN
	13	BF20	MIPI_CSIO.CKP					MIPI_CSIO.CKP
	21	BE23	MIPI_CSIO.DN0					MIPI_CSIO.DN0

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Interface/ Function	Expansion Connector Pin Number	i.MX 8 CPU Pin Number	Function 0	Function 1	Function 2	Function 3	GPIO	Default State
	19	BF22	MIPI_CSI0.DP0					MIPI_CSI0.DP0
	9	BE19	MIPI_CSI0.DN1					MIPI_CSI0.DN1
	7	BF18	MIPI_CSI0.DP1					MIPI_CSI0.DP1
	27	BE25	MIPI_CSI0.DN2					MIPI_CSI0.DN2
	25	BF24	MIPI_CSI0.DP2					MIPI_CSI0.DP2
	3	BE17	MIPI_CSI0.DN3					MIPI_CSI0.DN3
	1	BF16	MIPI_CSI0.DP3					MIPI_CSI0.DP3
	41	BJ23	MIPI_CSI0.ACM.MCLK_OUT			LSIO.GPIO1.IO24	GPIO1_24	MIPI_CSI0.ACM.MCLK_OUT
	37	BH24	MIPI_CSI0.I2C0.SCL			LSIO.GPIO1.IO25	GPIO1_25	MIPI_CSI0.I2C0.SCL
	39	BN19	MIPI_CSI0.I2C0.SDA			LSIO.GPIO1.IO26	GPIO1_26	MIPI_CSI0.I2C0.SDA
M41 UART0	51	AR45	M41.I2C0.SCL	M41.UART0.RX	M41.GPIO0.IO02	LSIO.GPIO0.IO10	GPIO0_10	M41.UART0.RX
	53	AU49	M41.I2C0.SDA	M41.UART0.TX	M41.GPIO0.IO03	LSIO.GPIO0.IO11	GPIO0_11	M41.UART0.TX

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Table 20: i.MX 8 QM/QP CPU IOMUX for Expansion Connector 3 interfaces

Interface/ Function	Expansion Connector Pin Number	i.MX 8 CPU Pin Number	Function 0	Function 1	Function 2	Function 3	GPIO	Default State
MIPI DSI1	46	BH30	MIPI_DSI1.CKN					MIPI_DSI1.CKN
	48	BG31	MIPI_DSI1.CKP					MIPI_DSI1.CKP
	52	BH32	MIPI_DSI1.DN0					MIPI_DSI1.DN0
	54	BG33	MIPI_DSI1.DP0					MIPI_DSI1.DP0
	40	BH28	MIPI_DSI1.DN1					MIPI_DSI1.DN1
	42	BG29	MIPI_DSI1.DP1					MIPI_DSI1.DP1
	58	BH34	MIPI_DSI1.DN2					MIPI_DSI1.DN2
	60	BG35	MIPI_DSI1.DP2					MIPI_DSI1.DP2
	34	BH26	MIPI_DSI1.DN3					MIPI_DSI1.DN3
	36	BG27	MIPI_DSI1.DP3					MIPI_DSI1.DP3
	5	AP48	DMA.SIM0.RST			LSIO.GPIO0.IO01	GPIO0_01	LSIO.GPIO0.IO01
	1	BL35	LVDS1.I2C0.SCL	LVDS1.GPIO0.IO02		LSIO.GPIO1.IO12	GPIO1_12	
	3	BE33	LVDS1.I2C0.SDA	LVDS1.GPIO0.IO03		LSIO.GPIO1.IO13	GPIO1_13	
MIPI CSI1	16	BH16	MIPI_CSI1.CKN					MIPI_CSI1.CKN
	18	BJ17	MIPI_CSI1.CKP					MIPI_CSI1.CKP
	22	BH18	MIPI_CSI1.DN0					MIPI_CSI1.DN0
	24	BJ19	MIPI_CSI1.DP0					MIPI_CSI1.DP0
	10	BH14	MIPI_CSI1.DN1					MIPI_CSI1.DN1
	12	BJ15	MIPI_CSI1.DP1					MIPI_CSI1.DP1
	28	BH20	MIPI_CSI1.DN2					MIPI_CSI1.DN2
	30	BJ21	MIPI_CSI1.DP2					MIPI_CSI1.DP2
	4	BH12	MIPI_CSI1.DN3					MIPI_CSI1.DN3
	6	BJ13	MIPI_CSI1.DP3					MIPI_CSI1.DP3
	47	BN17	MIPI_CSI1.I2C0.SCL			LSIO.GPIO2.IO00	GPIO2_00	MIPI_CSI1.I2C0.SCL
	49	BE15	MIPI_CSI1.I2C0.SDA			LSIO.GPIO2.IO01	GPIO2_01	MIPI_CSI1.I2C0.SDA
	51	BN23	MIPI_CSI1.ACM.MCLK_OUT			LSIO.GPIO1.IO29	GPIO1_29	MIPI_CSI1.ACM.MCLK_OUT
DMA I2C 1	11	AY52	LSIO.GPT0.CLK	DMA.I2C1.SCL	LSIO.KPP0.COL4	LSIO.GPIO0.IO14	GPIO0_14	DMA.I2C1.SCL
	13	AV52	LSIO.GPT0.CAPTURE	DMA.I2C1.SDA	LSIO.KPP0.COL5	LSIO.GPIO0.IO15	GPIO0_15	DMA.I2C1.SDA
UART3	7	AP44	M41.TPM0.CH0	M41.GPIO0.IO00	DMA.UART3.RX	LSIO.GPIO0.IO12	GPIO0_12	DMA.UART3.RX
		BE35	LVDS0.I2C1.SDA	DMA.UART2.RX		LSIO.GPIO1.IO09	GPIO1_09	
	9	AU47	M41.TPM0.CH1	M41.GPIO0.IO01	DMA.UART3.TX	LSIO.GPIO0.IO13	GPIO0_13	DMA.UART3.TX

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Interface/ Function	Expansion Connector Pin Number	i.MX 8 CPU Pin Number	Function 0	Function 1	Function 2	Function 3	GPIO	Default State
		BD32	LVDS1.I2C1.SCL	DMA.UART3.TX		LSIO.GPIO1.IO14	GPIO1_14	
CAN 2	15	C3	FLEXCAN2_RX			LSIO.GPIO4.IO01	GPIO4_01	FLEXCAN2_RX
	17	E7	FLEXCAN2_TX			LSIO.GPIO4.IO02	GPIO4_02	FLEXCAN2_TX
M40 UART0	19	AM44	M40.I2C0.SCL	M40.UART0.RX	M40.GPIO0.IO02	LSIO.GPIO0.IO06	GPIO0_06	M40.UART0.RX
	21	AU51	M40.I2C0.SDA	M40.UART0.TX	M40.GPIO0.IO03	LSIO.GPIO0.IO07	GPIO0_07	M40.UART0.TX
QSPI1A	31	J11	LSIO.QSPI1A.SS0_B			LSIO.GPIO4.IO19	GPIO4_19	LSIO.QSPI1A.SS0_B
	33	G11	LSIO.QSPI1A.SS1_B			LSIO.GPIO4.IO20	GPIO4_20	LSIO.QSPI1A.SS1_B
	35	F10	LSIO.QSPI1A.SCLK			LSIO.GPIO4.IO21	GPIO4_21	LSIO.QSPI1A.SCLK
	37	H12	LSIO.QSPI1A.DQS			LSIO.GPIO4.IO22	GPIO4_22	LSIO.GPIO4.IO22
	23	E11	LSIO.QSPI1A.DATA3			LSIO.GPIO4.IO23	GPIO4_23	LSIO.QSPI1A.DATA3
	25	E13	LSIO.QSPI1A.DATA2			LSIO.GPIO4.IO24	GPIO4_24	LSIO.QSPI1A.DATA2
	27	D14	LSIO.QSPI1A.DATA1			LSIO.GPIO4.IO25	GPIO4_25	LSIO.QSPI1A.DATA1
	29	D12	LSIO.QSPI1A.DATA0			LSIO.GPIO4.IO26	GPIO4_26	LSIO.QSPI1A.DATA0
GPIOs	39	AY10	AUD.ESAI1.SCKT	AUD.SAI2.RXC		LSIO.GPIO2.IO07	GPIO2_07	LSIO.GPIO2.IO07
	41	BF10	AUD.ESAI1.TX0	AUD.SAI2.RXD		LSIO.GPIO2.IO08	GPIO2_08	LSIO.GPIO2.IO08
	43	BA11	AUD.ESAI1.TX1	AUD.SAI2.RXFS		LSIO.GPIO2.IO09	GPIO2_09	LSIO.GPIO2.IO09
	53	BM22	MIPI_CSI0.GPIO0.IO01	DMA.I2C0.SDA		LSIO.GPIO1.IO28	GPIO1_28	LSIO.GPIO1.IO28

Note: The Expansion Connector 1, 2 & 3 Pins are configured as unused pins and to be used and configured based on the application requirement. Contact iWave support team for the configuration Support.

3. TECHNICAL SPECIFICATION

This section provides detailed information about the i.MX 8 Pico ITX SBC technical specification with Electrical, Environmental and Mechanical characteristics.

3.1 Electrical Characteristics

3.1.1 Power Input Requirement

The i.MX 8 QM/QP Pico ITX SBC is designed to work with 12V external power and uses on board voltage regulators for internal power management. 12V power input from an external power supply is connected to the i.MX 8 QM/QP Pico ITX SBC through Power Jack (J17). This 2.5mm x 6.5mm barrel connector Jack should fit standard DC Plugs with an inner dimension of 2.5mm and an outer dimension of 5.5mm. The Power Jack is physically placed at the top of the board as shown below.

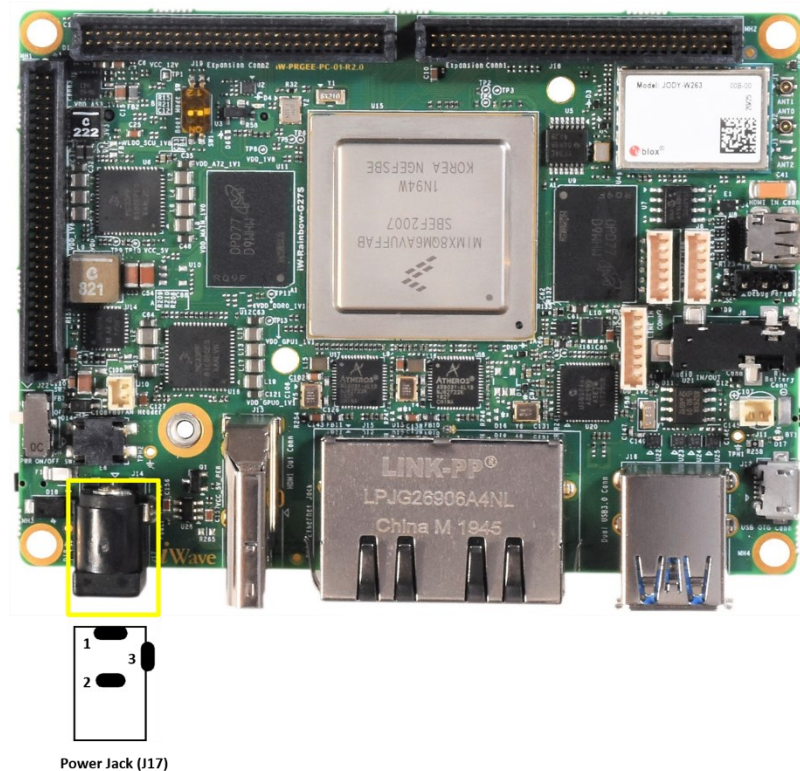


Figure 31: Power Input Jack

Table 21: Power Input Requirement

Sl. No.	Power Rail	Min (V)	Typical (V)	Max(V)	Max Input Ripple
1	VCC_12V	11.75V	12V	12.25V	±50mV
2	VRTC_3V0 ¹	2.8V	3V	3.3V	±20mV

¹ The i.MX 8 QM/QP Pico ITX SBC uses this voltage as backup power source to PMIC RTC controller when VCC is off.

3.1.2 Power Output Specification

The i.MX 8 QM/QP Pico ITX SBC has dedicated power regulator to provide +5V power to PMIC for VIN power supply. Also +3V RTC power from coin cell holder is provided to PMIC for Real time clock support.

The i.MX 8 QM/QP Pico ITX SBC shares the on board +12V, +5V and +3.3V power to Expansion connectors for Add-On Module power

Table 22: Power Output Specification

Sl. No.	Power Rail	Min (V)	Typical (V)	Max(V)	Max Output Current (mA)
Power to PMIC (through RTC connector)					
1	VRTC_3V0	2.8V	3V	3.3V	-
Power Output on Expansion Connector 1					
1	VCC_12V	11.75V	12V	12.25V	100mA
2	VCC_5V	4.85V	5V	5.15V	500mA
Power Output on Expansion Connector 2					
1	VCC_12V	11.75V	12V	12.25V	100mA
2	VCC_5V	4.85V	5V	5.15V	500mA
Power Output on Expansion Connector 3					
1	VCC_5V	4.85V	5V	5.15V	500mA
2	VCC_3V3	3.15	3.3	3.45	500mA
Power Output on M.2 Key B Connector					
1	VCC_3V3	3.15	3.3	3.45	2500mA
Power Output on JTAG Header					
1	VCC_1V8	1.71	1.8	1.89	100mA
Power Output on Tamper Header					
1	VCC_SNVS	1.71	1.8	1.89	5mA
Power Output on CAN Header					
1	VCC_5V	4.85V	5V	5.15V	100mA
Power Output on FAN Header					
1	VCC_5V	4.85V	5V	5.15V	500mA
Power Output on USB Header					
1	VCC_5V	4.85V	5V	5.15V	500mA

3.1.3 Power Output Specification

Table 23: Power Consumption

Task/Status	Power Rail	Current Drawn/ Power Consumption
Run Mode Power Consumption¹		
Play 4K@60Hz Video run in HDMI display	VCC_12V	10.67 W
Play 4K@30Hz Video run in HDMI display	VCC_12V	13.12 W
Play 1080p @30Hz Video run in HDMI display	VCC_12V	9.91 W
GPU Processor -Graphics 3D Test	VCC_12V	13.75 W
Play Audio	VCC_12V	6.08 W
Ping Bluetooth	VCC_12V	6.77 W
Ping Wi-Fi	VCC_12V	6.02 W
Ping Ethernet (Eth0 & Eth1) at 1000Mbps	VCC_12V	6.65 W
Ping Ethernet (Eth0 & Eth1) at 100Mbps	VCC_12V	5.81 W
Ping Ethernet (Eth0 & Eth1) at 10Mbps	VCC_12V	5.59 W
eMMC to Micro SD file transfer	VCC_12V	7.27 W
eMMC to USB2.0 OTG file transfer	VCC_12V	7.96 W
eMMC to USB3.0 file transfer	VCC_12V	8.98 W
eMMC to M.2 SATA file transfer	VCC_12V	8.26 W
Bluetooth file transfer	VCC_12V	5.94W
Wi-Fi file transfer	VCC_12V	7.38 W
Ethernet Streaming (Video Play)	VCC_12V	13.39 W
Dhrystone	VCC_12V	8.24 W
Maximum Power Test: - Run the below during Maximum Power Test, - Play Video run in MIPI display (Gplay) - Camera Streaming - Ethernet (eth0 & eth1) Run the ping (65500 packet size) - Wi-Fi- Run the ping testing in background - File Transfer - Transfer the 1GB files in storage devices - Run the dry2 application on background - GPU Processor -Graphics 3D Test	VCC_12V	18.19 W
Low Power Mode Power Consumption		
System Idle Mode.	VCC_12V	4.74 W
Deep Sleep Mode.	VCC_12V	3.30 W
RTC power when no VIN_3V3 supply is provided	VRTC_3V0	156 μW

¹ Power consumption measurements are done in iWave's i.MX 8 QM CPU based i.MX 8 QM/QP Pico ITX SBC with iWave's iW-PRGEE-SC-01-R2.0-REL1.0-Linux4.14.98.

3.2 Environmental Characteristics

3.2.1 Environmental Specification

The below table provides the Environment specification of i.MX 8 QM/QP Pico ITX SBC.

Table 24: Environmental Specification

Parameters	Min	Max
Operating temperature range ¹	-40°C	85°C

¹ iWave guarantees the component selection for the given operating temperature. The operating temperature at the system level will be affected by the various system components like carrier board and its components, system enclosure, air circulation in the system, system power supply etc. Based on the system design, specific heat dissipating approach might be required from system to system. It is recommended to do the necessary system level thermal simulation and find necessary thermal solution in the system before using this board in the end application.

² For more information on Thermal solution & Heat sink refer the following section.

3.2.2 Heat Sink & Fan Sink

For any highly integrated SBC, thermal design is a very important factor. As IC's size is decreasing and performance of module is increasing by rising processor frequencies, it generates high amount of heat which should be dissipated for the system to work as expected without fault.

To dissipate the heat, appropriate thermal management techniques like Heat spreader, Heat sink or Fan Sink must be used. Always need to remember that more effective thermal solution will give more performance out of the CPU.

Heat spreader acts as thermal coupling device between Module and external thermal solution. Heat spreader also provides thermal coupling to CPU via gap filler for better heat exchange. Heat spreader is not a complete thermal solution by itself. Heat spreader has to be used with application specific thermal solutions like heat sinks, Chassis, fans, Heat pipes etc.

The Heatsink and Fan sink supported for the i.MX 8 QM/QP Pico ITX SBC is shown in following figures.

Note: iWave supports Heat Sink Solution for i.MX 8 Pico ITX SBC. For more information on Heat Sink & Fan Sink contact iWave support team. Do not Power On the i.MX 8 QM/QP Pico ITX SBC without a proper thermal solution.

iW-Rainbow-G27S
i.MX8 Quad MAX/Quad Plus Pico ITX SBC HEAT SINK
ORDERING PART NO: iW-HSKALU-BLABLC-SB02

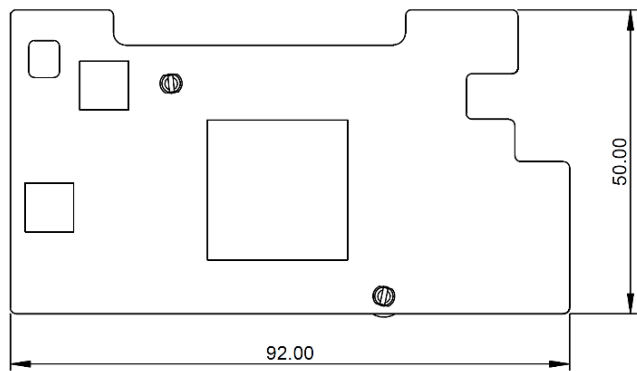


Fig 1.1

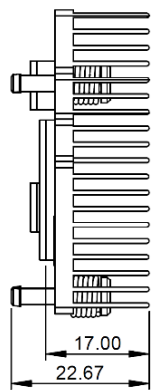


Fig 1.2

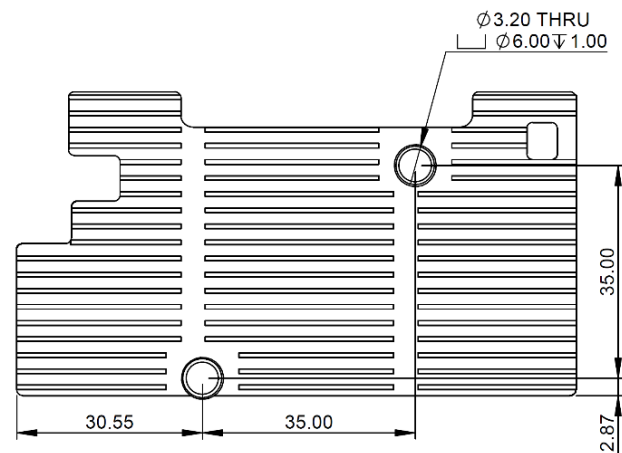


Fig 1.3

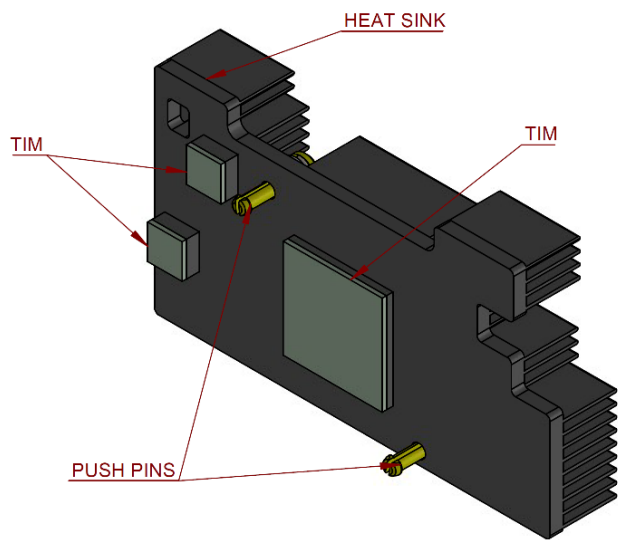


Fig 1.4

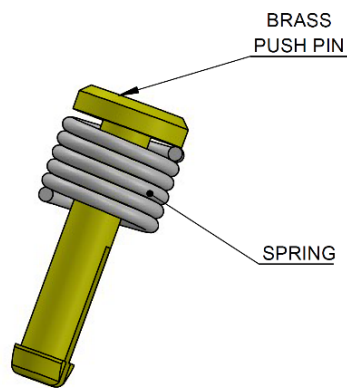


Fig 1.5

TABLE1.1: TIM SPECIFICATIONS	
MATERIAL	SILICONE RUBBER (BASE MATERIAL)
THERMAL CONDUCTIVITY	12.5W/mK
FLAME RATING	UL 94 V-0
HARDNESS	50 Shore 00
WORKING TEMP.	-50~+150 °C
ROHS	YES

Figure 32: Mechanical dimension of Heat Sink

iW-Rainbow-G27S
i.MX8 Quad MAX/Quad Plus Pico ITX SBC FAN SINK
ORDERING PART NO: iW-FSKALU-BLABLC-SB02

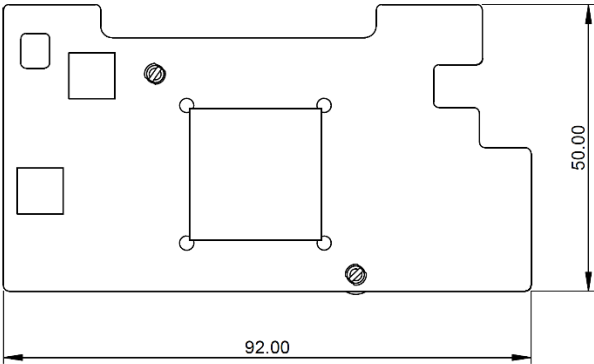


Fig 1.1

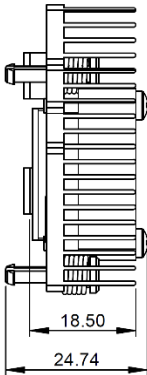


Fig 1.2

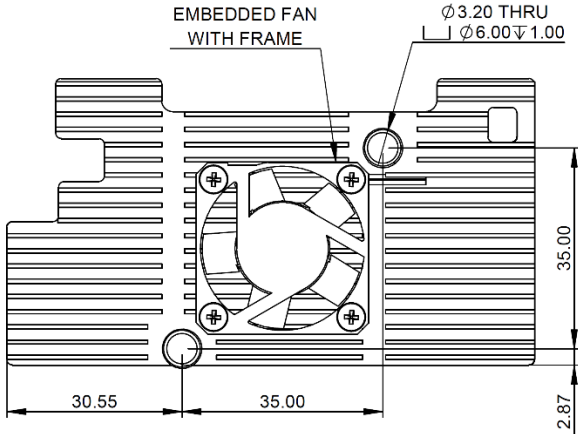


Fig 1.3

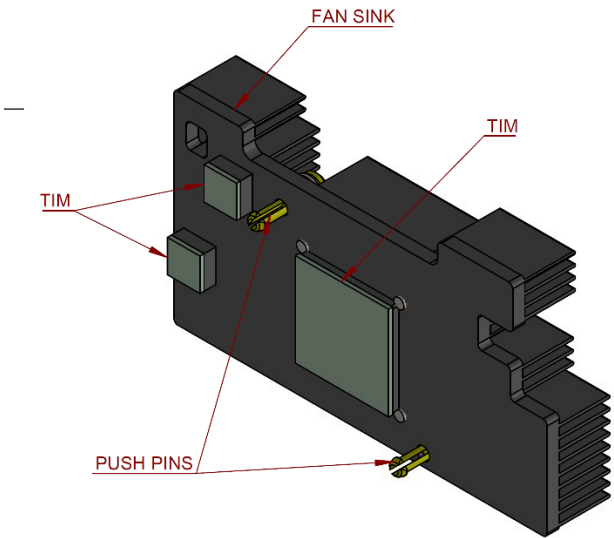


Fig 1.4

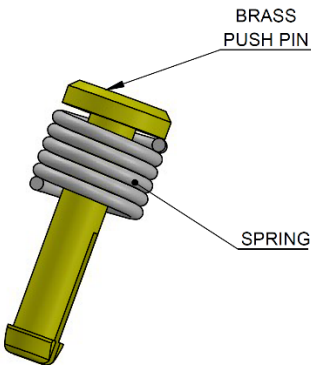


Fig 1.5

TABLE 1.1: FAN SPECIFICATIONS	
PART NO.	MR3010H05B-RSR
DIMENSIONS	30X30X10mm
AIR FLOW	6.4 CFM 0.18m3/min
STATIC PRESSURE	6.64mmH2O
RATED VOLTAGE	5V DC
FLAME RATING	UL 94 V-0
ROHS	YES

TABLE1.2: TIM SPECIFICATIONS	
MATERIAL	SILICONE RUBBER (BASE MATERIAL)
THERMAL CONDUCTIVITY	12.5W/mK
FLAME RATING	UL 94 V-0
HARDNESS	50 Shore 00
WORKING TEMP.	-50~+150 °C
ROHS	YES

Figure 33: Mechanical dimension of Fan Sink

i.MX 8 QM/QP PICO ITX SBC Also supports miniature Heat Sink. The Heat Sink details are below

Heat Sink Part Number - FSR30-15B-0N1T from Alpha

DC Fan Part Number - MR3010H05B-RSR from Mechatronics Fan Group

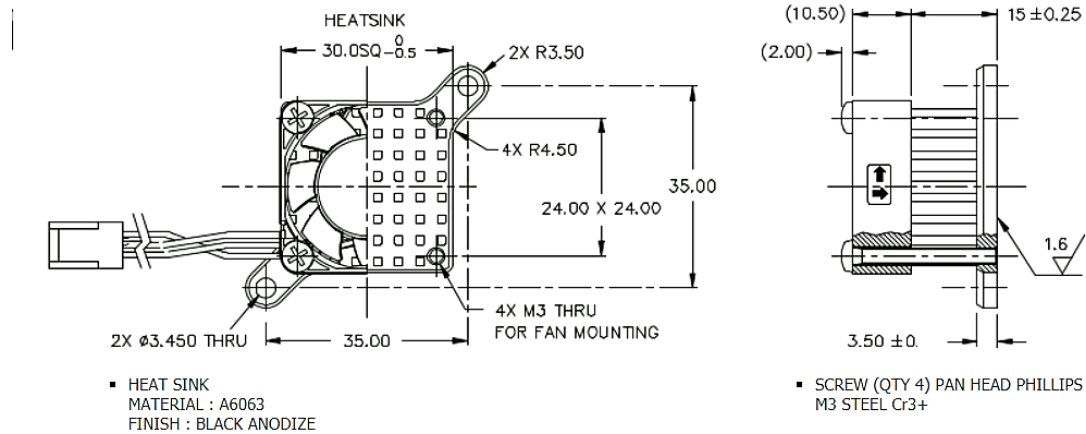


Figure 34: Mechanical dimension of Miniature Heat Sink

3.2.3 RoHS Compliance

iWave's i.MX 8 Pico ITX SBC is designed by using RoHS compliant components and manufactured on lead free production process.

3.2.4 Electrostatic Discharge

iWave's i.MX 8 Pico ITX SBC is sensitive to electro static discharge and so high voltages caused by static electricity could damage some of the devices on board. It is packed with necessary protection while shipping. Do not open or use the the i.MX 8 QM/QP Pico ITX SBC except at an electrostatic free workstation.

3.3 Mechanical Characteristics

3.3.1 i.MX 8 Pico ITX SBC Mechanical Dimensions

i.MX 8 Pico ITX SBC PCB size is 100mm x 72mm x 1.2mm. Pico ITX SBC mechanical dimension is shown below. (All dimensions are shown in mm)

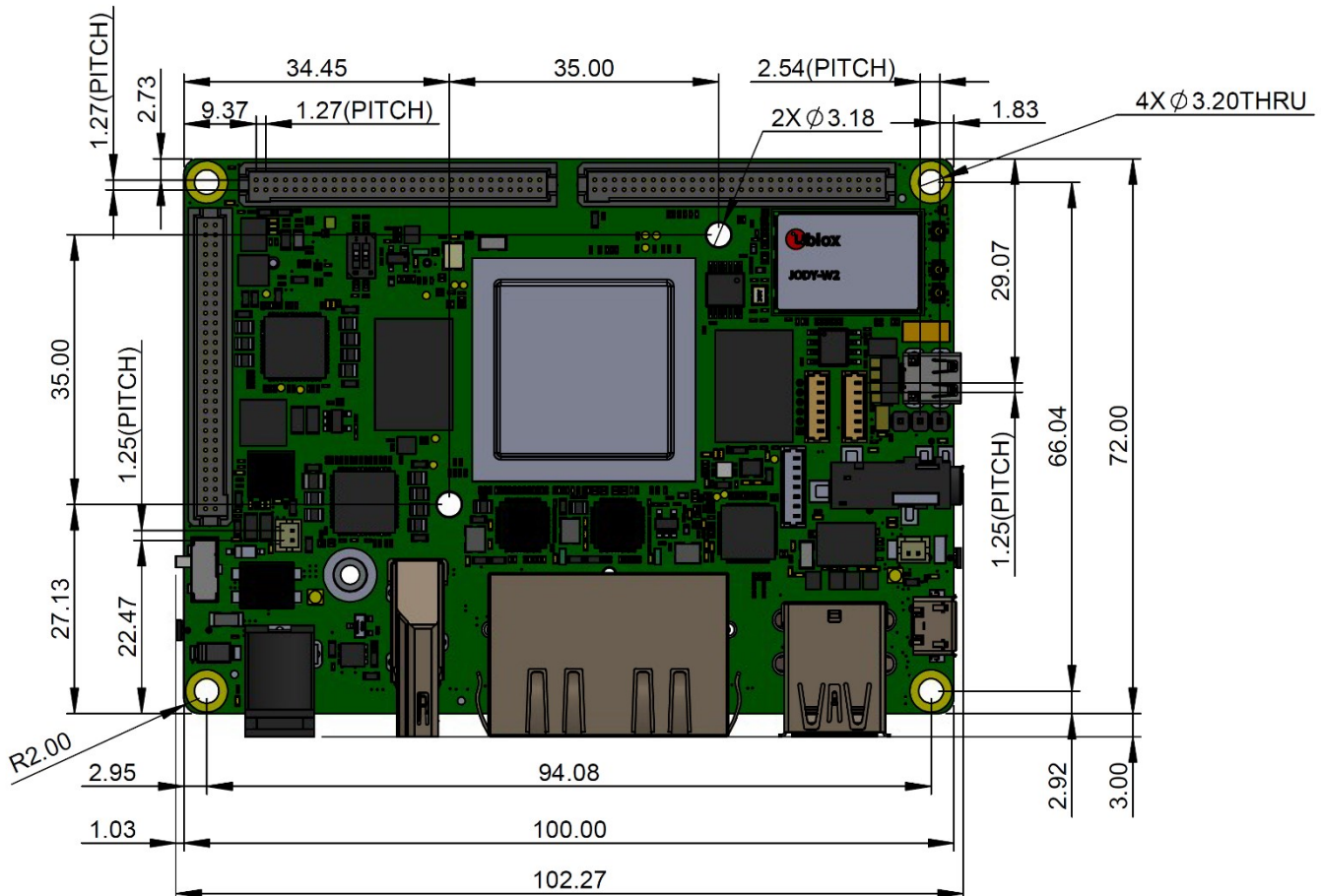


Figure 35: Mechanical dimensions of i.MX 8 Pico ITX SBC Top View

The i.MX 8 Pico ITX SBC PCB thickness is 1.2mm±0.15mm, top side maximum height component is 16.40mm (HDMI Connector), followed by Dual Ethernet Connector (16.40mm). In bottom side maximum height component is JTAG connector (5.91mm) followed by M.2 SMT spacer (3.99mm). Please refer the following figure s which gives the mechanical details of the i.MX 8 QM/QP Pico ITX SBC.

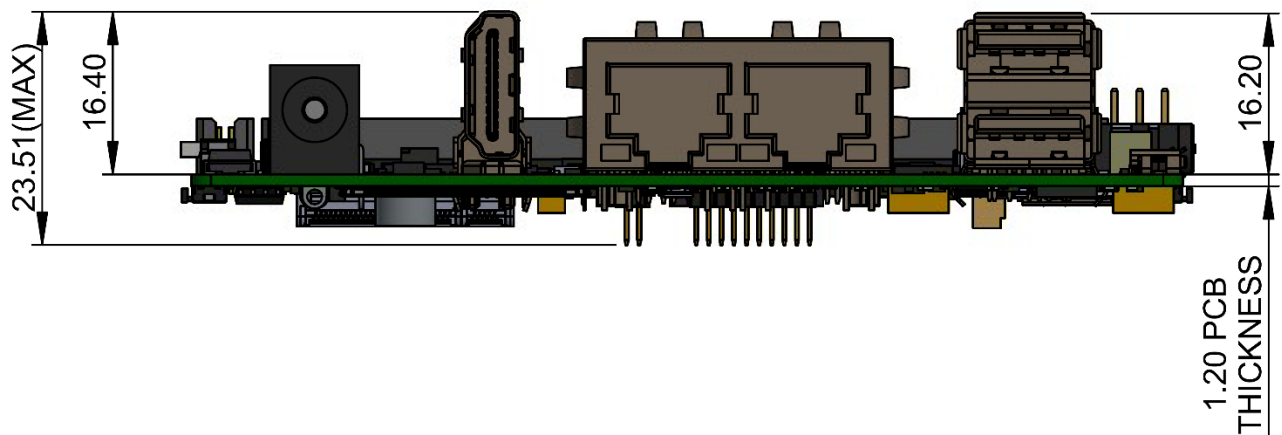


Figure 36: Mechanical dimensions of the i.MX 8 QM/QP Pico ITX SBC - Side View-1

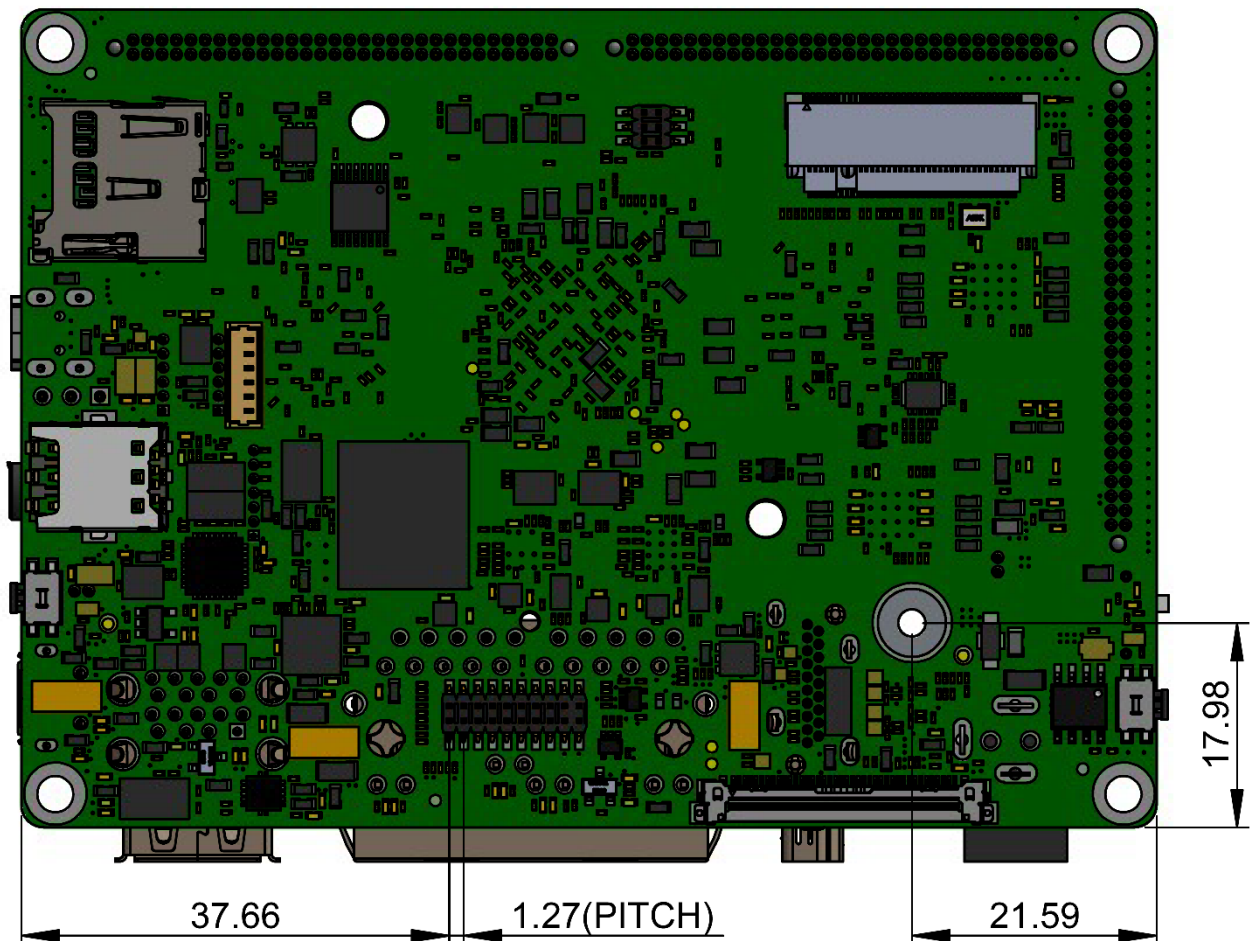


Figure 37: Mechanical dimensions of the i.MX 8 QM/QP Pico ITX SBC - Bottom View

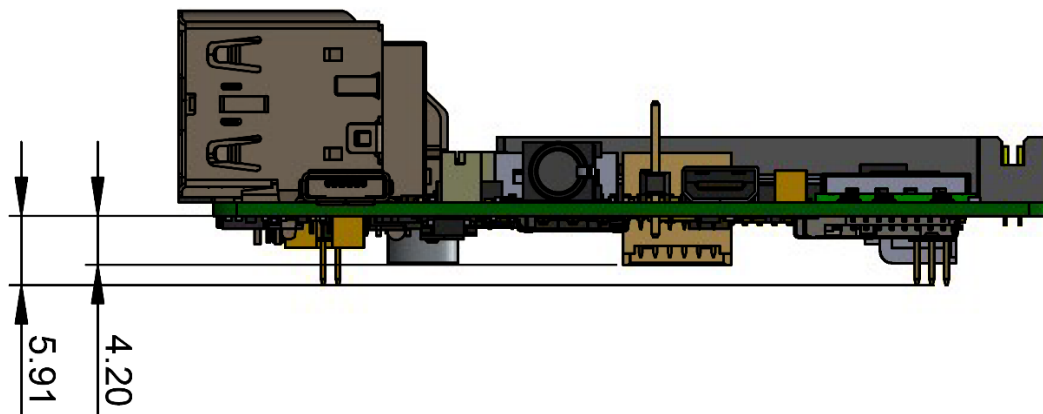


Figure 38: Mechanical dimensions of the i.MX 8 QM/QP Pico ITX SBC - Side View-2

3.3.2 i.MX 8 Pico ITX SBC Enclosure

iWave Systems offers fast, light, rugged, and flexible enclosure solution for Single Board Computers and System Designs. i.MX 8 QM/QP Pico ITX SBC along with solid, reliable, easy-to-use enclosure system enable ready to deploy for Various applications.

i.MX 8 QM/QP Pico ITX SBC Enclosure Systems features smooth outer walls, integrated pre-tapped mounting screw holes, counter-sunk panel mounting holes, and flush-mount hardware to provide a clean, finished unit with simplified assembly effort and maximum interior space.

i.MX 8 QM/QP Pico ITX SBC Sheet Metal Enclosure

- 2 Part Enclosure system along with Embedded Heatsink
- Allows easy access to Power Connector, HDMI, Ethernet, USB and Other IO ports
- Dimensions: 106.53 x 81.50 x 34.71mm
- Aluminium Sheet metal with Powder Coated finish
- Engraved Connector Symbols for Easy Identification
- Body Colour: Grey

i.MX 8 QM/QP Pico ITX SBC Machined Enclosure

- 2 Part Enclosure system, Top Part acts as Heatsink for CPU and PMIC.
- Captive Screws for Easy Assembly.
- Dimensions: 106 x 78 x 31.88mm
- Aluminium Alloy with Blue Anodized finish
- Fan-less Thermal Design
- Body Colour: Blue

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Note: Contact iWave Team for Customized Enclosure solutions for i.MX 8 QM/QP Pico ITX SBC to meet your application needs.

Please refer the below figure which gives the details of the i.MX 8 QM/QP Pico ITX SBC Sheet Metal Enclosure.

iW-RainboW-G27S

i.MX8 Quad MAX/Quad Plus Pico ITX SBC SHEET METAL ENCLOSURE
ORDERING PART NO: IW-EN-ALU-SM01

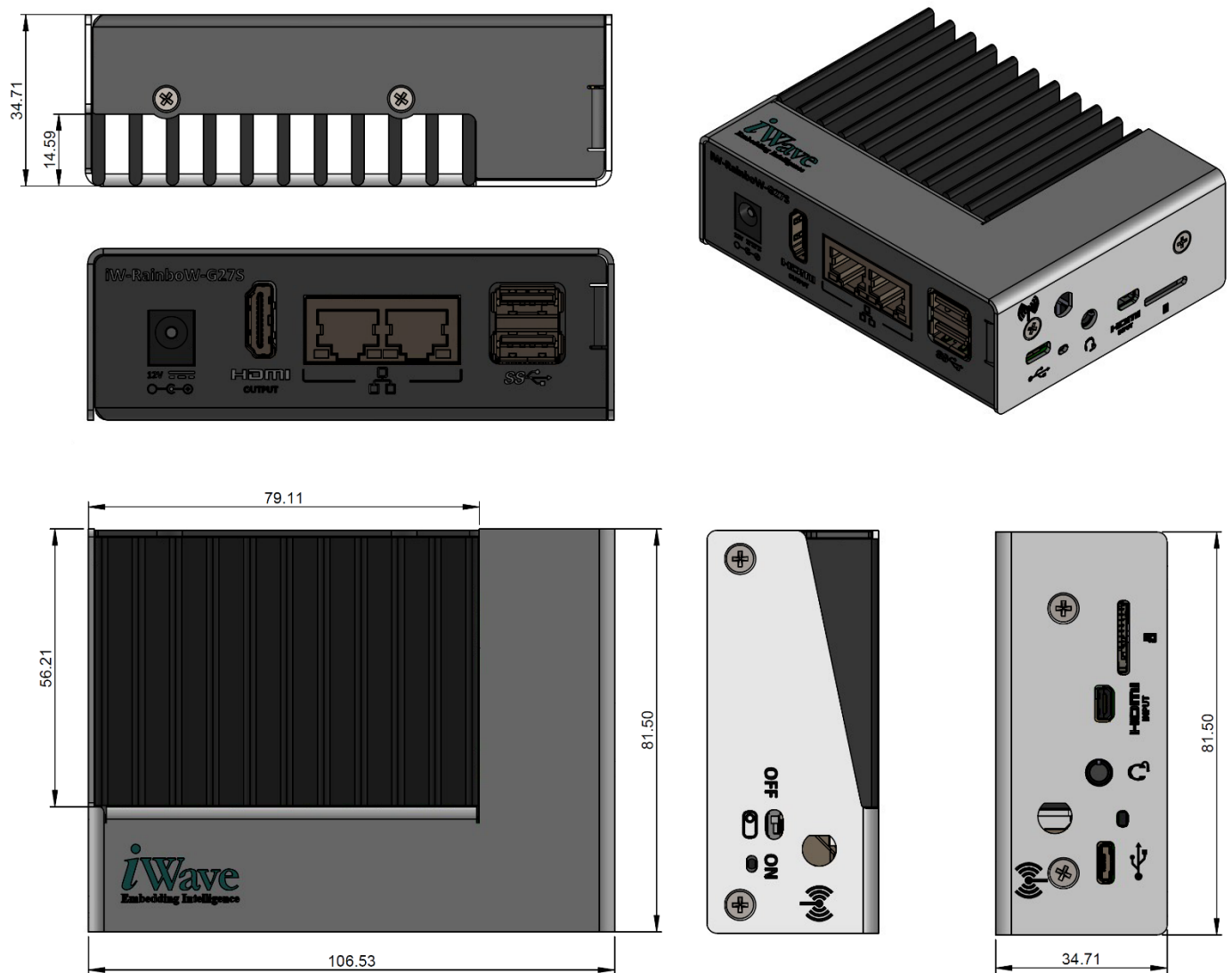


Figure 39: Mechanical dimensions of the i.MX 8 QM/QP Pico ITX SBC – Sheet metal Enclosure

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Please refer the below figure which gives the details of the i.MX 8 QM/QP Pico ITX SBC Machined Enclosure.

iW-RainboW-G27S

i.MX8 Quad MAX/Quad Plus Pico ITX SBC MACHINED ENCLOSURE

ORDERING PART NO: iW-EN-ALU-CN01

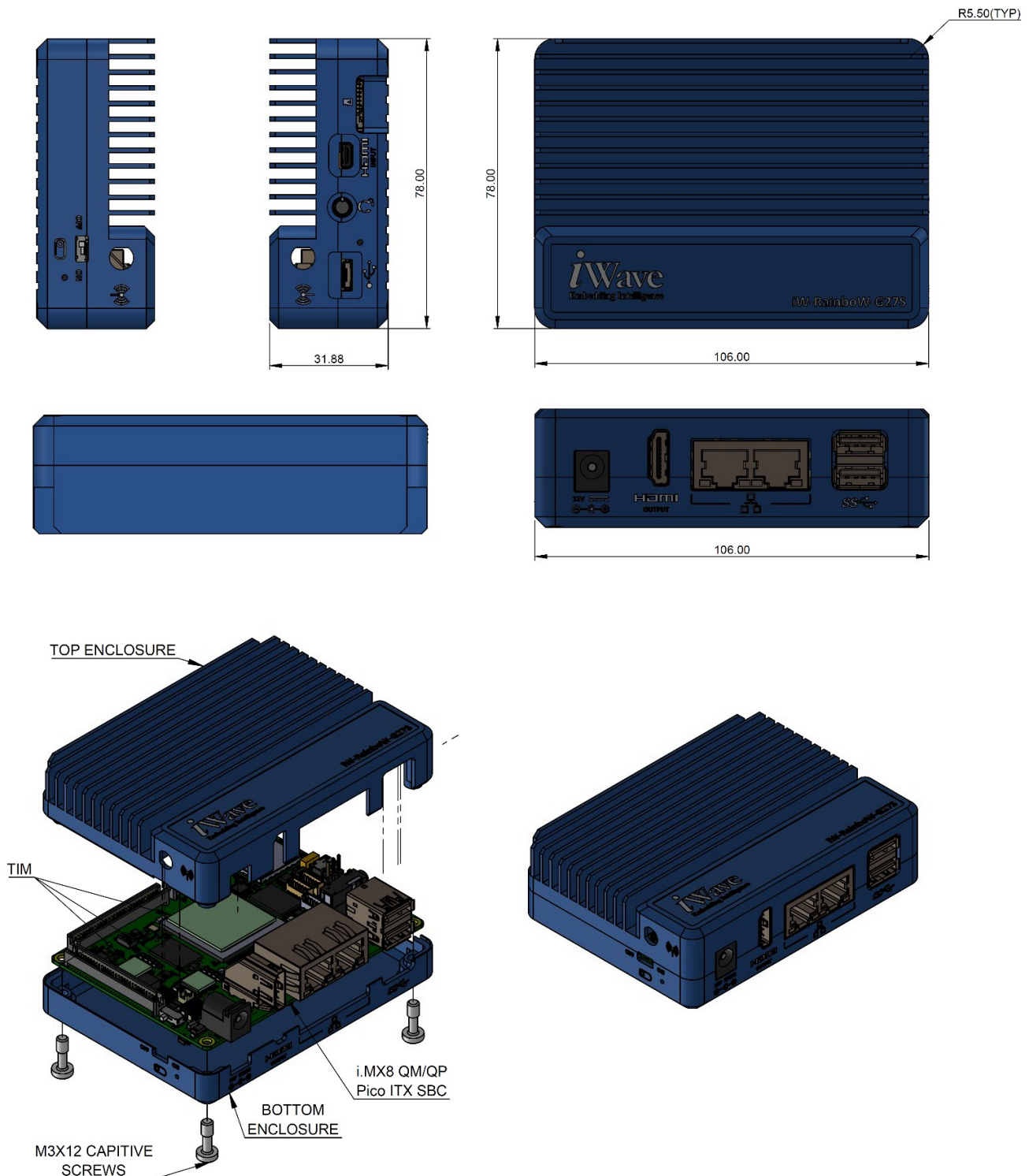


Figure 40: Mechanical dimensions of the i.MX 8 QM/QP Pico ITX SBC –Machined Enclosure

4. ORDERING INFORMATION

The below table provides the standard orderable part numbers for different i.MX8 Pico ITX SBC variations. If the desired part number with higher RAM memory size or Flash memory size is not listed in below table or if any custom configuration part number is required, please contact iWave

Table 25: Orderable Product Part Numbers

Product Part Number	Description	Temperature
iW-Rainbow G27S - i.MX 8 Quad Max Pico ITX SBC (Industrial grade)		
iW-G27S-SCQM-4L002G-E008G-BIC	i.MX 8 Quad Max, 2GB LPDDR4, 8GB eMMC With Wi-Fi, BT - Boot Code	-40°C to 85°C
iW-G27S-SCQM-4L002G-E008G-BID	i.MX 8 Quad Max, 2GB LPDDR4, 8GB eMMC Without Wi-Fi, BT - Boot Code	-40°C to 85°C
iW-G27S-SCQM-4L004G-E016G-BIC	i.MX 8 Quad Max, 4GB LPDDR4, 16GB eMMC With Wi-Fi, BT - Boot Code	-40°C to 85°C
iW-G27S-SCQM-4L004G-E016G-BID	i.MX 8 Quad Max, 4GB LPDDR4, 16GB eMMC Without Wi-Fi, BT - Boot Code	-40°C to 85°C
iW-G27S-SCQM-4L008G-E032G-BIC	i.MX 8 Quad Max, 8GB LPDDR4, 32GB eMMC With Wi-Fi, BT - Boot Code	-40°C to 85°C
iW-G27S-SCQM-4L008G-E032G-BID	i.MX 8 Quad Max, 8GB LPDDR4, 32GB eMMC Without Wi-Fi, BT - Boot Code	-40°C to 85°C
iW-Rainbow G27S - i.MX 8 Quad Plus Pico ITX SBC (Industrial grade)		
iW-G27S-SCQP-4L002G-E008G-BIC	i.MX 8 Quad Plus, 2GB LPDDR4, 8GB eMMC With Wi-Fi, BT - Boot Code	-40°C to 85°C
iW-G27S-SCQP-4L002G-E008G-BID	i.MX 8 Quad Plus, 2GB LPDDR4, 8GB eMMC Without Wi-Fi, BT - Boot Code	-40°C to 85°C
iW-G27S-SCQP-4L004G-E016G-BIC	i.MX 8 Quad Plus, 4GB LPDDR4, 16GB eMMC With Wi-Fi, BT - Boot Code	-40°C to 85°C
iW-G27S-SCQP-4L004G-E016G-BID	i.MX 8 Quad Plus, 4GB LPDDR4, 16GB eMMC Without Wi-Fi, BT - Boot Code	-40°C to 85°C
iW-G27S-SCQP-4L008G-E032G-BIC	i.MX 8 Quad Plus, 8GB LPDDR4, 32GB eMMC With Wi-Fi, BT - Boot Code	-40°C to 85°C
iW-G27S-SCQP-4L008G-E032G-BID	i.MX 8 Quad Plus, 8GB LPDDR4, 32GB eMMC Without Wi-Fi, BT - Boot Code	-40°C to 85°C

The below table provides the standard orderable Accessories part numbers, please contact iWave for further information.

Table 26: Orderable Product Accessories Part Numbers

Product Part Number	Description	Remarks
iW-HSKALU-BLABLC-SB02	i.MX 8 QM/QP Pico ITX SBC Full Heat Sink	
iW-FSKALU-BLABLC-SB02	i.MX 8 QM/QP Pico ITX SBC Full Fan Sink	
iW-EN-ALU-SM01	i.MX 8 QM/QP Pico ITX SBC Sheet Metal Enclosure	
iW-EN-ALU-CN01	i.MX 8 QM/QP Pico ITX SBC Machined Enclosure	
iW-MEPS12V2A_00	External AC-DC Power Adaptor (12V, 2A)	
iW-ALHSK_MEFAN_00	External Heat sink & Fan	

