

iW-RainboW-G21D

RZ/G1H Qseven Development Platform Hardware User Guide



Document Revision History

Document Number		iW-PREJD-UM-01-R2.0-REL1.1-Hardware-RZG1H_DevKit
Revision	Date	Change Description
1.0	30 th Dec 2016	Official Release Version
1.1	25 th May 2019	Changes throughout the document w.r.t Production Version SOM

PROPRIETARY NOTICE: This document contains proprietary material for the sole use of the intended recipient(s). Do not read this document if you are not the intended recipient. Any review, use, distribution or disclosure by others is strictly prohibited. If you are not the intended recipient (or authorized to receive for the recipient), you are hereby notified that any disclosure, copying distribution or use of any of the information contained within this document is STRICTLY PROHIBITED. Thank you. "iWave Systems Tech. Pvt. Ltd."

Disclaimer

iWave Systems reserves the right to change details in this publication including but not limited to any Product specification without notice.

No warranty of accuracy is given concerning the contents of the information contained in this publication. To the extent permitted by law no liability (including liability to any person by reason of negligence) will be accepted by iWave Systems, its subsidiaries or employees for any direct or indirect loss or damage caused by omissions from or inaccuracies in this document.

CPU and other major components used in this product may have several silicon errata associated with it. Under no circumstances, iWave Systems shall be liable for the silicon errata and associated issues.

Trademarks

All registered trademarks, product names mentioned in this publication are the property of their respective owners and used for identification purposes only.

Certification

iWave Systems Technologies Pvt. Ltd. is an ISO 9001:2015 Certified Company.



Warranty & RMA

Warranty support for Hardware: 1 Year from iWave or iWave's EMS partner.

For warranty terms, go through the below web link,

<http://www.iwavesystems.com/support/warranty.html>

For Return Merchandise Authorization (RMA), go through the below web link,

<http://www.iwavesystems.com/support/rma.html>

Technical Support

iWave Systems technical support team is committed to provide the best possible support for our customers so that our Hardware and Software can be easily migrated and used.

For assistance, contact our Technical Support team at,

Email : support.ip@iwavesystems.com

Website : www.iwavesystems.com

Address : iWave Systems Technologies Pvt. Ltd.
7/B, 29th Main, BTM Layout 2nd Stage,
Bangalore, Karnataka,
India – 560076

Table of Contents

1. INTRODUCTION.....	8
1.1 PURPOSE	8
1.2 OVERVIEW	8
1.3 LIST OF ACRONYMS.....	8
1.4 TERMINOLOGY DESCRIPTION	10
1.5 REFERENCES.....	10
2. ARCHITECTURE AND DESIGN – QSEVEN CARRIER BOARD.....	11
2.1 RZ/G1H QSEVEN CARRIER BOARD BLOCK DIAGRAM.....	11
2.2 RZ/G1H QSEVEN CARRIER BOARD FEATURES.....	12
2.3 QSEVEN MXM CONNECTOR	14
2.4 ON BOARD SWITCHES	33
2.4.1 Power ON/OFF Switch	33
2.4.2 Board Configuration Switch	34
2.4.3 Reset Switch	35
2.5 SERIAL INTERFACE FEATURES	36
2.5.1 Debug UART Port	36
2.5.2 Data UART Header	37
2.6 HIGH SPEED INTERFACE FEATURES.....	38
2.6.1 USB3.0 Port0 (Host).....	38
2.6.2 PCIe Channel0 Port.....	39
2.6.3 SATA Channel0 Port (Optional)	45
2.7 COMMUNICATION INTERFACE FEATURES.....	47
2.7.1 Gigabit Ethernet Port	47
2.7.2 USB2.0 Ports (Host).....	49
2.7.3 USB2.0 Port1 (OTG).....	51
2.7.4 SDIO Port.....	53
2.7.5 CAN Header.....	55
2.8 AUDIO/VIDEO FEATURES	56
2.8.1 Audio IN & OUT.....	56
2.8.2 7" LCD with Capacitive Touch.....	58
2.8.3 HDMI Port (Optional)	61
2.8.4 LVDS Port with Resistive Touch	63
2.9 ADDITIONAL FEATURES.....	67
2.9.1 SPI Flash	67
2.9.2 RTC Coin Cell Holder	67
2.9.3 Fan Header.....	68
2.9.4 JTAG Header (Optional).....	69
2.10 SOM EXPANSION CONNECTORS.....	71
2.11 CARRIER BOARD EXPANSION CONNECTORS	72
3. ARCHITECTURE AND DESIGN – CAMERA ADD-ON MODULE	79
3.1 RZ/G1H CAMERA ADD-ON MODULE BLOCK DIAGRAM	79
3.2 RZ/G1H CAMERA ADD-ON MODULE FEATURES.....	80
3.3 VIDEO FEATURES.....	81
3.3.1 Camera Selection Switch	81
3.3.2 8bit CMOS Cameras	82

3.3.3	16bit CMOS Cameras	87
3.4	COMMUNICATION FEATURES	92
3.4.1	CAN Header	92
3.4.2	10/100Mbps Ethernet Header	93
3.5	SERIAL INTERFACE FEATURES	94
3.5.1	Data UART Headers (RS232)	94
4.	TECHNICAL SPECIFICATION.....	96
4.1	ELECTRICAL CHARACTERISTICS.....	96
4.1.1	Power Input Requirement	96
4.1.2	Power Output Specification.....	97
4.2	ENVIRONMENTAL CHARACTERISTICS.....	98
4.2.1	Environmental Specification.....	98
4.2.2	RoHS Compliance	98
4.2.3	Electrostatic Discharge.....	98
4.3	MECHANICAL CHARACTERISTICS	99
4.3.1	RZ/G1H Qseven Carrier Board Mechanical Dimensions	99
4.3.2	RZ/G1H Camera Add-On Module Mechanical Dimensions	100
4.3.3	Guidelines to insert the Qseven SOM into Carrier Board	100
5.	ORDERING INFORMATION	101
6.	APPENDIX	102
6.1	CAMERA ADD-ON MODULE INTEGRATION PROCEDURE	102
6.2	8BIT CMOS CAMERAS CONNECTING PROCEDURE	106

List of Figures

FIGURE 1: RZ/G1H QSEVEN CARRIER BOARD BLOCK DIAGRAM	11
FIGURE 2: QSEVEN MXM CONNECTOR	14
FIGURE 3: POWER ON/OFF SWITCH	33
FIGURE 4: BOARD CONFIGURATION SWITCH	34
FIGURE 5: RESET SWITCH	35
FIGURE 6: DEBUG UART	36
FIGURE 7: DATA UART HEADER.....	37
FIGURE 8: USB3.0 HOST PORT0.....	38
FIGURE 9: PCIex4 CONNECTOR.....	40
FIGURE 10: MINI PCIE CONNECTOR.....	42
FIGURE 11: SATA CONNECTOR.....	45
FIGURE 12: RJ45 MAGJACK	47
FIGURE 13: USB2.0 PORT0 (HOST)	49
FIGURE 14: USB2.0 PORT3 (HOST)	50
FIGURE 15: USB2.0 PORT1 (OTG).....	52
FIGURE 16: SD/MMC CONNECTOR	53
FIGURE 17: CAN HEADER	55
FIGURE 18: AUDIO IN/OUT JACK.....	56
FIGURE 19: RGB LCD CONNECTOR	58
FIGURE 20: RGB LCD TOUCH CONNECTOR	60
FIGURE 21: HDMI CONNECTOR.....	61
FIGURE 22: LVDS LCD CONNECTOR	63
FIGURE 23: LVDS BACKLIGHT CONNECTOR	65
FIGURE 24: LVDS RESISTIVE TOUCH CONNECTOR.....	66
FIGURE 25: COIN CELL HOLDER.....	67
FIGURE 26: FAN HEADER	68
FIGURE 27: JTAG HEADER.....	69
FIGURE 28: SOM EXPANSION CONNECTORS.....	71
FIGURE 29: CARRIER BOARD EXPANSION CONNECTORS	72
FIGURE 30: RZ/G1H CAMERA ADD-ON MODULE BLOCK DIAGRAM	79
FIGURE 31: CAMERA ADD-ON MODULE EXPANSION CONNECTORS.....	80
FIGURE 32 CAMERA SELECTION SWITCH	81
FIGURE 33 8BIT CMOS CAMERA HEADER.....	82
FIGURE 34 16BIT CMOS CAMERA HEADER.....	87
FIGURE 35: CAN HEADER	92
FIGURE 36 10/100 ETHERNET HEADER.....	93
FIGURE 37: DATA UART 0 HEADER.....	94
FIGURE 38: POWER JACK	96
FIGURE 39: RZ/G1H QSEVEN CARRIER BOARD MECHANICAL DIMENSION – TOP VIEW	99
FIGURE 40: RZ/G1H QSEVEN CARRIER BOARD MECHANICAL DIMENSION - SIDE VIEW.....	99
FIGURE 41: RZ/G1H CAMERA ADD-ON MODULE MECHANICAL DIMENSION – BOTTOM VIEW	100
FIGURE 42: QSEVEN SOM INSERTION PROCEDURE	100
FIGURE 43: INSERT PAN HEAD SCREW	103
FIGURE 44: TIGHTEN METALLIC HEX SPACER	103
FIGURE 45: INSERT CAMERA ADD-ON MODULE	104
FIGURE 46: INSERT NON-METALLIC FLAT WASHER	104
FIGURE 47: TIGHTEN THE NUT	105
FIGURE 48: CAMERA CONNECTION	106

FIGURE 49: CAMERA LENS CAP	106
----------------------------------	-----

List of Tables

TABLE 1: ACRONYMS & ABBREVIATIONS	8
TABLE 2: TERMINOLOGY	10
TABLE 3: QSEVEN MXM CONNECTOR PIN OUT	15
TABLE 4: BOARD CONFIGURATION SWITCH	35
TABLE 5: DATA UART HEADER PIN OUT	37
TABLE 6: DUAL STACK USB 3.0 CONNECTOR PIN OUT (BOTTOM PORT)	39
TABLE 7: PCIEX4 CONNECTOR PIN OUT	40
TABLE 8: MINI-PCIE CONNECTOR PIN OUT	43
TABLE 9: SATA CONNECTOR PIN OUT	46
TABLE 10: RJ45 MAGJACK PIN OUT	48
TABLE 11: USB2.0 PORT0 (HOST) CONNECTOR PIN OUT	50
TABLE 12: DUAL STACK USB 3.0 CONNECTOR PIN OUT (TOP PORT)	50
TABLE 13: USB2.0 PORT1 (OTG) CONNECTOR PIN OUT	52
TABLE 14: SD/MMC CONNECTOR PIN OUT	54
TABLE 15: CAN HEADER PIN OUT	55
TABLE 16: AUDIO OUT JACK PIN OUT	57
TABLE 17: AUDIO IN JACK PIN OUT	57
TABLE 18: 7" RGB LCD CONNECTOR PIN OUT	59
TABLE 19: CAPACITIVE TOUCH CONNECTOR PIN OUT	60
TABLE 20: HDMI CONNECTOR PIN OUT	62
TABLE 21: LVDS CONNECTOR	64
TABLE 22: LVDS BACKLIGHT CONNECTOR PIN OUT	65
TABLE 23: RESISTIVE TOUCH CONNECTOR PIN OUT	66
TABLE 24: FAN HEADER PIN OUT	68
TABLE 25: JTAG HEADER PIN OUT	70
TABLE 26: EXPANSION CONNECTOR3 PIN OUT	73
TABLE 27: CAMERA SELECTION SWITCH	81
TABLE 28: 8BIT CAMERA CONNECTOR1 PIN OUT (J13)	83
TABLE 29: 8BIT CAMERA CONNECTOR2 PIN OUT (J14)	84
TABLE 30: 8BIT CAMERA CONNECTOR3 PIN OUT (J12)	85
TABLE 31: 8BIT CAMERA CONNECTOR4 PIN OUT (J11)	86
TABLE 32: 16BIT CAMERA CONNECTOR PIN OUT (J1)	88
TABLE 33: 16BIT CAMERA CONNECTOR2 PIN OUT (J15)	90
TABLE 34: CAN0 HEADER PIN OUT	92
TABLE 35: 10/100 ETHERNET HEADER PIN OUT	93
TABLE 36: SCIF0 UART HEADER PIN OUT (J9)	94
TABLE 37: SCIF1 UART HEADER PIN OUT (J6)	95
TABLE 38: SCIF2 UART HEADER PIN OUT (J8)	95
TABLE 39: SCIFB1 UART HEADER PIN OUT (J3)	95
TABLE 40: HSCIF0 UART HEADER PIN OUT (J2)	95
TABLE 41: POWER JACK PIN OUT	96
TABLE 42: POWER INPUT REQUIREMENT	97
TABLE 43: POWER OUTPUT SPECIFICATION	97
TABLE 44: ENVIRONMENTAL SPECIFICATION	98
TABLE 45: ORDERABLE PRODUCT PART NUMBERS	101
TABLE 46: CAMERA ADD-ON MODULE ACCESSORIES	102

1. INTRODUCTION

1.1 Purpose

The RZ/G1H Qseven Development platform incorporates RZ/G1H CPU based Qseven SOM and Qseven Carrier board for complete validation of RZ/G1H CPU functionality. This document is the Hardware User Guide for the RZ/G1H Qseven Carrier Board. This Guide provides detailed information on the overall design and usage of the Qseven Carrier Board from a Hardware Systems perspective. Complete information about the RZ/G1H Qseven SOM hardware is explained in another document named “iW-RainboW-G21M-RZG1H_QsevenSOM-HardwareUserGuide-RELx.y”.

1.2 Overview

iWave's RZ/G1H Qseven Development platform incorporates RZ/G1H Qseven SOM which is based on Renesas's high performance RZ/G1H Quad ARM Cortex A15 + Quad ARM Cortex A7 processor and the Qseven carrier board with 7" Capacitive Touch LCD. The development board can be used for quick prototyping of various applications targeted by the RZ/G1H processor. With the 120mmx120mm Nano ITX size, Qseven carrier board is highly packed with all the necessary on-board connectors to validate the Qseven features of RZ/G1H Qseven SOM. iWave also supports Camera Add-On Module for RZ/G1H Qseven Development platform to validate Expansion connector interfaces of RZ/G1H Qseven SOM.

1.3 List of Acronyms

The following acronyms will be used throughout this document.

Table 1: Acronyms & Abbreviations

Acronyms	Abbreviations
ARM	Advanced RISC Machine
BPP	Bits Per Pixel
CAN	Controller Area Network
CMOS	Complementary Metal-Oxide Semiconductor
CPU	Central Processing Unit
GPIO	General Purpose Input Output
HSCIF	High Speed Serial Communication Interface with FIFO
I2C	Inter-Integrated Circuit
IC	Integrated Circuit
JTAG	Joint Test Action Group
LCD	Liquid Crystal Display
Mbps	Megabits per sec
MHz	Mega Hertz
MSIOF	Clock-Synchronized Serial Interface with FIFO

Acronyms	Abbreviations
NC	No Connect
NPTH	Non Plated Through hole
PCB	Printed Circuit Board
PCIe	Peripheral Component Interconnect Express
PTH	Plated Through hole
PWM	Pulse Width Modulation
RTC	Real Time Clock
SATA	Serial AT Attachment
SCIF	Serial Communication Interface with FIFO
SDIO	Secure Digital Input Output
SDHI	SD Card Host Interface
SSI	Serial Sound Interface
SOM	System On Module
UART	Universal Asynchronous Receiver/Transmitter
USB	Universal Serial Bus
USB OTG	USB On The Go

1.4 Terminology Description

In this document, wherever Signal Type is mentioned, below terminology is used.

Table 2: Terminology

Terminology	Description
I	Input Signal
O	Output Signal
IO	Bidirectional Input/output Signal
CMOS	Complementary Metal Oxide Semiconductor Signal
DIFF	Differential Signal
TMDS	Transition-Minimized Differential Signalling
OD	Open Drain Signal
OC	Open Collector Signal
Analog	Analog Signal
Power	Power Pin
PU	Pull Up
PD	Pull Down
NA	Not Applicable
NC	Not Connected

Note: Signal Type does not include internal pull-ups or pull-downs implemented by the chip vendors and only includes the pull-ups or pull-downs implemented on board.

1.5 References

- RZ/G1H Qseven SOM Hardware User Guide
- Renesas' RZ/G1H CPU Hardware User Manual
- Qseven® Specification Version 2.0
- Qseven® Design Guide

2. ARCHITECTURE AND DESIGN – QSEVEN CARRIER BOARD

This section provides detailed information about the RZ/G1H Qseven Development Platform carrier board features with high level block diagram and detailed information about each block.

2.1 RZ/G1H Qseven Carrier Board Block Diagram

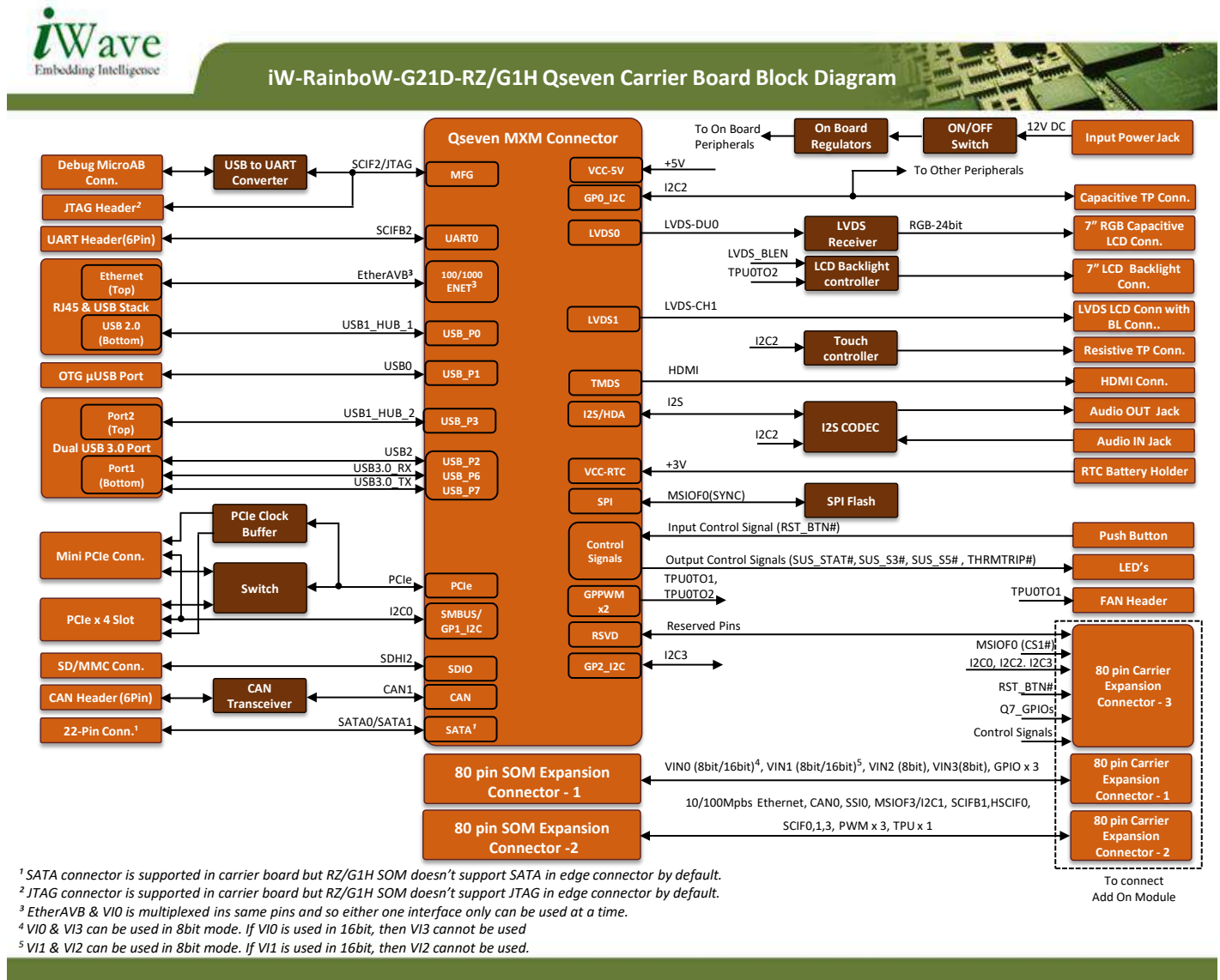


Figure 1: RZ/G1H Qseven Carrier Board Block Diagram

2.2 RZ/G1H Qseven Carrier Board Features

The RZ/G1H Qseven carrier board supports the following features to validate RZ/G1H Qseven SOM Edge connector Interfaces.

On Board Switches

- Power ON/OFF Switch
- Board Configuration Switch
- Reset Switch

Serial Interface Features

- Debug UART through USB Micro AB Connector
- Data UART (SCIFB2) x 1 Port through Header

High Speed Interface Features

- USB 3.0/USB 2.0 Host x 1 Port through Dual stack USB 3.0 Type A Connector (Bottom)
- PCIe x 1 Port through x4 connector or Mini-PCIe connector
- SATA x 1 Port through 22pin Serial ATA Connector (Optional)¹

Communication Features

- 100/1000Mbps Ethernet through RJ45MagJack
- USB 2.0 Host x 1 Port through Type A Connector (Dual stack USB 3.0 - Top)
- USB 2.0 Host x 1 Port through Type A Connector
- USB 2.0 OTG x 1 Port through Micro AB Connector
- SDHI (4bit) x 1 Port through Standard SD Connector
- CAN x 1 Port through Header

Audio/Video Features

- I2S Audio Codec with 3.5mm Audio IN and OUT jack
- 7" RGB LCD Connector through LVDS to RGB transmitter with Capacitive Touch
- 2nd LVDS port display connector

Additional Features

- SPI Flash (MSIOF0 with SS#0)
- RTC Coin Cell holder
- Fan Header
- 20-Pin JTAG Header (Optional)²

Carrier board Expansion Connectors

- Carrier board Expansion Connector1³
- Carrier board Expansion Connector2⁴
- Carrier board Expansion Connector3
 - SPI (MSIOF0 with SS1#) x 1 Port
 - I2C x 3 Ports
 - GPIOs & Power

General Specification

- Power Supply : 12V, 2A Power Input Jack
- Form Factor : 120mm X 120mm Nano ITX

¹ SATA connector is supported always in Qseven carrier board hardware. If Qseven SOM supports SATA interface on Qseven Edge connector, then SATA can be tested in Qseven carrier board. In RZ/G1H CPU based Qseven SOM, SATA is not supported in Qseven Edge connector by default.

² JTAG connector is supported always in Qseven carrier board hardware. If Qseven SOM supports JTAG interface on Qseven Edge connector, then JTAG can be tested in Qseven carrier board. In RZ/G1H CPU based Qseven SOM, JTAG is not supported in Qseven Edge connector by default.

³ The RZ/G1H Qseven SOM Expansion connector1 interfaces are one to one directly connected to Qseven carrier board expansion connector1 in Qseven carrier board. Please check the RZ/G1H SOM user guide for the detailed interface availability on this connector.

⁴ The RZ/G1H Qseven SOM Expansion connector2 interfaces are one to one directly connected to Qseven carrier board expansion connector2 in Qseven carrier board. Please check the RZ/G1H SOM user guide for the detailed interface availability on this connector.

2.3 Qseven MXM Connector

The RZ/G1H Qseven carrier board supports 230Pin Qseven MXM Edge mating connector for Qseven SOM attachment. This standard 230-pin robust connector is capable of handling high-speed serialized signals and can be used for size constrained embedded applications. This Qseven MXM Edge mating connector (J11) is physically located at the top of the board as shown below.

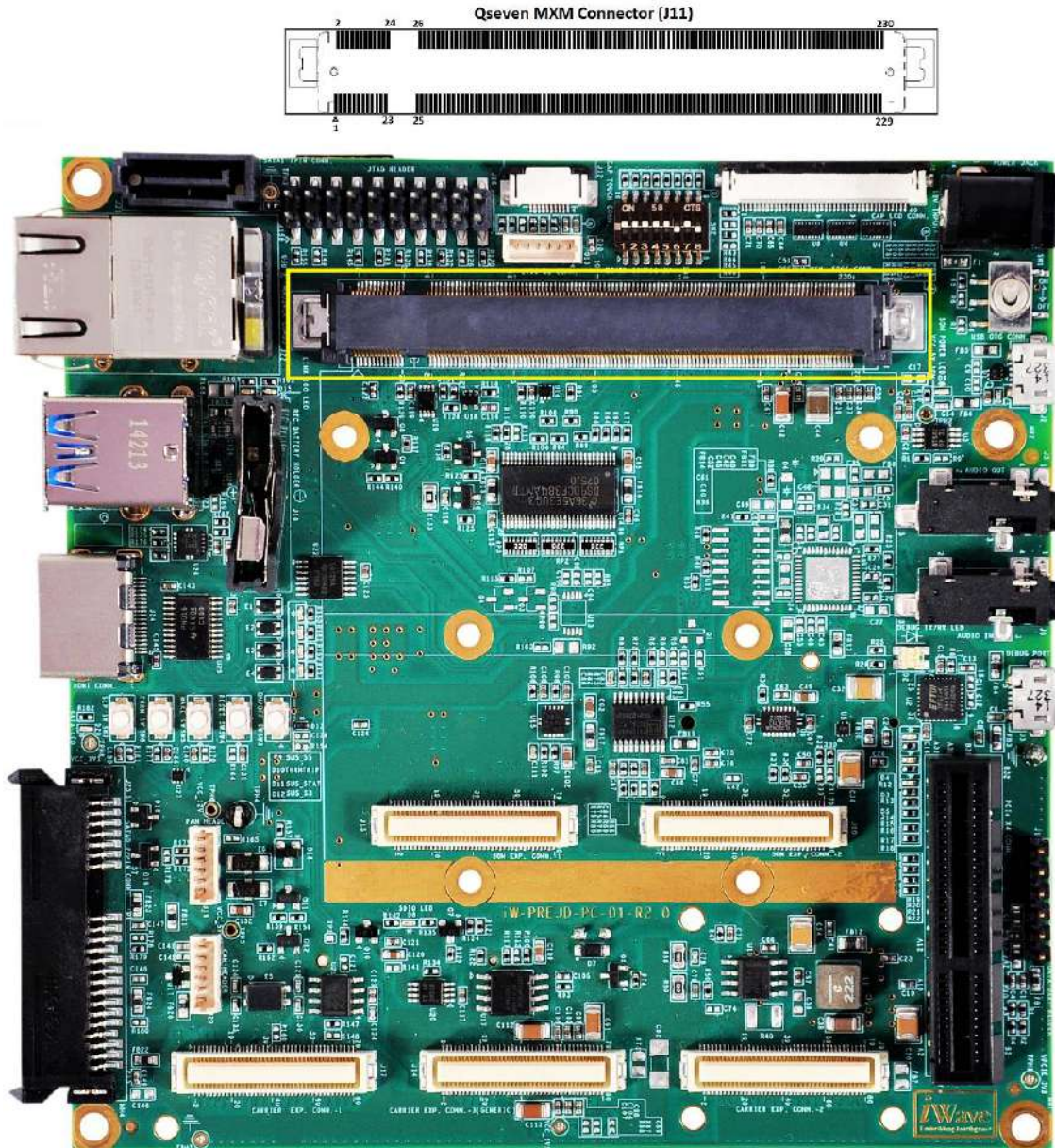


Figure 2: Qseven MXM Connector

Table 3: Qseven MXM Connector Pin Out

Pin No.	Qseven MXM Connector Pin Name	Signal Name	Signal Type/ Termination	Description
1	GND	GND	Power	Ground.
2	GND	GND	Power	Ground.
3	GBE_MDI3-	GPHY_DTXRXM	IO, DIFF	Gigabit Ethernet MDI differential pair 3 negative. This pin is connected to RJ45 Magjack J22.
4	GBE_MDI2-	GPHY_CTXRXM	IO, DIFF	Gigabit Ethernet MDI differential pair 2 negative. This pin is connected to RJ45 Magjack J22.
5	GBE_MDI3+	GPHY_DTXRXP	IO, DIFF	Gigabit Ethernet MDI differential pair 3 positive. This pin is connected to RJ45 Magjack J22.
6	GBE_MDI2+	GPHY_CTXRXP	IO, DIFF	Gigabit Ethernet MDI differential pair 2 positive. This pin is connected to RJ45 Magjack J22.
7	GBE_LINK100#	GPHY_LINK_LED2	-	100Mbps Ethernet link status LED. This pin is connected to D15 Green LED.
8	GBE_LINK1000#	GPHY_LINK_LED2	-	Gigabit Ethernet link status LED. This pin is connected to D16 Green LED.
9	GBE_MDI1-	GPHY_BTXXRM	IO, DIFF	Gigabit Ethernet MDI differential pair 1 negative. This pin is connected to RJ45 Magjack J22.
10	GBE_MDI0-	GPHY_ATXXRM	IO, DIFF	Gigabit Ethernet MDI differential pair 0 negative. This pin is connected to RJ45 Magjack J22.
11	GBE_MDI1+	GPHY_BTXXRP	IO, DIFF	Gigabit Ethernet MDI differential pair 1 positive. This pin is connected to RJ45 Magjack J22.
12	GBE_MDI0+	GPHY_ATXXRP	IO, DIFF	Gigabit Ethernet MDI differential pair 0 positive. This pin is connected to RJ45 Magjack J22.
13	GBE_LINK#	GPHY_LINK_LED2	-	Gigabit Ethernet link status LED. This pin is connected to RJ45 Magjack J22.
14	GBE_ACT#	GPHY_ACTIVITY_LED 1	-	Gigabit Ethernet Activity status LED. This pin is connected to RJ45 Magjack J22.
15	GBE_CTREF	NC	-	NC in RZ/G1H Qseven SOM. This pin is connected to RJ45 Magjack J22 centre tap pins through resistor and default populated in carrier board.

Pin No.	Qseven MXM Connector Pin Name	Signal Name	Signal Type/ Termination	Description
16	SUS_S5#	SUS_S5_Q7	I, 3.3V CMOS	S5 State. This pin is connected to indication LED D9. <i>Note: This pin is optionally connected to Expansion Connector3 (J14) 8th Pin.</i>
17	WAKE#	NC	-	NC in RZ/G1H Qseven SOM. This pin is connected to Push button (SW5) in carrier board. <i>Note: This pin is optionally connected to Expansion Connector3 (J14) 16th Pin.</i>
18	SUS_S3#	SUS_S3_Q7	I, 3.3V CMOS	S3 state. This pin is connected to indication LED D12. <i>Note: This pin is optionally connected to Expansion Connector3 (J14) 7th Pin.</i>
19	SUS_STAT#	SUS_STAT_Q7	I, 3.3V CMOS	Suspend Status. This pin is connected to indication LED D10. <i>Note: This pin is optionally connected to Expansion Connector3 (J14) 10th Pin.</i>
20	PWRBTN#	PWRBTN#	-	Power Button output. This pin is connected to Push button (SW3) in the carrier board used for SOM On/Off control. <i>Note: This pin is optionally connected to Expansion Connector3 (J14) 24th Pin.</i>
21	SLP_BTN#	NC	-	NC in RZ/G1H Qseven SOM. This pin is connected to Push button (SW7) in carrier board. <i>Note: This pin is optionally connected to Expansion Connector3 (J14) 22nd Pin.</i>
22	LID_BTN#	NC	-	NC in RZ/G1H Qseven SOM. This pin is connected from 8bit DIP switch (SW2) 3 rd position in carrier board. <i>Note: This pin is optionally connected to Expansion Connector3 (J14) 28th Pin.</i>
23	GND	GND	Power	Ground.
24	GND	GND	Power	Ground.
25	GND	GND	Power	Ground.
26	PWGIN	PWGIN	O, 5V CMOS/ 10K PU	Power Good Output.

RZ/G1H Qseven Development Platform Hardware User Guide

Pin No.	Qseven MXM Connector Pin Name	Signal Name	Signal Type/ Termination	Description
27	BATLOW#	NC	-	NC in RZ/G1H Qseven SOM. This pin is connected from 8bit DIP switch (SW2) 2 nd position in carrier board. <i>Note: This pin is optionally connected to Expansion Connector3 (J14) 30th Pin.</i>
28	RSTBTN#	RSTBN	O, 3.3V CMOS	Active low Reset button Output. This pin is connected to Push button SW4 in carrier board for reset generation. <i>Note: This pin is optionally connected to Expansion Connector3 (J14) 12th Pin.</i>
29	SATA0_TX+	NC	-	NC in RZ/G1H Qseven SOM. This pin is connected to 22pin SATA Connector (J25) for SATA Channel0 Transmit differential pair positive.
30	SATA1_TX+	NC	-	NC in RZ/G1H Qseven SOM. This pin connected to 7pin SATA Connector (J21) in carrier board.
31	SATA0_TX-	NC	-	NC in RZ/G1H Qseven SOM. This pin connected to 22pin SATA Connector (J25) for SATA Channel0 Transmit differential pair negative.
32	SATA1_TX-	NC	-	NC in RZ/G1H Qseven SOM. This pin connected to 7pin SATA Connector (J21) in carrier board.
33	SATA_ACT#	NC	-	NC in RZ/G1H Qseven SOM. This pin connected from 22pin SATA Connector (J25) for SATA Channel0 command Activity line.
34	GND	GND	Power	Ground.
35	SATA0_RX+	NC	-	NC in RZ/G1H Qseven SOM. This pin connected to 22pin SATA Connector (J25) for SATA Channel0 Receive differential pair positive.
36	SATA1_RX+	NC	-	NC in RZ/G1H Qseven SOM. This pin connected to 7pin SATA Connector (J21) in carrier board.
37	SATA0_RX-	NC	-	NC in RZ/G1H Qseven SOM. This pin connected to 22pin SATA Connector (J25) for SATA Channel0 Receive differential pair negative.

Pin No.	Qseven MXM Connector Pin Name	Signal Name	Signal Type/ Termination	Description
38	SATA1_RX-	NC	-	NC in RZ/G1H Qseven SOM. This pin connected to 7pin SATA Connector (J21) in carrier board.
39	GND	GND	Power	Ground.
40	GND	GND	Power	Ground.
41	BIOS_DISABLE#/ BOOT_ALT#	NC	-	NC in RZ/G1H Qseven SOM. This pin is connected from 8bit DIP switch (SW2) 1 st position in carrier board. <i>Note: This pin is optionally connected to Expansion Connector3 (J14) 32nd Pin.</i>
42	SDIO_CLK#	SD2_CLK(GP3_16)	I, 3.3V CMOS	SDHI2 Clock. This pin is connected to SD/MMC connector (J30).
43	SDIO_CD#	SD2_CD(GP3_22)	O, 3.3V CMOS	SDHI2 Card Detect. This pin is connected from SD/MMC connector (J30).
44	SDIO_LED	GPIO_SD1_LED(GP5_22)	I, 3.3V CMOS	SDIO LED. This pin is connected to D8 Green LED.
45	SDIO_CMD	SD2_CMD(GP3_17)	IO, 3.3V CMOS	SDHI2 command. This pin is connected to SD/MMC connector (J30).
46	SDIO_WP	SD2_WP(GP3_23)	O, 3.3V CMOS	SDHI2 Write Protect. This pin is connected to SD/MMC connector (J30).
47	SDIO_PWR#	GPIO_SD1_PWR(GP1_27)	I, 3.3V CMOS/ 10K PD	SD/MMC Interface Power Enable. This pin is used control the power input to the SD/MMC connector.
48	SDIO_DAT1	SD2_DAT1(GP3_19)	IO, 3.3V CMOS	SD2 Data1. This pin is connected to SD/MMC connector (J30).
49	SDIO_DAT0	SD2_DAT0(GP3_18)	IO, 3.3V CMOS	SD2 Data0. This pin is connected to SD/MMC connector (J30).
50	SDIO_DAT3	SD2_DAT3(GP3_21)	IO, 3.3V CMOS	SD2 Data3. This pin is connected to SD/MMC connector (J30).
51	SDIO_DAT2	SD2_DAT2(GP3_20)	IO, 3.3V CMOS	SD2 Data2. This pin is connected to SD/MMC connector (J30).
52	SDIO_DAT5	NC	-	NC in RZ/G1H Qseven SOM. This pin is connected to SD/MMC connector (J30) in carrier board.

RZ/G1H Qseven Development Platform Hardware User Guide

Pin No.	Qseven MXM Connector Pin Name	Signal Name	Signal Type/ Termination	Description
53	SDIO_DAT4	NC	-	NC in RZ/G1H Qseven SOM. This pin is connected to SD/MMC connector (J30) in carrier board.
54	SDIO_DAT7	NC	-	NC in RZ/G1H Qseven SOM. This pin is connected to SD/MMC connector (J30) in carrier board.
55	SDIO_DAT6	NC	-	NC in RZ/G1H Qseven SOM. This pin is connected to SD/MMC connector (J30) in carrier board.
56	USB_DRIVE_VBUS	USB0_PWEN(GP5_18)	I, 3.3V CMOS	USB OTG Power enable.
57	GND	GND	Power	Ground.
58	GND	GND	Power	Ground.
59	HDA_SYNC/ I2S_WS	SSI_WS34(GP4_9)	I, 3.3V CMOS	SSI Audio transmit frame synchronization. This pin is connected to I2S audio codec.
60	SMB_CLK/ GP1_I2C_CLK	I2C0_SCL	I, 3.3V OD	I2C0 clock. This pin is connected to PCIe Clock buffer, PClex4 connector, Mini PCIe connector and Expansion Connector3 (J14) 77 th Pin.
61	HDA_RST#/ I2S_RST#	GPIO_SSI_RST(GP1_29)	I, 3.3V CMOS/ 10K PU	Audio Codec Reset. This pin is connected to Capacitive Touch Connector for touch reset & Expansion connector3 (J14) 42 nd Pin.
62	SMB_DAT/ GP1_I2C_DAT	I2C0_SDA	IO, 3.3V OD	I2C0 Data. This pin is connected to PCIe Clock buffer, PClex4 connector, Mini PCIe connector and Expansion Connector3 (J14) 79 th Pin.
63	HDA_BCLK/ I2S_CLK	SSI_SCK34(GP4_8)	O, 3.3V CMOS	SSI Audio transmit clock. This pin is connected from I2S audio codec.
64	SMB_ALERT#	NC	-	NC in RZ/G1H Qseven SOM. This pin is connected to Expansion connector3 (J14) 11 th Pin in carrier board.
65	HDA_SDI/ I2S_SDI	SSI_SDATA3(GP4_10)	O, 3.3V CMOS	SSI Audio Transmit Data. This pin is connected from I2S audio codec.
66	GP0_I2C_CLK	I2C2_SCL(GP4_0)	I, 3.3V OD	I2C2 clock. This pin is connected to I2S Audio Codec, Capacitive touch connector, Resistive touch connector, and Expansion Connector3 (J14) 78 th Pin.
67	HDA_SDO/ I2S_SDO	SSI_SDATA4(GP4_13)	I, 3.3V CMOS	SSI Audio Receive Data. This pin is connected to I2S audio codec.

RZ/G1H Qseven Development Platform Hardware User Guide

Pin No.	Qseven MXM Connector Pin Name	Signal Name	Signal Type/ Termination	Description
68	GP0_I2C_DAT	I2C2_SDA(GP4_1)	IO, 3.3V OD	I2C2 Data. This pin is connected to I2S Audio Codec, Capacitive touch connector, Resistive touch connector, and Expansion Connector3 (J14) 80 th Pin.
69	THRM#	NC	-	NC in RZ/G1H Qseven SOM. This pin is connected from Push button (SW6) in carrier board. <i>Note: This pin is optionally connected to Expansion Connector3 (J14) 20th Pin.</i>
70	WDTRIG#	NC	-	NC in RZ/G1H Qseven SOM. This pin is connected to Expansion connector3 (J14) 17 th Pin in carrier board.
71	THRMTRIP#	GPIO_THRMTRIP_Q7 (GP4_11)	O, 3.3V CMOS	Thermal trip. This pin is connected to indication LED D11 and Expansion connector3 (J14) 53 rd Pin.
72	WDOUT	NC	-	NC in RZ/G1H Qseven SOM. This pin is connected to Expansion connector3 (J14) 15 th Pin in carrier board.
73	GND	GND	Power	Ground.
74	GND	GND	Power	Ground.
75	USB_P7-/ USB_SSTX0-	USB3_TXN	IO, DIFF	USB3.0 Host Port0 Transmit Differential pair negative. This pin is connected to Dual stack USB3.0 TypeA connector (J23) bottom port.
76	USB_P6-/ USB_SSRX0-	USB3_RXN	IO, DIFF	USB3.0 Host Port0 Receive Differential pair negative. This pin is connected to Dual stack USB3.0 TypeA connector (J23) bottom port.
77	USB_P7+/ USB_SSTX0+	USB3_TXP	IO, DIFF	USB3.0 Host Port0 Transmit Differential pair positive. This pin is connected to Dual stack USB3.0 TypeA connector (J23) bottom port.
78	USB_P6+/ USB_SSRX0+	USB3_RXP	IO, DIFF	USB3.0 Host Port0 Receive Differential pair positive. This pin is connected to Dual stack USB3.0 TypeA connector (J23) bottom port.
79	USB_6_7_OC#	USB_6_7_OC#	-	Over current sense signal for USB3.0 Host Port0. This pin is connected from USB3.0 Host Port0 Over current indicator.

Pin No.	Qseven MXM Connector Pin Name	Signal Name	Signal Type/ Termination	Description
80	USB_4_5_OC#	NC	-	NC in RZ/G1H Qseven SOM. This pin is connected to USB3.0 Host Port1 Over current indicator in carrier board.
81	USB_P5-/ USB_SSTX1-	NC	-	NC in RZ/G1H Qseven SOM. This pin is connected to Dual stack USB3.0 TypeA connector (J23) top port in carrier board.
82	USB_P4-/ USB_SSRX1-	NC	-	NC in RZ/G1H Qseven SOM. This pin is connected to Dual stack USB3.0 TypeA connector (J23) top port in carrier board.
83	USB_P5+/ USB_SSTX1+	NC	-	NC in RZ/G1H Qseven SOM. This pin is connected to Dual stack USB3.0 TypeA connector (J23) top port in carrier board.
84	USB_P4+/ USB_SSRX1+	NC	-	NC in RZ/G1H Qseven SOM. This pin is connected to Dual stack USB3.0 TypeA connector (J23) top port in carrier board.
85	USB_2_3_OC#	USB_2_3_OC	O, 3.3V CMOS	Over current sense signal for USB Host Port2 and Port3. This pin is connected from USB Host Port2 Over current indicator.
86	USB_0_1_OC#	USB_0_1_OC	O, 3.3V CMOS/ 10K PU	Over current sense signal for USB Host Port0 and OTG Port1. This pin is connected from Host Port0 and USB OTG Port1 Over current indicator.
87	USB_P3-	USB_HUB2OUT_DM	-	USB 2.0 Host Port3 Data negative. This pin is connected to Dual stack USB3.0 TypeA connector (J23) top port in carrier board (from the USB HUB output port2 of the RZ/G1H SOM).
88	USB_P2-	USB2_DM	IO, DIFF	USB 2.0 Host Port2 Data negative. This pin is connected to Dual stack USB3.0 TypeA connector (J23) bottom port.
89	USB_P3+	USB_HUB2OUT_DP	-	USB 2.0 Host Port3 Data positive. This pin is connected to Dual stack USB3.0 TypeA connector (J23) top port in carrier board (from the USB HUB output port2 of the RZ/G1H SOM).

Pin No.	Qseven MXM Connector Pin Name	Signal Name	Signal Type/ Termination	Description
90	USB_P2+	USB2_DP	IO, DIFF	USB 2.0 Host Port2 Data positive. This pin is connected to Dual stack USB3.0 TypeA connector (J23) bottom port.
91	USB_VBUS	VBUS_BUS	O, 5V Power	Reference voltage to USB controller.
92	USB_ID	GPIO_USBOTG_ID(GP5_20)	O, 3.3V CMOS	USB OTG ID. This pin is connected from Micro USB OTG connector (J2).
93	USB_P1-	USB_P1-	IO, DIFF	USB 2.0 OTG Port1 Data negative. This pin is connected to Micro USB OTG connector (J2).
94	USB_P0-	USB_HUB1OUT_DM	IO, DIFF	USB 2.0 Host Port0 Data negative. This pin is connected to USB TypeA combo connector (J22) (from the USB HUB output port1 of the RZ/G1H SOM).
95	USB_P1+	USB_P1+	IO, DIFF	USB 2.0 OTG Port1 Data positive. This pin is connected to Micro USB OTG connector (J2).
96	USB_P0+	USB_HUB1OUT_DP	IO, DIFF	USB 2.0 Host Port0 Data positive. This pin is connected to USB TypeA combo connector (J22) (from the USB HUB output port1 of the RZ/G1H SOM).
97	GND	GND	Power	Ground.
98	GND	GND	Power	Ground.
99	eDP0_TX0+/ LVDS_A0+	DU_LVDS0_CH0_P	I, 1.8V LVDS	LVDS primary channel differential pair0 positive. This pin is connected to LVDS Receiver.
100	eDP1_TX0+/ LVDS_B0+	DU_LVDS1_CH0_P	I, 1.8V LVDS	LVDS secondary channel differential pair0 positive. This pin is connected to secondary LVDS connector (J27) in carrier board.
101	eDP0_TX0-/ LVDS_A0-	DU_LVDS0_CH0_N	I, 1.8V LVDS	LVDS primary channel differential pair0 negative. This pin is connected to LVDS Receiver.
102	eDP1_TX0-/ LVDS_B0-	DU_LVDS1_CH0_N	I, 1.8V LVDS	LVDS secondary channel differential pair0 negative. This pin is connected to secondary LVDS connector (J27) in carrier board.
103	eDP0_TX1+/ LVDS_A1+	DU_LVDS0_CH1_P	I, 1.8V LVDS	LVDS primary channel differential pair1 positive. This pin is connected to LVDS Receiver.

Pin No.	Qseven MXM Connector Pin Name	Signal Name	Signal Type/ Termination	Description
104	eDP1_TX1+/ LVDS_B1+	DU_LVDS1_CH1_P	I, 1.8V LVDS	LVDS secondary channel differential pair1 positive. This pin is connected to secondary LVDS connector (J27) in carrier board.
105	eDP0_TX1-/ LVDS_A1-	DU_LVDS0_CH1_N	I, 1.8V LVDS	LVDS primary channel differential pair1 negative. This pin is connected to LVDS Receiver.
106	eDP1_TX1-/ LVDS_B1-	DU_LVDS1_CH1_N	I, 1.8V LVDS	LVDS secondary channel differential pair1 negative. This pin is connected to secondary LVDS connector (J27) in carrier board.
107	eDP0_TX2+/ LVDS_A2+	DU_LVDS0_CH2_P	I, 1.8V LVDS	LVDS primary channel differential pair2 positive. This pin is connected to LVDS Receiver.
108	eDP1_TX2+/ LVDS_B2+	DU_LVDS1_CH2_P	I, 1.8V LVDS	LVDS secondary channel differential pair2 positive. This pin is connected to secondary LVDS connector (J27) in carrier board.
109	eDP0_TX2-/ LVDS_A2-	DU_LVDS0_CH2_N	I, 1.8V LVDS	LVDS primary channel differential pair2 negative. This pin is connected to LVDS Receiver.
110	eDP1_TX2-/ LVDS_B2-	DU_LVDS1_CH2_N	I, 1.8V LVDS	LVDS secondary channel differential pair2 negative. This pin is connected to secondary LVDS connector (J27) in carrier board.
111	LVDS_PPEN	GPIO_LVDS_PPEN(GP5_28)	I, 3.3V CMOS/ 10K PU	LCD Panel Power Enable.
112	LVDS_BLEN	GPIO_LVDS_BLEN(GP3_11)	I, 3.3V CMOS/ 10K PU	LCD Panel Backlight Enable Control.
113	eDP0_TX3+/ LVDS_A3+	DU_LVDS0_CH3_P	I, 1.8V LVDS	LVDS primary channel differential pair3 positive. This pin is connected to LVDS Receiver.
114	eDP1_TX3+/ LVDS_B3+	DU_LVDS1_CH3_P	I, 1.8V LVDS	LVDS secondary channel differential pair3 positive. This pin is connected to secondary LVDS connector (J27) in carrier board.
115	eDP0_TX3-/ LVDS_A3-	DU_LVDS0_CH3_N	I, 1.8V LVDS	LVDS primary channel differential pair3 negative. This pin is connected to LVDS Receiver.

Pin No.	Qseven MXM Connector Pin Name	Signal Name	Signal Type/ Termination	Description
116	eDP1_TX3-/LVDS_B3-	DU_LVDS1_CH3_N	I, 1.8V LVDS	LVDS secondary channel differential pair3 negative. This pin is connected to secondary LVDS connector (J27) in carrier board.
117	GND	GND	Power	Ground.
118	GND	GND	Power	Ground.
119	eDP0_AUX+/LVDS_A_CLK+	DU_LVDS0_CLK_P	I, 1.8V LVDS	LVDS primary channel differential Clock positive. This pin is connected to LVDS Receiver.
120	eDP1_AUX+/LVDS_B_CLK+	DU_LVDS1_CLK_P	I, 1.8V LVDS	LVDS secondary channel differential Clock positive. This pin is connected to secondary LVDS connector in carrier board.
121	eDP0_AUX-/LVDS_A_CLK-	DU_LVDS0_CLK_N	I, 1.8V LVDS	LVDS primary channel differential Clock negative. This pin is connected to LVDS Receiver.
122	eDP1_AUX-/LVDS_B_CLK-	DU_LVDS1_CLK_N	I, 1.8V LVDS	LVDS secondary channel differential Clock negative. This pin is connected to secondary LVDS connector (J27) in carrier board.
123	LVDS_BLT_CTRL/ GP_PWM_OUT0	TPU0TO2/MD22(GP0_22) ¹	I, 3.3V CMOS/ 10K PU	RGB & LVDS LCD Panel Backlight Control.
124	GP_1-Wire_Bus	NC	-	NC in RZ/G1H Qseven SOM. This pin is connected to HDMI connector (J24) in carrier board.
125	GP2_I2C_DAT/LVDS_DID_DAT	I2C3_SDA	-	I2C3 Data. This pin is directly connected to Expansion Connector3 (J14) 35 th Pin in carrier board.
126	eDP0_HPD#/ LVDS_BLC_DAT	NC	-	NC in RZ/G1H Qseven SOM. This pin is directly connected to Expansion Connector3 (J14) 19 th Pin in carrier board.
127	GP2_I2C_CLK/ LVDS_DID_CLK	I2C3_SCL	-	I2C3 Clock. This pin is directly connected to Expansion Connector3 (J14) 37 th Pin in carrier board.
128	eDP1_HPD#/ LVDS_BLC_CLK	NC	-	NC in RZ/G1H Qseven SOM. This pin is directly connected to Expansion Connector3 (J14) 21 st Pin in carrier board.
129	CAN0_TX	CAN1_TX(GP4_6)	I, 3.3V CMOS	Transmit input for CAN0 bus. This pin is connected to CAN0 Transceiver.

Pin No.	Qseven MXM Connector Pin Name	Signal Name	Signal Type/ Termination	Description
130	CAN0_RX	CAN1_RX(GP4_7)	O, 3.3V CMOS	Receive output for CAN0 bus. This pin is connected from CAN0 Transceiver.
131	DP_LANE3+/ TMDS_CLK+	NC	-	NC in RZ/G1H Qseven SOM. HDMI differential data lane clock positive. This pin is connected to HDMI connector (J24) in carrier board.
132	RSVD	NC	-	NC in RZ/G1H Qseven SOM. Note: This pin is directly connected to Expansion Connector3 (J14) 23 rd Pin in carrier board.
133	DP_LANE3-/ TMDS_CLK-	NC	-	NC in RZ/G1H Qseven SOM. HDMI differential data clock negative. This pin is connected to HDMI connector (J24) in carrier board.
134	RSVD	NC	-	NC in RZ/G1H Qseven SOM. Note: This pin is directly connected to Expansion Connector3 (J14) 25 th Pin in carrier board.
135	GND	GND	Power	Ground.
136	GND	GND	Power	Ground.
137	DP_LANE1+/ TMDS_LANE1+	NC	-	NC in RZ/G1H Qseven SOM. HDMI differential data lane 1 positive. This pin is connected to HDMI connector (J24) in carrier board.
138	DP_AUX+	NC	-	NC in RZ/G1H Qseven SOM. Note: This pin is directly connected to Expansion Connector3 (J14) 52 nd Pin in carrier board.
139	DP_LANE1-/ TMDS_LANE1-	NC	-	NC in RZ/G1H Qseven SOM. HDMI differential data lane 1 negative. This pin is connected to HDMI connector (J24) in carrier board.
140	DP_AUX-	NC	-	NC in RZ/G1H Qseven SOM. Note: This pin is directly connected to Expansion Connector3 (J14) 54 th Pin in carrier board.
141	GND	GND	Power	Ground.
142	GND	GND	Power	Ground.

Pin No.	Qseven MXM Connector Pin Name	Signal Name	Signal Type/ Termination	Description
143	DP_LANE2+/ TMDS_LANE0+	NC	-	NC in RZ/G1H Qseven SOM. HDMI differential data lane 0 positive. This pin is connected to HDMI connector (J24) in carrier board.
144	RSVD	NC	-	NC in RZ/G1H Qseven SOM. Note: This pin is directly connected to Expansion Connector3 (J14) 29 th Pin in carrier board.
145	DP_LANE2-/ TMDS_LANE0-	NC	-	NC in RZ/G1H Qseven SOM. HDMI differential data lane 0 negative. This pin is connected to HDMI connector (J24) in carrier board.
146	RSVD	NC	-	NC in RZ/G1H Qseven SOM. Note: This pin is directly connected to Expansion Connector3 (J14) 31 st Pin in carrier board.
147	GND	GND	Power	Ground.
148	GND	GND	Power	Ground.
149	DP_LANE0+/ TMDS_LANE2+	NC	-	NC in RZ/G1H Qseven SOM. HDMI differential data lane 2 positive. This pin is connected to HDMI connector (J24) in carrier board.
150	HDMI_CTRL_DAT	NC	-	NC in RZ/G1H Qseven SOM. HDMI I2C Data. This pin is connected to HDMI connector (J24) in carrier board.
151	DP_LANE0-/ TMDS_LANE2-	NC	-	NC in RZ/G1H Qseven SOM. HDMI differential data lane 2 negative. This pin is connected to HDMI connector (J24) in carrier board.
152	HDMI_CTRL_CLK	NC	-	NC in RZ/G1H Qseven SOM. HDMI I2C Clock. This pin is connected to HDMI connector (J24) in carrier board.
153	DP_HDMI_HPD#	NC	-	NC in RZ/G1H Qseven SOM. HDMI hot plug detect. This pin is connected to HDMI connector (J24) in carrier board.
154	RSVD	NC	-	NC in RZ/G1H Qseven SOM. Note: This pin is directly connected to Expansion Connector3 (J14) 39 th Pin in carrier board.

RZ/G1H Qseven Development Platform Hardware User Guide

Pin No.	Qseven MXM Connector Pin Name	Signal Name	Signal Type/ Termination	Description
155	PCIE_CLK_REF+	PCle_REFCLK_DP	I, DIFF	PCle differential reference clock positive. This pin is connected to PCle clock buffer.
156	PCIE_WAKE#	GPIO_PCl_e_WAKE(GP2_14)	O, 3.3V CMOS/ 10K PU	PCle wake event. This pin is connected to PCle x 4 connector (J4) and Mini PCle connector(J26).
157	PCIE_CLK_REF-	PCle_REFCLK_DN	I, DIFF	PCle differential reference clock negative. This pin is connected to PCle clock buffer.
158	PCIE_RST#	GPIO_PCl_e_RST/MD4(GP4_31) ⁷	I, 3.3V CMOS	PCle reset. This pin is connected to PCle x 4 connector (J7) and Mini PCle connector (J26).
159	GND	GND	Power	Ground.
160	GND	GND	Power	Ground.
161	PCIE3_TX+	NC	-	NC in RZ/G1H Qseven SOM. This pin is connected to PClex4 connector (J4) in carrier board.
162	PCIE3_RX+	NC	-	NC in RZ/G1H Qseven SOM. This pin is connected to PClex4 connector (J4) in carrier board.
163	PCIE3_TX-	NC	-	NC in RZ/G1H Qseven SOM. This pin is connected to PClex4 connector (J4) in carrier board.
164	PCIE3_RX-	NC	-	NC in RZ/G1H Qseven SOM. This pin is connected to PClex4 connector (J4) in carrier board.
165	GND	GND	Power	Ground.
166	GND	GND	Power	Ground.
167	PCIE2_TX+	NC	-	NC in RZ/G1H Qseven SOM. This pin is connected to PClex4 connector (J4) in carrier board.
168	PCIE2_RX+	NC	-	NC in RZ/G1H Qseven SOM. This pin is connected to PClex4 connector (J4) in carrier board.
169	PCIE2_TX-	NC	-	NC in RZ/G1H Qseven SOM. This pin is connected to PClex4 connector (J4) in carrier board.
170	PCIE2_RX-	NC	-	NC in RZ/G1H Qseven SOM. This pin is connected to PClex4 connector (J4) in carrier board.
171	UART0_TX	SCIFB2_TXD(GP4_23)	I, 3.3V CMOS	SCIFB2 interface serial data transmitter. This pin is connected to Data UART Header (J1) 05 th Pin.

Pin No.	Qseven MXM Connector Pin Name	Signal Name	Signal Type/ Termination	Description
172	UART0_ RTS #	SCIFB2_RTS#(GP4_25)	I, 3.3V CMOS	SCIFB2 interface ready to receive handshake signal. This pin is connected to Data UART Header (J1) 06 th Pin.
173	PCIE1_TX+	NC	-	NC in RZ/G1H Qseven SOM. This pin is connected to PClex4 connector (J7) in carrier board.
174	PCIE1_RX+	NC	-	NC in RZ/G1H Qseven SOM. This pin is connected to PClex4 connector (J7) in carrier board.
175	PCIE1_TX-	NC	-	NC in RZ/G1H Qseven SOM. This pin is connected to PClex4 connector (J7) in carrier board.
176	PCIE1_RX-	NC	-	NC in RZ/G1H Qseven SOM. This pin is connected to PClex4 connector (J7) in carrier board.
177	UART0_RX	SCIFB2_RXD(GP4_22)	O, 3.3V CMOS	SCIFB2 interface serial data receiver. This pin is connected from Data UART Header (J1) 04 th Pin.
178	UART0_CTS#	SCIFB2_CTS#(GP4_24)	O, 3.3V CMOS	SCIFB2 interface ready to send handshake signal. This pin is connected from Data UART Header (J1) 02 nd Pin.
179	PCIE0_TX+	PCle1_TXP	I, DIFF	PCle Channel0 Transmit data output positive. This pin is connected to PCle x 4 connector (J7) or Mini PCle connector (J26) through PCle Switch.
180	PCIE0_RX+	PCle1_RXP	O, DIFF	PCle Channel0 Receive data input positive. This pin is connected to PCle x 4 connector (J7) or Mini PCle connector (J26) through PCle Switch.
181	PCIE0_TX-	PCle1_TXN	I, DIFF	PCle Channel0 Transmit data output negative. This pin is connected to PCle x 4 connector (J7) or Mini PCle connector (J26) through PCle Switch.
182	PCIE0_RX-	PCle1_RXN	O, DIFF	PCle Channel0 Receive data input negative. This pin is connected to PCle x 4 connector (J7) or Mini PCle connector (J26) through PCle Switch.
183	GND	GND	Power	Ground.

Pin No.	Qseven MXM Connector Pin Name	Signal Name	Signal Type/ Termination	Description
184	GND	GND	Power	Ground.
185	LPC_AD0/ GPIO0	Q7_GPIO0_(GP0_24)	IO,3.3VCMOS/ 10K PU	General purpose Input/Output0. This GPIO is used for Touch Interrupt and connected from Capacitive Touch Connector or Resistive Touch Controller. <i>Note: This pin is also connected to Expansion Connector3 (J14) 36th Pin through resistor and default populated.</i>
186	LPC_AD1/ GPIO1	Q7_GPIO1_(GP0_25)	IO,3.3VCMOS/ 10K PU	General purpose Input/Output1. This pin is connected to Expansion Connector3 (J14) 34 th Pin through resistor. <i>Note: This pin is also connected to Mini PCIe connector (J26) 20th Pin through resistor and default populated.</i>
187	LPC_AD2 / GPIO2	Q7_GPIO2_(GP0_26)	IO,3.3VCMOS/ 10K PU	General purpose Input/Output2. This GPIO is used for Mic Input Detect and connected from Audio IN Jack. <i>Note: This pin is also connected to Expansion connector3 (J14) 45th Pin through resistor and default populated.</i>
188	LPC_AD3/ GPIO3	Q7_GPIO3_(GP4_19)	IO,3.3VCMOS/ 10K PU	General purpose Input/Output3. This GPIO is used for Headphone Detect and connected from Audio Out Jack. <i>Note: This pin is also connected to Expansion connector3 (J14) 41st Pin through resistor and default populated.</i>
189	LPC_CLK/ GPIO4	Q7_GPIO4_(GP1_28)	IO, 3.3V CMOS	General purpose Input/Output4. This GPIO is used for CAN0 Transceiver Power down control and connected to CAN transceiver. <i>Note: This pin is also connected to Expansion connector3 (J14) 47th Pin.</i>
190	LPC_FRAME#/ GPIO5	Q7_GPIO5_(GP2_17)	IO,3.3VCMOS/ 10K PU	LVDS LCD Panel Backlight Enable Control. <i>Note: Also, this pin is connected to Expansion Connector3 (J14) 44th Pin through resistor and default populated.</i>
191	SERIRQ / GPIO6	Q7_GPIO6_(GP4_2)	IO,3.3VCMOS/ 10K PU	LVDS LCD Panel Power Enable. <i>Note: Also, this pin is connected to Expansion Connector3 (J14) 40th Pin through resistor and default populated.</i>

RZ/G1H Qseven Development Platform Hardware User Guide

Pin No.	Qseven MXM Connector Pin Name	Signal Name	Signal Type/ Termination	Description
192	LPC_LDRQ#/ GPIO7	Q7_GPIO7_(GP4_14)	IO, 3.3V CMOS	General purpose Input/Output7. <i>Note: This pin is connected to Expansion Connector3 (J14) 09th Pin through resistor and default populated.</i>
193	VCC_RTC	VRTC_3V0	O, 3V Power	3V backup coin cell input for RTC.
194	SPKR/ GP_PWM_OUT2	TPU0TO0/MD24(GP0_20) ¹	I, 3.3V CMOS	Buzzer control PWM input. This pin is connected to buzzer in carrier board. <i>Note: Also, this pin is used as a GPIO for LVDS LCD Backlight control through resistor and default populated.</i>
195	FAN_TACHOIN/ GP_TIMER_IN	NC	-	NC in RZ/G1H Qseven SOM. This pin is connected to Fan Header (J19) 04 th Pin in carrier board.
196	FAN_PWMOUT/ GP_PWM_OUT1	TPU0TO1/MD23(GP0_21) ¹	I, 3.3V CMOS	Fan Control PWM input. This pin is connected to Fan Header (J19) 2 nd Pin.
197	GND	GND	Power	Ground.
198	GND	GND	Power	Ground.
199	SPI_MOSI	MSIOF0_TXD/MDT1(GP5_15) ¹	I, 3.3V CMOS	SPI Master Out Slave In. This Pin is connected to SPI Flash. <i>Note: This pin is also connected to Expansion connector3 (J14) 48th Pin.</i>
200	SPI_CS0#	MSIOF0_SYNC(GP5_13)	I, 3.3V CMOS/ 10K PU	SPI Chip Select1. This Pin is connected to SPI Flash.
201	SPI_MISO	MSIOF0_RXD(GP5_17)	O, 3.3V CMOS	SPI Master In Slave Out. This Pin is connected from SPI Flash. <i>Note: This pin is also connected to Expansion connector3 (J14) 46th Pin.</i>
202	SPI_CS1#	MSIOF0_SS1/MD0(GP5_14) ¹	I, 3.3V CMOS	SPI Chip Select2. This pin is also connected to Expansion connector3 (J14) 49 th Pin.
203	SPI_SCK	MSIOF0_SCK(GP5_12)	I, 3.3V CMOS	SPI Clock. This Pin is connected to SPI Flash. <i>Note: This pin is also connected to Expansion connector3 (J14) 51st Pin.</i>
204	MFG_NC4	NC	-	NC in RZ/G1H Qseven SOM. JTAG Test Reset. This pin is connected from JTAG Header (J16) 03 rd Pin through buffer.

RZ/G1H Qseven Development Platform Hardware User Guide

Pin No.	Qseven MXM Connector Pin Name	Signal Name	Signal Type/ Termination	Description
205	VCC_5V_SB	NC	-	NC in RZ/G1H Qseven SOM. This pin is connected to 5V standby power supply in carrier board.
206	VCC_5V_SB	NC	-	NC in RZ/G1H Qseven SOM. This pin is connected to 5V standby power supply in carrier board.
207	MFG_NC0	JTAG_TCK	O, 3.3V CMOS/ 10K PD	JTAG Test Clock. This pin is connected from JTAG Header (J16) 09 th Pin through buffer.
208	MFG_NC2	SCIFA2_RXD(GP5_31)	O, 3.3V CMOS	SCIFA2 serial data receiver. This pin is connected from Serial to USB converter for Debug console. <i>Note: This pin is also connected to JTAG Header (J16) 05th Pin (JTAG_TDI) through buffer.</i>
209	MFG_NC1	SCIFA2_TXD/MD6(GP5_30)	I, 3.3V CMOS	SCIFA2 serial data transmitter. This pin is connected to Serial to USB converter for Debug console. <i>Note: This pin is also connected to JTAG Header (J16) 13th Pin (JTAG_TDO) through buffer.</i>
210	MFG_NC3	JTAG_TMS	O, 3.3V CMOS/ 10K PU	JTAG Test Mode Select. This pin is connected from JTAG Header (J16) 07 th Pin through buffer.
211	VCC	VCC_5V	O, 5V Power	Supply Voltage.
212	VCC	VCC_5V	O, 5V Power	Supply Voltage.
213	VCC	VCC_5V	O, 5V Power	Supply Voltage.
214	VCC	VCC_5V	O, 5V Power	Supply Voltage.
215	VCC	VCC_5V	O, 5V Power	Supply Voltage.
216	VCC	VCC_5V	O, 5V Power	Supply Voltage.
217	VCC	VCC_5V	O, 5V Power	Supply Voltage.
218	VCC	VCC_5V	O, 5V Power	Supply Voltage.
219	VCC	VCC_5V	O, 5V Power	Supply Voltage.
220	VCC	VCC_5V	O, 5V Power	Supply Voltage.
221	VCC	VCC_5V	O, 5V Power	Supply Voltage.
222	VCC	VCC_5V	O, 5V Power	Supply Voltage.
223	VCC	VCC_5V	O, 5V Power	Supply Voltage.
224	VCC	VCC_5V	O, 5V Power	Supply Voltage.
225	VCC	VCC_5V	O, 5V Power	Supply Voltage.
226	VCC	VCC_5V	O, 5V Power	Supply Voltage.
227	VCC	VCC_5V	O, 5V Power	Supply Voltage.

Pin No.	Qseven MXM Connector Pin Name	Signal Name	Signal Type/ Termination	Description
228	VCC	VCC_5V	O, 5V Power	Supply Voltage.
229	VCC	VCC_5V	O, 5V Power	Supply Voltage.
230	VCC	VCC_5V	O, 5V Power	Supply Voltage.

¹ Important Note: These signals are also used for RZ/G1H CPU bootstrap setting on RZ/G1H Qseven SOM.

2.4 On Board Switches

2.4.1 Power ON/OFF Switch

The RZ/G1H Qseven carrier board has power ON/OFF switch (SW1) to control the Main Power Input On/Off functionality. This power ON/OFF switch is physically located at the top of the board as shown below.

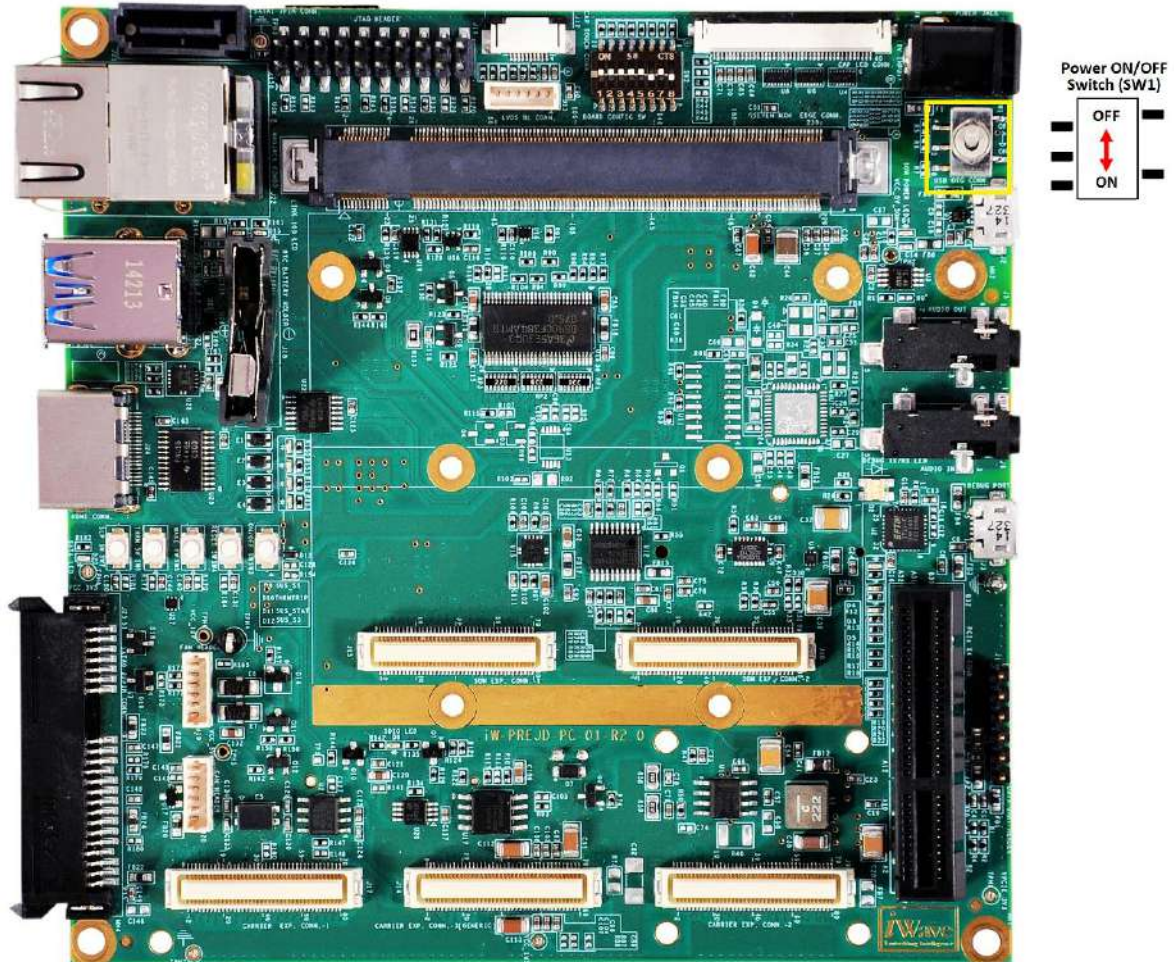


Figure 3: Power ON/OFF Switch

2.4.2 Board Configuration Switch

The RZ/G1H Qseven carrier board has one 8bit Board configuration switch (SW2) to configure board specific feature setting. Each bit of this switch is used to select the different features or modes. This Board configuration switch is physically located at the top of the board as shown below.

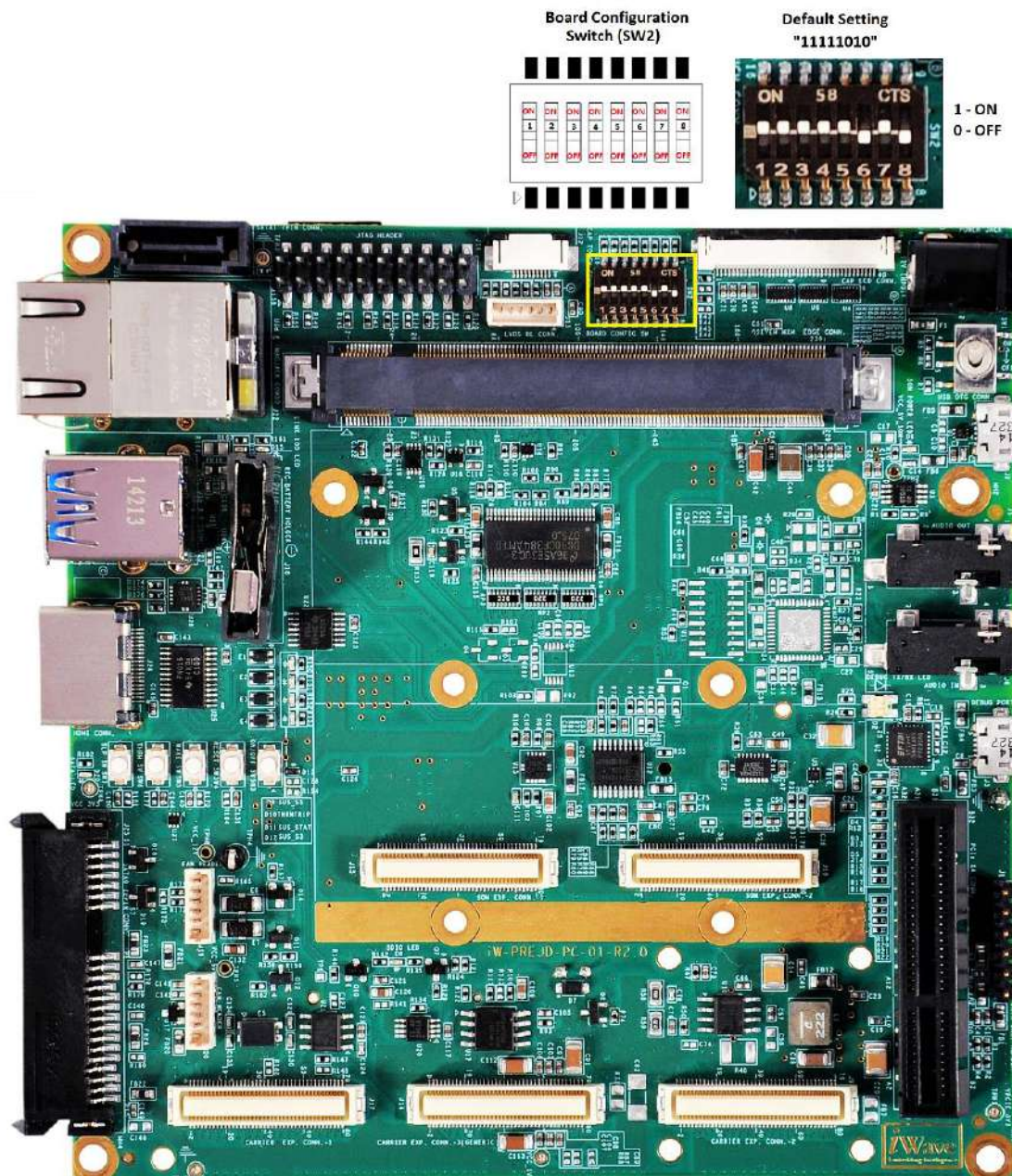


Figure 4: Board Configuration Switch

The functionality of Board configuration switch (SW2) in RZ/G1H carrier board is explained in the following table. All the bits of Board configuration switch are not used in RZ/G1H carrier board and so only the required bits are explained with default setting highlighted.

Table 4: Board Configuration Switch

SW2 Bits	SW2 Bit Name	Description	
		OFF	ON
1	BIOS_DSIABLE#	-	-
2	BATLOW#	-	-
3	LID_BTN#	-	-
4	USB_SELECT	-	-
5	CODEC_SELECT	-	-
6	PCIe_SELECT	PCIe channel0 is connected to Mini-PCIe Slot.	PCIe channel0 is connected to PClex4 Slot.
7	DEBUG_SELECT	-	Debug Port is selected as UART.
8	USB_ID	USB0 acts as Host mode or Device mode based on the connected cable in USB MicroAB connector (J2).	USB0 is forced to Host Mode.

2.4.3 Reset Switch

The RZ/G1H Qseven carrier board supports Push button switch (SW4) to reset the RZ/G1H CPU. “RSTBTN” signal of Qseven MXM connector is directly connected from Reset Push button switch. This Reset Push button switch (SW4) is physically located at the top of the board as shown below.

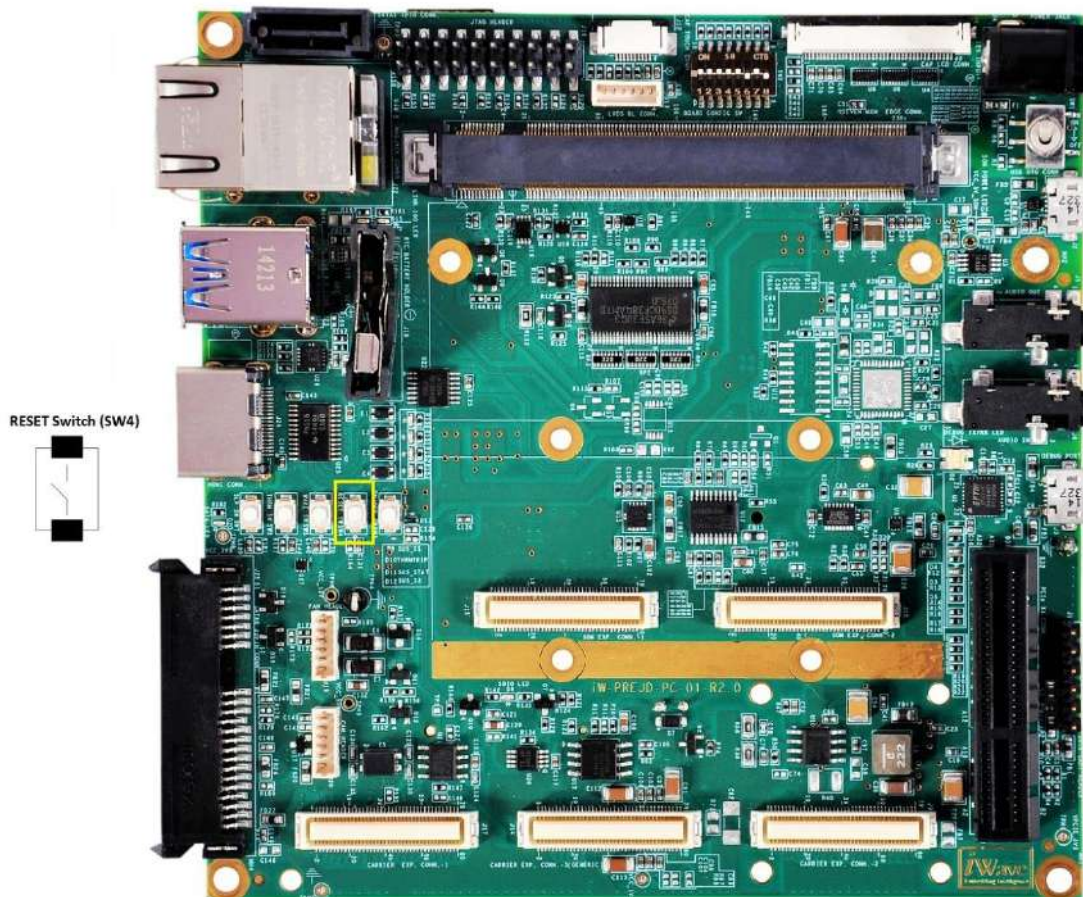


Figure 5: Reset Switch

2.5 Serial Interface Features

2.5.1 Debug UART Port

The RZ/G1H Qseven carrier board supports debug interface through RZ/G1H CPU's SCIFA2 interface. This SCIFA2 signals from Qseven MXM connector is connected to UART to USB Converter "FT232RQ" and to USB Micro AB Connector (J3). This USB Micro AB Connector can be used for Debug purpose which is physically located at the top of the board as shown below.

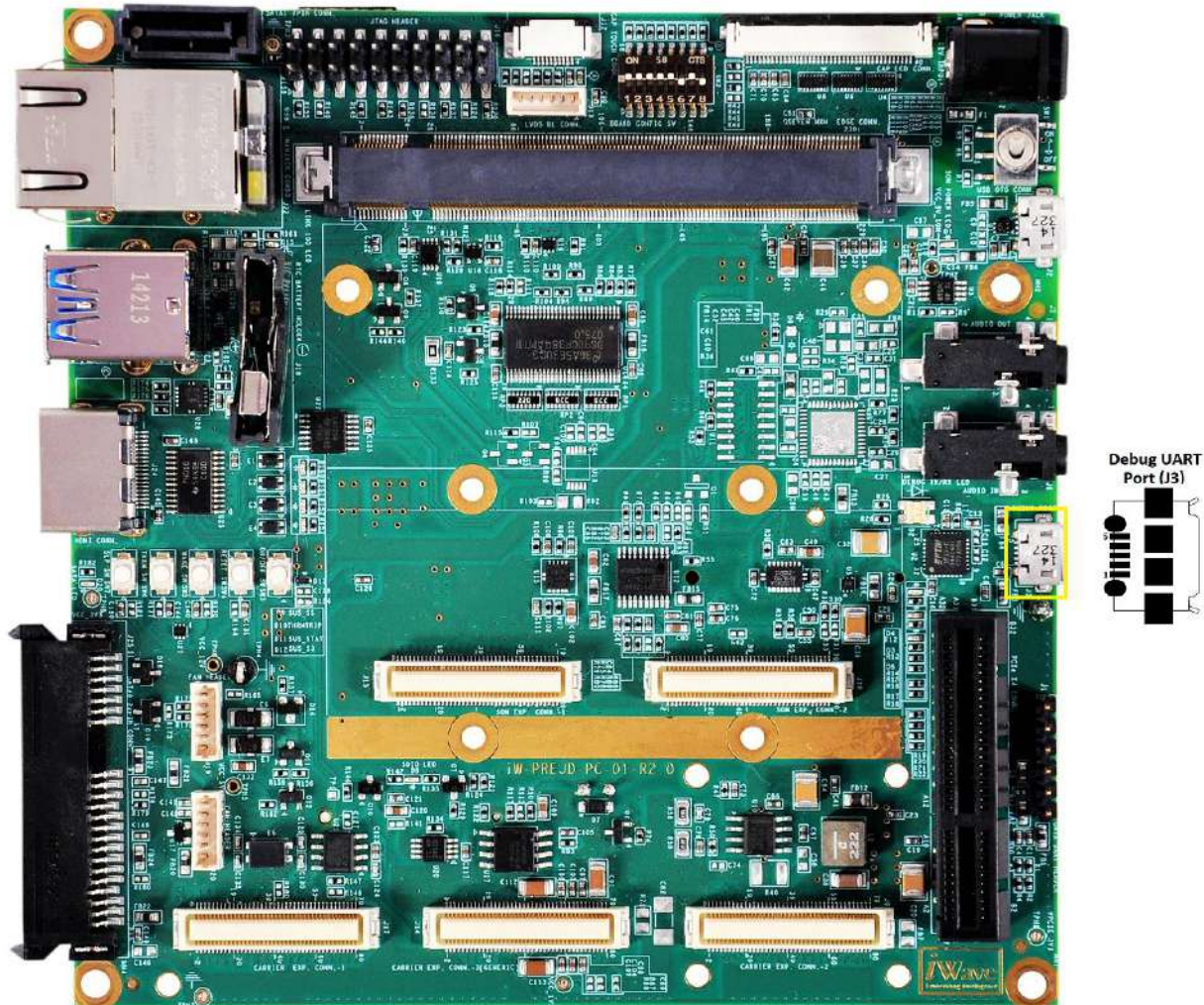


Figure 6: Debug UART

As per Qseven specification version 2.0, Debug UART interface and JTAG interface are shared the same pins in Qseven Edge connector and so either one interface only can be used at a time. The required debug interface can be selected by setting the 7th bit of Board configuration switch (SW2) to the appropriate position. Since RZ/G1H Qseven SOM supports only Debug UART (SCIFA2) on Qseven Edge connector by default, 7th bit of Board configuration switch must be set to Debug UART.

2.5.2 Data UART Header

The RZ/G1H Qseven carrier board supports full functional Data UART interface through RZ/G1H CPU's SCIFB2 interface. This SCIFB2 signals from Qseven MXM connector is connected directly to 6pin Header (J1) for easy accessibility. This Data UART header is physically located at the top of the board as shown below.

Number of Pins : 6

Connector Part number : 5-146280-6 from TE Connectivity

Mating Connector : 534237-4 from TE Connectivity

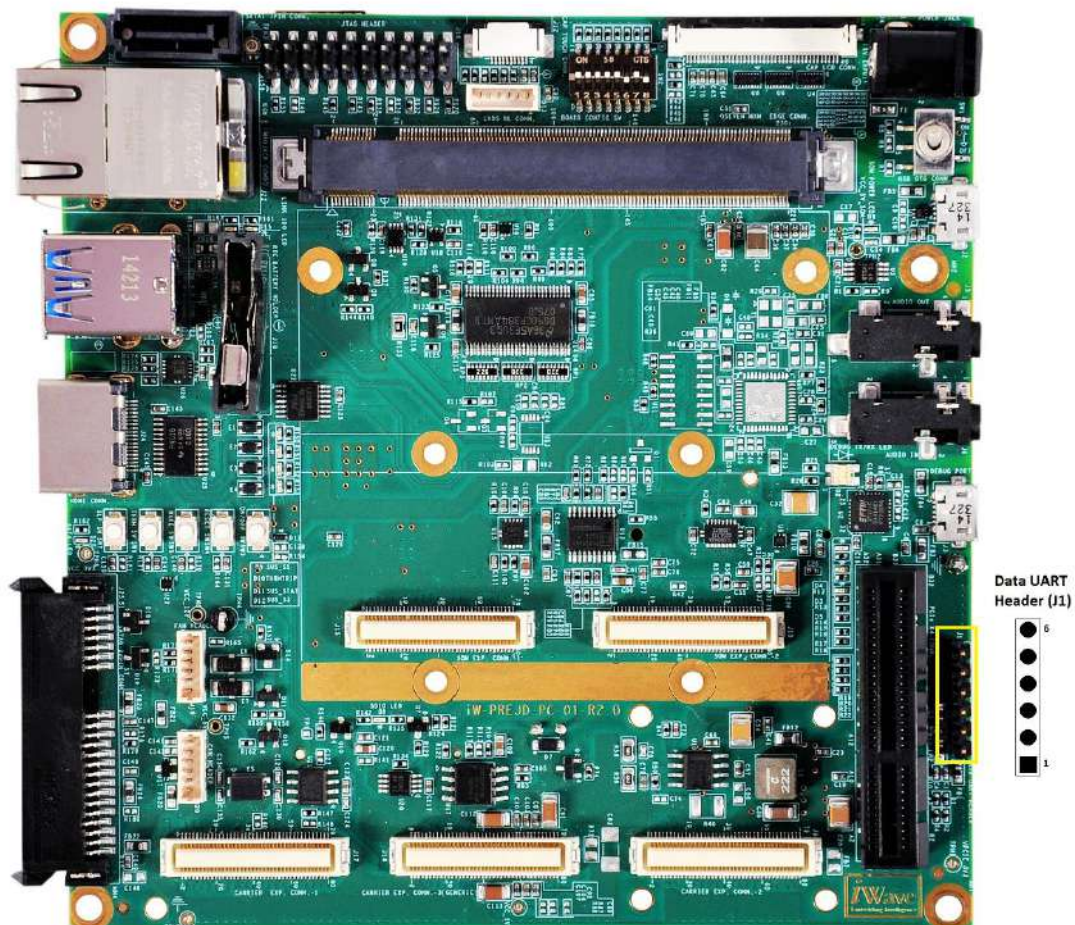


Figure 7: Data UART Header

Table 5: Data UART Header Pin Out

Pin No	Pin Name	Signal Name	Signal Type/ Termination	Description
1	GND	GND	Power	Ground.
2	UART_CTS#	SCIFB2_CTS#(GP4_24)	O, 3.3V CMOS	SCIFB2 interface Clear to Send signal.
3	VCC_3V3	VCC_3V3	O, 3.3V Power	3.3V Supply Voltage.
4	UART_RXD	SCIFB2_RXD(GP4_22)	I, 3.3V CMOS	SCIFB2 interface Receive signal.
5	UART_TXD	SCIFB2_TXD(GP4_23)	O, 3.3V CMOS	SCIFB2 interface Transmit signal.
6	UART_RTS#	SCIFB2_RTS#(GP4_25)	I, 3.3V CMOS	SCIFB2 interface Ready to Send signal.

2.6 High Speed Interface Features

2.6.1 USB3.0 Port0 (Host)

The RZ/G1H Qseven carrier board supports Super Speed USB3.0 Host interface through RZ/G1H CPU's USB3.0 interface. This USB3.0 Port0 signals of Qseven MXM connector is directly connected to bottom port of dual stack USB3.0 TypeA connector (J23). Also USB2.0 Port2 signals of Qseven MXM connector is connected to this connector for USB2.0 host interface from RZ/G1H CPU's USB2 interface.

The VBUS power of this USB3.0 connector is connected through current limit power switch and limit is set as 900mA. If connected USB3.0 device takes more than 900mA current, this power switch limits the current to constant mode and sends the over current indication signal to the over current indicator pin of Qseven MXM connector USB port 6 & 7. This USB3.0 connector (J23) is physically located at the top of the board as shown below.

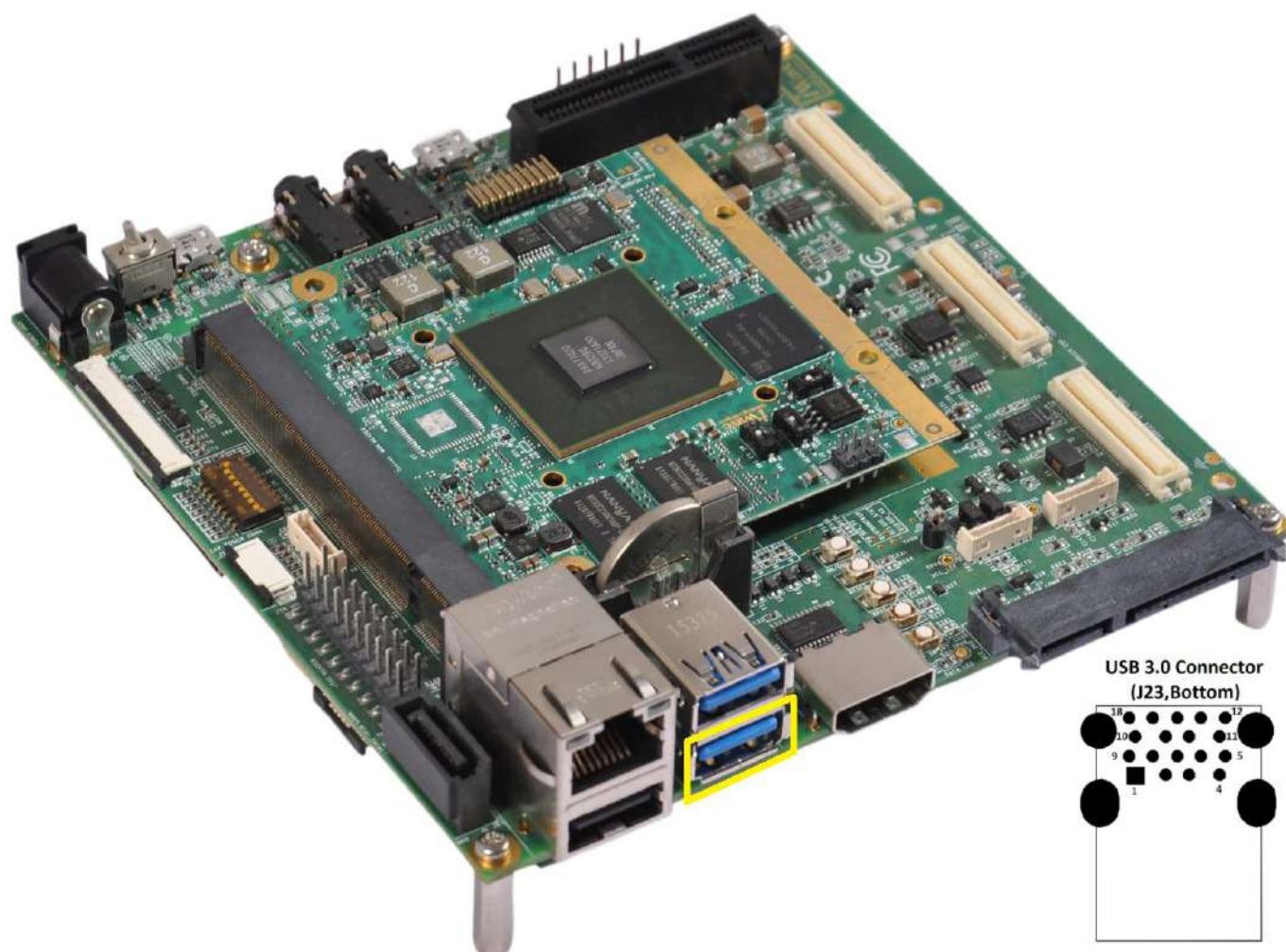


Figure 8: USB3.0 Host Port0

Table 6: Dual stack USB 3.0 Connector Pin Out (Bottom port)

Pin No	Pin Name	Signal Name	Signal Type/ Termination	Description
1	VCC_5V	VBUS	O, 5V Power	5V Supply Voltage.
2	USB_DM	USB_P2-	IO, DIFF	USB2.0 Host Port2 data negative.
3	USB_DP	USB_P2+	IO, DIFF	USB2.0 Host Port2 data positive.
4	GND	GND	Power	Ground.
5	USB_RXN	USB3_RXN	IO, DIFF	USB3.0 Host Port0 Receive pair negative.
6	USB_RXP	USB3_RXP	IO, DIFF	USB3.0 Host Port0 Receive pair positive.
7	GND	GND	Power	Ground.
8	USB_TXN	USB3_TXN	IO, DIFF	USB3.0 Host Port0 Transmit pair negative.
9	USB_TXP	USB3_TXP	IO, DIFF	USB3.0 Host Port0 Transmit pair positive.

2.6.2 PCIe Channel0 Port

The RZ/G1H Qseven carrier board supports one PCI Express Gen2.0 lane through RZ/G1H CPU's PCIe interface. PCIe reference clock from Qseven MXM connector is connected to two output clock buffer and then connected to PClex4 connector and Mini PCIe connector for clock reference.

The PCIe channel0 signals of Qseven MXM connector is connected to 1:2 Multiplexer/Demultiplexer switch and then one output of this Multiplexer/Demultiplexer switch is connected to PClex4 connector and other one to Mini-PCIe connector. The selection between PClex4 connector and Mini-PCIe connector can be done by setting the 6th bit of Board configuration switch (SW2) to appropriate position.

If the 6th bit of Board configuration switch is set to ON position, then PCIe channel0 of Qseven MXM connector is connected to PClex4 connector which is physically located at the top of the board as shown below.

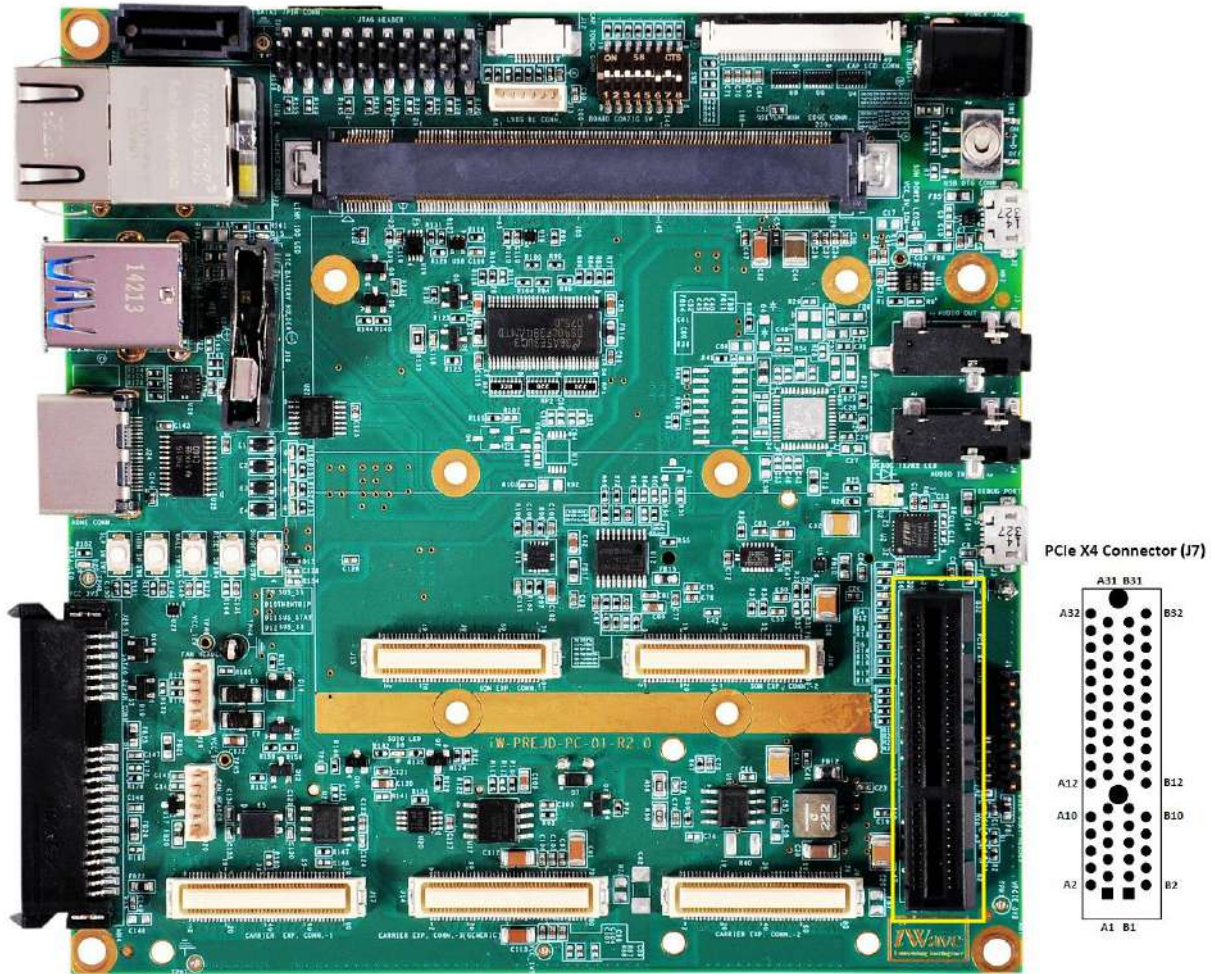


Figure 9: PCIe4 Connector

Table 7: PCIe4 Connector Pin Out

Pin No	Pin Name	Signal Name	Signal Type/ Termination	Description
A1	PRSENT1#	PRSENT1#	O, 3.3V CMOS	Default Grounded.
B1	+12V	VCC_12V	O, 12V Power	12V Supply Voltage.
A2	+12V	VCC_12V	O, 12V Power	12V Supply Voltage.
B2	+12V	VCC_12V	O, 12V Power	12V Supply Voltage.
A3	+12V	VCC_12V	O, 12V Power	12V Supply Voltage.
B3	RSVD1	NC	-	NC, Reserved Pin.
A4	GND	GND	Power	Ground.
B4	GND	GND	Power	Ground.
A5	TCK	NC	-	NC.
B5	SMCLK	I2C0_SCL	O, 3.3V CMOS	SMB Clock.
A6	TDI	NC	-	NC.
B6	SMDAT	I2C0_SDA	IO, 3.3V CMOS	SMB Data.
A7	TDO	NC	-	NC.
B7	GND	GND	Power	Ground.

RZ/G1H Qseven Development Platform Hardware User Guide

Pin No	Pin Name	Signal Name	Signal Type/ Termination	Description
A8	TMS	NC	-	NC.
B8	+3.3V	VPCle_3V3	O, 3.3V Power	3.3V Supply Voltage.
A9	+3.3V	VPCle_3V3	O, 3.3V Power	3.3V Supply Voltage.
B9	TRST#	NC	-	NC.
A10	+3.3V	VPCle_3V3	O, 3.3V Power	3.3V Supply Voltage.
B10	3V3AUX	VAUX_3V3	O, 3.3V Power	3.3V Supply Voltage.
A11	PERST#	GPIO_PCl_e_RST/MD4(GP4_31)	O, 3.3V CMOS	PCl_e PERST#.
B11	WAKE#	GPIO_PCl_e_WAKE(GP2_14)	O, 3.3V CMOS	PCl_e WAKE#.
A12	GND	GND	Power	Ground.
B12	RSVD2	NC	-	NC, Reserved Pin.
A13	REFCLK+	PCl_e_REFCLK_DP	O, DIFF	PCl_e Clock positive.
B13	GND	GND	Power	Ground.
A14	REFCLK-	PCl_e_REFCLK_DN	O, DIFF	PCl_e Clock negative.
B14	PCIE0_TX+	PCl_e1_TXP	O, DIFF	PCl_e Port 0 Transmit pair positive.
A15	GND	GND	Power	Ground.
B15	PCIE0_TX-	PCl_e1_TXN	O, DIFF	PCl_e Port 0 Transmit pair negative.
A16	PCIE0_RX+	PCl_e1_RXP	I, DIFF	PCl_e Port 0 Receive pair positive.
B16	GND	GND	Power	Ground.
A17	PCIE0_RX-	PCl_e1_RXN	I, DIFF	PCl_e Port 0 Receive pair negative.
B17	PRSNT2#	NC	-	NC.
A18	GND	GND	Power	Ground.
B18	GND	GND	Power	Ground.
A19	RSVD	NC	-	NC, Reserved Pin.
B19	PCIE1_TX+	NC	-	NC, PCl_e Port 1 Transmit pair positive.
A20	GND	GND	Power	Ground.
B20	PCIE1_TX-	NC	-	NC, PCl_e Port 1 Transmit pair negative.
A21	PCIE1_RX+	NC	-	NC, PCl_e Port 1 Receive pair positive.
B21	GND	GND	Power	Ground.
A22	PCIE1_RX-	NC	-	NC, PCl_e Port 1 Receive pair negative.
B22	GND	GND	Power	Ground.
A23	GND	GND	Power	Ground.
B23	PCIE2_TX+	NC	-	NC, PCl_e Port 2 Transmit pair positive.
A24	GND	GND	Power	Ground.
B24	PCIE2_TX-	NC	-	NC, PCl_e Port 2 Transmit pair negative.
A25	PCIE2_RX+	NC	-	NC, PCl_e Port 2 Receive pair positive.
B25	GND	GND	Power	Ground.
A26	PCIE2_RX-	NC	-	NC, PCl_e Port 2 Receive pair negative.
B26	GND	GND	Power	Ground.
A27	GND	GND	Power	Ground.
B27	PCIE3_TX+	NC	-	NC, PCl_e Port 3 Transmit pair positive.

Pin No	Pin Name	Signal Name	Signal Type/ Termination	Description
A28	GND	GND	Power	Ground.
B28	PCIE3_TX-	NC	-	NC, PCIe Port 3 Transmit pair negative.
A29	PCIE3_RX+	NC	-	NC, PCIe Port 3 Receive pair positive.
B29	GND	GND	Power	Ground.
A30	PCIE3_RX-	NC	-	NC, PCIe Port 3 Receive pair negative.
B30	RSVD	NC	-	NC, Reserved Pin.
A31	GND	GND	Power	Ground.
B31	PRSENT3#	NC	-	NC.
A32	RSVD	NC	-	NC, Reserved Pin.
B32	GND	GND	Power	Ground.

If the 6th bit of Board configuration switch is set to OFF position, then PCIe channel0 of Qseven MXM connector is connected to Mini PCIe connector which is physically located at the bottom of the board as shown below.

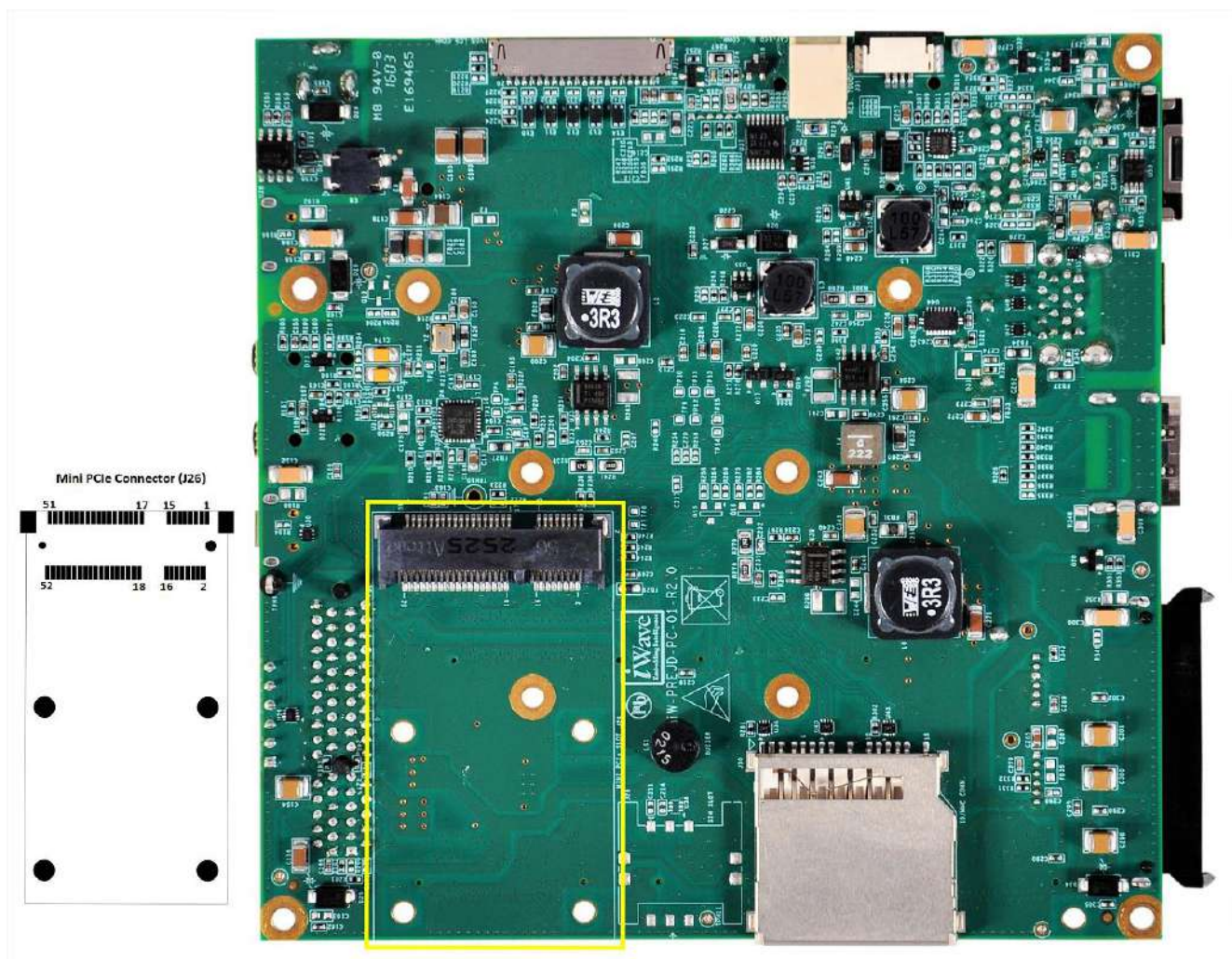


Figure 10: Mini PCIe Connector

Table 8: Mini-PCle Connector Pin Out

Pin No	Pin Name	Signal Name	Signal Type/ Termination	Description
1	PCle_WAKE	GPIO_PcLe_WAKE(GP2_14)	O, 3.3V CMOS	PCle WAKE#.
2	+3.3V_aux	VPCle_3V3	O, 3.3V Power	3.3V Supply Voltage.
3	COEX1	NC.	-	NC.
4	GND	GND	Power	Ground.
5	COEX2	NC.	-	NC.
6	1.5V	VCC_1V5	O, 1.5V Power	1.5V Supply Voltage.
7	CLK_REQ#	CLK_REQ#	O, 3.3V CMOS	Used to enable PCle Clock.
8	UIM_PWR	NC.	-	NC.
9	GND	GND	Power	Ground.
10	UIM_DATA	NC.	-	NC.
11	REFCLK-	PCle_REFCLK_DM	O, DIFF	PCle Clock negative.
12	UIM_CLK	NC.	-	NC.
13	REFCLK+	PCle_REFCLK_DP	O, DIFF	PCle Clock positive.
14	UIM_RESET	NC.	-	NC.
15	GND	GND	Power	Ground.
16	UIM_VPP	NC.	-	NC.
17	RESERVED	NC.	-	NC.
18	GND	GND	Power	Ground.
19	RESERVED	NC.	-	NC.
20	W_DISABLE#	Q7_GPIO1_(GP0_25)	O, 3.3V CMOS	Wireless Disable. <i>Note: This pin is also connected to Expansion connector3 (J14) 34th Pin through resistor and default populated.</i>
21	GND	GND	Power	Ground.
22	PERST#	GPIO_PcLe_RST/MD4(GP4_31)	O, 3.3V CMOS	PCle Reset.
23	PCIE0_RX-	PCle1_RXN	I, DIFF	PCle Channel0 Receive pair negative.
24	+3.3V_aux	VPCle_3V3	O, 3.3V Power	3.3V Supply Voltage.
25	PCIE0_RX+	PCle1_RXP	I, DIFF	PCle Channel0 Receive pair positive.
26	GND	GND	Power	Ground.
27	GND	GND	Power	Ground.
28	1.5V	VCC_1V5	O, 1.5V Power	1.5V Supply Voltage.
29	GND	GND	Power	Ground.
30	SMB_CLK	I2C0_SCL	O, 3.3V CMOS	SMB Clock.
31	PCIE0_TX-	PCle1_TXN	O, DIFF	PCle Channel0 Transmit pair negative.
32	SMB_DATA	I2C0_SDA	IO, 3.3V CMOS	SMB DATA.
33	PCIE0_TX+	PCle1_TXP	O, DIFF	PCle Channel0 Transmit pair positive.
34	GND	GND	Power	Ground.
35	GND	GND	Power	Ground.
36	USB_D-	NC.	-	NC.
37	GND	GND	Power	Ground.

Pin No	Pin Name	Signal Name	Signal Type/ Termination	Description
38	USB_D+	NC.	-	NC.
39	+3.3V_aux	VPCle_3V3	O, 3.3V Power	3.3V Supply Voltage.
40	GND	GND	Power	Ground.
41	+3.3V_aux	VPCle_3V3	O, 3.3V Power	3.3V Supply Voltage.
42	LED_WWAN#	LED_WWAN#	O, 3.3V CMOS	Connected to D4 Green LED cathode.
43	GND	GND	Power	Ground.
44	LED_WLAN#	LED_WLAN#	O, 3.3V CMOS	Connected to D5 Green LED cathode.
45	RESERVED	NC.	-	NC.
46	LED_WPAN#	LED_WPAN#	O, 3.3V CMOS	Connected to D3 Green LED cathode.
47	RESERVED	NC.	-	NC.
48	1.5V	VCC_1V5	O, 1.5V Power	1.5V Supply Voltage.
49	RESERVED	NC.	-	NC.
50	GND	GND	Power	Ground.
51	RESERVED	NC.	-	NC.
52	+3.3V_aux	VPCle_3V3	O, 3.3V Power	3.3V Supply Voltage.

2.6.3 SATA Channel0 Port (Optional)

The RZ/G1H Qseven carrier board supports one 22Pin SATA connector for SATA channel0 interface. If Qseven SOM supports SATA channel0, then it can be tested through this 22pin SATA connector (J25). The RZ/G1H Qseven SOM doesn't support SATA channel0 interface by default and it is only the optional feature.

The RZ/G1H Qseven Carrier board also supports SATA activity Green LED (D20) on board for SATA activity indication. This 22Pin SATA connector is physically located at the top of the board as shown below.

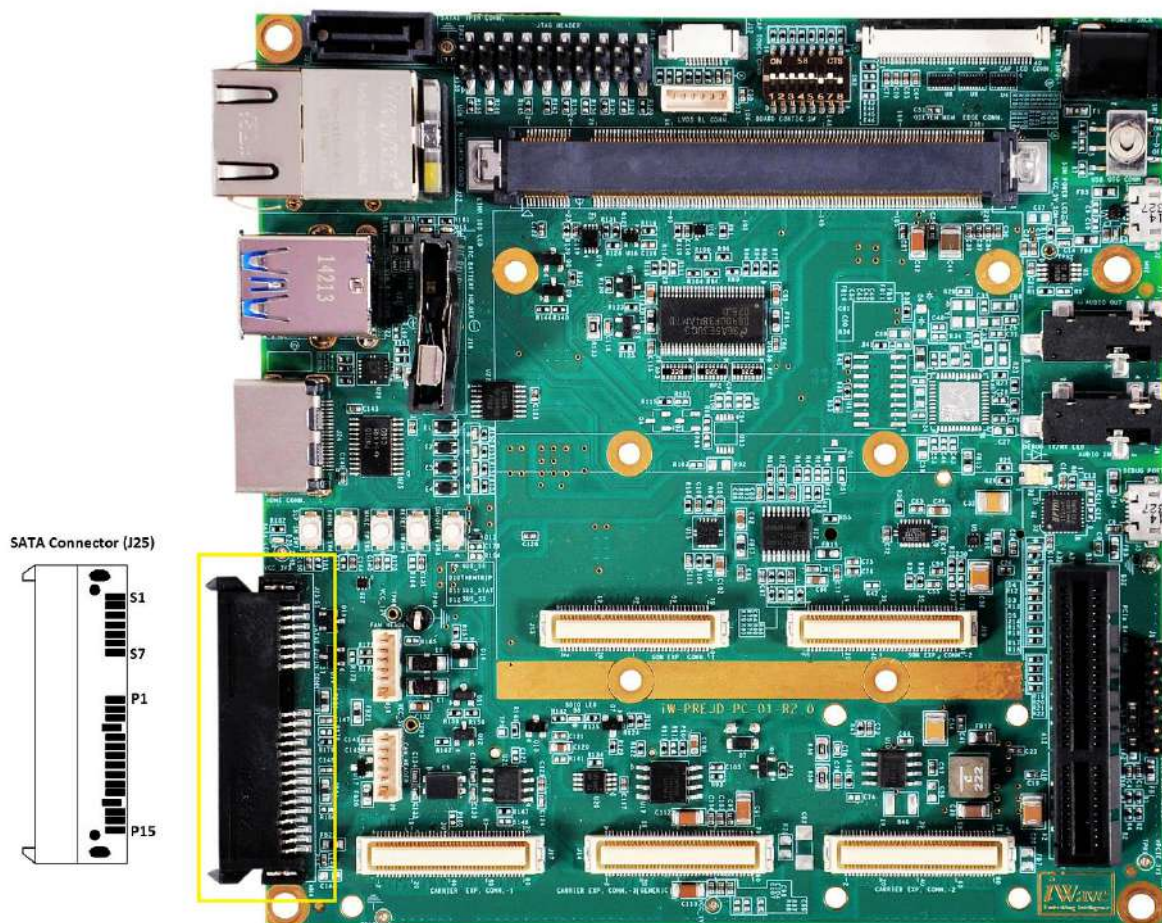


Figure 11: SATA Connector

Table 9: SATA Connector Pin Out

Pin No	Pin Name	Signal Name	Signal Type/ Termination	Description
S1	GND	GND	Power	Ground.
S2	SATA1_TXP	SATA1_TXP	O, DIFF	SATA Transmit Differential pair positive.
S3	SATA1_TXN	SATA1_TXN	O, DIFF	SATA Transmit Differential pair negative.
S4	GND	GND	Power	Ground.
S5	SATA1_RXN	SATA1_RXN	I, DIFF	SATA Receive Differential pair negative.
S6	SATA1_RXP	SATA1_RXP	I, DIFF	SATA Receive Differential pair positive.
S7	GND	GND	Power	Ground.
P1	V33	VCC_3V3	O, 3.3V Power	3.3V Supply Voltage.
P2	V33	VCC_3V3	O, 3.3V Power	3.3V Supply Voltage.
P3	V33	VCC_3V3	-	NC.
P4	GND	GND	Power	Ground.
P5	GND	GND	Power	Ground.
P6	GND	GND	Power	Ground.
P7	V5	VCC_5V	O, 5V Power	5V Supply Voltage.
P8	V5	VCC_5V	O, 5V Power	5V Supply Voltage.
P9	V5	VCC_5V	O, 5V Power	5V Supply Voltage.
P10	GND	GND	Power	Ground.
P11	DAS_DSS	NC	-	NC.
P12	GND	GND	Power	Ground.
P13	V12	VCC_12V	O, 12V Power	12V Supply Voltage.
P14	V12	VCC_12V	O, 12V Power	12V Supply Voltage.
P15	V12	VCC_12V	O, 12V Power	12V Supply Voltage.

2.7 Communication Interface Features

2.7.1 Gigabit Ethernet Port

The RZ/G1H Qseven carrier board supports Ethernet interface through RZ/G1H CPU's EtherAVB interface which supports 100/1000Mbps Ethernet. The Ethernet PHY output signals from Qseven MXM connector is directly connected to RJ45 Magjack (J22). Also it supports Speed (Yellow) and Link/Activity (Green) LED indications on RJ45 Magjack. This RJ45 Magjack combo connector is physically located at the top of the board as shown below.

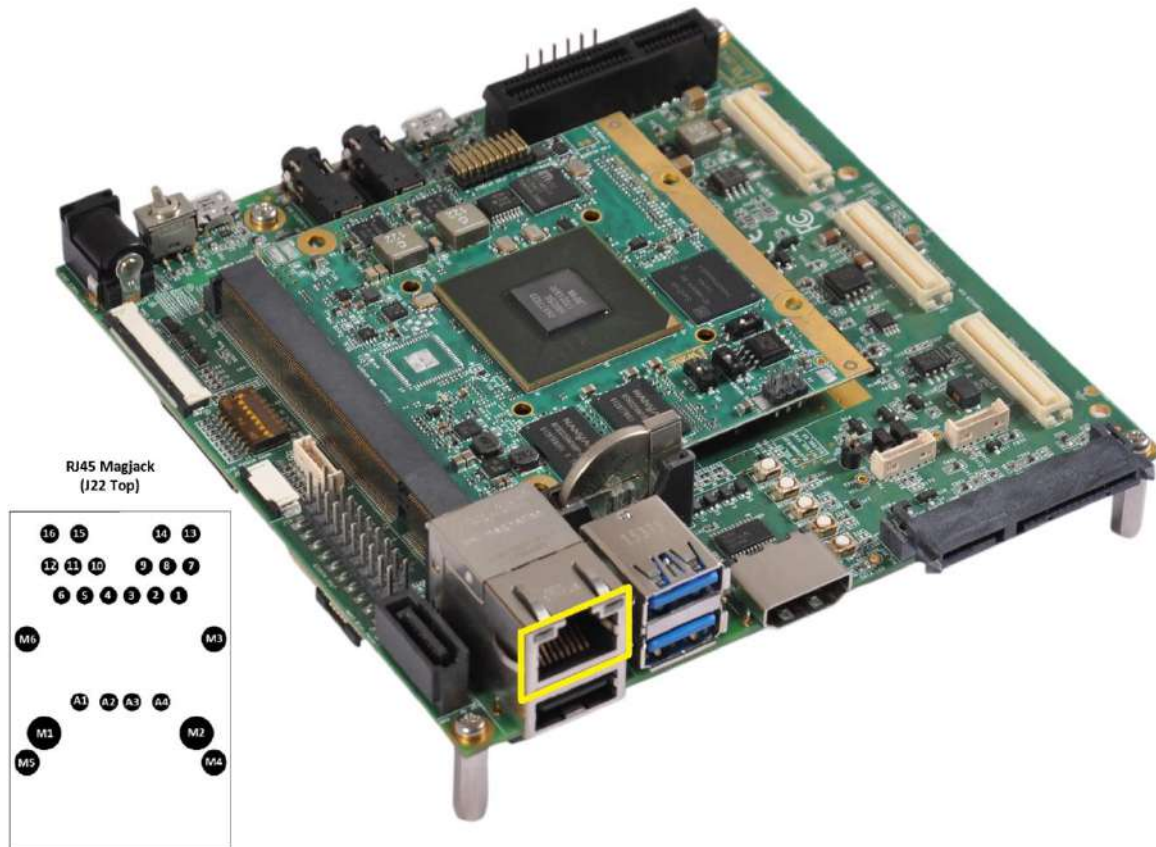


Figure 12: RJ45 Magjack

Important Note: RZ/G1H CPU's EtherAVB interface doesn't support 10Mbps speed.

Table 10: RJ45 MagJack Pin Out

Pin No	Pin Name	Signal Name	Signal Type/ Termination	Description
1	CT3	TRCT3	-	Transformer Centre Tap 3.
2	TRX2-	GPHY_CTXXRM	IO, DIFF	Gigabit Ethernet MDI differential pair 2 negative.
3	TRX2+	GPHY_CTXXRP	IO, DIFF	Gigabit Ethernet MDI differential pair 2 positive.
4	TRX1+	GPHY_BTXXRP	IO, DIFF	Gigabit Ethernet MDI differential pair 1 positive.
5	TRX1-	GPHY_BTXXRM	IO, DIFF	Gigabit Ethernet MDI differential pair 1 negative.
6	CT2	TRCT2	-	Transformer Centre Tap 2.
7	CT4	TRCT4	-	Transformer Centre Tap 4.
8	TRX3+	GPHY_DTXRXP	IO, DIFF	Gigabit Ethernet MDI differential pair 3 positive.
9	TRX3-	GPHY_DTXRXM	IO, DIFF	Gigabit Ethernet MDI differential pair 3 negative.
10	TRX0-	GPHY_ATXXRM	IO, DIFF	Gigabit Ethernet MDI differential pair 0 negative.
11	TRX0+	GPHY_ATXXRP	IO, DIFF	Gigabit Ethernet MDI differential pair 0 positive.
12	CT1	TRCT1	-	Transformer Centre Tap 1.
13	LED-Y_K	GPHY_ACTIVITY_LED1	I, 3.3V CMOS	Gigabit Ethernet Speed indication Yellow LED Cathode.
14	LED-Y_A	LED-Y_A	I, 3.3V Power	Gigabit Ethernet Speed indication Yellow LED Anode.
15	LED-GO_K	GPHY_LINK_LED2	I, 3.3V CMOS	Gigabit Ethernet Link/Activity indication Green LED Cathode.
16	LED-GO_A	LED-GO_A	I, 3.3V Power	Gigabit Ethernet Link/Activity indication Green LED Anode.

2.7.2 USB2.0 Ports (Host)

The RZ/G1H Qseven carrier Board supports three USB2.0 High Speed Host interface. The RZ/G1H CPU's USB1 interface is expanded to dual USB host ports through USB HUB on RZ/G1H Qseven SOM and available in USB2.0 Port0 and Port3 signals of Qseven MXM connector. These two USB2.0 Port0 and Port3 host ports from the Qseven MXM connector is directly connected to USB2.0 TypeA combo connector (J22) and top port of dual stack USB3.0 TypeA connector (J23) respectively.

The VBUS power of USB2.0 Port0 connector is connected through current limit power switches which limits the current above 500mA. If connected USB2.0 device takes more than 500mA current, this power switch limits the current to constant mode and sends the over current indication signal to the over current indicator pin of Qseven MXM connector USB port 0 & 1 (86th Pin).

The VBUS power of USB2.0 Port3 connector is connected through current limit power switches which limits the current above 1000mA. If connected USB2.0 device takes more than 1000mA current, this power switch limits the current to constant mode and sends the over current indication signal to the over current indicator pin of Qseven MXM connector USB port 2 & 3 (85th Pin).

Note: RZ/G1H CPU's USB2 interface which is connected to USB2.0 Port2 of Qseven MXM connector in RZ/G1H SOM is directly connected to bottom port of dual stack USB3.0 TypeA connector (J23).

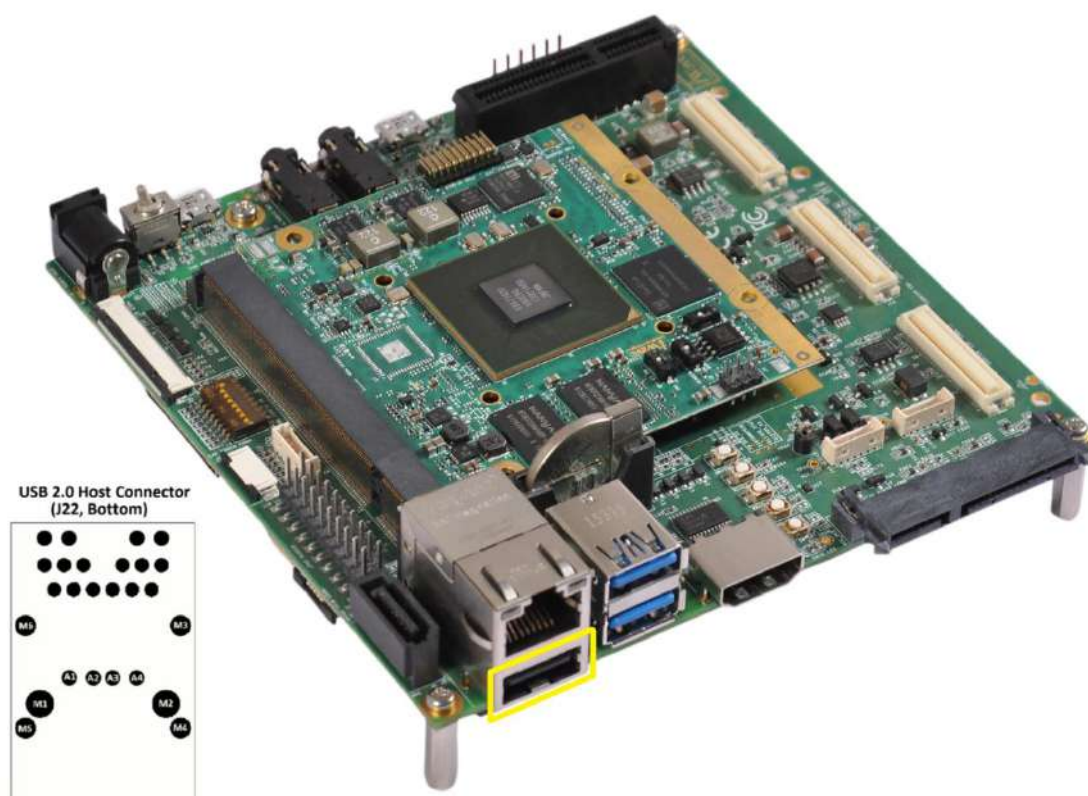


Figure 13: USB2.0 Port0 (Host)

Table 11: USB2.0 Port0 (Host) Connector Pin Out

Pin No	Pin Name	Signal Name	Signal Type/ Termination	Description
A1	VCC_5V	V_HOST	O, 5V Power	5V Supply Voltage.
A2	USB_DM	USB_HUB10U T_DM	IO, DIFF	USB Host Port0 data negative of Qseven MXM connector.
A3	USB_DP	USB_HUB10U T_DP	IO, DIFF	USB Host Port0 data positive of Qseven MXM connector.
A4	GND	GND	Power	Ground.

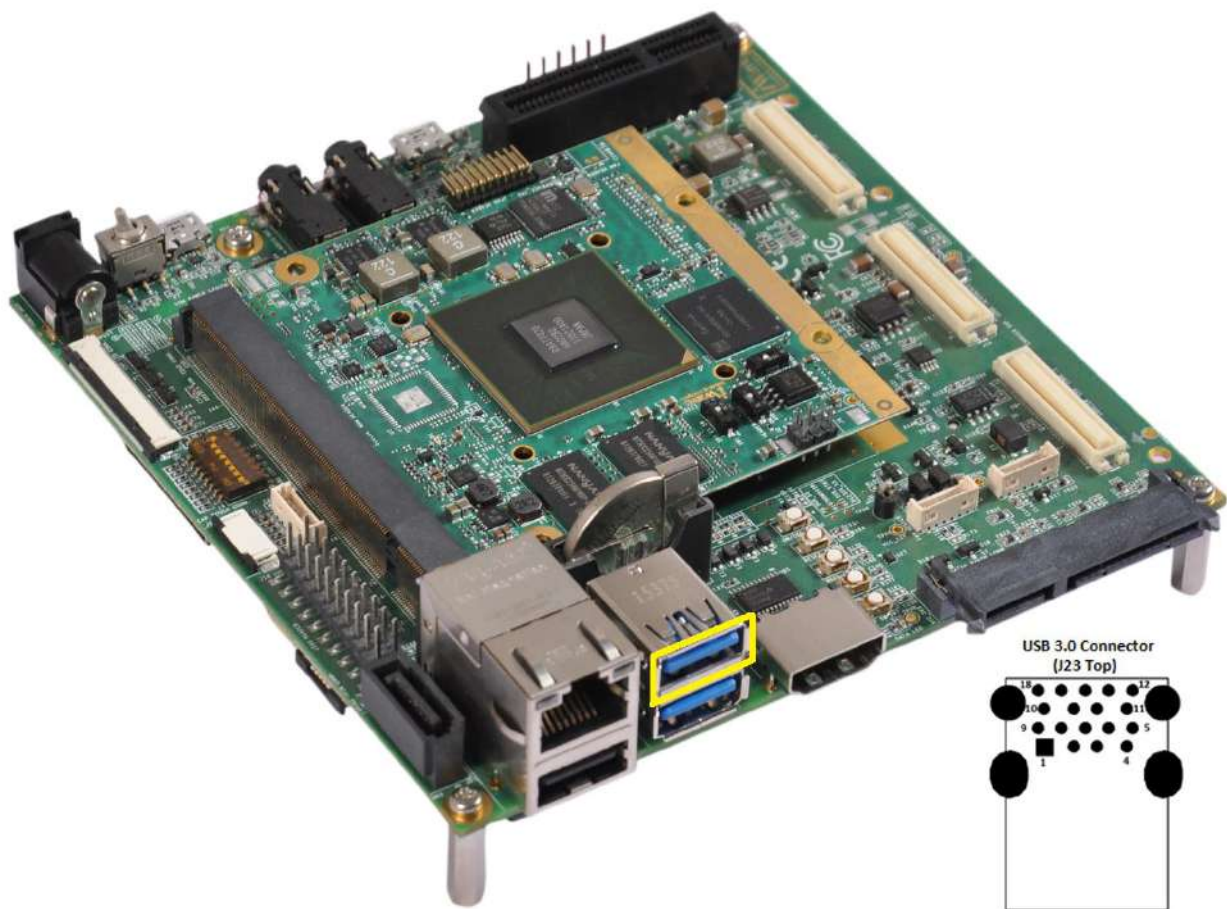


Figure 14: USB2.0 Port3 (Host)

Table 12: Dual stack USB 3.0 Connector Pin Out (Top port)

Pin No	Pin Name	Signal Name	Signal Type/ Termination	Description
10	VCC_5V	VBUS	O, 5V Power	5V Supply Voltage.
11	USB_DM	USB_HUB2OUT_D M	IO, DIFF	USB2.0 Host Port3 data negative of Qseven MXM connector.
12	USB_DP	USB_HUB2OUT_DP	IO, DIFF	USB2.0 Host Port3 data positive of Qseven MXM connector.
13	GND	GND	Power	Ground.

Pin No	Pin Name	Signal Name	Signal Type/ Termination	Description
14	USB_RXN	NC	-	NC.
15	USB_RXP	NC	-	NC.
16	GND	GND	Power	Ground.
17	USB_TXN	NC	-	NC.
18	USB_TXP	NC	-	NC.

2.7.3 USB2.0 Port1 (OTG)

The RZ/G1H Qseven carrier Board supports USB2.0 High Speed OTG interface through RZ/G1H CPU's USB0 interface. This USB2.0 Port1 signals of Qseven MXM connector is directly connected to USB2.0 MicroAB connector (J2). This port can be used as USB OTG functionality which supports USB host and USB device based on USB ID pin status. This USB ID pin is also connected to DIP switch (SW2) 8th position and can be used to force this port as USB host alone by setting to ON position. When the DIP switch (SW2) 8th position is OFF position, either Host or device functionality can be set based on the USB ID pin status.

The VBUS power of this USB2.0 connector is connected through current limit power switch which can be used to switch On/Off the power based on the device or Host and also limits the current above 500mA in host mode. The connected Qseven SOM detects the USB functionality through USB ID pin and controls the power using the USB_DRIVE_VBUS pin (56th pin) of Qseven MXM connector. In Host mode, USB_DRIVE_VBUS should drive high to enable the power to the connector and in device mode, USB_DRIVE_VBUS should drive low to disable the power to the connector.

If connected USB2.0 device takes more than 500mA current, current limit power switch limits the current to constant mode and sends the over current indication signal to the over current indicator pin of Qseven MXM connector USB port 0 & 1. This USB2.0 OTG connector is physically located at the top of the board as shown below.

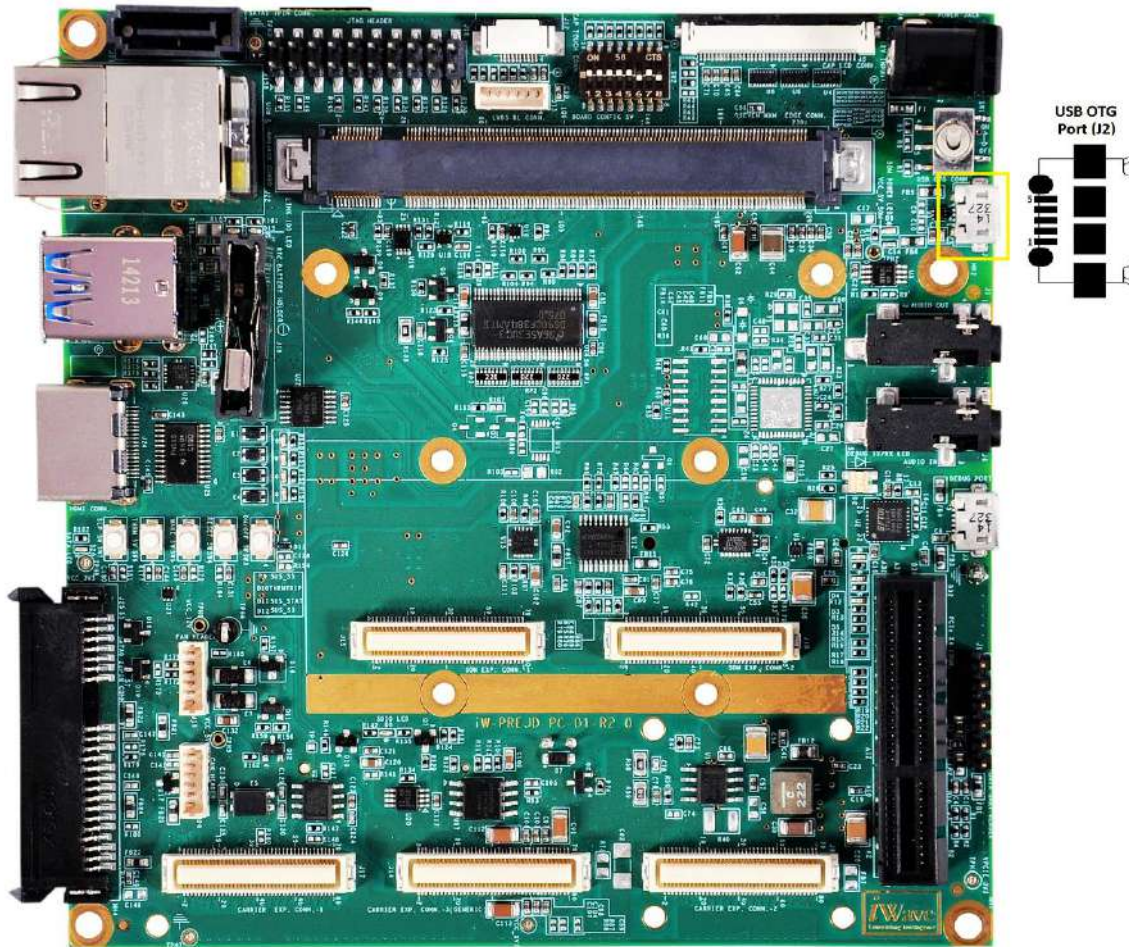


Figure 15: USB2.0 Port1 (OTG)

Table 13: USB2.0 Port1 (OTG) Connector Pin Out

Pin No	Pin Name	Signal Name	Signal Type/ Termination	Description
1	VCC_5V	V_OTG	I, 5V Power	5V Supply Voltage.
2	USB_DM	USB_P1-	IO, DIFF	USB2.0 OTG Port1 data negative.
3	USB_DP	USB_P1+	IO, DIFF	USB2.0 OTG Port1 data positive.
4	USB_ID	GPIO_USBOTG_ID(GP5_20)	O, 3.3V CMOS	USD OTG ID signal.
5	GND	GND	Power	Ground.

2.7.4 SDIO Port

The RZ/G1H Qseven Carrier Board supports SDIO interface through RZ/G1H CPU's SDHI2 interface. This SDHI2 signals from Qseven MXM connector is connected to SD/MMC connector (J30) to support Standard SD interface. This connector supports up to 4-bit data transfer with card detect and write protect. Also it supports SDIO activity Green LED (D8) on board for SDIO bus transfer indication.

The main power to SD/MMC connector is 3.3V and it is connected through power switch to support power enable/disable feature. This power enable/disable is controlled from the SDIO_PWR# pin of Qseven MXM connector. This SD/MMC connector (J30) is physically located at the bottom of the board as shown below.

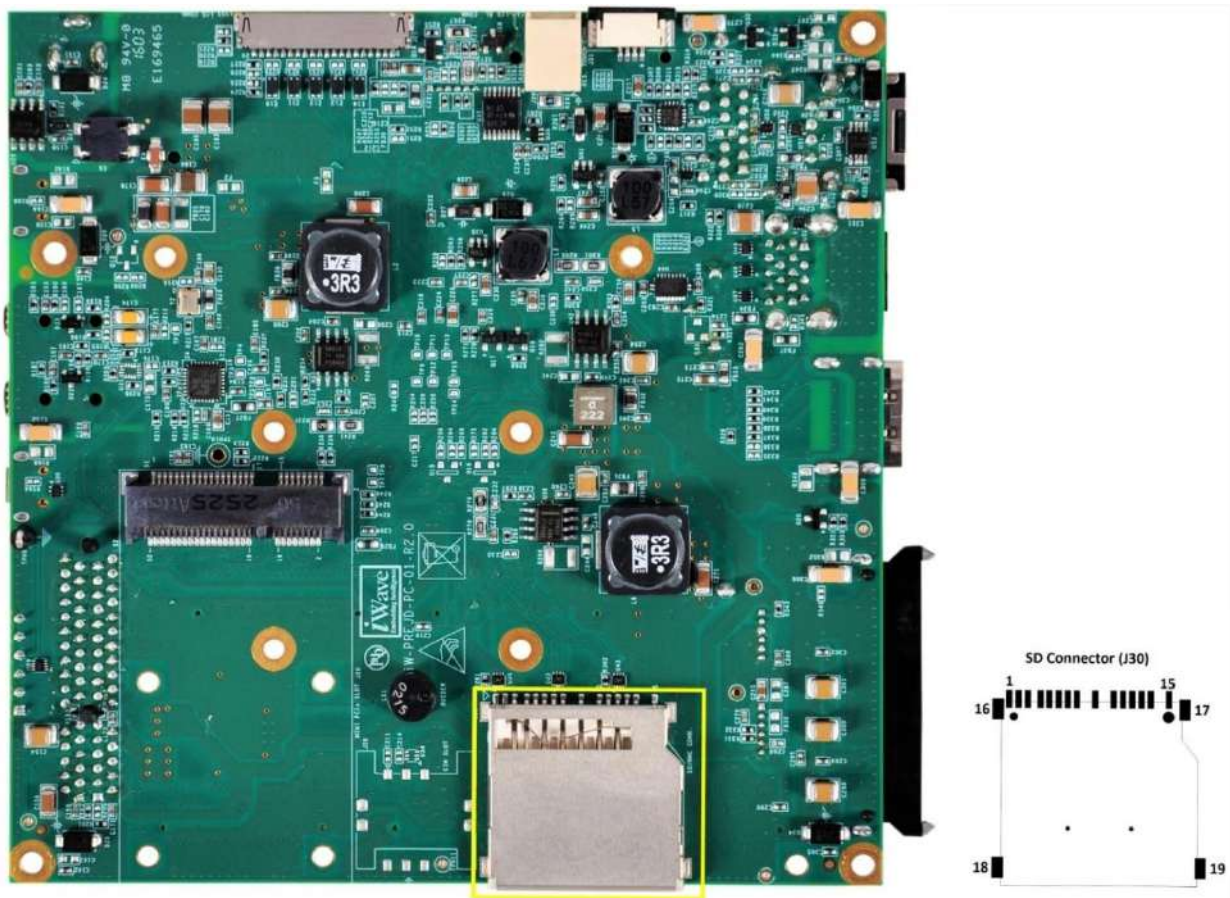


Figure 16: SD/MMC Connector

Table 14: SD/MMC Connector Pin Out

Pin No	Pin Name	Signal Name	Signal Type/ Termination	Description
1	SD_WP	SD2_WP(GP3_23)	I, 1.8/3.3V CMOS/ 10K PU	SD/MMC Interface Write Protect.
2	SD_CD	SD2_CD(GP3_22)	I, 1.8/3.3V CMOS/ 10K PU	SD/MMC Interface Card Detect.
3	SD_DATA1	SD2_DAT1(GP3_19)	IO, 1.8/3.3V CMOS	SD/MMC Interface Data Line1.
4	SD_DATA0	SD2_DAT0(GP3_18)	IO, 1.8/3.3V CMOS	SD/MMC Interface Data Line0.
5	SD_DATA7	NC	-	NC in RZ/G1H carrier board. <i>Note: This pin is connected from Qseven MXM connector 54th pin.</i>
6	GND	GND	Power	Ground.
7	SD_DATA6	NC	-	NC in RZ/G1H carrier board. <i>Note: This pin is connected from Qseven MXM connector 55th pin.</i>
8	SD_CLK	SD2_CLK(GP3_16)	O, 1.8/3.3V CMOS	SD/MMC Interface Clock.
9	VCC_3V	VCC/VDD	O,3.3V Power	3.3V Supply Voltage.
10	GND	GND	Power	Ground.
11	SD_DATA5	NC	-	NC in RZ/G1H carrier board. <i>Note: This pin is connected from Qseven MXM connector 52nd pin.</i>
12	SD_CMD	SD2_CMD(GP3_17)	IO, 1.8/3.3V CMOS	SD/MMC Interface Command Line.
13	SD_DATA4	NC	-	NC in RZ/G1H carrier board. <i>Note: This pin is connected from Qseven MXM connector 53rd pin.</i>
14	SD_DATA3	SD2_DAT3(GP3_21)	IO, 1.8/3.3V CMOS	SD/MMC Interface Data Line3.
15	SD2_DATA2	SD2_DAT2(GP3_20)	IO, 1.8/3.3V CMOS	SD/MMC Interface Data Line2.

2.7.5 CAN Header

The RZ/G1H Qseven Carrier Board supports CAN interface through RZ/G1H CPU's CAN1 interface. This CAN1 interface signals from Qseven MXM connector (pins 129th & 130th) is connected to CAN Bus transceiver "SN65HVD230DR" and to 6pin custom CAN header (J20). Mode select pin (Rs) of the CAN Bus transceiver is connected to GPIO4 (189th Pin) of the Qseven MXM connector. This CAN header is physically located at the top of the board as shown below.

Number of Pins : 6

Connector Part number : 53047-0610 from Molex

Mating Connector : 0510210600 from Molex with crimping pins

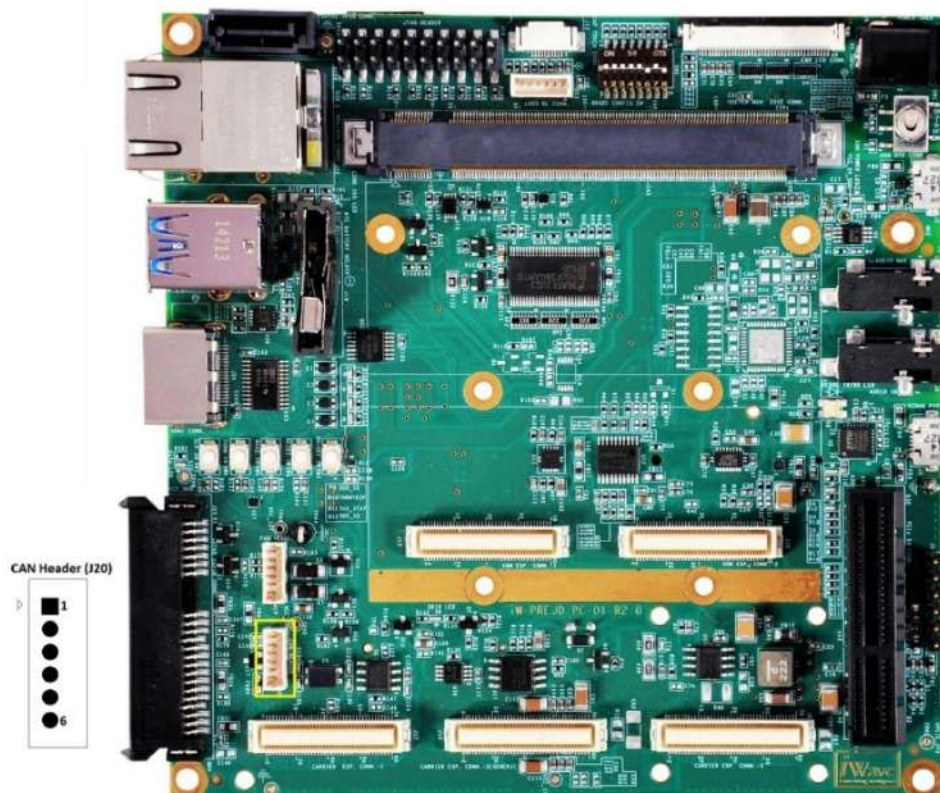


Figure 17: CAN Header

Table 15: CAN Header Pin Out

Pin No	Pin Name	Signal Name	Signal Type / Termination	Description
1	VCC_5V	VCC_5V_CAN	O, 5V Power	5V Supply Voltage.
2	VCC_12V	NC	-	NC. <i>Note: Optionally connected to on board 12V through resistor and not populated.</i>
3	CANL	CANL	IO, DIFF	CAN Differential negative.
4	GND	GND	Power	Ground.
5	CANH	CANH	IO, DIFF	CAN Differential positive.
6	GND	GND	Power	Ground.

2.8 Audio/Video Features

2.8.1 Audio IN & OUT

The RZ/G1H Qseven carrier board supports Audio In and Out through RZ/G1H CPU's SSI3/4 interface which can support I2S format. This four wire I2S signals from Qseven MXM connector is connected to I2S Audio Codec "SGTL5000" to support Headphone Stereo output and Mono Mic input which is supported through 3.5mm Jack J5 and J6 correspondingly. Also Headphone detect and Mic detect is supported through Qseven MXM connector pins GPIO3 (188th Pin) & GPIO2 (187th Pin) correspondingly. These Audio Jacks are physically located at the top of the board as shown below.

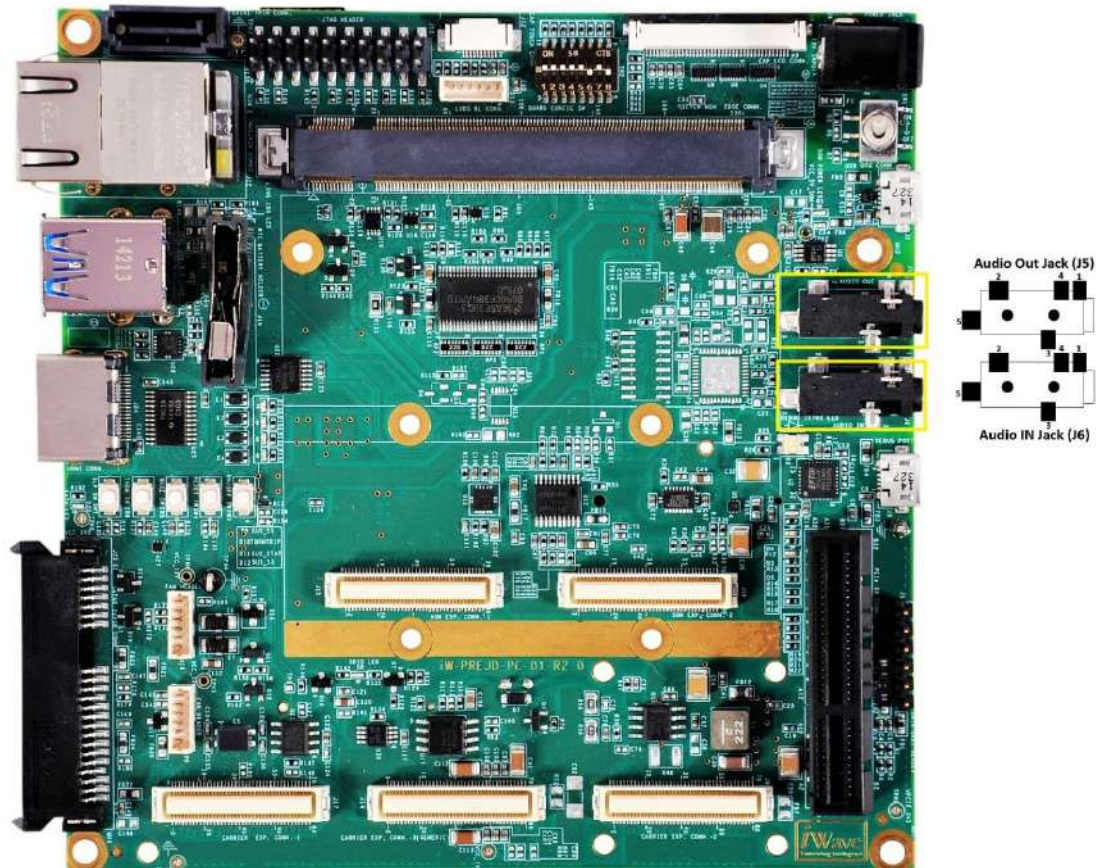


Figure 18: Audio IN/OUT Jack

Table 16: Audio OUT Jack Pin Out

Pin No	Pin Name	Signal Name	Signal Type / Termination	Description
1	AGND	GND_SIGNAL	Power	Analog Ground.
2	HP_Left	HP_L	O, Analog	Headphone Output Left.
3	HP_Right	HP_R	O, Analog	Headphone Output Right.
4	HP_Detect	Q7_GPIO3_(GP4_19)	I, 3.3V CMOS/ 10K PU	Headphone detect Signal.
5	NC	NC	-	NC.

Table 17: Audio IN Jack Pin Out

Pin No	Pin Name	Signal Name	Signal Type / Termination	Description
1	AGND	GND_SIGNAL	Power	Analog Ground.
2	MIC	MIC	I, Analog	Microphone Input Signal.
3	NC	NC	-	NC.
4	MIC_Detect	Q7_GPIO2_(GP0_26)	I, 3.3V CMOS/ 10K PU	Microphone detect Signal.
5	NC	NC	-	NC.

2.8.2 7" LCD with Capacitive Touch

The RZ/G1H Qseven carrier board supports 7inch, 18bpp RGB LCD “ETM070001ADH6” from Emerging Display Technologies Corporation (EDT) with capacitive touch panel. RZ/G1H CPU’s LVDS0 port is connected to primary LVDS channel of Qseven MXM connector. This primary LVDS interface signals are directly connected to LVDS transmitter (DS90CF384A) in carrier board which converts LVDS Interface signals to RGB and connects to RGB LCD connector (J8). This RGB LCD connector (J8) is physically located at the top of board as shown below.

This RGB LCD’s power enable and backlight enable is connected from LVDS_PPEN (111th pin) & LVDS_BLEN (112th pin) of Qseven MXM connector which is RZ/G1H CPU’s GPIO pins “GP5_28” and “GP3_11” respectively. Also, RGB LCD’s brightness is controlled from LVDS_BLT_CTRL (123rd pin) of Qseven MXM connector which is RZ/G1H CPU’s TPU0TO2(GP0_22).

Note In RZ/G1H carrier board, LVDS brightness control GPIO from Qseven MXM connector (123rd Pin) is shared to both primary & secondary LCD’s brightness control.

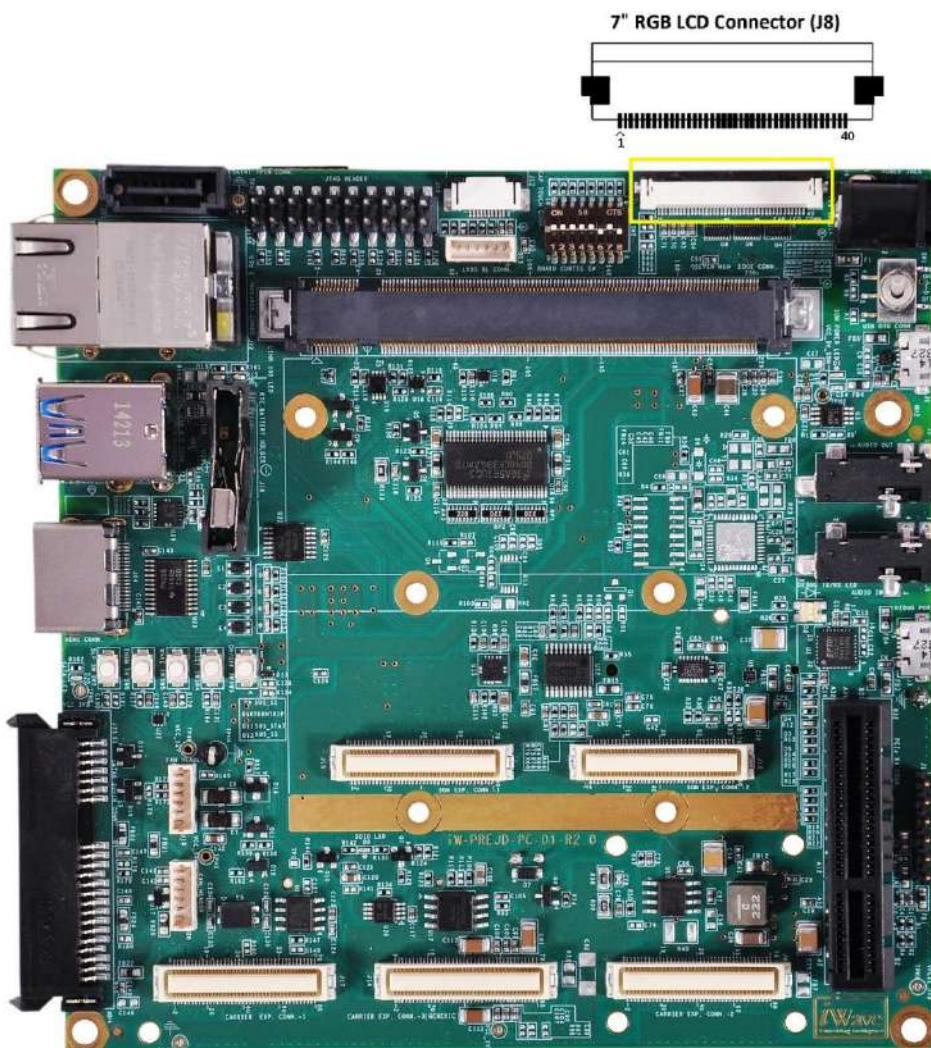


Figure 19: RGB LCD Connector

Table 18: 7" RGB LCD Connector Pin Out

Pin No	Pin Name	Signal Name	Signal Type / Termination	Description
1	U/D	U/D	O, 3.3V CMOS	Up or Down Scanning Direction.
2	L/R	L/R	O, 3.3V CMOS	Left or Right Scanning Direction.
3	NC	NC	-	-
4	VCC1	VCC1	O, 3.3V Power	3.3V Supply voltage for LED Driver Circuit.
5	VCC2	VCC2	O, 3.3V Power	3.3V Supply voltage for LED Driver Circuit.
6	VCC3	VCC3	O, 3.3V Power	3.3V Supply voltage for LED Driver Circuit.
7	VCC4	VCC4	O, 3.3V Power	3.3V Supply voltage for LED Driver Circuit.
8	NC	NC	-	-
9	DIS_DE	DIS_DE	O, 3.3V CMOS	Data Enable Output.
10	VSS1	GND	Power	Ground.
11	VSS2	GND	Power	Ground.
12	VSS3	GND	Power	Ground.
13	B5	DIS_B7	O, 3.3V CMOS	Display Blue Data 7(MSB).
14	B4	DIS_B6	O, 3.3V CMOS	Display Blue Data 6.
15	B3	DIS_B5	O, 3.3V CMOS	Display Blue Data 5.
16	VSS4	GND	Power	Ground.
17	B2	DIS_B4	O, 3.3V CMOS	Display Blue Data 4.
18	B1	DIS_B3	O, 3.3V CMOS	Display Blue Data 3.
19	B0	DIS_B2	O, 3.3V CMOS	Display Blue Data 2(LSB).
20	VSS5	GND	Power	Ground.
21	G5	DIS_G7	O, 3.3V CMOS	Display Green Data 7(MSB).
22	G4	DIS_G6	O, 3.3V CMOS	Display Green Data 6.
23	G3	DIS_G5	O, 3.3V CMOS	Display Green Data 5.
24	VSS6	GND	Power	Ground.
25	G2	DIS_G4	O, 3.3V CMOS	Display Green Data 4.
26	G1	DIS_G3	O, 3.3V CMOS	Display Green Data 3.
27	G0	DIS_G2	O, 3.3V CMOS	Display Green Data 2(LSB).
28	VSS7	GND	Power	Ground.
29	R5	DIS_R7	O, 3.3V CMOS	Display Red Data 7(MSB).
30	R4	DIS_R6	O, 3.3V CMOS	Display Red Data 6.
31	R3	DIS_R5	O, 3.3V CMOS	Display Red Data 5.
32	VSS8	GND	Power	Ground.
33	R2	DIS_R4	O, 3.3V CMOS	Display Red Data 4.
34	R1	DIS_R3	O, 3.3V CMOS	Display Red Data 3.
35	R0	DIS_R2	O, 3.3V CMOS	Display Red Data 2(LSB).
36	VSS9	GND	Power	Ground.
37	NC	NC	-	-
38	CLK	DIS_CLK	O, 3.3V CMOS	DOT Data Clock.
39	HSYNC	DIS_HSYNC	O, 3.3V CMOS	Horizontal SYNC Output.
40	VSYNC	DIS_VSYNC	O, 3.3V CMOS	Vertical SYNC Output.

This RGB LCD also supports capacitive touch panel through RZ/G1H CPU's I2C2 interface which connects to capacitive touch connector (J12). The touch interrupt from capacitive touch controller is connected to GPIO0 (185th pin) of Qseven MXM connector which is RZ/G1H CPU's GPIO pin "GP0_24". This Capacitive Touch Connector (J12) is physically located at the top of board as shown below.

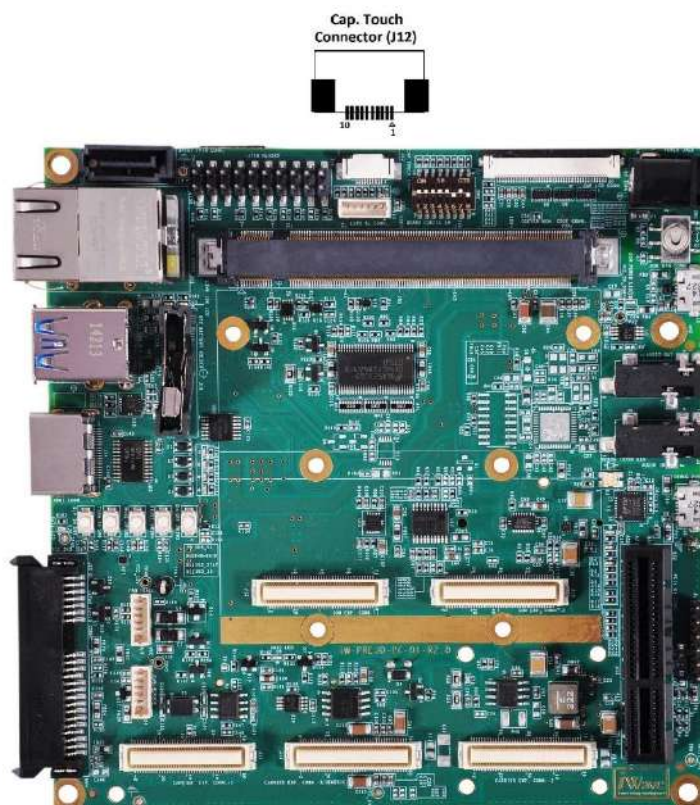


Figure 20: RGB LCD Touch Connector

Table 19: Capacitive Touch Connector Pin Out

Pin No	Pin Name	Signal Name	Signal Type / Termination	Description
1	VSS1	VSS1	Power	Ground.
2	VDD	VDD	O, 3.3V Power	3.3V Supply voltage.
3	I2C_SCL	I2C2_SCL(GP4_0)	O, 3.3V OD	I2C2 Clock Signal
4	NC	NC	-	-
5	I2C_SDA	I2C2_SDA(GP4_1)	IO, 3.3V OD	I2C2 Data Signal
6	NC	NC	-	-
7	RST	GPIO_SSI_RST(GP1_29)	O, 3.3V CMOS/ 10K PU	Touch Controller Reset.
8	WAKE#	CAP_WAKE#	O, 3.3V CMOS/ 10K PU	Wake Interrupt.
9	INT	Q7_GPIO0_(GP0_24)	I, 3.3V CMOS/ 10K PU	Touch Controller Interrupt.
10	VSS	GND	Power	Ground.

2.8.3 HDMI Port (Optional)

The RZ/G1H Qseven SOM optionally supports external HDMI transmitter through its LVDS1 display port. By default, RZ/G1H CPU's LVDS1 port is directly connected to secondary LVDS channel of the Qseven Edge connector through resistor. But have the option to isolate the LVDS1 port from the secondary LVDS channel of the Qseven Edge connector and connect to HDMI transmitter if required.

The HDMI display output from HDMI transmitter is available on the TMDS port of the Qseven MXM connector. This TMDS signals from Qseven MXM connector along with HDMI DDC clock & data is connected to HDMI connector with ESD protection circuit in the RZ/G1H HDMI carrier board.

HDMI connector (J24) is physically located on top of the board as shown below.

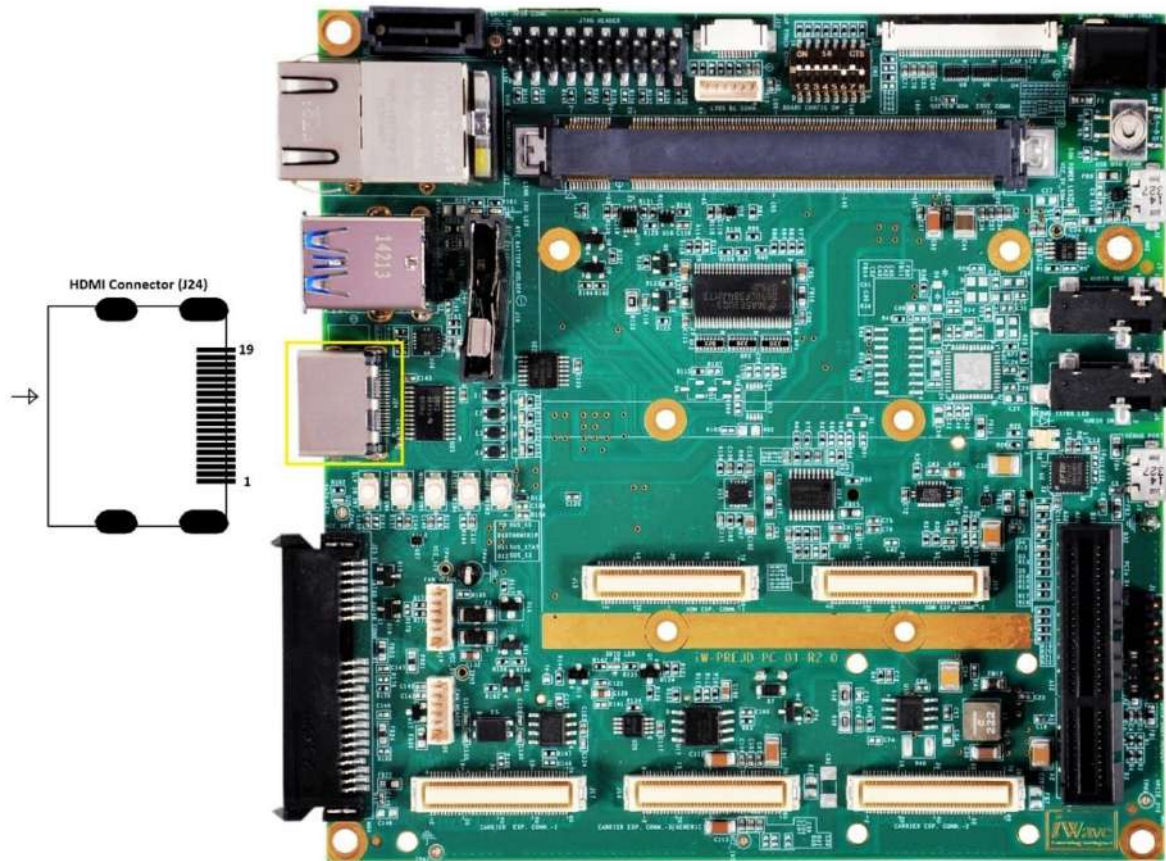


Figure 21: HDMI Connector

Table 20: HDMI Connector Pin Out

Pin No	Pin Name	Signal Name	Signal Type / Termination	Description
1	D2+	HDMI_D2P	O, TMDS	HDMI data2 pair positive.
2	D2_GND	GND	Power	Ground.
3	D2-	HDMI_D2M	O, TMDS	HDMI data2 pair negative.
4	D1+	HDMI_D1P	O, TMDS	HDMI data1 pair positive.
5	D1_GND	GND	Power	Ground.
6	D1-	HDMI_D1N	O, TMDS	HDMI data1 pair negative.
7	D0+	HDMI_D0P	O, TMDS	HDMI data0 pair positive.
8	D0_GND	GND	Power	Ground.
9	D0-	HDMI_D0N	O, TMDS	HDMI data0 pair negative.
10	CLK+	HDMI_CLKP	O, TMDS	HDMI Clock pair positive.
11	CLK_GND	GND	Power	Ground.
12	CLK-	HDMI_CLKN	O, TMDS	HDMI Clock pair negative.
13	CEC	NC	-	-
14	RSV/NC	NC	-	-
15	SCL	HDMI_CTL_CLK	O, 3.3V CMOS	EDID I2C Clock.
16	SDA	HDMI_CTL_DAT	IO, 3.3V CMOS	EDID I2C Data
17	DDC/CEC_GND	GND	Power	Ground.
18	+5V	VOUT_5	O, 5V Power	5V Supply Voltage.
19	HPD	HDMI_HPD	I, 3.3V CMOS	HDMI Cable Hot plug detect.
20	MH1, MH2, MH3, MH4	HDMI_GND	Mechanical support	Mechanical support

2.8.4 LVDS Port with Resistive Touch

The RZ/G1H Qseven carrier board can support LVDS LCD interface through RZ/G1H CPU's LVDS1 display port if LVDS1 port supported RZ/G1H SOM is used. These LVDS signals from Qseven MXM connector is directly connected to 20pin LVDS connector (J27). And LVSD LCD's power enable and backlight enable is connected from GPIO6 (191st pin) & GPIO5 (190th pin) of Qseven MXM connector which is RZ/G1H CPU's GPIO pins "GP4_2" and "GP2_17" respectively. This LVDS LCD connector (J27) is physically located at the bottom of board as shown below.

if LVDS display support is not required, then RZ/G1H SOM has the option to isolate LVDS1 port from secondary LVDS channel of the Qseven Edge connector and directly connect to HDMI transmitter, then the HDMI display output from HDMI transmitter is available on the TMDS port of the Qseven MXM connector. Thus, either HDMI display or secondary LVDS can be used at a time and by default, LVDS display is supported.

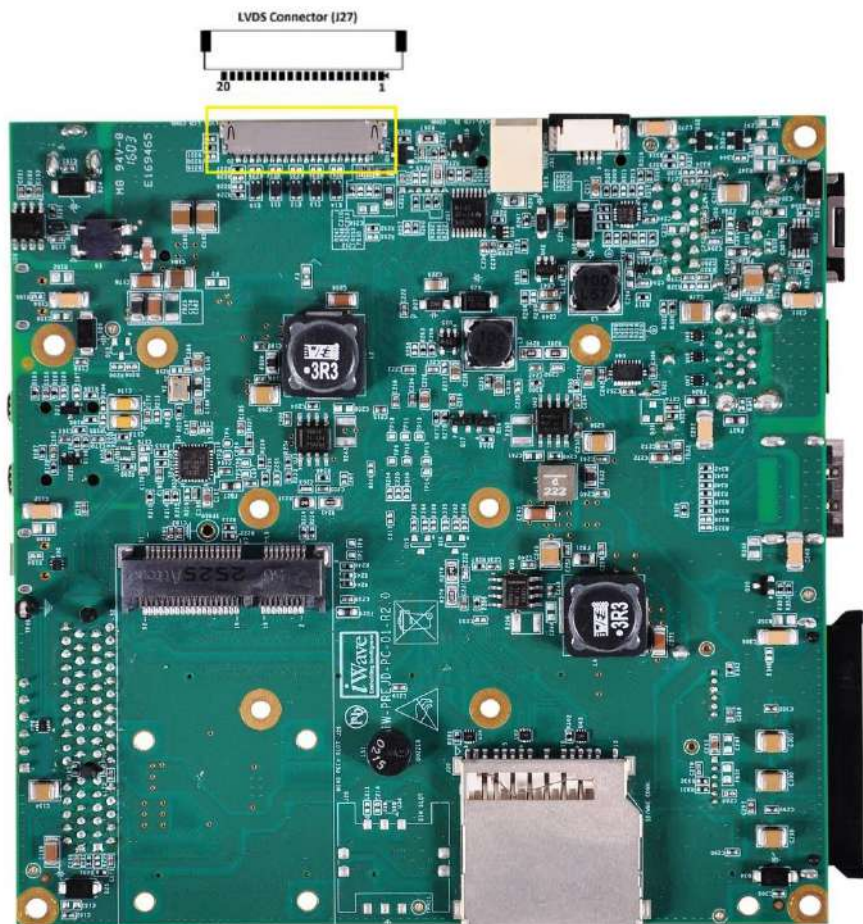


Figure 22: LVDS LCD Connector

Compatible LCDs

1. Part Number: OSD104T0571-19TS

Manufacturer Name: OSD Displays

2. Part Number: T-51944D104J-FW-A-ABN

Manufacturer Name: OPTREX Corporation

3. Part Number: TLM-TA40T3130-01

Manufacturer Name: Varitronix

Table 21 LVDS Connector

Pin No	Pin Name	Signal Name	Signal Type / Termination	Description
1	VDD1	VDD	O, 3.3V Power	3.3V Supply Voltage.
2	VDD2	VDD	O, 3.3V Power	3.3V Supply Voltage.
3	GND1	GND	Power	Ground.
4	GND2	GND	Power	Ground.
5	RIN0-	DU_LVDS1_CH0_N	O, 2.5V LVDS	LVDS secondary channel differential pair 0 negative.
6	RIN0+	DU_LVDS1_CH0_P	O, 2.5V LVDS	LVDS secondary channel differential pair 0 positive.
7	GND3	GND	Power	Ground.
8	RIN1-	DU_LVDS1_CH1_N	O, 2.5V LVDS	LVDS secondary channel differential pair 1 negative.
9	RIN1+	DU_LVDS1_CH1_P	O, 2.5V LVDS	LVDS secondary channel differential pair 1 positive.
10	GND4	GND	Power	Ground.
11	RIN2-	DU_LVDS1_CH2_N	O, 2.5V LVDS	LVDS secondary channel differential pair 2 negative.
12	RIN2+	DU_LVDS1_CH2_P	O, 2.5V LVDS	LVDS secondary channel differential pair 2 positive.
13	GND5	GND	Power	Ground.
14	CLKIN-	DU_LVDS1_CLK_N	O, 2.5V LVDS	LVDS secondary channel differential clock negative.
15	CLKIN+	DU_LVDS1_CLK_P	O, 2.5V LVDS	LVDS secondary channel differential clock positive.
16	GND6	GND	Power	Ground.
17	RIN3-	DU_LVDS1_CH3_N	O, 2.5V LVDS	LVDS secondary channel differential pair 3 negative.
18	RIN3+	DU_LVDS1_CH3_P	O, 2.5V LVDS	LVDS secondary channel differential pair 3 positive.
19	GND7	GND	Power	Ground.
20	GND8	GND	Power	Ground.

RZ/G1H Carrier board supports on board LED driver “LM3410XMF/NOPB” to drive the backlight of LVDS LCDs. This LED driver output is set as 19.2V, 120mA (per LED string) which is compatible for ISD’s “OSD104T0571-19TS” LCD and connected to LVDS LCD backlight connector (J13). Also, this LVDS LCD’s brightness is controlled from LVDS_BLT_CTRL (123rd pin) of Qseven MXM connector which is RZ/G1H CPU’s TPU0TO2(GP0_22) This backlight connector (J13) is physically located at the top of the board as shown below.

Note In RZ/G1H carrier board, LVDS brightness control GPIO from Qseven MXM connector (123rd Pin) is shared to both primary & secondary LCD’s brightness control.

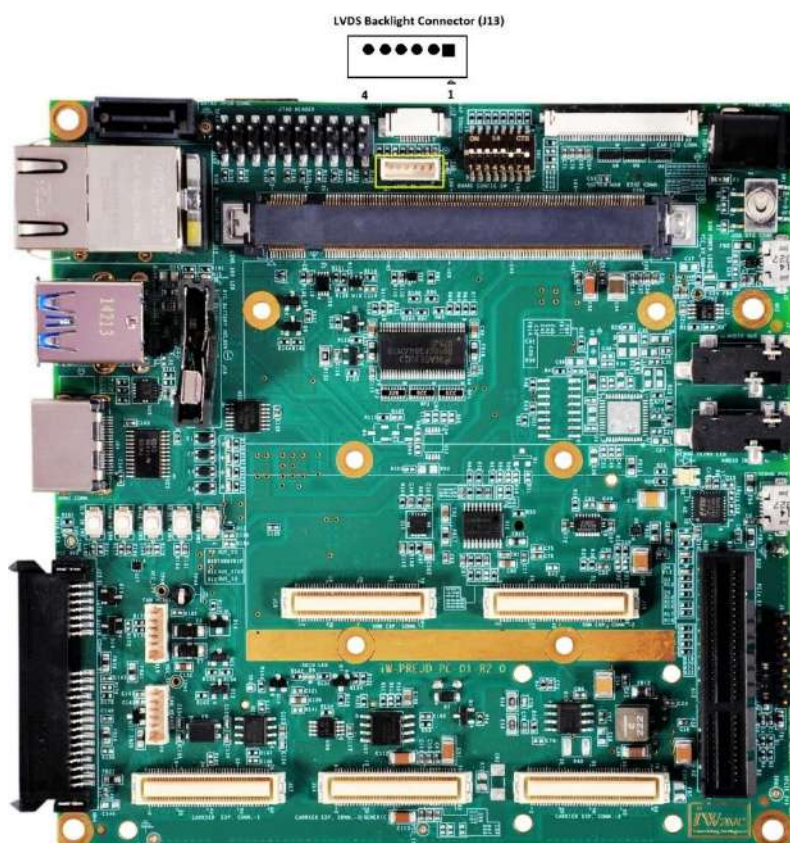


Figure 23: LVDS Backlight Connector

Table 22: LVDS Backlight Connector Pin Out

Pin No	Pin Name	Signal Name	Signal Type / Termination	Description
1	VCC_12V	VCC_12V_BL	O, 12V Power	12V Supply Voltage.
2	GND	GND	Power	Ground.
3	EN	Q7_GPIO5_(GP2_17)	O, 3.3V CMOS	LVDS Backlight Enable Output.
4	PWM	TPU0TO2/MD22(GP0_22)	O, 3.3V CMOS	LVDS Backlight control Output.
5	LED_K	V_LED_K1	O, Power	LED Cathode Voltage
6	LED_A	V_LED_A1	O, Power	LED Anode Voltage

The RZ/G1H Qseven carrier board supports STMPE811 resistive touch controller for this 2nd LVDS display port. This resistive touch controller is connected to RZ/G1H CPU through I2C2 channel. The touch interrupt from this touch controller is connected to GPIO0 (185th pin) of Qseven MXM connector which is RZ/G1H CPU's GPIO pin "GP0_24". Since touch interrupt from both capacitive touch controller and resistive touch controller is connected to same GPIO pin, either one touch interface only can be used at a time. The 4-wire resistive touch interface is available in the resistive touch connector (J31). This connector is located at the bottom of the board as shown below.

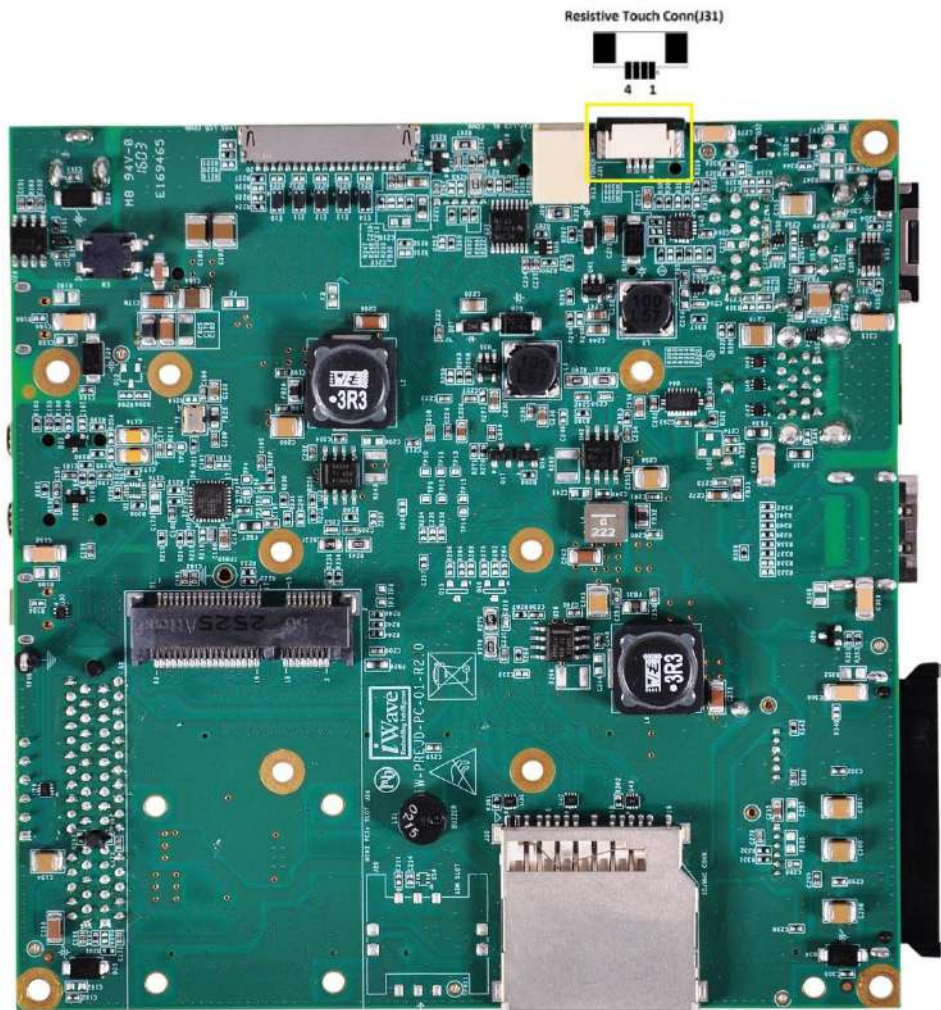


Figure 24: LVDS Resistive Touch Connector

Table 23: Resistive Touch Connector Pin Out

Pin No	Pin Name	Signal Name	Signal Type / Termination	Description
1	Y1	TSC_Y1	I, Analog	Touch Left Signals
2	X2	TSC_X2	I, Analog	Touch Down Signals
3	Y2	TSC_Y2	I, Analog	Touch Right Signals
4	X1	TSC_X1	I, Analog	Touch Up Signals

2.9 Additional Features

2.9.1 SPI Flash

The RZ/G1H Qseven carrier board supports SPI Flash through RZ/G1H CPU's MSIOF0 interface. This SPI interface signals from Qseven MXM connector is connected to SPI Flash "SST25VF016B-50" in the Qseven carrier board and operating at 3.3V Level.

2.9.2 RTC Coin Cell Holder

The RZ/G1H Qseven carrier board supports Coin Cell Holder to connect "2032" series coin cell. This coin cell voltage is connected to Qseven SOM for RTC back up voltage when VCC main power is off. This Coin Cell Holder (J18) is physically located at the top of the board as shown below.

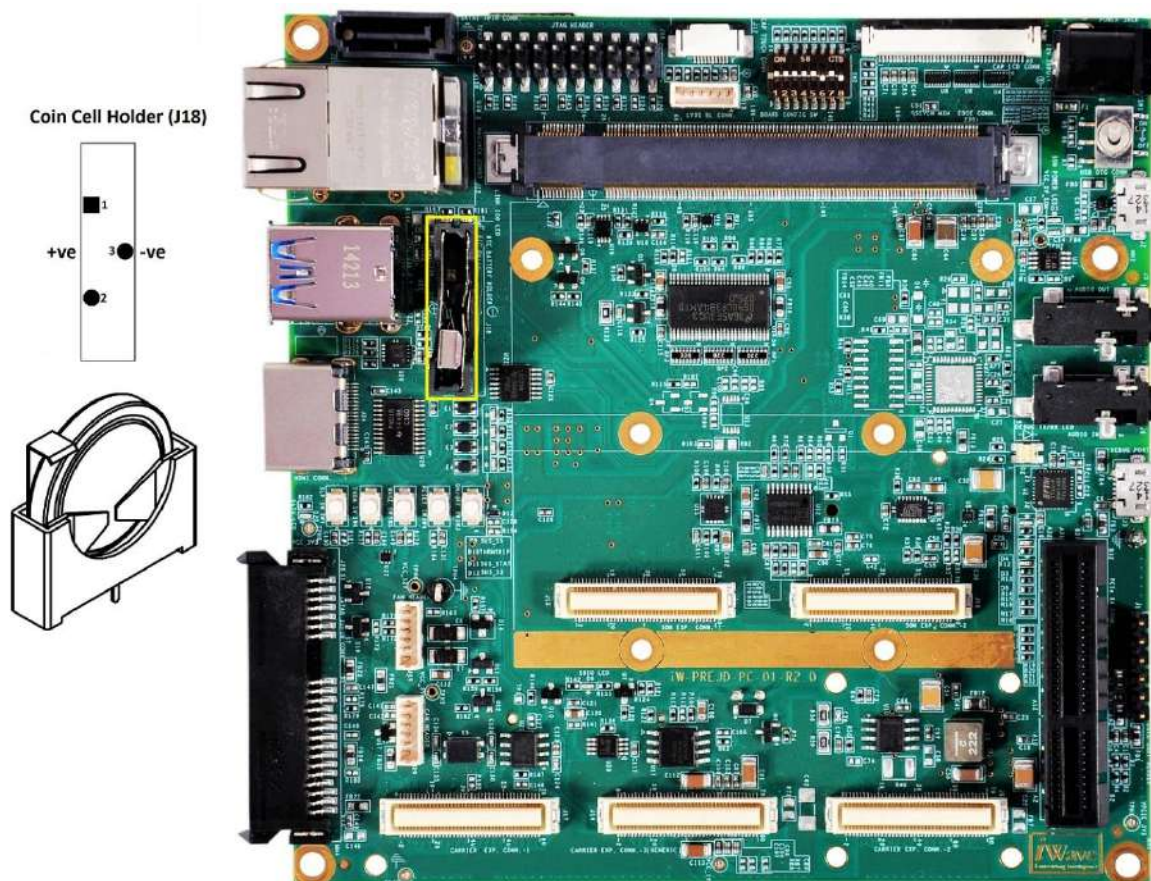


Figure 25: Coin Cell Holder

2.9.3 Fan Header

The RZ/G1H Qseven carrier board supports 6pin Fan Header (J19) to connect the Fan if required. The “FAN_PWMOUT” signal of Qseven MXM connector is connected to Fan header to control the speed of the Fan. The RZ/G1H CPU’s TPU0TO1 interface is used for Fan speed control PWM. This Fan Header (J19) is physically located at the top of the board as shown below.

Number of Pins : 6

Connector Part number : 53047-0610 from Molex

Mating Connector : 0510210600 from Molex with crimping pins

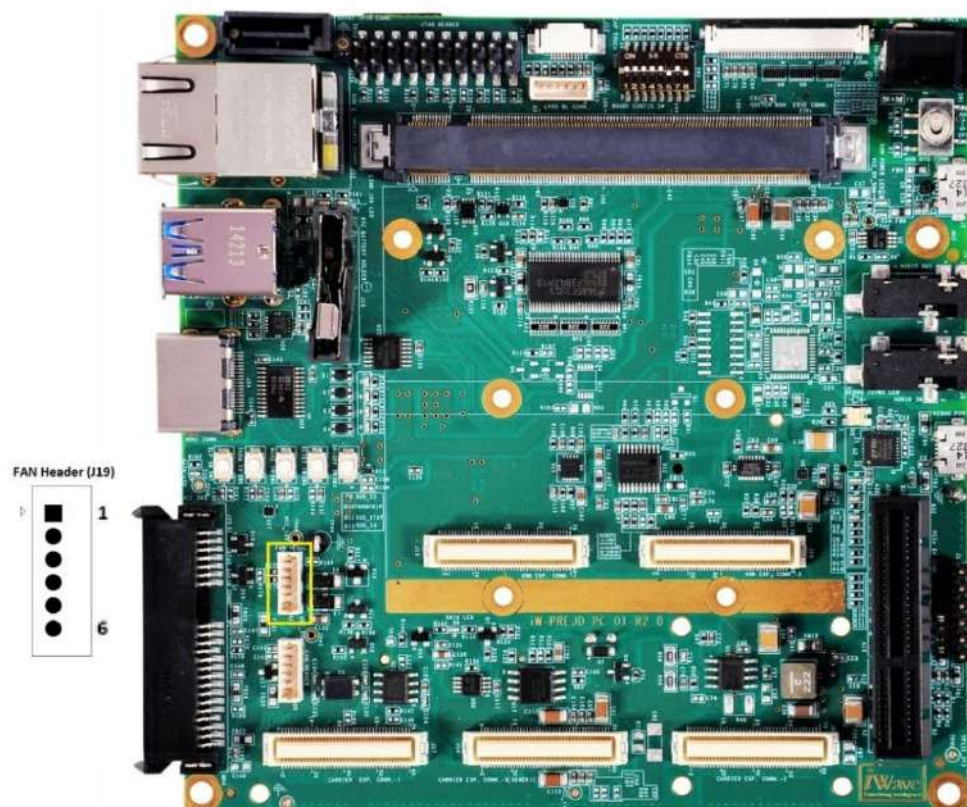


Figure 26: Fan Header

Table 24: Fan Header Pin Out

Pin No	Pin Name	Signal Name	Signal Type / Termination	Description
1	VCC	VCC_12V	O, 12V Power	12V Supply Voltage.
2	PWM	TPU0TO1/MD23(GP0_21)	O, 3.3 CMOS	Fan Speed control.
3	GND	GND	Power	Ground.
4	NC	NC	-	-
5	FAN_PWR	VCC_FAN	O, Power	Fan Power Control.
6	GND	GND	Power	Ground.

2.9.4 JTAG Header (Optional)

A Standard 20-pin ARM JTAG Header is available in RZ/G1H Qseven carrier board for debug purpose. JTAG signals from Qseven MXM connector is connected to JTAG Header (J16) through 3.3V level Buffer. This JTAG Header (J16) is physically located at the top of the board as shown below.

As per Qseven specification version 2.0, Debug UART and JTAG interfaces share the same pins in Qseven Edge connector. Hence either debug UART or JTAG interface can be used at a time. By default, Debug UART (SCIFA2) is supported in the RZ/G1H Qseven SOM and hence JTAG connector on RZ/G1H Qseven carrier board cannot be used for debugging.

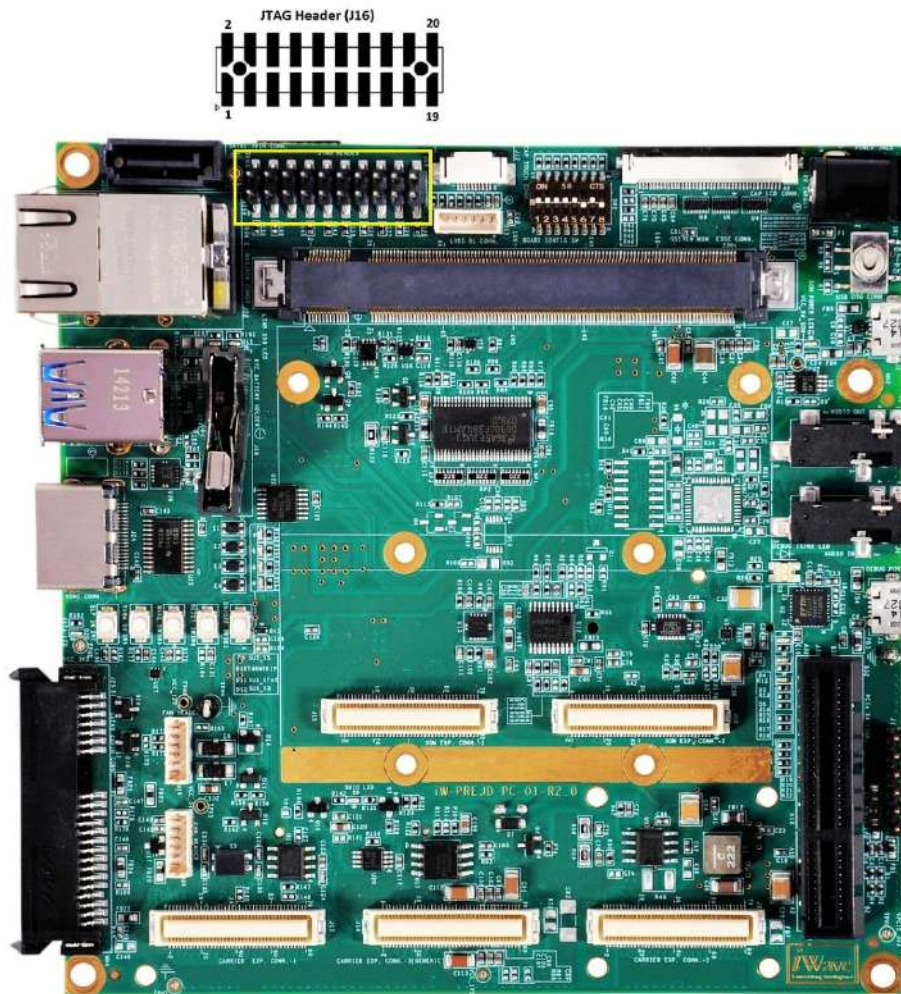


Figure 27: JTAG Header

Table 25: JTAG Header Pin Out

Pin No	Pin Name	Signal Name	Signal Type / Termination	Description
1	VCC	VCC_3V3	O, 3.3V Power	JTAG target reference Voltage.
2	VCC	VCC_3V3	O, 3.3V Power	Supply Voltage.
3	JTAG_TRSTB	JTAG_TRSTB	I, 3.3V CMOS	JTAG test reset signal.
4	GND	GND	Power	Ground.
5	JTAG_TDI	JTAG_TDI	I, 3.3V CMOS	JTAG test data Input.
6	GND	GND	Power	Ground.
7	JTAG_TMS	JTAG_TMS	I, 3.3V CMOS/ 10K PU	JTAG test mode select.
8	GND	GND	Power	Ground.
9	JTAG_TCK	JTAG_TCK	I, 3.3V CMOS/ 10K PD	JTAG test clock.
10	GND	GND	Power	Ground.
11	-	-	10K PD	-
12	GND	GND	Power	Ground.
13	JTAG_TDO	JTAG_TDO	O, 3.3V CMOS	JTAG test data Output.
14	GND	GND	Power	Ground.
15	RSTBN	RSTBN	I,3.3V CMOS/ 10K PU	Reset Signal.
16	GND	GND	Power	Ground.
17	NC	NC	-	NC.
18	GND	GND	Power	Ground.
19	-	-	10K PD	-
20	GND	GND	Power	Ground.

2.10 SOM Expansion Connectors

The RZ/G1H Qseven carrier board has two 80pin Expansion Connectors for mating with RZ/G1H Qseven SOM. This SOM Expansion connector 1 & 2 (J15 & J10) pins are one to one directly connected to Carrier board Expansion connector 1 & 2 (J17 & J9) pins in RZ/G1H Qseven carrier board.

These Expansion connectors J15 & J10 are physically located at the top of the board as shown below.

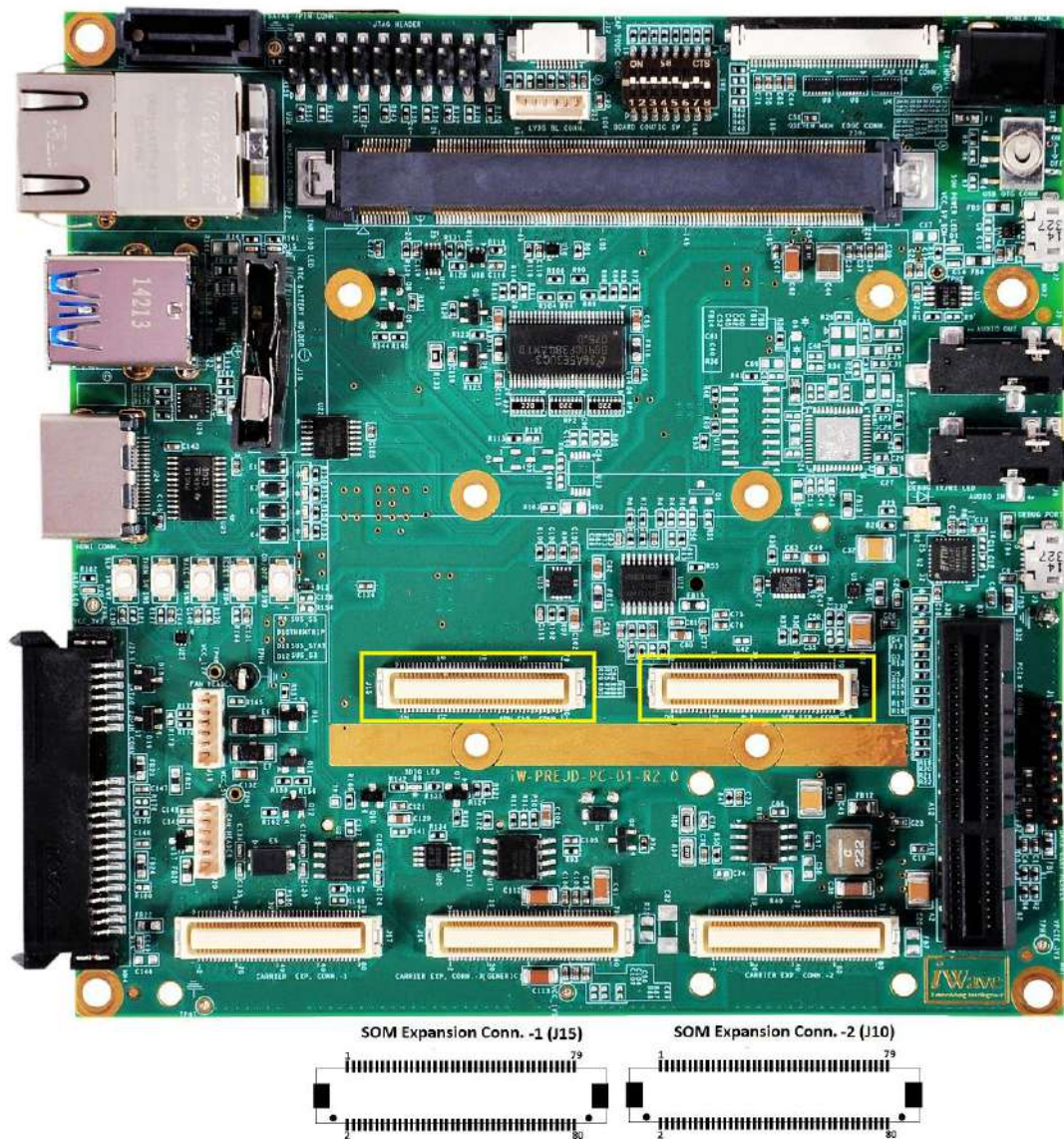


Figure 28: SOM Expansion Connectors

2.11 Carrier Board Expansion Connectors

The RZ/G1H Qseven carrier board has three 80pin Expansion Connectors for expansion purpose. In these three connectors, Carrier Board Expansion connector 1 & 2 (J17 & J9) pins are one to one directly connected from SOM Expansion connector 1 & 2 (J15 & J10) pins in RZ/G1H Qseven carrier board.

The RZ/G1H CPU's MSIOF0 (with SS2), I2C0, I2C2 interfaces and unused GPIOs from Qseven MXM connector are directly connected to Expansion Connector3 (J14). Also on-board 5V, 3.3V & 1.5V power pins are connected to this connector for Add-On Module power.

These Expansion connectors J17, J9 & J14 are physically located at the top of the board as shown below.

Connectors Part number: DF17(3.0)-80DS-0.5V(57) from Hirose

Mating Connector : DF17(2.0)-80DP-0.5V(57) from Hirose

Important Note: Since carrier board Expansion connector 1 & 2 pins are one to one directly connected from RZ/G1H Qseven SOM Expansion connector 1 & 2 pins, these connectors pinout information are not included in this document. Refer RZ/G1H Qseven SOM hardware user guide for Expansion connector 1 & 2 pinout details.

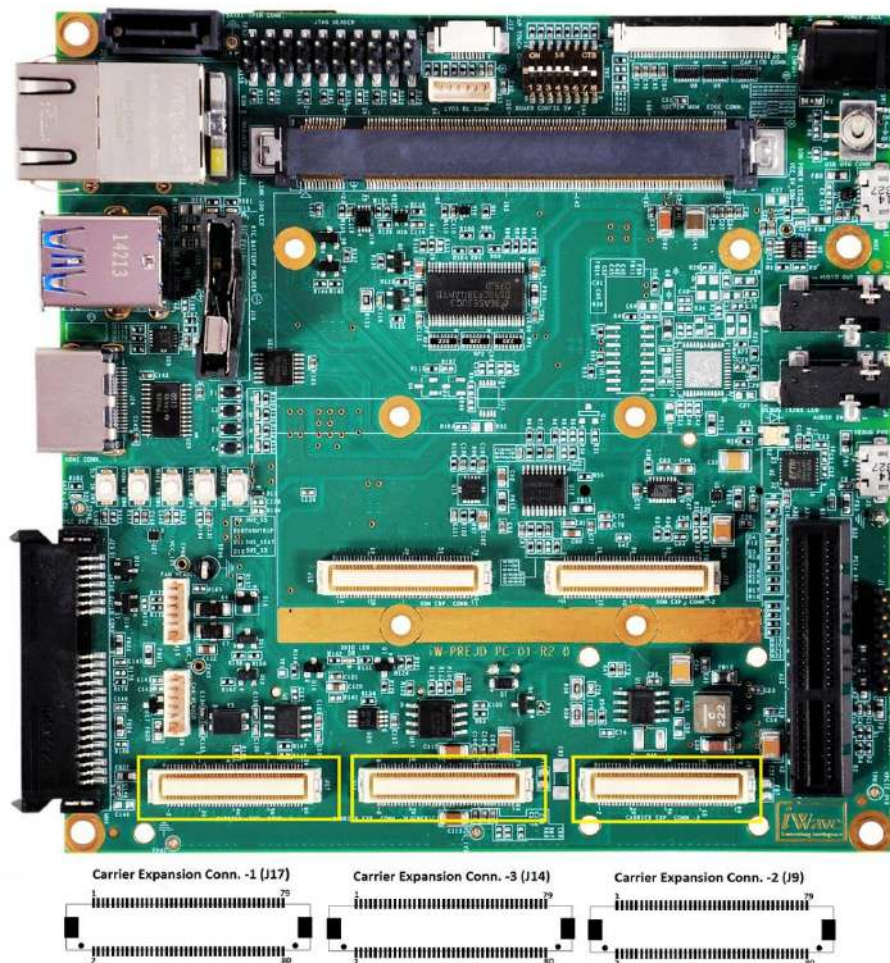


Figure 29: Carrier Board Expansion Connectors

Table 26: Expansion Connector3 Pin Out

Pin No	Signal Name	Signal Type / Termination	Description
1	GND	Power	Ground.
2	GND	Power	Ground.
3	GND	Power	Ground.
4	GND	Power	Ground.
5	GND	Power	Ground.
6	GND	Power	Ground.
7	SUS_S3_Q7	-	Not used in RZ/G1H carrier board. <i>Note: This pin is connected from Qseven MXM connector 18th pin.</i>
8	SUS_S5_Q7	-	Not used in RZ/G1H carrier board. <i>Note: This pin is connected from Qseven MXM connector 16th pin.</i>
9	Q7_GPIO7_(GP4_14)	IO, 3.3V CMOS	Qseven General purpose Input/Output7. <i>Note: This pin is connected to GP4_14 GPIO of G1H CPU through Qseven MXM connector 192nd pin.</i>
10	SUS_STAT_Q7	-	Not used in RZ/G1H carrier board. <i>Note: This pin is connected from Qseven MXM connector 19th pin.</i>
11	SMB_ALERT#	-	Not used in RZ/G1H carrier board. <i>Note: This pin is connected to Qseven MXM connector 64th pin.</i>
12	RSTBN	O, 3.3V CMOS	Active low Reset button Output. <i>Note: This pin is connected to Qseven MXM connector 28th pin.</i>
13	GND	Power	Ground.
14	GND	Power	Ground.
15	WDOUT	-	Not used in RZ/G1H carrier board. <i>Note: This pin is connected to Qseven MXM connector 72nd pin.</i>
16	WAKE#	-	Not used in RZ/G1H carrier board. <i>Note: This pin is connected to Qseven MXM connector 17th pin.</i>
17	WDTRIG#	-	Not used in RZ/G1H carrier board. <i>Note: This pin is connected to Qseven MXM connector 70th pin.</i>
18	GND	Power	Ground.
19	LVDS_BLC_DAT	-	Not used in RZ/G1H carrier board. <i>Note: This pin is optionally connected to I2C3_SDA line of RZ/G1H CPU through Qseven MXM connector 126th pin.</i>

Pin No	Signal Name	Signal Type / Termination	Description
20	THRM#	-	Not used in RZ/G1H carrier board. <i>Note: This pin is connected to Qseven MXM connector 69th pin.</i>
21	LVDS_BLC_CLK	-	Not used in RZ/G1H carrier board. <i>Note: This pin is connected to Qseven MXM connector 128th pin.</i>
22	SLP_BTN#	-	Not used in RZ/G1H carrier board. <i>Note: This pin is connected to Qseven MXM connector 21st pin.</i>
23	RSVD-DP1	-	Not used in RZ/G1H carrier board. <i>Note: This pin is connected to Qseven MXM connector 132nd pin.</i>
24	PWRBTN#	-	Not used in RZ/G1H carrier board. <i>Note: This pin is connected to Qseven MXM connector 20th pin.</i>
25	RSVD-DP2	-	Not used in RZ/G1H carrier board. <i>Note: This pin is connected to Qseven MXM connector 134th pin.</i>
26	GND	Power	Ground.
27	GND	Power	Ground.
28	LID_BTN#	-	Not used in RZ/G1H carrier board. <i>Note: This pin is connected to Qseven MXM connector 22nd pin.</i>
29	RSVD-DP3	-	Not used in RZ/G1H carrier board. <i>Note: This pin is connected to Qseven MXM connector 144th pin.</i>
30	BATLOW#	-	Not used in RZ/G1H carrier board. <i>Note: This pin is connected to Qseven MXM connector 27th pin.</i>
31	RSVD-DP4	-	Not used in RZ/G1H carrier board. <i>Note: This pin is connected to Qseven MXM connector 146th pin.</i>
32	BIOS_DISABLE#	-	Not used in RZ/G1H carrier board. <i>Note: This pin is connected to Qseven MXM connector 41st pin.</i>
33	GND	Power	Ground.

Pin No	Signal Name	Signal Type / Termination	Description
34	Q7_GPIO1_(GP0_25)	IO, 3.3V CMOS/ 10K PU	Qseven General Purpose Input/Output1. <i>Note: This pin is connected to RZ/G1H CPU's GPIO line GP0_25 through Qseven MXM connector 186th pin through default populated resistor.</i> <i>Note: Also, this pin is connected to Mini PCIe connector (J26) 20th pin through default populated resistor.</i>
35	GP2_I2C_DAT	-	Not used in RZ/G1H carrier board. <i>Note: This pin is connected to I2C3_SDA line of RZ/G1H CPU through Qseven MXM connector 125th pin.</i>
36	Q7_GPIO0_(GP0_24)	I,3.3V CMOS/ 10K PU	Qseven General Purpose Input/Output0. This pin is connected to Capacitive Touch Connector and Resistive Touch Controller for touch interrupt. <i>Note: This pin is connected to RZ/G1H CPU GPIO pin GP0_24 through Qseven MXM connector 185th pin through default populated resistor.</i>
37	GP2_I2C_CLK	-	Not used in RZ/G1H carrier board. <i>Note: This pin is connected to I2C3_SCL line of RZ/G1H CPU through Qseven MXM connector 127th pin.</i>
38	GND	Power	Ground.
39	DP_HPD#	-	Not used in RZ/G1H carrier board. <i>Note: This pin is optionally connected to RZ/G1H CPU GPIO line GP5_13 through Qseven MXM connector 154th pin.</i>
40	Q7_GPIO6_(GP4_2)	IO, 3.3V CMOS/ 10K PU	Qseven General purpose Input/Output6. This pin is used to enable the LVDS display Power. <i>Note: This pin is connected to RZ/G1H CPU GPIO line GP4_2 through Qseven MXM connector 191st pin through resistor and default populated.</i>
41	Q7_GPIO3_(GP4_19)	I, 3.3V CMOS/ 10K PU	Qseven General purpose Input/Output3 This pin is connected from Audio Out Jack for Headphone detect. <i>Note: This pin is connected to RZ/G1H CPU GPIO line GP4_19 through Qseven MXM connector 188th pin through resistor and default populated.</i>

Pin No	Signal Name	Signal Type / Termination	Description
42	GPIO_SSI_RST(GP1_29)	O, 3.3V CMOS	Touch Panel Reset. This pin is connected to Capacitive touch panel connector for reset. <i>Note: This pin is connected to RZ/G1H CPU GPIO line GP1_29 through Qseven MXM connector 61st pin through default populated resistor.</i>
43	GND	Power	Ground.
44	Q7_GPIO5_(GP2_17)	IO, 3.3V CMOS	Qseven General purpose Input/Output5. This pin is connected to control the LVDS Backlight Power. <i>Note: This pin is connected to RZ/G1H CPU GPIO line GP2_17 through Qseven MXM connector 190th pin through default populated resistor.</i>
45	Q7_GPIO2_(GP0_26)	I, 3.3V CMOS/ 10K PU	Qseven General purpose Input/Output2. This pin is connected from Audio IN Jack for Headphone Mic detect. <i>Note: This pin is also connected to RZ/G1H CPU GPIO line GP0_26 through Qseven MXM connector 187th pin through default populated resistor.</i>
46	MSIOF0_RXD(GP5_17)	I, 3.3V CMOS	SPI Master In Slave Out. This Pin is used for On Board SPI Flash. <i>Note: This pin is connected to RZ/G1H CPU MSIOF0_RXD line through Qseven MXM connector 201st pin.</i>
47	Q7_GPIO4_(GP1_28)	IO, 3.3V CMOS	Qseven General purpose Input/Output4. This pin is connected to CAN0 Transceiver Power down control. <i>Note: This pin is connected to RZ/G1H CPU GPIO line GP1_28 through Qseven MXM Connector 189th pin.</i>
48	MSIOF0_TXD/MDT1(GP5_15) ¹	O, 3.3V CMOS	SPI Master Out Slave In. This pin is used for On Board SPI Flash. <i>Note: This pin is connected to RZ/G1H CPU MSIOF0_TXD line through Qseven MXM connector 199th pin.</i>
49	MSIOF0_SS1/MD0(GP5_14) ¹	I, 3.3V CMOS	SPI Chip Select2. <i>Note: This pin is connected to RZ/G1H CPU MSIOF0_SS1 line through Qseven MXM connector 202nd pin.</i>
50	GND	Power	Ground.

RZ/G1H Qseven Development Platform Hardware User Guide

Pin No	Signal Name	Signal Type / Termination	Description
51	MSIOF0_SCK(GP5_12)	I, 3.3V CMOS	SPI Clock. This Pin is used for On Board SPI Flash. <i>Note: This pin is connected to RZ/G1H CPU MSIOF0_SCK line through Qseven MXM connector 203rd pin.</i>
52	DP_AUX+	-	Not used in RZ/G1H carrier board. <i>Note: This pin is connected to Qseven MXM connector 138th pin.</i>
53	GPIO_THRMTRIP_Q7(GP4_11)	I, 3.3V CMOS	Connected to LED (D11) through buffer in carrier board for thermal trip indication. <i>Note: This pin is connected RZ/G1H GPIO line GP4_11 through Qseven MXM connector 71st pin.</i>
54	DP_AUX-	-	Not used in RZ/G1H carrier board. <i>Note: This pin is connected to Qseven MXM connector 140th pin.</i>
55	GND	Power	Ground.
56	GND	Power	Ground.
57	VCC_3V3	O, 3.3V Power	3.3V Supply Voltage.
58	VCC_1V5	O, 1.5V Power	1.5V Supply Voltage.
59	VCC_3V3	O, 3.3V Power	3.3V Supply Voltage.
60	VCC_1V5	O, 1.5V Power	1.5V Supply Voltage.
61	GND	Power	Ground.
62	GND	Power	Ground.
63	VCC_5V	O, 5V Power	5V Supply Voltage.
64	VCC_5V	O, 5V Power	5V Supply Voltage.
65	VCC_5V	O, 5V Power	5V Supply Voltage.
66	VCC_5V	O, 5V Power	5V Supply Voltage.
67	VCC_5V	O, 5V Power	5V Supply Voltage.
68	VCC_5V	O, 5V Power	5V Supply Voltage.
69	VCC_5V	O, 5V Power	5V Supply Voltage.
70	VCC_5V	O, 5V Power	5V Supply Voltage.
71	GND	Power	Ground.
72	GND	Power	Ground.
73	GND	Power	Ground.
74	GND	Power	Ground.
75	GND	Power	Ground.
76	GND	Power	Ground.
77	I2C0_SCL	O, 3.3V OD	I2C0 clock. <i>Note: This pin is connected to RZ/G1H CPU I2C0_SCL line through Qseven MXM Connector 60th pin through default populated resistor.</i>

Pin No	Signal Name	Signal Type / Termination	Description
78	I2C2_SCL(GP4_0)	O, 3.3V OD	I2C2 clock. <i>Note: This pin is connected to RZ/G1H CPU I2C2_SCL line through Qseven MXM Connector 66th pin through default populated resistor.</i>
79	I2C0_SDA	IO, 3.3V OD	I2C0 Data. <i>Note: This pin is connected to RZ/G1H CPU I2C0_SDA line through Qseven MXM Connector 62nd pin through default populated resistor.</i>
80	I2C2_SDA(GP4_1)	IO, 3.3V OD	I2C2 Data. <i>Note: This pin is connected to RZ/G1H CPU I2C2_SDA line through Qseven MXM Connector 68th pin through default populated resistor.</i>

¹ Important Note: These signals are also used for RZ/G1H CPU bootstrap setting on RZ/G1H Qseven SOM.

3. ARCHITECTURE AND DESIGN – CAMERA ADD-ON MODULE

This section provides detailed information about the RZ/G1H Camera Add-On Module features with high level block diagram and detailed information about each block.

3.1 RZ/G1H Camera Add-On Module Block Diagram

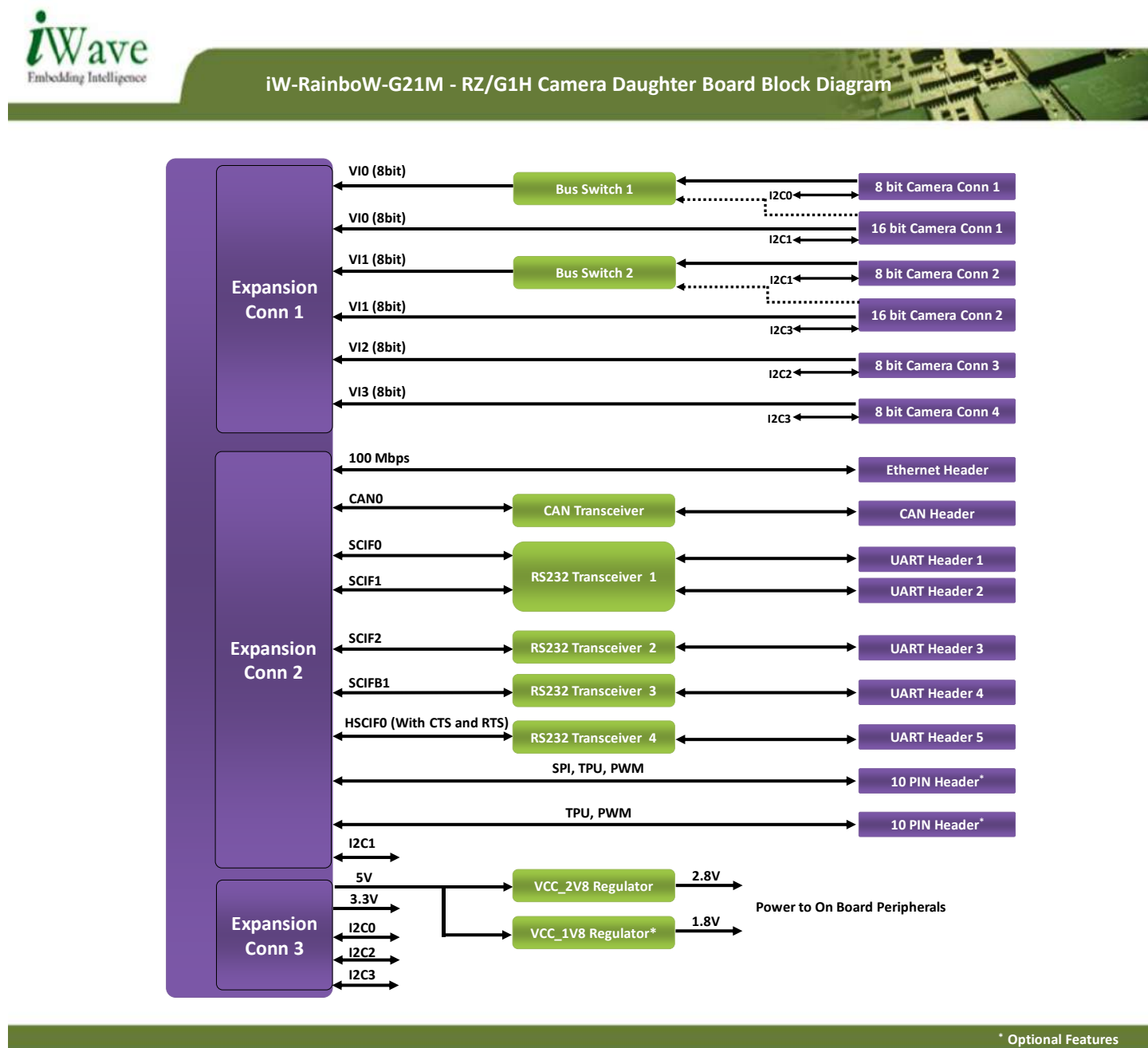


Figure 30: RZ/G1H Camera Add-On Module Block Diagram

3.2 RZ/G1H Camera Add-On Module Features

The RZ/G1H Camera Add-On Module has three expansion connectors to connect the RZ/G1H carrier board as shown below and supports following features.

Video Features

- 8bit CMOS Camera (VIN0, VIN1, VIN2 and VIN3) x 4 Ports
- 16bit CMOS Camera (VIN0 & VIN1) x 2 Ports

Communication Features

- CAN0 Header x 1 Port
- 10/100Mbps Ethernet Header (EtherMAC) x 1 Port

Serial Interface Features

- Data UART RS232 Header (SCIF0, SCIF1, SCIF2, SCIFB1 & HSCIF0) x 5 Ports

General Specification

- Form Factor : 90mm X 60mm

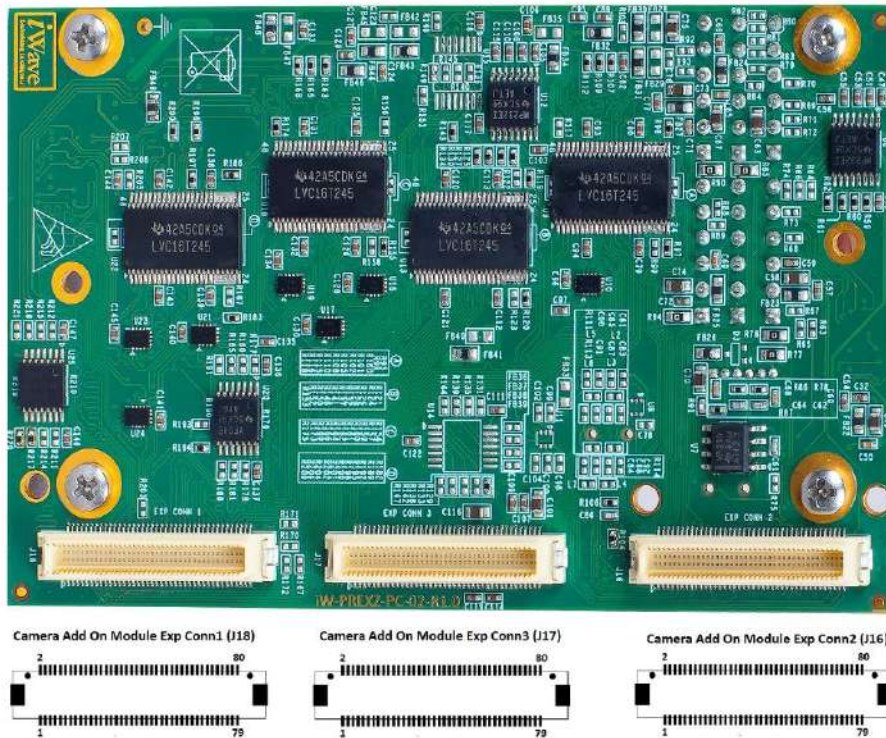


Figure 31: Camera Add-On Module Expansion Connectors

Important Note: At a time either four 8bit cameras or two 16bit cameras only can be used and it can be selected through Camera selection switch (SW1).

*Important Note: Refer **APPENDIX** for guidelines to integrate Camera Add-On Module in to RZ/G1H Development platform carrier board.*

3.3 Video Features

3.3.1 Camera Selection Switch

The RZ/G1H Camera Add-On Module has one single bit DIP switch (SW1) for camera selection. This switch can be used to select four 8bit cameras or two 16bit cameras. This switch SW1 is also connected to RZ/G1H CPU's GPIO "GP5_7" for reading the switch status. This camera selection switch SW1 is physically located at the top of the board as shown below.

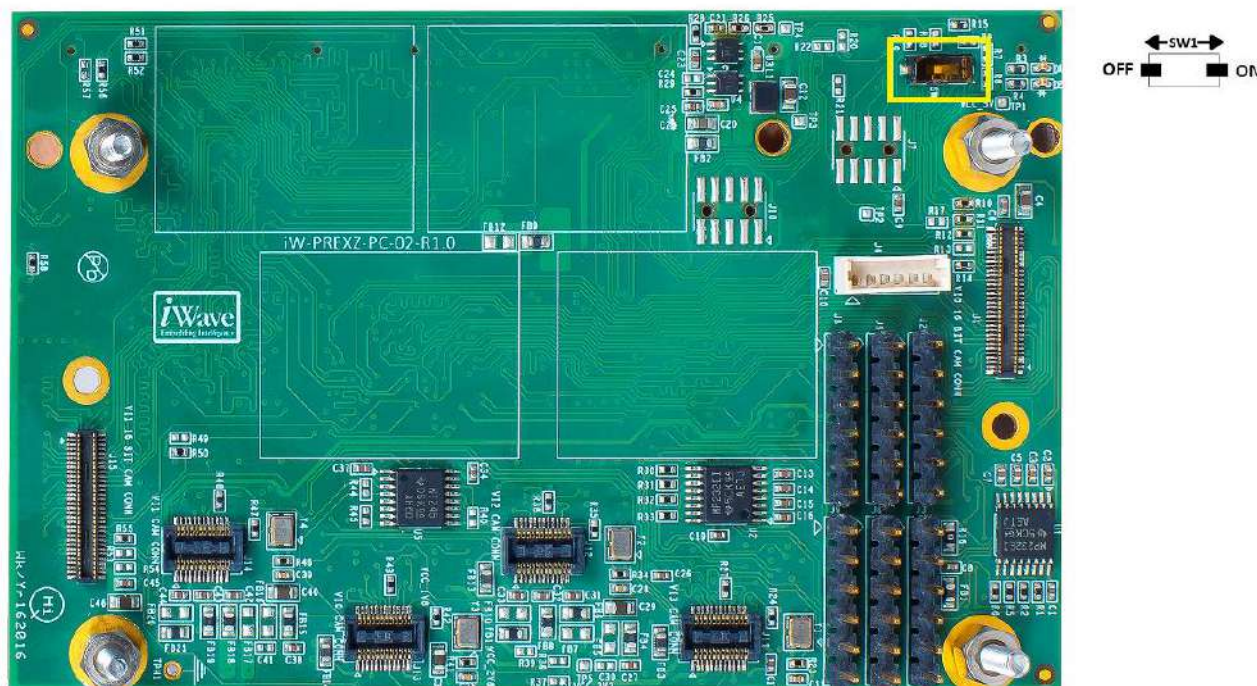


Figure 32 Camera Selection Switch

Table 27 Camera Selection Switch

Switch	Switch Position	
	OFF (Low)	ON (High)
SW1	Four 8bit CMOS cameras through VIN0, VIN1, VIN2 & VIN3 on J13, J14, J12 & J11 respectively	Two 16bit cameras through VIN0 & VIN1 through J1 & J5 respectively

3.3.2 8bit CMOS Cameras

The RZ/G1H Camera Add-On Module supports four 8bit Camera connectors J13, J14, J12 and J11 to support four CMOS camera interfaces through RZ/G1H CPU's VIN0, VIN1, VIN2 and VIN3 respectively. RZ/G1H CPU's I2C0, I2C1, I2C2 and I2C3 interface is connected to J13, J14, J12 and J11 connectors respectively for camera control & configuration. Also reference clock for each camera is provided externally on-board through 26MHz Oscillator. Four 8bit camera connectors (J13, J14, J12 and J11) are physically located on top of the board as shown below.

Compatible Camera Module:

Part Number: CN003VEF2052

Description: VGA (640x480 pixel) CMOS camera based on OmniVision's OV7725 sensor

Manufacturer Name: Global Digital Star Limited

Manufacturer Web link: <http://www.globaldigitalstar.com>

Part Number: G-5640-2052R

Description: 5Mega pixel CMOS camera based on OmniVision's OV5640 sensor

Manufacturer Name: Global Digital Star Limited

Manufacturer Web link: <http://www.globaldigitalstar.com>

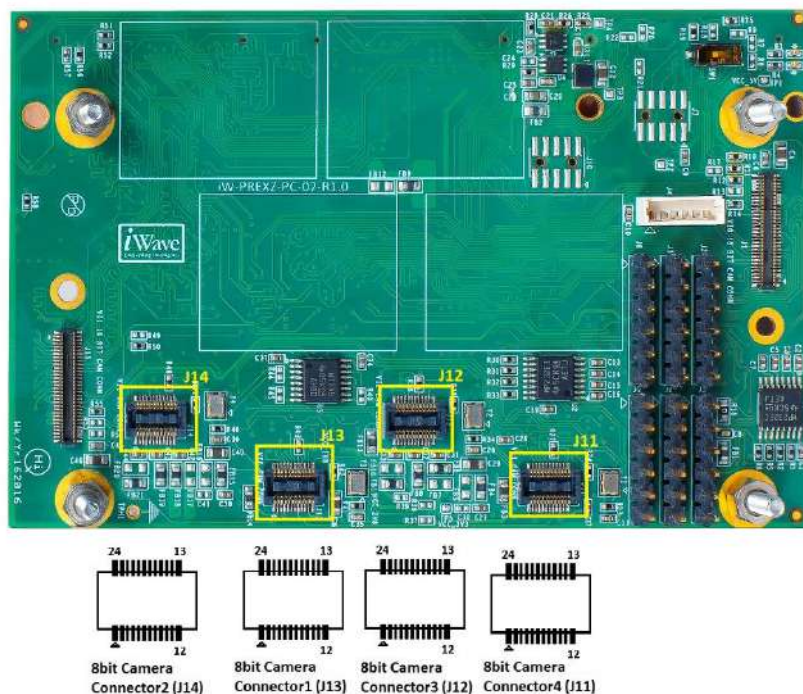


Figure 33 8bit CMOS Camera Header

Table 28:8bit Camera Connector1 Pin Out (J13)

Pin No	Pin Name	Signal Name	Signal Type / Termination	Description
1	STROBE	NC	-	NC.
2	AGND	AGND	Power	Analog Ground.
3	I2C_SDA	I2C0_SDA	IO, 2.8V OD	I2C0 Data.
4	AVDD	AVDD	O, 2.8V Power	Camera Analog Power Supply.
5	I2C_SCL	I2C0_SCL	O, 2.8V OD	I2C0 Clock.
6	RESETB	PRESETOUT#	O, 2.8V CMOS	Reset Out, Active Low.
7	VSYN	VIO_VSYN#(GP0_13)	I, 2.8V CMOS	VIN0 Camera Vertical Synchronization.
8	PWDN	-	O, 3.3V CMOS/ 10K PD	Active high Camera Power Down. This pin is connected to GND in camera Add-On Module to enable the camera always. <i>Note: GP1_13 signal is optionally connected to this pin through resistor and default not populated.</i>
9	HSYN	VIO_HSYN#(GP0_12)	I, 2.8V CMOS	VIN0 Camera Horizontal Synchronization.
10	DVDD	NC	-	Default NC. Digital Power Supply.
11	DOVDD	DOVDD	O, 2.8V Power	Camera IO Power Supply.
12	DATA9	VIO_DATA7/VIO_B7(GP2_8)	I, 2.8V CMOS	VIN0 Camera Data7.
13	XCLK	MCLK_CAM1	O, 2.8V CMOS	Camera Reference Clock. This pin is connected to On-board 26MHz Oscillator.
14	DATA8	VIO_DATA6/VIO_B6(GP2_7)	I, 2.8V CMOS	VIN0 Camera Data6.
15	DGND	DGND	Power	Digital Ground.
16	DATA7	VIO_DATA5/VIO_B5(GP2_6)	I, 2.8V CMOS	VIN0 Camera Data5.
17	PCLK	VIO_CLK(GP2_0)	I, 2.8V CMOS	VIN0 Camera Pixel Clock.
18	DATA6	VIO_DATA4/VIO_B4(GP2_5)	I, 2.8V CMOS	VIN0 Camera Data4.
19	DATA2	VIO_DATA0/VIO_B0(GP2_1)	I, 2.8V CMOS	VIN0 Camera Data0.
20	DATA5	VIO_DATA3/VIO_B3(GP2_4)	I, 2.8V CMOS	VIN0 Camera Data3.
21	DATA3	VIO_DATA1/VIO_B1(GP2_2)	I, 2.8V CMOS	VIN0 Camera Data1.
22	DATA4	VIO_DATA2/VIO_B2(GP2_3)	I, 2.8V CMOS	VIN0 Camera Data2.
23	DATA1	NC	-	NC.
24	DATA0	NC	-	NC.

Table 29 8bit Camera Connector2 Pin Out (J14)

Pin No	Pin Name	Signal Name	Signal Type / Termination	Description
1	STROBE	NC	-	NC.
2	AGND	AGND	Power	Analog Ground.
3	I2C_SDA	MSIOF3_SS2(GP4_27)	IO, 2.8V OD/ 10K PU	I2C1 Data.
4	AVDD	AVDD	O, 2.8V Power	Camera Analog Power Supply.
5	I2C_SCL	MSIOF3_SYNC(GP4_30)	O, 2.8V OD/ 10K PU	I2C1 Clock.
6	RESETB	PRESETOUT#	O, 2.8V CMOS	Reset Out, Active Low.
7	VSYNC	VI1_VSYNC#(GP1_25)	I, 2.8V CMOS	VIN1 Camera Vertical Synchronization.
8	PWDN	-	O, 3.3V CMOS/ 10K PD	Active high Camera Power Down. This pin is connected to GND in camera Add-On Module to enable the camera always. <i>Note: GP0_15 signal is optionally connected to this pin through resistor and default not populated.</i>
9	HSYNC	VI1_HSYNC#(GP1_24)	I, 2.8V CMOS	VIN1 Camera Horizontal Synchronization.
10	DVDD	NC	-	Default NC. Digital Power Supply.
11	DOVDD	DOVDD	O, 2.8V Power	Camera IO Power Supply.
12	DATA9	VI1_B7/VI1_DATA7(GP3_7)	I, 2.8V CMOS	VIN1 Camera Data7.
13	XCLK	MCLK_CAM2	O, 2.8V CMOS	Camera Reference Clock. This pin is connected to On-board 26MHz Oscillator.
14	DATA8	VI1_B6/VI1_DATA6(GP3_6)	I, 2.8V CMOS	VIN1 Camera Data6.
15	DGND	DGND	Power	Digital Ground.
16	DATA7	VI1_B5/VI1_DATA5(GP3_5)	I, 2.8V CMOS	VIN1 Camera Data5.
17	PCLK	VI1_CLK(GP3_15)	I, 2.8V CMOS	VIN1 Camera Pixel Clock.
18	DATA6	VI1_B4/VI1_DATA4(GP3_4)	I, 2.8V CMOS	VIN1 Camera Data4.
19	DATA2	VI1_B0/VI1_DATA0(GP3_0)	I, 2.8V CMOS	VIN1 Camera Data0.
20	DATA5	VI1_B3/VI1_DATA3(GP3_3)	I, 2.8V CMOS	VIN1 Camera Data3.
21	DATA3	VI1_B1/VI1_DATA1(GP3_1)	I, 2.8V CMOS	VIN1 Camera Data1
22	DATA4	VI1_B2/VI1_DATA2(GP3_2)	I, 2.8V CMOS	VIN1 Camera Data2.
23	DATA1	NA	-	NC.
24	DATA0	NA	-	NC.

Table 30 8bit Camera Connector3 Pin Out (J12)

Pin No	Pin Name	Signal Name	Signal Type / Termination	Description
1	STROBE	NC	-	NC.
2	AGND	AGND	Power	Analog Ground.
3	I2C_SDA	I2C2_SDA(GP4_1)	IO, 2.8V OD	I2C2 Data.
4	AVDD	AVDD	O, 2.8V Power	Camera Analog Power Supply.
5	I2C_SCL	I2C2_SCL(GP4_0)	O, 2.8V OD	I2C2 Clock.
6	RESETB	PRESETOUT#	O, 2.8V CMOS	Reset Out, Active Low.
7	VSNC	GPIO_EXP(GP1_21)	I, 2.8V CMOS	VIN2 Camera Vertical Synchronization. <i>Note: This pin is optionally connected to 65th pin of expansion connector1 through resistor and default not populated</i>
8	PWDN	-	O, 3.3V CMOS/ 10K PD	Active high Camera Power Down. This pin is connected to GND in camera Add-On Module to enable the camera always. <i>Note: GP2_27 signal is optionally connected to this pin through resistor and default not populated.</i>
9	HSYNC	VI3_HSYNC#(GP1_16)	I, 2.8V CMOS	VIN2 Camera Horizontal Synchronization. <i>Note: This pin is optionally connected to 35th pin of expansion connector1 through resistor and default not populated</i>
10	DVDD	NC	-	Default NC. Digital Power Supply.
11	DOVDD	DOVDD	O, 2.8V Power	Camera IO Power Supply.
12	DATA9	VI2_G7/QSPI_IO2/VI1_G7(GP1_7)	I, 2.8V CMOS	VIN2 Camera Data7. <i>Note: This pin is optionally connected to 1st pin of expansion connector1 through resistor and default not populated</i>
13	XCLK	MCLK_CAM3	O, 2.8V CMOS	Camera Reference Clock. This pin is connected to On-board 26MHz Oscillator.
14	DATA8	VI2_G6(GP1_6)	I, 2.8V CMOS	VIN2 Camera Data6.
15	DGND	DGND	Power	Digital Ground.
16	DATA7	VI2_G5(GP1_5)	I, 2.8V CMOS	VIN2 Camera Data5.
17	PCLK	VI2_CLK(GP1_11)	I, 2.8V CMOS	VIN2 Camera Pixel Clock.
18	DATA6	VI2_G4(GP1_4)	I, 2.8V CMOS	VIN2 Camera Data4.
19	DATA2	VI2_G0(GP0_27)	I, 2.8V CMOS	VIN2 Camera Data0.
20	DATA5	VI2_G3(GP1_10)	I, 2.8V CMOS	VIN2 Camera Data3.
21	DATA3	VI2_G1(GP0_28)	I, 2.8V CMOS	VIN2 Camera Data1
22	DATA4	VI2_G2(GP0_29)	I, 2.8V CMOS	VIN2 Camera Data2.
23	DATA1		-	NC.
24	DATA0		-	NC.

Table 31 8bit Camera Connector4 Pin Out (J11)

Pin No	Pin Name	Signal Name	Signal Type / Termination	Description
1	STROBE	NA	-	NC.
2	AGND	AGND	Power	Analog Ground.
3	I2C_SDA	I2C3_SDA	IO, 2.8V OD	I2C3 Data.
4	AVDD	AVDD	O, 2.8V Power	Camera Analog Power Supply.
5	I2C_SCL	I2C3_SCL	O, 2.8V OD	I2C3 Clock.
6	RESETB	PRESETOUT#	O, 2.8V CMOS	Reset Out, Active Low.
7	VSYNC	VI3_VSYNC#/VI1_G2(GP1_17)	I, 2.8V CMOS	VIN3 Camera Vertical Synchronization.
8	PWDN	-	O, 3.3V CMOS/ 10K PD	Active high Camera Power Down. This pin is connected to GND in camera Add-On Module to enable the camera always. <i>Note: GP2_26 signal is optionally connected to this pin through resistor and default not populated.</i>
9	HSYNC	VI3_HSYNC#(GP1_16)	I, 2.8V CMOS	VIN3 Camera Horizontal Synchronization.
10	DVDD	NC	-	Default NC. Digital Power Supply.
11	DOVDD	DOVDD	O, 2.8V Power	Camera IO Power Supply.
12	DATA9	VI3_DATA7(GP0_7)	I, 2.8V CMOS	VIN3 Camera Data7.
13	XCLK	MCLK_CAM4	O, 2.8V CMOS	Camera Reference Clock. This pin is connected to On-board 26MHz Oscillator.
14	DATA8	VI3_DATA6(GP0_6)	I, 2.8V CMOS	VIN3 Camera Data6.
15	DGND	DGND	Power	Digital Ground.
16	DATA7	VI3_DATA5(GP0_5)	I, 2.8V CMOS	VIN3 Camera Data5.
17	PCLK	VI3_CLK(GP1_23)	I, 2.8V CMOS	VIN3 Camera Pixel Clock.
18	DATA6	VI3_DATA4(GP0_4)	I, 2.8V CMOS	VIN3 Camera Data4.
19	DATA2	VI3_DATA0/VI0_G4(GP0_0)	I, 2.8V CMOS	VIN3 Camera Data0.
20	DATA5	VI3_DATA3/VI0_G7(GP0_3)	I, 2.8V CMOS	VIN3 Camera Data3.
21	DATA3	VI3_DATA1/VI0_G5(GP0_1)	I, 2.8V CMOS	VIN3 Camera Data1
22	DATA4	VI3_DATA2/VI0_G6(GP0_2)	I, 2.8V CMOS	VIN3 Camera Data2.
23	DATA1	NA	-	NC.
24	DATA0	NA	-	NC.

3.3.3 16bit CMOS Cameras

The RZ/G1H Camera Add-On Module supports two 16bit Camera connectors (J1 and J15) to support two 16bit CMOS camera interfaces through RZ/G1H CPU's VIN0 and VIN1 respectively. RZ/G1H CPU's I2C1 and I2C3 interface is connected to J1 and J15 connectors respectively for camera control & configuration. Two 16bit camera connectors (J1 and J15) are physically located on top of the board as shown below.

Compatible Camera Module:

Part Number: KBCR-S02TXG

Description: 2Mega pixel CMOS camera based on Sony sensor

Manufacturer Name: Shikino High-Tech Co. Ltd

Manufacturer Web link: <http://www.shikino.co.jp/eng/products/product-kbcr-s02txg.html>

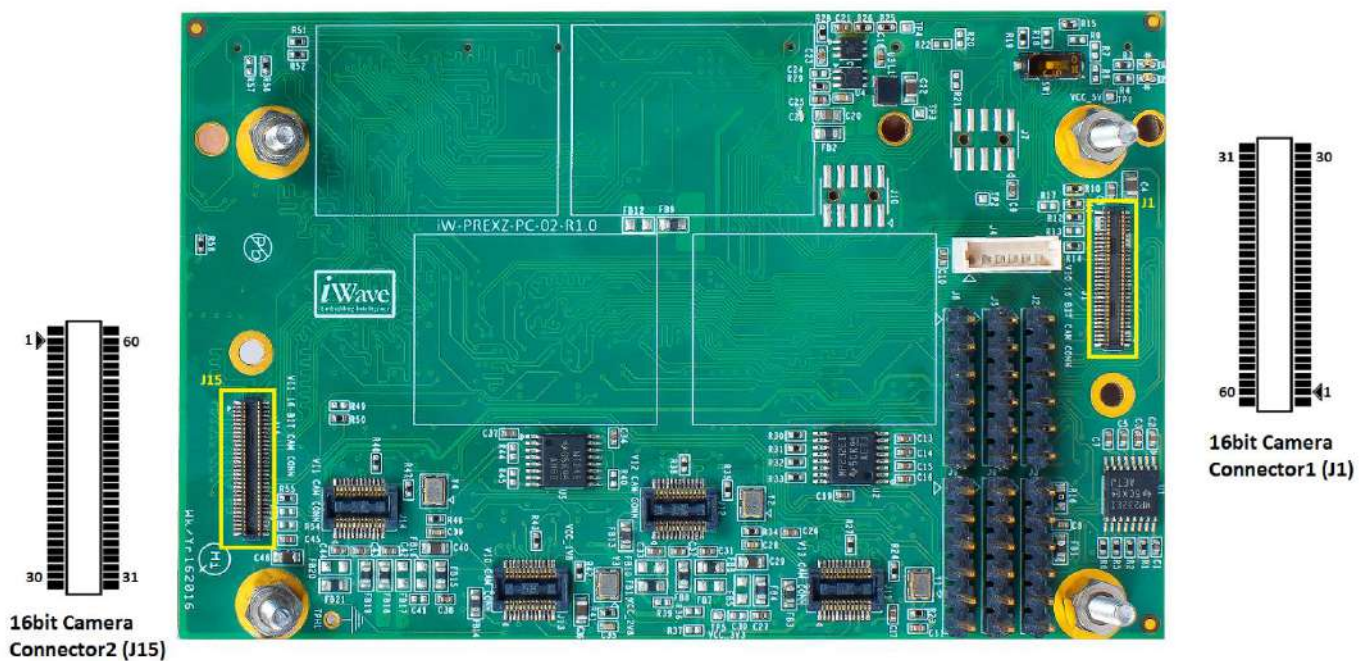


Figure 34 16bit CMOS Camera Header

Table 32 16bit Camera Connector Pin Out (J1)

Pin No	Pin Name	Signal Name	Signal Type / Termination	Description
1	GND	GND	Power	Ground.
2	GND	GND	Power	Ground.
3	GND	GND	Power	Ground.
4	YOUT0	VI0_G0(GP0_8)	I, 3.3V CMOS	VIN0 Camera Data0.
5	YOUT1	VI0_G1(GP0_9)	I, 3.3V CMOS	VIN0 Camera Data1.
6	YOUT2	VI0_G2(GP0_10)	I, 3.3V CMOS	VIN0 Camera Data2.
7	YOUT3	VI0_G3(GP0_11)	I, 3.3V CMOS	VIN0 Camera Data3.
8	YOUT4	VI3_DATA0/VI0_G4(GP0_0)	I, 3.3V CMOS	VIN0 Camera Data4.
9	YOUT5	VI3_DATA1/VI0_G5(GP0_1)	I, 3.3V CMOS	VIN0 Camera Data5.
10	YOUT6	VI3_DATA2/VI0_G6(GP0_2)	I, 3.3V CMOS	VIN0 Camera Data6.
11	YOUT7	VI3_DATA3/VI0_G7(GP0_3)	I, 3.3V CMOS	VIN0 Camera Data7.
12	GND	GND	Power	Ground.
13	BCK	VI0_CLK(GP2_0)	I, 3.3V CMOS	VIN0 Camera Pixel Clock.
14	GND	GND	Power	Ground.
15	BDEN	VI0_CLKENB(GP0_14)	I, 3.3V CMOS	VIN0 Camera Data Enable.
16	BHD	VI0_HSYNC#(GP0_12)	I, 3.3V CMOS	VIN0 Camera Horizontal Synchronization.
17	BVD	VI0_VSYNC#(GP0_13)	I, 3.3V CMOS	VIN0 Camera Vertical Synchronization.
18	GND	GND	Power	Ground.
19	NC	-	-	-
20	GND	GND	Power	Ground.
21	NC	-	-	-
22	NC	-	-	-
23	GND	GND	Power	Ground.
24	GND	GND	Power	Ground.
25	GND	GND	Power	Ground.
26	GND	GND	Power	Ground.
27	NC	-	-	-
28	NC	-	-	-
29	NC	-	-	-
30	NC	-	-	-
31	EXTVIN	EXTVIN	O, 5V, Power	Camera Power Supply
32	EXTVIN	EXTVIN	O, 5V, Power	Camera Power Supply
33	EXTVIN	EXTVIN	O, 5V, Power	Camera Power Supply
34	EXTVIN	EXTVIN	O, 5V, Power	Camera Power Supply
35	NC	-	-	-
36	GND	GND	Power	Ground.
37	SCL	MSIOF3_SYNC(GP4_30)	O, 3.3V CMOS	I2C1 Clock.

38	SDA	MSIOF3_SS2(GP4_27)	IO, 3.3V CMOS	I2C1 Data.
39	GND	GND	Power	Ground.
40	EXTRST	PRESETOUT#	O, 3.3V CMOS	Reset Out Active Low
41	PWDN	-	O, 3.3V CMOS/ PD 10K	Active high Camera Power Down. This pin is connected to GND in camera Add-On Module to enable the camera always. <i>Note: G4_31 signal is optionally connected to this pin through resistor and default not populated.</i>
42	NC	-	-	-
43	GND	GND	Power	Ground.
44	NC	-	-	-
45	NC	-	-	-
46	NC	-	-	-
47	NC	-	-	-
48	NC	-	-	-
49	NC	-	-	-
50	UVOUT0	VI0_DATA0/VI0_B0(G P2_1)	I, 3.3V CMOS	VIN0 Camera Data8.
51	UVOUT1	VI0_DATA1/VI0_B1(G P2_2)	I, 3.3V CMOS	VIN0 Camera Data9.
52	UVOUT2	VI0_DATA2/VI0_B2(G P2_3)	I, 3.3V CMOS	VIN0 Camera Data10.
53	UVOUT3	VI0_DATA3/VI0_B3(G P2_4)	I, 3.3V CMOS	VIN0 Camera Data11.
54	UVOUT4	VI0_DATA4/VI0_B4(G P2_5)	I, 3.3V CMOS	VIN0 Camera Data12.
55	UVOUT5	VI0_DATA5/VI0_B5(G P2_6)	I, 3.3V CMOS	VIN0 Camera Data13.
56	UVOUT6	VI0_DATA6/VI0_B6(G P2_7)	I, 3.3V CMOS	VIN0 Camera Data14.
57	UVOUT7	VI0_DATA7/VI0_B7(G P2_8)	I, 3.3V CMOS	VIN0 Camera Data15.
58	NC	-	-	-
59	NC	-	-	-
60	NC	-	-	-

Table 33 16bit Camera Connector2 Pin Out (J15)

Pin No	Pin Name	Signal Name	Signal Type / Termination	Description
1	GND	GND	Power	Ground.
2	GND	GND	Power	Ground.
3	GND	GND	Power	Ground.
4	YOUT0	VI3_CLKENB/VI1_G0(GP1_14)	I, 3.3V CMOS	VIN1 Camera Data0.
5	YOUT1	VI3_FIELD/VI1_G1(GP1_15)	I, 3.3V CMOS	VIN1 Camera Data1.
6	YOUT2	VI3_VSYNC#/VI1_G2(GP1_17)	I, 3.3V CMOS	VIN1 Camera Data2.
7	YOUT3	VI1_G3(GP1_20)	I, 3.3V CMOS	VIN1 Camera Data3.
8	YOUT4	VI1_G4(GP1_22)	I, 3.3V CMOS	VIN1 Camera Data4.
9	YOUT5	VI1_G5(GP1_12)	I, 3.3V CMOS	VIN1 Camera Data5.
10	YOUT6	VI2_FIELD/VI1_G6(GP1_9)	I, 3.3V CMOS	VIN1 Camera Data6.
11	YOUT7	VI2_G7/QSPI_IO2/VI1_G7(GP1_7)	I, 3.3V CMOS	VIN1 Camera Data7. <i>Note: This pin is optionally connected to 1st pin of expansion connector1 and default not populated.</i>
12	GND	GND	Power	Ground.
13	BCK	VI1_CLK(GP3_15)	I, 3.3V CMOS	VIN0 Camera Pixel Clock.
14	GND	GND	Power	Ground.
15	BDEN	VI1_CLKENB(GP1_26)	I, 3.3V CMOS	VIN1 Camera Data Enable.
16	BHD	VI1_HSYNC#(GP1_24)	I, 3.3V CMOS	VIN1 Camera Horizontal Synchronization.
17	BVD	VI1_VSYNC#(GP1_25)	I, 3.3V CMOS	VIN1 Camera Vertical Synchronization.
18	GND	GND	Power	Ground.
19	NC	-	-	-
20	GND	GND	Power	Ground.
21	NC	-	-	-
22	NC	-	-	-
23	GND	GND	Power	Ground.
24	GND	GND	Power	Ground.
25	GND	GND	Power	Ground.
26	GND	GND	Power	Ground.
27	NC	-	-	-
28	NC	-	-	-
29	NC	-	-	-
30	NC	-	-	-
31	EXTVIN	EXTVIN	O, 5V, Power	Camera Power Supply
32	EXTVIN	EXTVIN	O, 5V, Power	Camera Power Supply
33	EXTVIN	EXTVIN	O, 5V, Power	Camera Power Supply
34	EXTVIN	EXTVIN	O, 5V, Power	Camera Power Supply
35	NC	-	-	-

36	GND	GND	Power	Ground.
37	SCL	I2C3_SCL	O, 3.3V CMOS	I2C3 Clock.
38	SDA	I2C3_SDA	IO, 3.3V CMOS	I2C Data.
39	GND	GND	Power	Ground.
40	EXTRST	PRESETOUT#	O, 3.3V CMOS	Reset Out Active Low
41	PWDN	GPIO_EXP(GP1_21)	O, 3.3V CMOS/ 10K PD	Active high Camera Power Down. This pin is connected to GND in camera Add-On Module to enable the camera always. <i>Note: G1_21 signal is optionally connected to this pin through resistor and default not populated.</i>
42	NC	-	-	-
43	GND	GND	Power	Ground.
44	NC	-	-	-
45	NC	-	-	-
46	NC	-	-	-
47	NC	-	-	-
48	NC	-	-	-
49	NC	-	-	-
50	UVOUT0	VI1_B0/VI1_DATA0(GP3_0)	I, 3.3V CMOS	VIN1 Camera Data8.
51	UVOUT1	VI1_B1/VI1_DATA1(GP3_1)	I, 3.3V CMOS	VIN1 Camera Data9.
52	UVOUT2	VI1_B2/VI1_DATA2(GP3_2)	I, 3.3V CMOS	VIN1 Camera Data10.
53	UVOUT3	VI1_B3/VI1_DATA3(GP3_3)	I, 3.3V CMOS	VIN1 Camera Data11.
54	UVOUT4	VI1_B4/VI1_DATA4(GP3_4)	I, 3.3V CMOS	VIN1 Camera Data12.
55	UVOUT5	VI1_B5/VI1_DATA5(GP3_5)	I, 3.3V CMOS	VIN1 Camera Data13.
56	UVOUT6	VI1_B6/VI1_DATA6(GP3_6)	I, 3.3V CMOS	VIN1 Camera Data14.
57	UVOUT7	VI1_B7/VI1_DATA7(GP3_7)	I, 3.3V CMOS	VIN1 Camera Data15.
58	NC	-	-	-
59	NC	-	-	-
60	NC	-	-	-

3.4 Communication Features

3.4.1 CAN Header

The RZ/G1H Camera Add-On Module supports 2nd CAN interface through RZ/G1H CPU's CAN0 interface. This CAN0 signals from expansion connector2 (pins 41st & 45th) is connected to CAN Bus transceiver "SN65HVD230DR" and to 6pin custom CAN header (J4). Mode select pin (Rs) of the CAN Bus transceiver is optionally connected to RZ/G1H CPU GPIO "GP2_18" from expansion connector2. This CAN header (J4) is physically located at the top of the board as shown below.

Number of Pins : 6

Connector Part number : 53047-0610 from Molex

Mating Connector : 0510210600 from Molex with crimping pins

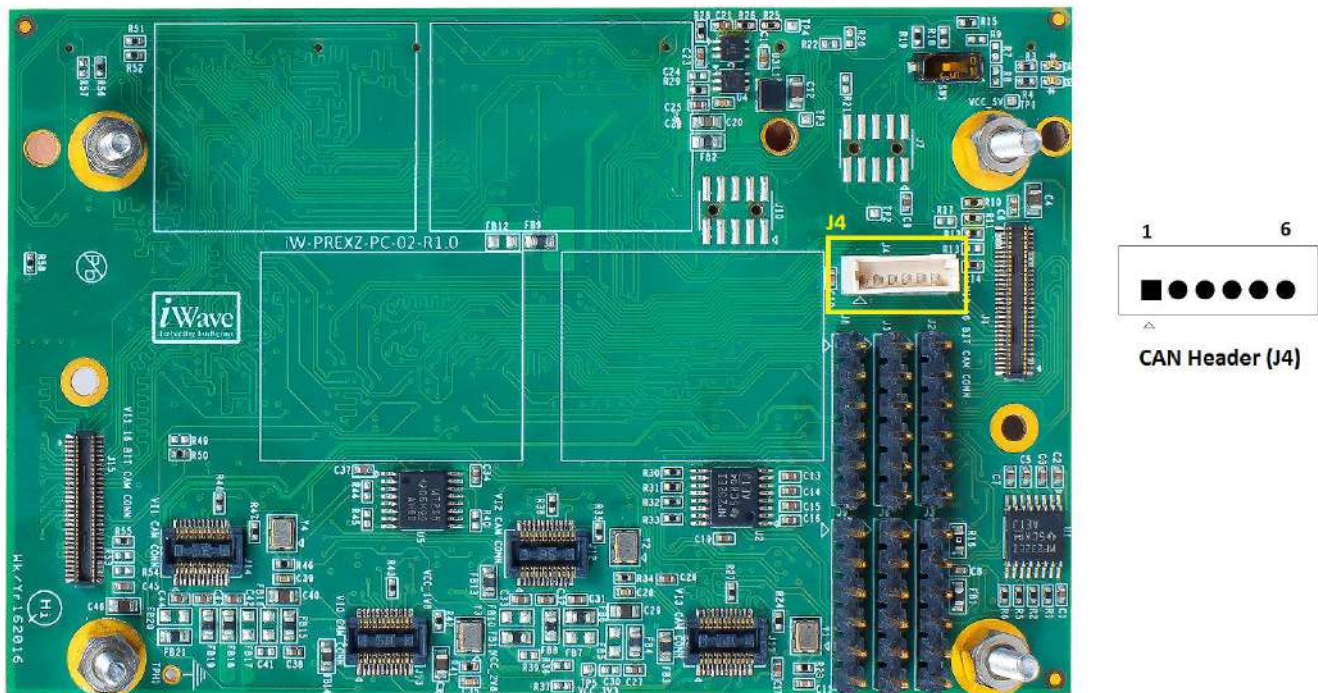


Figure 35: CAN Header

Table 34: CAN0 Header Pin Out

Pin No	Pin Name	Signal Name	Signal Type / Termination	Description
1	VCC_5V	VCC_5V_CAN	O, 5V Power	5V Supply Voltage.
2	NC	NC	-	NC.
3	CANL	CANL	IO, DIFF	CAN Differential negative.
4	GND	GND	Power	Ground.
5	CANH	CANH	IO, DIFF	CAN Differential positive.
6	GND	GND	Power	Ground.

3.4.2 10/100Mbps Ethernet Header

The RZ/G1H Camera Add-On Module supports Ethernet interface through RZ/G1H CPU's EtherMAC interface which supports 10/100Mbps Ethernet. The Ethernet PHY output signals from expansion connector2 is directly connected to 6pin custom Ethernet header (J5). Also it supports Speed (Yellow) and Link/Activity (Green) LED indications on Ethernet header (J5). This Ethernet header (J5) is physically located at the top of the board as shown below.

Number of Pins : 6

Connector Part number : 53047-0610 from Molex

Mating Connector : 0510210600 from Molex with crimping pins

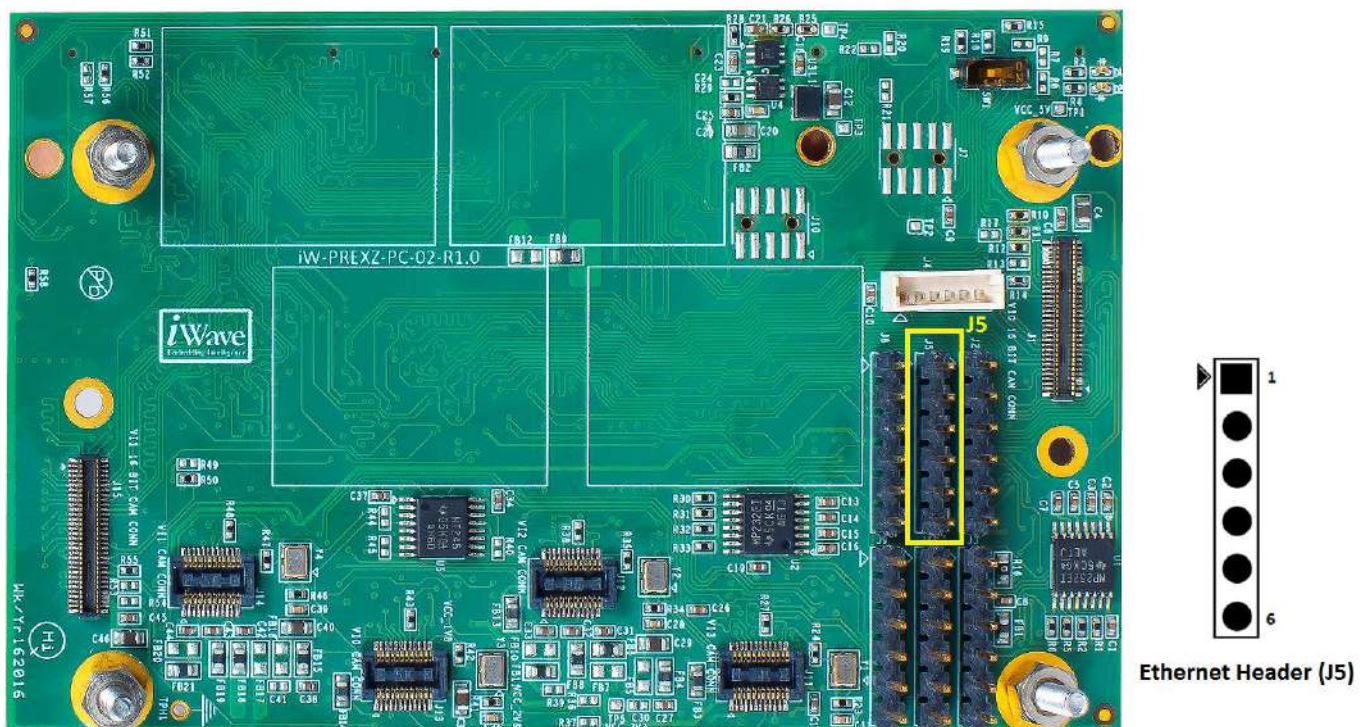


Figure 36 10/100 Ethernet Header

Table 35 10/100 Ethernet Header Pin Out

Pin No	Pin Name	Signal Name	Signal Type / Termination	Description
1	RXP	ETH_RXP	IO, Diff	10/100Mbps Ethernet Receive pair positive.
2	RXM	ETH_RXM	IO, Diff	10/100Mbps Ethernet Receive pair negative.
3	TXM	ETH_TXM	IO, Diff	10/100Mbps Ethernet Transmit pair negative.
4	TXP	ETH_TXP	IO, Diff	10/100Mbps Ethernet Transmit pair positive.
5	ACT_LED	ETH_SPEED_LED1	O, 3.3V CMOS	Ether speed indication LED
6	LINK_LCD	ETH_LINK_LED0	O, 3.3V CMOS	Ether Link/Activity indication LED

3.5 Serial Interface Features

3.5.1 Data UART Headers (RS232)

The RZ/G1H Camera Add-On Module supports five Data UART Headers J9, J6, J8, J3 & J2 to support UART interfaces through RZ/G1H CPU's SCIF0, SCIF1, SCIF2, SCIFB1 & HSCIF0 respectively. The UART interface signals from the Expansion connector2 is connected to "MAX3232E" RS232 transceiver which converts 3.3V level into RS232 level and connected to 6pin headers. These Data UART headers are physically located at the top of the board as shown below.

In RZ/G1H Camera Add-On Module, Data UART interface with Transmit & Receive signal only supported on SCIF0, SCIF1, SCIF2 & SCIFB1 headers. But Data UART interface with hardware flow control for request to send and clear to send signals also supported on HSCIF0 header (J2).

Number of Pins : 6

Connector Part number : 5-146280-6 from TE Connectivity

Mating Connector : 534237-4 from TE Connectivity

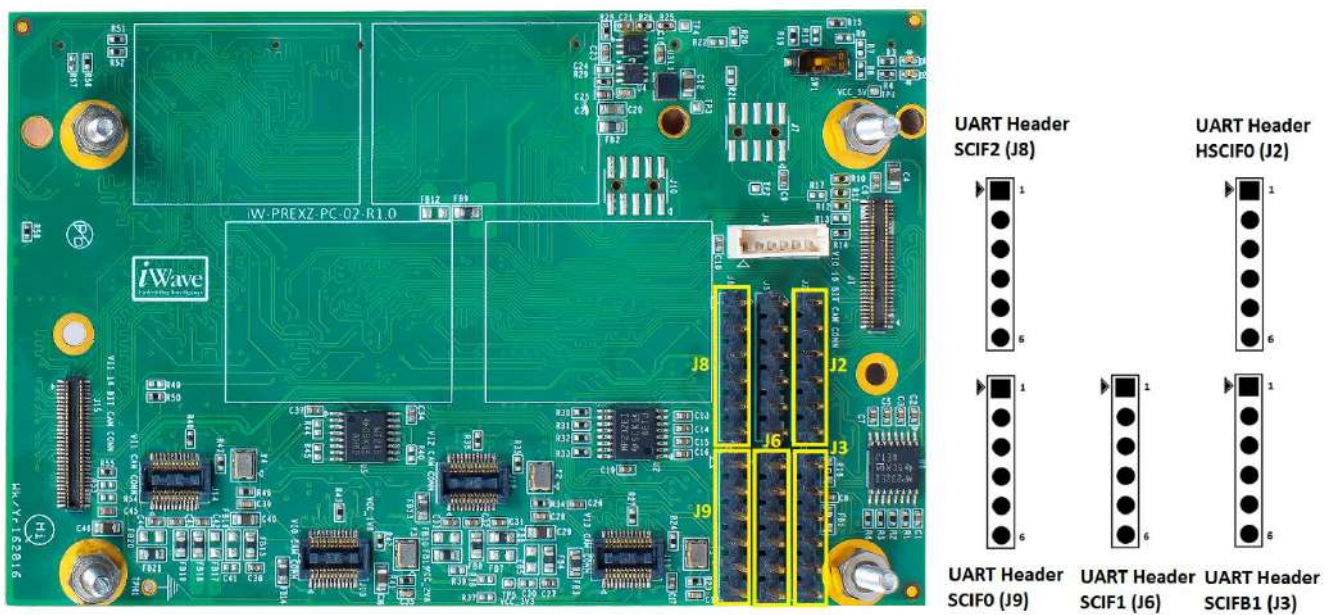


Figure 37: Data UART 0 Header

Table 36: SCIF0 UART Header Pin Out (J9)

Pin No	Pin Name	Signal Name	Signal Type / Termination	Description
1	GND	GND	Power	Ground.
2	NC	NC	-	NC.
3	VCC_3V3	VCC_3V3	O, 3.3V Power	3.3V Supply Voltage.
4	UART0_RXD	SCIF0_RX0(GP4_28)	I, RS232	SCIF0 Receive signal.
5	UART0_TXD	SCIF0_TX0/MD5(GP4_29)	O, RS232	SCIF0 Transmit signal.
6	NC	NC	-	NC.

Table 37 SCIF1 UART Header Pin Out (J6)

Pin No	Pin Name	Signal Name	Signal Type / Termination	Description
1	GND	GND	Power	Ground.
2	NC	NC	-	NC.
3	VCC_3V3	VCC_3V3	O, 3.3V Power	3.3V Supply Voltage.
4	UART1_RXD	SCIF1_RX1(GP5_0)	I, RS232	SCIF1 Receive signal.
5	UART1_TXD	SCIF1_TX1/MD3(GP5_1)	O, RS232	SCIF1 Transmit signal.
6	NC	NC	-	NC.

Table 38 SCIF2 UART Header Pin Out (J8)

Pin No	Pin Name	Signal Name	Signal Type / Termination	Description
1	GND	GND	Power	Ground.
2	NC	NC	-	NC.
3	VCC_3V3	VCC_3V3	O, 3.3V Power	3.3V Supply Voltage.
4	UART2_RXD	SCIF2_RX2(GP5_6)	I, RS232	SCIF2 Receive signal.
5	UART2_TXD	SCIF2_TX2(GP5_5)	O, RS232	SCIF2 Transmit signal.
6	NC	NC	-	NC.

Table 39 SCIFB1 UART Header Pin Out (J3)

Pin No	Pin Name	Signal Name	Signal Type / Termination	Description
1	GND	GND	Power	Ground.
2	CTS#	NC	-	NC.
3	VCC_3V3	VCC_3V3	O, 3.3V Power	3.3V Supply Voltage.
4	UART3_RXD	SCIFB1_RXD(GP4_15)	I, RS232	SCIFB1 Receive signal.
5	UART3_TXD	SCIFB1_TXD(GP4_16)	O, RS232	SCIFB1 Transmit signal.
6	RTS#	NC	-	NC.

Table 40: HSCIF0 UART Header Pin Out (J2)

Pin No	Pin Name	Signal Name	Signal Type / Termination	Description
1	GND	GND	Power	Ground.
2	UART4_CTS	HSCIF0_HCTS0#(GP5_10)	O, RS232	HSCIF1 Clear to Send signal.
3	VCC_3V3	VCC_3V3	O, 3.3V Power	3.3V Supply Voltage.
4	UART4_RXD	HSCIF0_HRX0(GP5_8)	I, RS232	HSCIF1Receive signal.
5	UART4_TXD	HSCIF0_HTX0/MD1(GP5_9)	O, RS232	HSCIF1Transmit signal.
6	UART4_RTS	HSCIF0_HRTS0#(GP5_11)	I, RS232	HSCIF1 Ready To Send signal.

4. TECHNICAL SPECIFICATION

This section provides detailed information about the RZ/G1H Qseven Carrier Board technical specification with Electrical, Environmental and Mechanical characteristics.

4.1 Electrical Characteristics

4.1.1 Power Input Requirement

The RZ/G1H Qseven Carrier Board is designed to work with a +12V external power and uses on board voltage regulators for internal power management. 12V power input from an external power supply is connected to the Qseven Carrier Board through Power Jack (J4). This 2.5mm x 6.5mm barrel connector Jack should fit standard DC Plugs with an inner dimension of 2.5mm and an outer dimension of 5.5mm (DC Plug Centre Pin is Positive). This connector is physically placed at the top of the board as shown below.

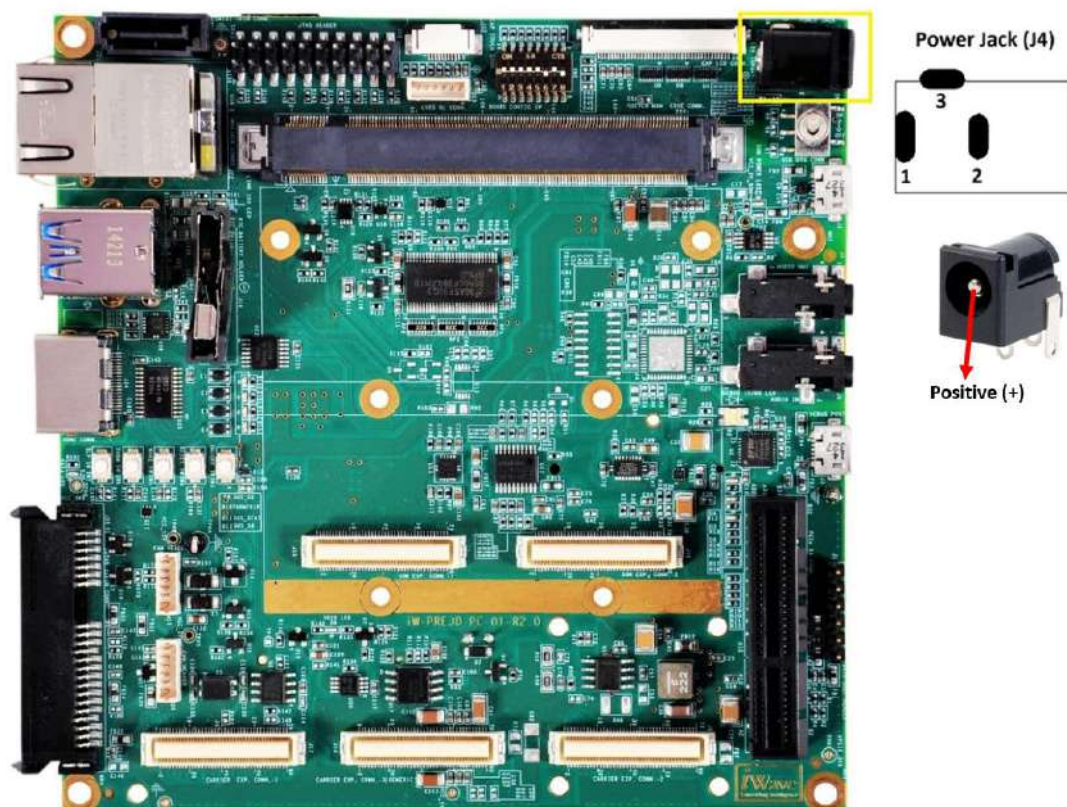


Figure 38: Power Jack

Table 41: Power Jack Pin Out

Pin No	Pin Name	Signal Name	Signal Type / Termination	Description
1	VCC	VCC_12V	12V, Power	Input Supply Voltage.
2	GND	GND	Power	Ground.
3	GND	GND	Power	Ground.

The below table provides the Power Input Requirement of RZ/G1H Qseven Carrier Board.

Table 42: Power Input Requirement

Sl. No.	Power Rail	Min (V)	Typical (V)	Max(V)	Max Input Ripple
1	VCC_12V ¹	11.75V	12V	12.25V	±50mV
2	VRTC_3V0 ²	2.8V	3V	3.3V	±20mV

¹ RZ/G1H Qseven Carrier Board is designed to work with 12V, 2A input power from external Power adapter.

² This voltage is from Coin cell holder and used as backup power source to RTC circuit of RZ/G1H Qseven SOM when SOM VCC is off. This is an optional power and required only if RTC functionality is used.

Important Note: All carrier board power supplies should be powered ON only after the RZ/G1H CPU is powered ON completely in the RZ/G1H Qseven SOM. This is to ensure that there is no back voltage (leakage) from any supply on the board towards the RZ/G1H CPU IO pins.

4.1.2 Power Output Specification

The RZ/G1H Qseven carrier board has dedicated power regulator to provide +5V power to Qseven SOM for VCC power supply. Also +3V RTC power from coin cell holder is provided to Qseven SOM for Real time clock support.

The RZ/G1H Qseven carrier board also shares on board +5V, +3.3V and +1.5V power to Expansion connector3 for Add-On Module power.

Table 43: Power Output Specification

Sl. No.	Power Rail	Min (V)	Typical (V)	Max(V)	Max Output Current (mA)
Power to Qseven SOM (through Qseven MXM connector)					
1	VCC_5V_SOM	4.85V	5V	5.15V	4000mA
2	VRTC_3V0	2.8V	3V	3.3V	-
Power to Add-On Module (through Expansion connector3)					
2	VCC_5V	4.85V	5V	5.15V	1500mA
3	VCC_3V3	3.15	3.3	3.45	1000mA
3	VCC_1V5	1.35	1.5	1.65	500mA

4.2 Environmental Characteristics

4.2.1 Environmental Specification

The below table provides the Environment specification of RZ/G1H Qseven Development Platform.

Table 44: Environmental Specification

Parameters	Min	Max
Operating temperature range (Commercial) ¹	0°C	60°C
Storage temperature range	0°C	60°C

¹ iWave only guarantees the component selection for the given operating temperature.

4.2.2 RoHS Compliance

iWave's RZ/G1H Qseven Development Platform is designed by using RoHS compliant components and manufactured on lead free production process.

4.2.3 Electrostatic Discharge

iWave's RZ/G1H Qseven Development Platform is sensitive to electro static discharge and so high voltages caused by static electricity could damage some of the devices on board. It is packed with necessary protection while shipping. Do not open or use board except at an electrostatic free workstation.

4.3 Mechanical Characteristics

4.3.1 RZ/G1H Qseven Carrier Board Mechanical Dimensions

The RZ/G1H Qseven carrier board PCB form factor is Nano ITX with 120mm x 120mm. Qseven Carrier Board mechanical dimension is shown below.

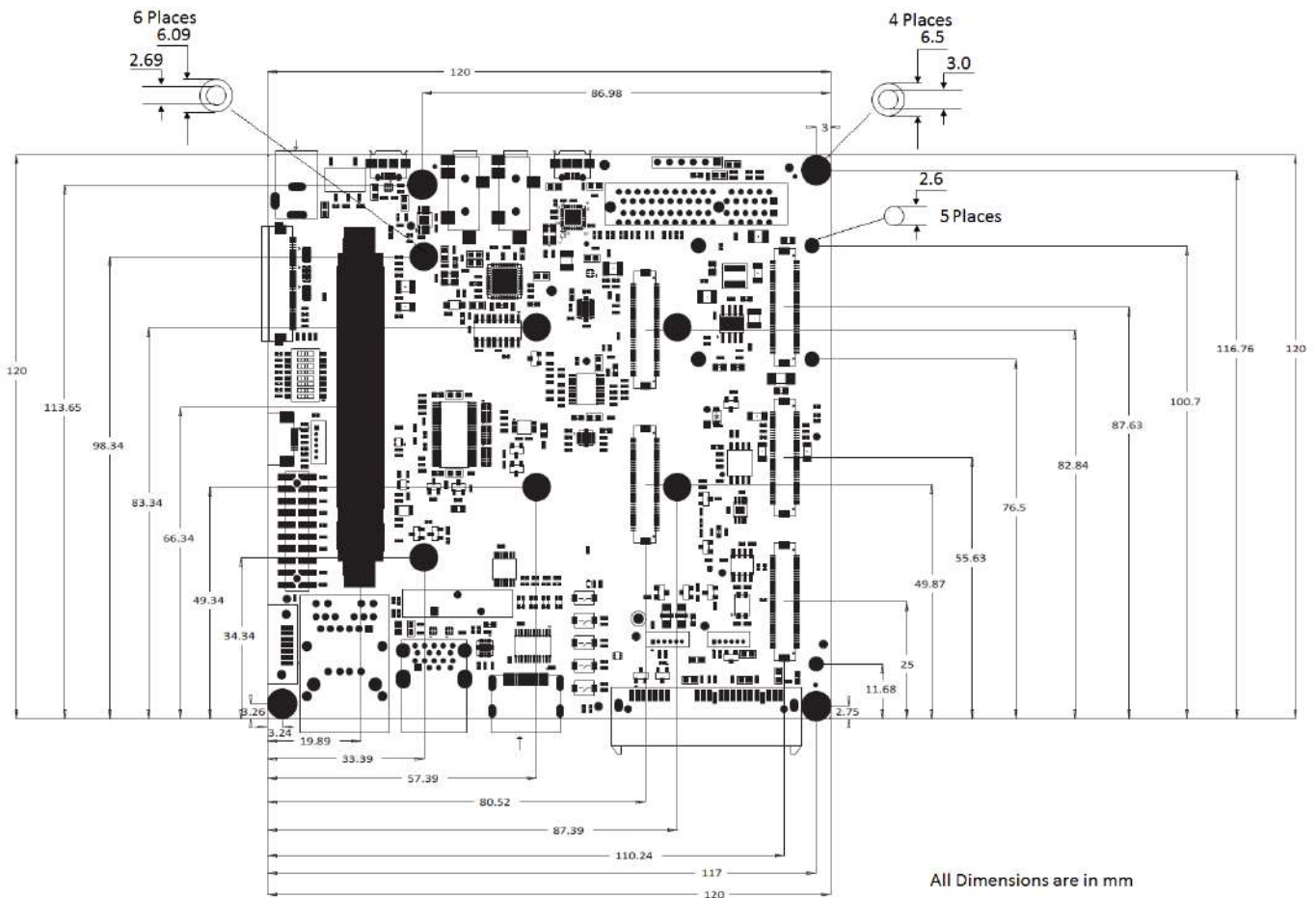


Figure 39: RZ/G1H Qseven carrier board Mechanical dimension – Top View

The RZ/G1H Qseven carrier board PCB thickness is 1.6mm±0.1mm, top side maximum height component is Ethernet Jack (23.24mm) and bottom side maximum height component is Ground Test Point (5.59mm). Please refer the below figure for height details of the RZ/G1H Qseven Carrier Board.

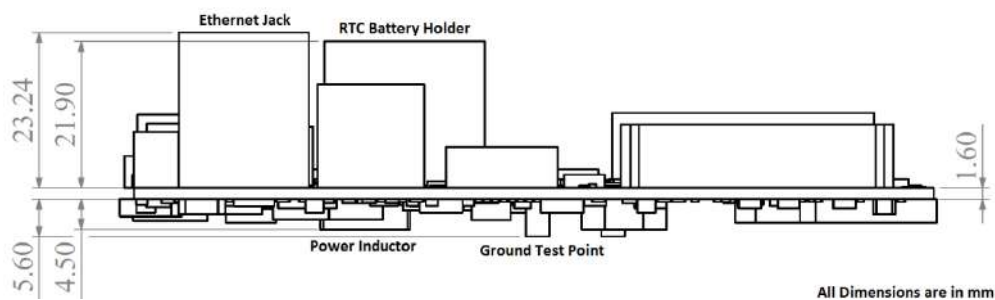


Figure 40: RZ/G1H Qseven carrier board Mechanical dimension - Side View

4.3.2 RZ/G1H Camera Add-On Module Mechanical Dimensions

The RZ/G1H Camera Add-On Module PCB form factor is 94mm x 60mm as shown below.

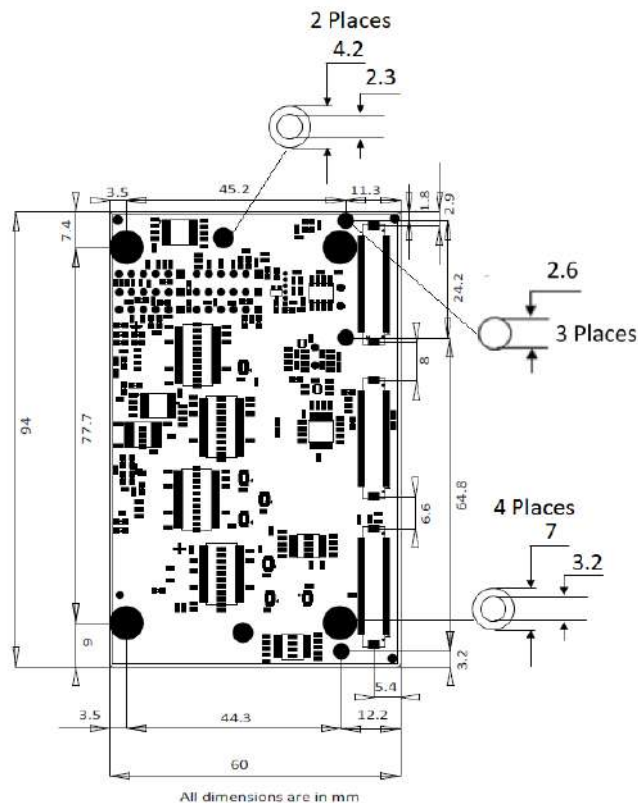


Figure 41: RZ/G1H Camera Add-On Module Mechanical dimension – Bottom View

4.3.3 Guidelines to insert the Qseven SOM into Carrier Board

- Make sure that power is not provided to the carrier board.
- Insert the Qseven module in to the MXM connector at an angle of 30° as shown below in the first photo.
- Check the Notch position of Qseven module is proper while inserting.
- Once the Qseven module is inserted to the MXM connector properly, press the board vertically down as shown below (in the second photo), such that the board is fixed firmly into the expansion connectors.

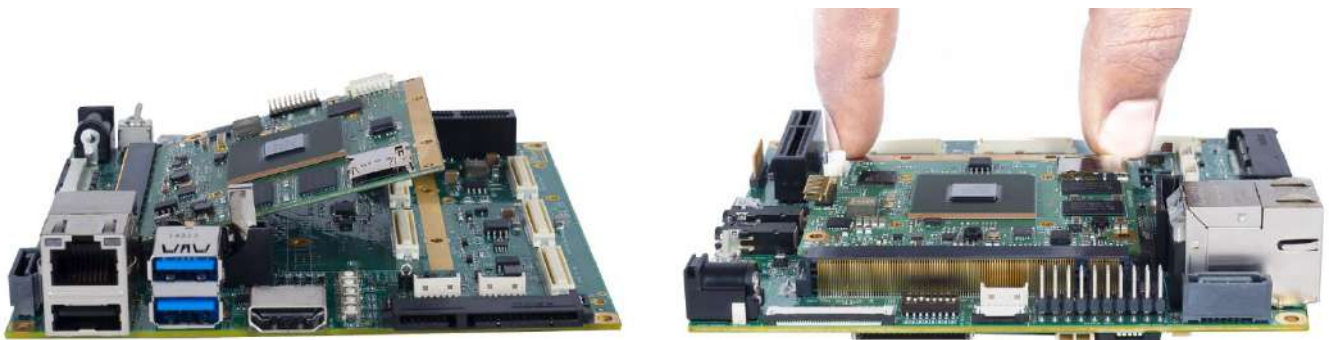


Figure 42: Qseven SOM Insertion procedure

5. ORDERING INFORMATION

The below table provides the standard orderable part numbers for RZ/G1H Qseven Development Platform which includes RZ/G1H Qseven SOM and Qseven carrier board.

Table 45: Orderable Product Part Numbers

Product Part Number	Description	Temperature
Rainbow G21D - RZ/G1H R4.0 Platform Version Development Kit (No HDMI)		
iW-G21D-Q74H-3D002G-E008G-LCK	RZ/G1H PF CPU, 2GB RAM, 8GB eMMC dev.kit with 7" CAP touch display - Linux (USB3.0 & PCIe)	Commercial
iW-G21D-Q74H-3D002G-E008G-LCL	RZ/G1H PF CPU, 2GB RAM, 8GB eMMC dev.kit without 7" CAP touch display - Linux (USB3.0 & PCIe)	Commercial
iW-G21D-Q74H-3D002G-E008G-LCM	RZ/G1H PF CPU, 2GB RAM, 8GB eMMC dev.kit with 7" CAP touch display - Linux (USB3.0 & SATA)	Commercial
iW-G21D-Q74H-3D002G-E008G-LCN	RZ/G1H PF CPU, 2GB RAM, 8GB eMMC dev.kit without 7" CAP touch display - Linux (USB3.0 & SATA)	Commercial
iW-G21D-Q74H-3D002G-E008G-LCO	RZ/G1H PF CPU, 2GB RAM, 8GB eMMC dev.kit with 7" CAP touch display - Linux (SATA & PCIe)	Commercial
iW-G21D-Q74H-3D002G-E008G-LCP	RZ/G1H PF CPU, 2GB RAM, 8GB eMMC dev.kit without 7" CAP touch display - Linux (SATA & PCIe)	Commercial
RZ/G1H Camera Add-On Module		
iW-G21D-DBCM-CA ¹	Camera Add-On Module for RZ/G1H Qseven SOM Development Platform	Commercial

¹ Camera Add-On Module does not come with Camera. Camera has to be purchased separately from Camera Manufacturer or contact iWave.

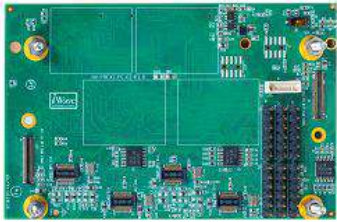
Note: For Development platform identification purpose, Product part number is pasted as Label with Barcode readable format.

6. APPENDIX

6.1 Camera Add-On Module Integration Procedure

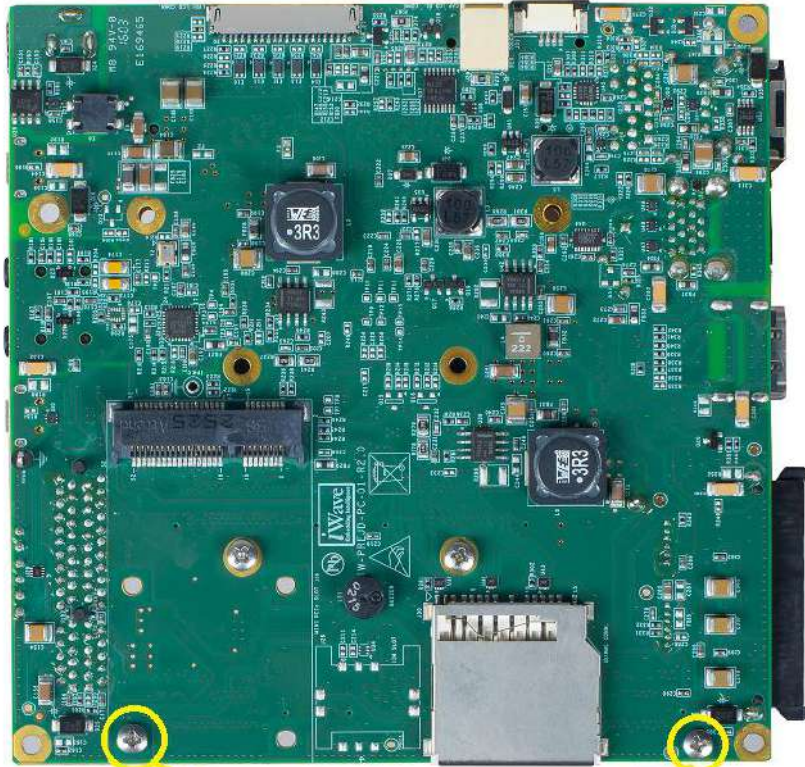
The RZ/G1H Camera Add-On Module comes with the following accessories.

Table 46: Camera Add-On Module Accessories

SL. No	Accessory Description	Image	Quantity
1	Camera Add-On Module		1
2	M2.5 x 12mm Pan Head Screw		2
3	M2.5 x 5mm Threaded Metallic Hex Spacer		2
4	2.5mm Non-Metallic Flat Washer		2
5	M2.5mm Nut		2

Follow the below step by step procedure to integrate the RZ/G1H Camera Add-On Module in to RZ/G1H Development platform.

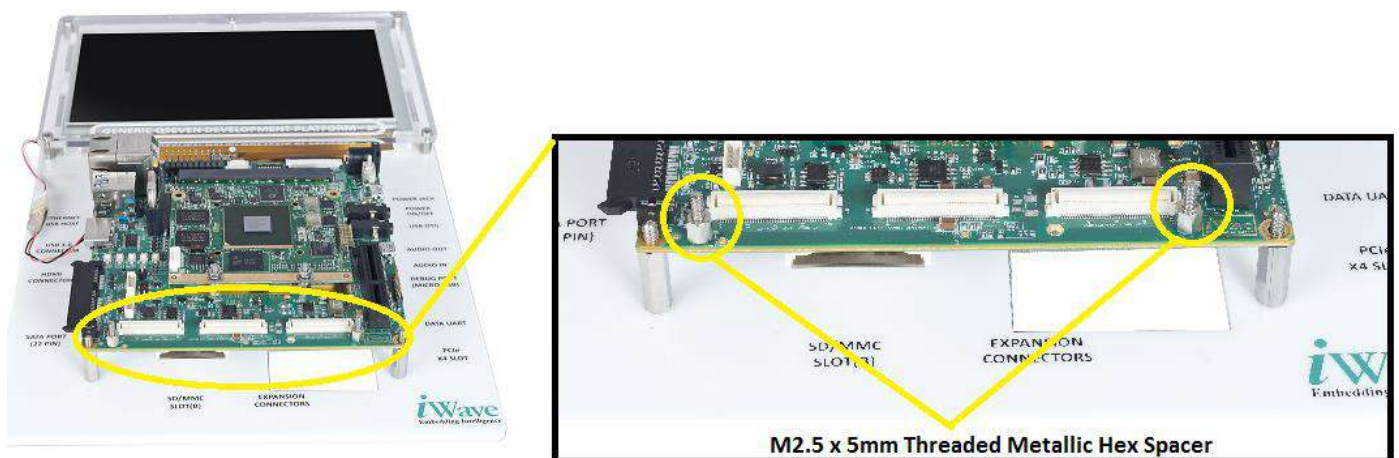
1. Insert M2.5x12mm pan head screw from RZ/G1H Qseven carrier board bottom side as shown below.



Insert M2.5x12mm Pan Head Screw

Figure 43: Insert Pan Head Screw

2. Tighten the M2.5 x 5mm threaded metallic hex spacer into the inserted screw from RZ/G1H Qseven carrier board top side as shown below.



M2.5 x 5mm Threaded Metallic Hex Spacer

Figure 44: Tighten Metallic Hex Spacer

3. Insert the Camera Add-On Module into the RZ/G1H Qseven carrier board through the M2.5mm screw as shown below. Press and make sure all three mating connector of Camera Add-On Module is inserted properly into the carrier board Expansion connectors.

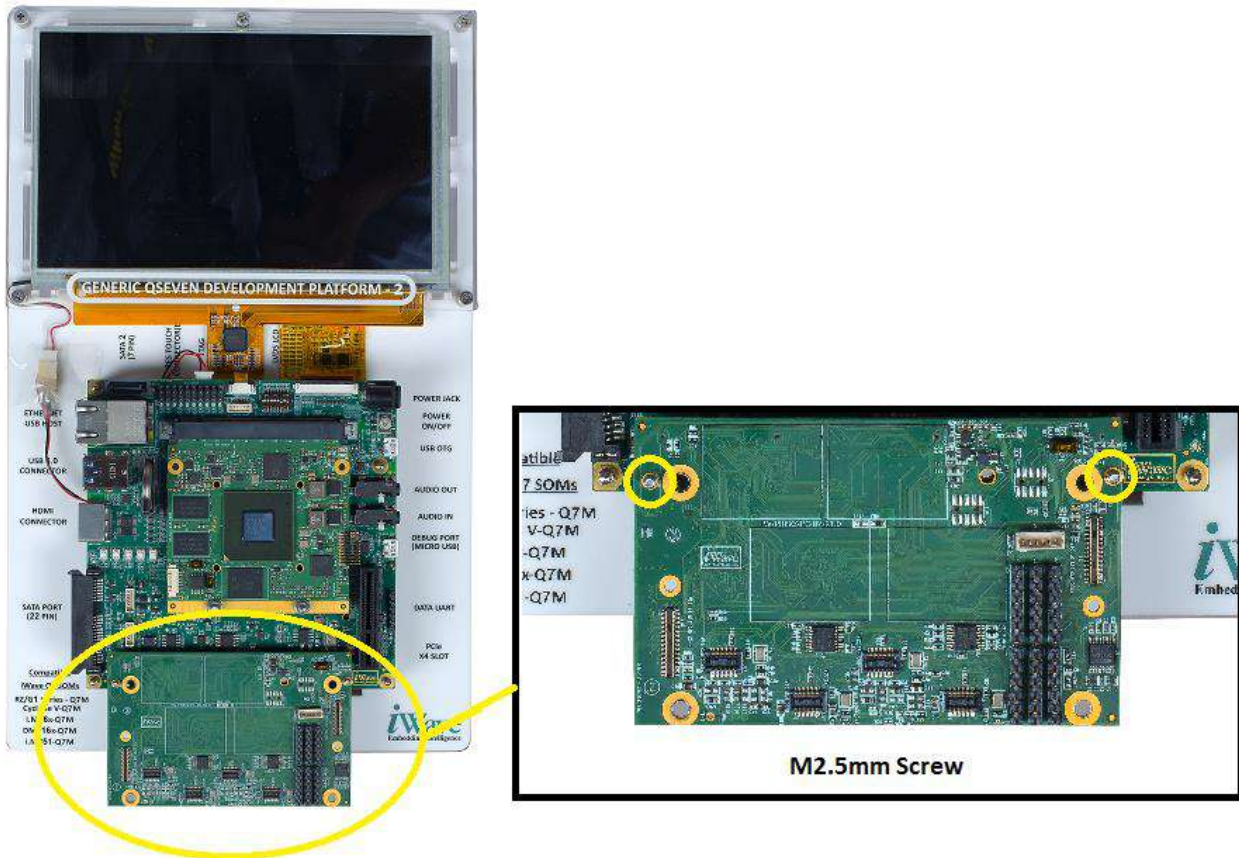


Figure 45: Insert Camera Add-On Module

4. Insert the 2.5mm Non-metallic flat washer into the screw as shown below.

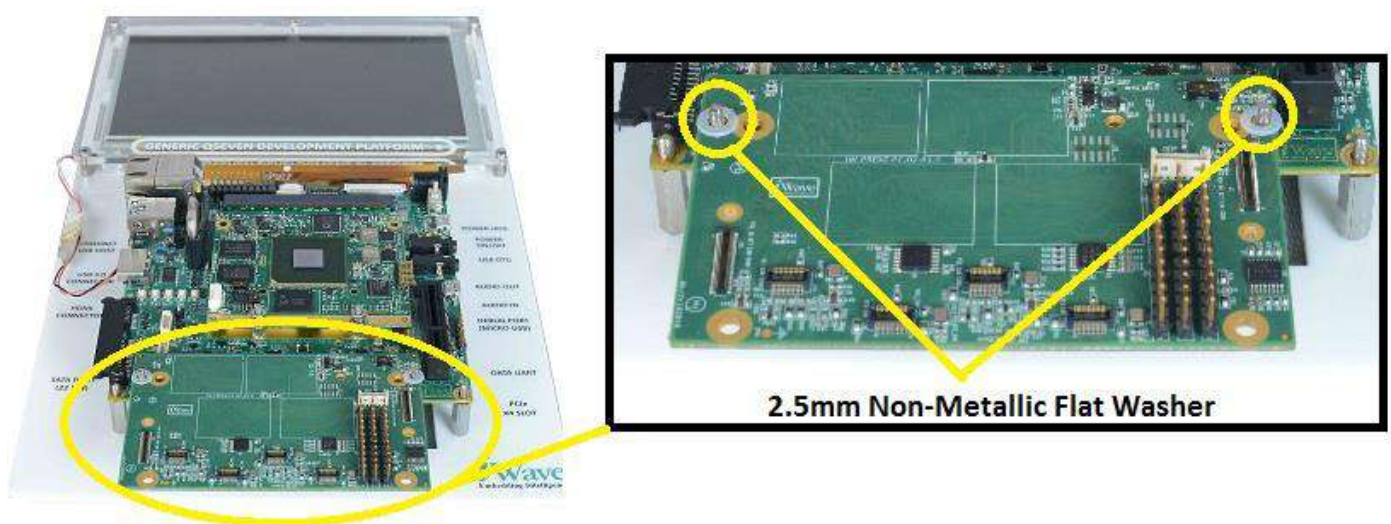


Figure 46: Insert Non-Metallic Flat Washer

- Finally, tighten the M2.5mm nut into screw as shown below to finish the RZ/G1H Camera Add-On Module integration in to RZ/G1H Development platform.

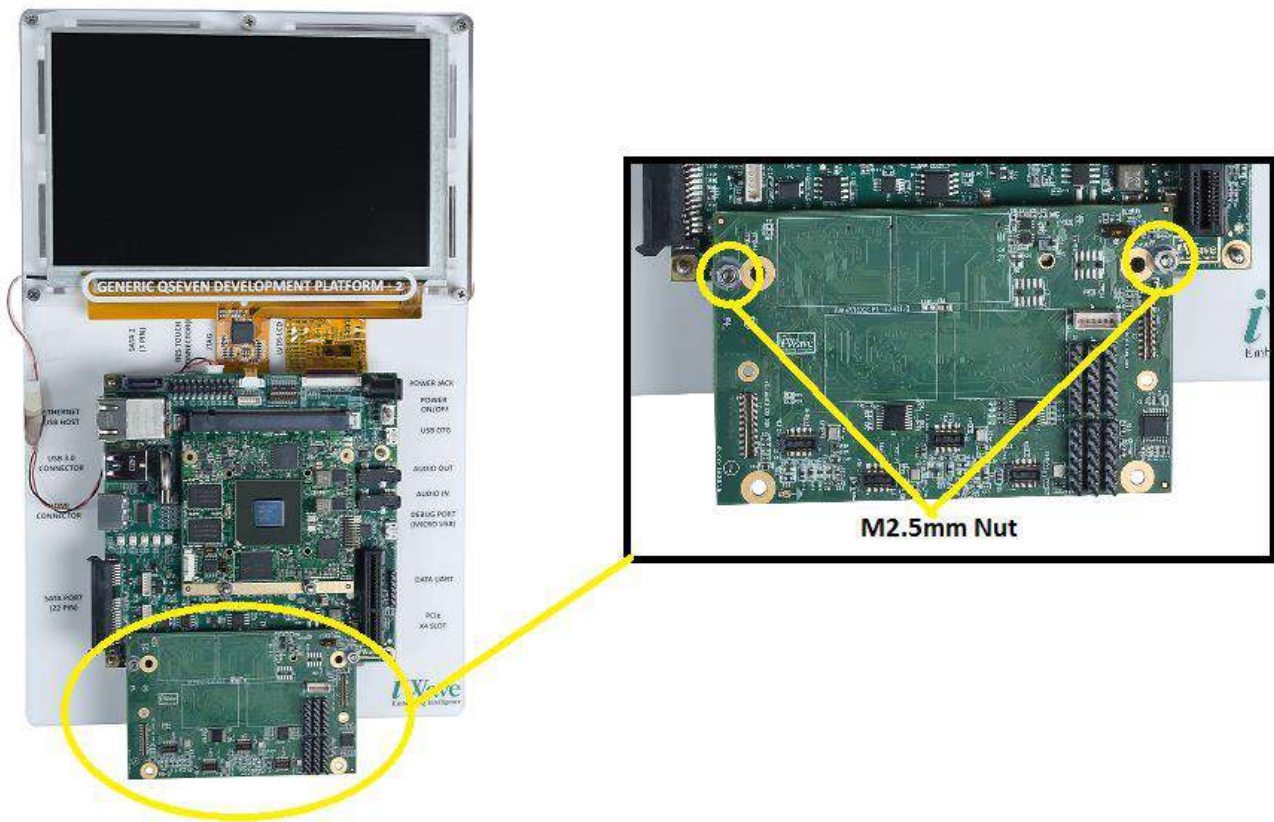


Figure 47: Tighten the Nut

6.2 8bit CMOS Cameras Connecting Procedure

Follow the below procedure to connect the 8bit CMOS camera in to the RZ/G1H Camera Add-On Module.

1. Connect the 8bit CMOS cameras in to the camera connectors (J13, J14, J12 and J11) of RZ/G1H Camera Add-On Module as shown below.

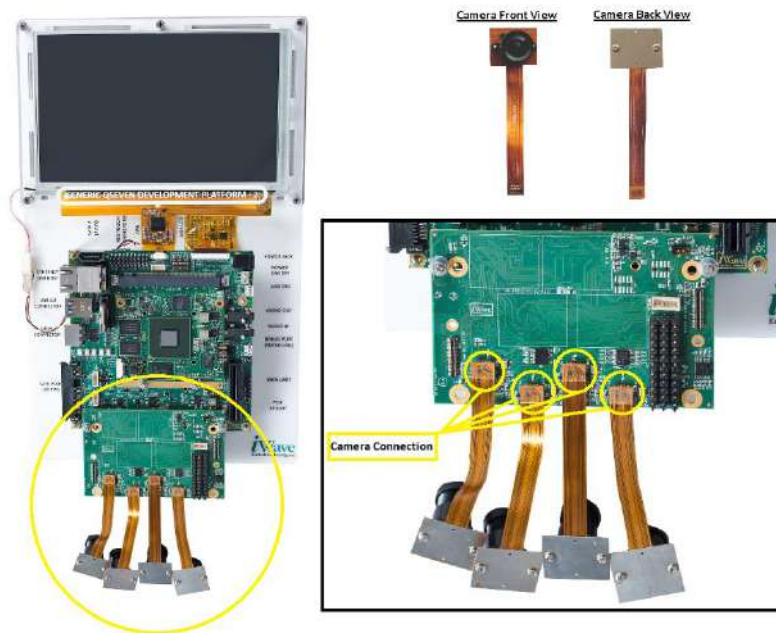


Figure 48: Camera Connection

2. Remove the Camera Lens Cap from cameras and fix it on the board as shown below if needed.

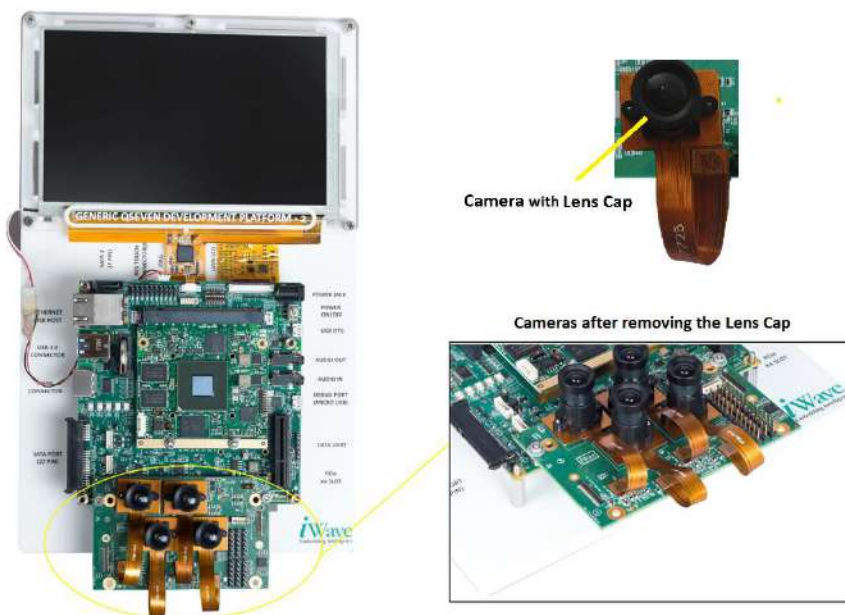


Figure 49: Camera Lens Cap

