iW-RainboW-G40D
i.MX 8M Plus Quad/QuadLite/Dual SMARC Development Platform Hardware User Guide

iWave
Embedding Intelligence

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1. INTRODUCTION

1.1 Purpose

The iW-RainboW-G40D i.MX 8M Plus SMARC SOM development platform incorporates i.MX 8M Plus Quad/QuadLite/Dual (Q/QL/D) SoC based SMARC SOM and generic SMARC Carrier board for complete validation of i.MX 8M Plus Q/QL/D SoC functionality. This document is the hardware user guide for the i.MX 8M Plus SMARC Carrier board. This guide provides detailed information on the overall design and usage of the SMARC carrier board from a hardware systems perspective. Complete information about the i.MX 8M Plus SMARC SOM hardware is explained in another document "iW-RainboW-G40M-i.MX 8M Plus-SMARC-SOM-HardwareUserGuide".

1.2 Overview

iW-RainboW-G40D-i.MX 8M Plus Development Platform comes with i.MX 8M Plus Q/QL/D based SMARC SOM, SMARC V2.1.1 Generic Carrier. The development board can be used for quick prototyping of various applications targeted by the i.MX 8M Plus Q/QL/D application processor. With the 120mmx120mm Nano ITX form factor, SMARC carrier board is highly packed with all the necessary on-board connectors to validate the features of i.MX 8M Plus Q/QL/D SMARC SOM.

1.3 List of Acronyms

The following acronyms will be used throughout this document.

Table 1: Acronyms & Abbreviations

Acronyms	Abbreviations
CMOS	Complementary Metal-Oxide Semiconductor
CPU	Central Processing Unit
CSI	Camera Serial Interface
DSI	Display Serial Interface
eMMC	Enhanced Multi Media Card
GB	Giga Byte
Gbps	Gigabits per sec
GPIO	General Purpose Input Output
Hz	Hertz
I2C	Inter-Integrated Circuit
I2S	Inter-IC Sound Bu
IC	Integrated Circuit
MIPI	Mobile Industry Processor Interface
PCB	Printed Circuit Board
RoHS	Restriction of Hazardous Substances
RTC	Real Time Clock

Acronyms	Abbreviations
SD	Secure Digital
SMARC SOM	Smart Mobility Architecture
TBD	To Be Defined
UART	Universal Asynchronous Receiver/Transmitter
USB	Universal Serial Bus
USB OTG	USB On The Go
V	Voltage

1.4 Terminology Description

In this document, wherever Signal Type is mentioned, below terminology is used.

Table 2: Terminology

Terminology	Description
I	Input Signal
O	Output Signal
IO	Bidirectional Input/output Signal
CMOS	Complementary Metal Oxide Semiconductor Signal
DIFF	Differential Signal
LVDS	Low Voltage Differential Signal
GBE	Gigabit Ethernet Media Dependent Interface differential pair signals
USB HS	Universal Serial Bus High Speed differential pair signals
USB SS	Universal Serial Bus Super Speed differential pair signals
MIPI	Mobile Industry Processor Interface signals
TMDS	Transition Minimized Differential Signaling
OD	Open Drain Signal
OC	Open Collector Signal
Power	Power Pin
PU	Pull Up
PD	Pull Down
NA	Not Applicable
NC	Not Connected

Note: Signal Type does not include internal pull-ups or pull-downs implemented by the chip vendors and only includes the pull-ups or pull-downs implemented On-SMARC SOM.

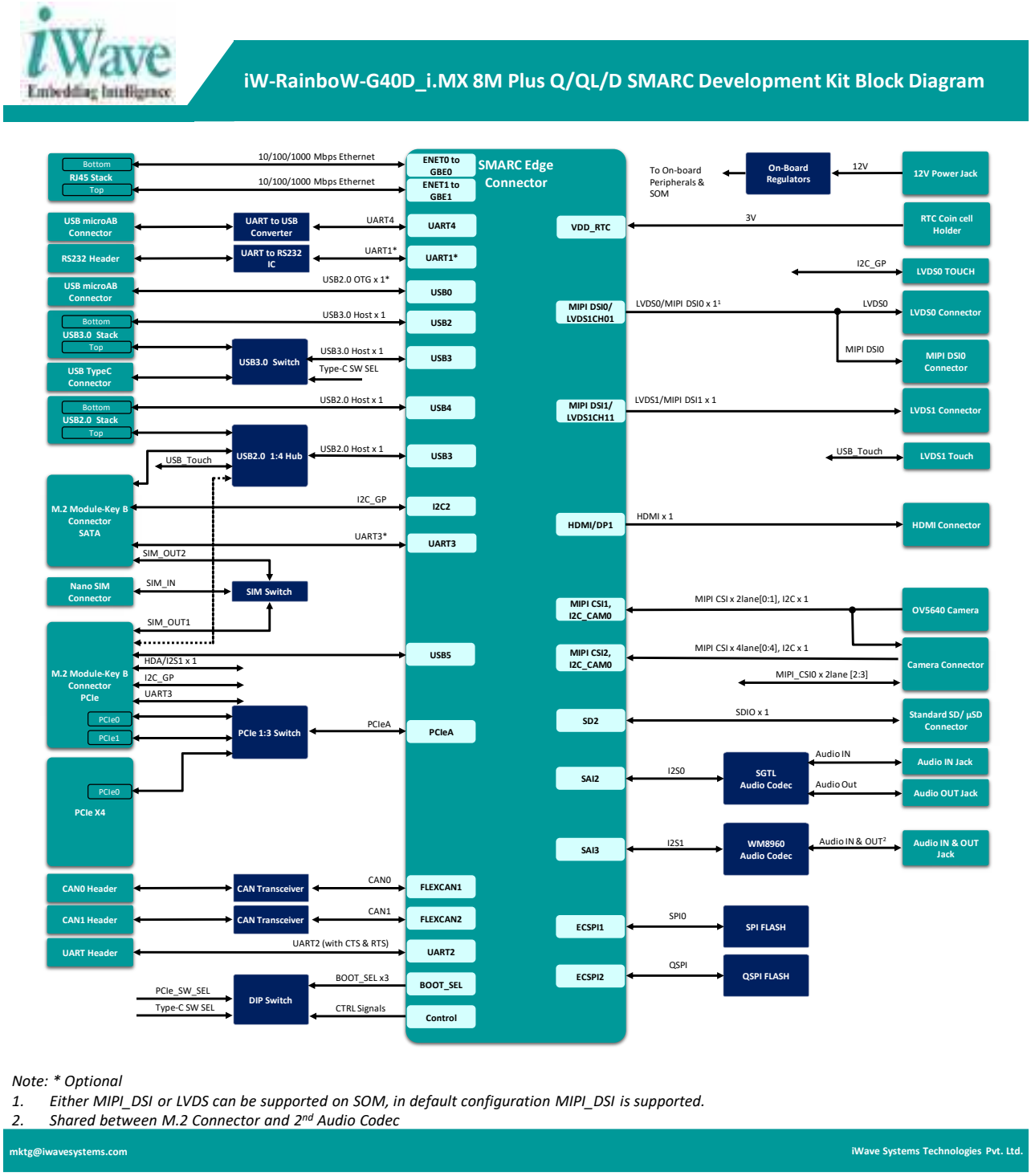
1.5 References

- IMX8MPXEC_Rev_x.pdf
- iMX_8M_Plus_RM_Revx.pdf
- SMARC Specification V2.1.1

2. ARCHITECTURE AND DESIGN

This section provides detailed information about the i.MX 8M Plus Q/QL/D SMARC SOM Development Platform Carrier board features with high level block diagram and detailed information about each block.

2.1 i.MX 8M Plus Q/QL/D SMARC Development Platform Block Diagram



*Note: * Optional*

1. *Either MIPI_DSI or LVDS can be supported on SOM, in default configuration MIPI_DSI is supported.*
2. *Shared between M.2 Connector and 2nd Audio Codec*

Figure 1: i.MX 8M Plus Q/QL/D SMARC Development Platform Block Diagram

2.2 i.MX 8M Plus Q/QL/D SMARC Development Platform Features

The i.MX 8M Plus Q/QL/D SMARC carrier board supports the following features to validate the NXP's i.MX 8M Plus Q/QL/D SMARC SOM Edge connector interfaces.

Serial Interface Features

- Debug UART through USB Micro AB Connector
- Data UART x 1 Port through Header
- RS232 UART Interface (Optional)

High Speed Interface Features

- PCIe x 1 Port through x4 connector or M.2 connector [1,2]
- USB 3.0 Host x 2 Port through USB 3.0 Type A Connector[3]
- USB Type C x 1 Port[3]

Communication Features

- Dual 10/100/1000Mbps Ethernet through dual stack RJ45MagJack
- USB 2.0 Host x 2 Ports through USB 2.0 dual stack USB Type A Connector
- SDHC/SDIO (4bit) x 1 Port through Standard SD Connector
- CAN FD x 2 Port through Header
- USB2.0 OTG Interface (Optional)

Audio & Video Features

- MIPI DSI 4lane Display connector with Capacitive touch
- MIPI CSI 2lane Camera Connector
- HDMI X 1 Port through Type A Connector
- I2S Audio codec with 3.5mm Audio IN and OUT Jack
- LVDS0 Connector (Optional)
- LVDS1 Display Connector

Additional Features

- QSPI and SPI Flash
- RTC Coin Cell holder
- Capacitive Touch Connector
- LVDS Backlight Header

On Board Switches

- Power ON/OFF Switch
- Board Configuration DIP Switch
- Boot Selection DIP Switch

- Reset Switch
- Force Recovery switch

General Specification

- Power Supply : 12V, 2A Power Input Jack
- Temperature Supported: 0°C to +60°C
- Form Factor : 120mm X 120mm Nano ITX

[1.] PCIe Channel A can be connected to either M.2 Connector or PETp0 of PCIe X4 connector by using on Board Switches.

[2.] At a time, do not set Both the PCIe Channel A & B neither to M.2 connector nor to PCIe X4 connector.

[3.] Either USB Type C connector or USB 3.0 Type A TOP connector can be supported at a time. Anyone can be selected using on Board Switches.

2.3 SMARC MXM Connector

The i.MX 8M Plus Q/QL/D SMARC carrier board supports 314Pin SMARC MXM Edge mating connector for SMARC SOM attachment. This standard 314-pin robust connector is capable of handling high-speed serialized signals and can be used for size constrained embedded applications. This SMARC MXM Edge mating connector (J18) is physically located at the top of the board as shown below.

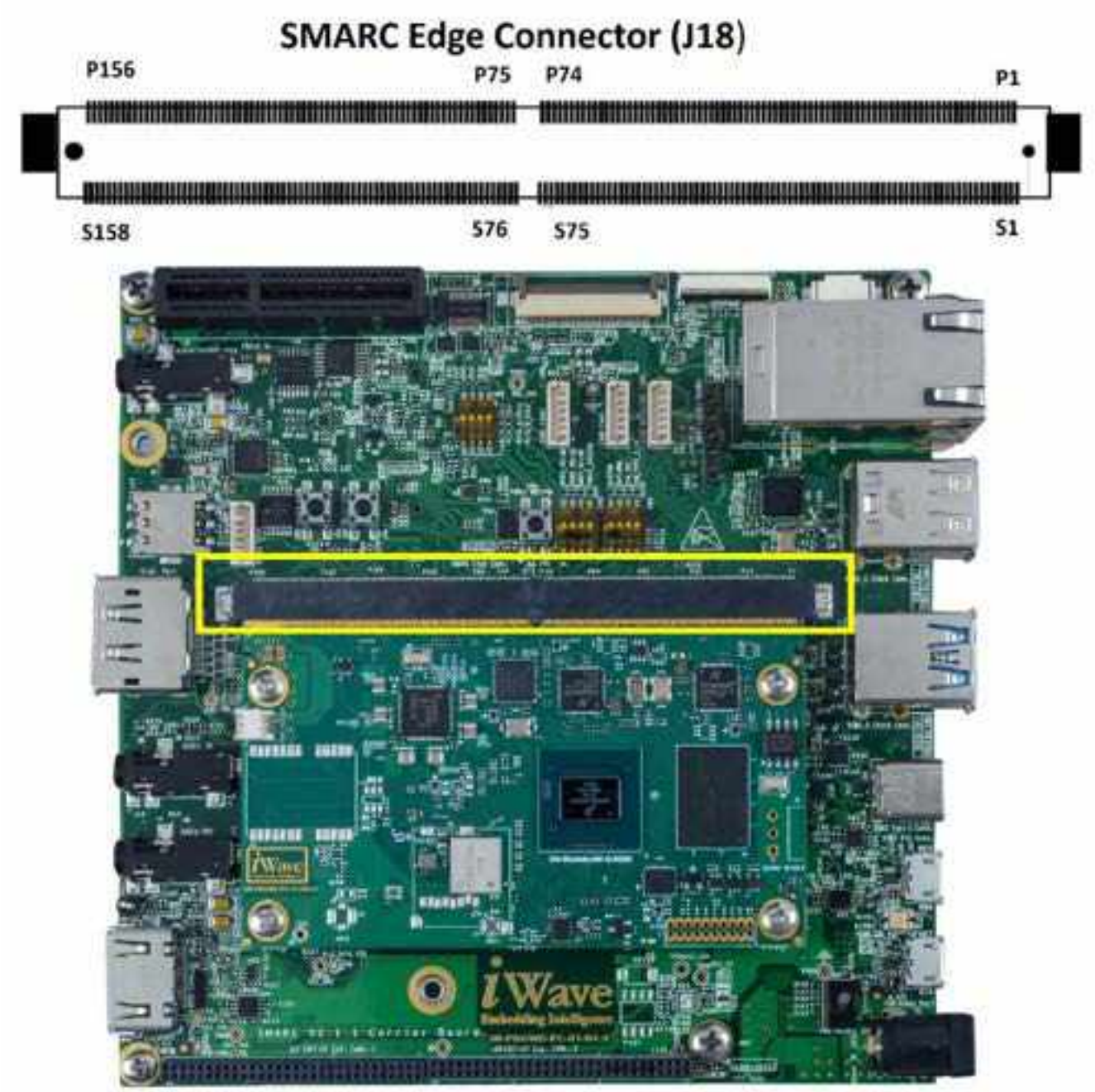


Figure 2: SMARC MXM Connector

2.3.1 SMARC PCB Edge Connector Pin Assignment

Table 3: SMARC MXM Connector Pin Assignment

Pin No.	SMARC Edge Connector Pin Name	Signal Name	CPU Ball Name/Pin Number	Signal Type/ Termination	Description
SMARC Primary Side					
P1	SMB_ALERT#	GPIO_SMB_ALERT_GPIO5_02	SAI3_MCLK/AJ20	I, 1.8V CMOS	SM Bus Alert# (interrupt) Signal through GPIO.
P2	GND	GND	NA	Power	Ground.
P3	CSI1_CK+	MIPI_CSI2_CLK_P	MIPI_CSI2_CLK_P/A23	O, MIPI	MIPI CSI2 differential clock positive.
P4	CSI1_CK-	MIPI_CSI2_CLK_N	MIPI_CSI2_CLK_N/B23	O, MIPI	MIPI CSI2 differential clock negative.
P5	GBE1_SDP	GBE1_PPS_SDP	NA	NA	NC.
P6	GBE0_SDP	GBE0_PPS_SDP	NA	O, 3.3V CMOS	NC
P7	CSI1_RX0+	MIPI_CSI2_D0_P	MIPI_CSI2_D0_P/ A25	O, MIPI	MIPI CSI2 differential data lane 0 positive.
P8	CSI1_RX0-	MIPI_CSI2_D0_N	MIPI_CSI2_D0_N/ B25	O, MIPI	MIPI CSI2 differential data lane 0 negative.
P9	GND	GND	NA	Power	Ground.
P10	CSI1_RX1+	MIPI_CSI2_D1_P	MIPI_CSI2_D1_P/ A24	O, MIPI	MIPI CSI2 differential data lane 1 positive.
P11	CSI1_RX1-	MIPI_CSI2_D1_N	MIPI_CSI2_D1_N/ B24	O, MIPI	MIPI CSI2 differential data lane 1 negative.
P12	GND	GND	NA	Power	Ground.
P13	CSI1_RX2+	MIPI_CSI2_D2_P	MIPI_CSI2_D2_P/ A22	O, MIPI	MIPI CSI2 differential data lane 2 positive.
P14	CSI1_RX2-	MIPI_CSI2_D2_N	MIPI_CSI2_D2_N/ B22	O, MIPI	MIPI CSI2 differential data lane 2 negative.
P15	GND	GND	NA	Power	Ground.
P16	CSI1_RX3+	MIPI_CSI2_D3_P	MIPI_CSI2_D3_P/ A21	O, MIPI	MIPI CSI2 differential data lane 3 positive.
P17	CSI1_RX3-	MIPI_CSI2_D3_N	MIPI_CSI2_D3_N/ B21	O, MIPI	MIPI CSI2 differential data lane 3 negative.
P18	GND	GND	NA	Power	Ground.
P19	GBE0_MDI3-	GBE0_MDI3-	NA	IO, GBE	Gigabit Ethernet0 MDI differential pair 3 negative to bottom port of Dual Magjack.
P20	GBE0_MDI3+	GBE0_MDI3+	NA	IO, GBE	Gigabit Ethernet0 MDI differential pair 3 positiveto bottom port of Dual Magjack.
P21	GBE0_LINK100#	GBE0_LINK100#	NA	I, 3.3V CMOS	Ethernet0 100Mbps linkstatus LED

Pin No.	SMARC Edge Connector Pin Name	Signal Name	CPU Ball Name/Pin Number	Signal Type/ Termination	Description
					signal to bottom port of Dual Magjack.
P22	GBE0_LINK1000#	GBE0_LINK1000#	NA	I, 3.3V CMOS	Gigabit Ethernet0 1000Mbps link status LED signal.
P23	GBE0_MDI2-	GBE0_MDI2-	NA	IO, GBE	Gigabit Ethernet0 MDI differential pair 2 negative to bottom port of Dual Magjack.
P24	GBE0_MDI2+	GBE0_MDI2+	NA	IO, GBE	Gigabit Ethernet0 MDI differential pair 2 positiveto bottom port of Dual Magjack.
P25	GBE0_LINK_ACT#	GBE0_LINK_ACT#	NA	I, 3.3V CMOS	Gigabit Ethernet0 activitystatus LED signal to bottom port of Dual Magjack.
P26	GBE0_MDI1-	GBE0_MDI1-	NA	IO, GBE	Gigabit Ethernet0 MDI differential pair 1 negative to bottom port of Dual Magjack.
P27	GBE0_MDI1+	GBE0_MDI1+	NA	IO, GBE	Gigabit Ethernet0 MDI differential pair 1 positiveto bottom port of Dual Magjack.
P28	GBE0_CTREF	VPHY0_DVDDL	NA	I, 3.3V Power	CTREF Power for Ethernet0 to Centre Tapof bottom port of Dual Magjack.
P29	GBE0_MDI0-	GBE0_MDI0-	NA	IO, GBE	Gigabit Ethernet0 MDI differential pair 0 negative to bottom port of Dual Magjack.
P30	GBE0_MDI0+	GBE0_MDI0+	NA	IO, GBE	Gigabit Ethernet0 MDI differential pair 0 positiveto bottom port of Dual Magjack.
P31	SPI0_CS1#	NC	NA	-	NC.
P32	GND	GND	NA	Power	Ground.

Pin No.	SMARC Edge Connector Pin Name	Signal Name	CPU Ball Name/Pin Number	Signal Type/ Termination	Description
P33	SDIO_WP	GPIO2_20(SD2_WP)	SD2_WP/AC26	O, 1.8V/3.3V CMOS	SD write Protect.
P34	SDIO_CMD	SD2_CMD	SD2_CMD/AB28	IO, 1.8/3.3V CMOS	SD command.
P35	SDIO_CD#	GPIO2_12(SD2_CD_B)	SD2_CD_B/AD29	O, 1.8V/3.3V CMOS	SD Card Detect.
P36	SDIO_CK	SD2_CLK	SD2_CLK/ AB29	I, 1.8/3.3V CMOS	SD Clock.
P37	SDIO_PWR_EN	GPIO2_19(SD2_RESET_B)	SD2_RESET_B/ AD28	I, 3.3V CMOS	SD Power enable.
P38	GND	GND	NA	Power	Ground.
P39	SDIO_D0	SD2_DATA0	SD2_DATA0/ AC28	IO, 1.8/3.3V CMOS	SD data 0.
P40	SDIO_D1	SD2_DATA1	SD2_DATA1/ AC29	IO, 1.8/3.3V CMOS	SD data 1
P41	SDIO_D2	SD2_DATA2	SD2_DATA2/ AA26	IO, 1.8/3.3V CMOS	SD data 2
P42	SDIO_D3	SD2_DATA3	SD2_DATA3/ AA25	IO, 1.8/3.3V CMOS	SD data 3
P43	SPI0_CS0#	ECSPI1_SS0	ECSPI1_SS0/AE20	I, 1.8V CMOS	eCSPI1 Chip Select 0.
P44	SPI0_CK	ECSPI1_SCLK	ECSPI1_SCLK/AF20	I, 1.8V CMOS	eCSPI1 Clock.
P45	SPI0_DIN	ECSPI1_MISO	ECSPI1_MISO/AD20	O, 1.8V CMOS	eCSPI1 Master In Slave Out.
P46	SPI0_DO	ECSPI1_MOSI	ECSPI1_MOSI/AC20	I, 1.8V CMOS	eCSPI1 Master Out Slave In.
P47	GND	GND	NA	Power	Ground.
P48	SATA_TX+	NC	NA	-	NC.
P49	SATA_TX-	NC	NA	-	NC.
P50	GND	GND	NA	Power	Ground.
P51	SATA_RX+	NC	NA	-	NC.
P52	SATA_RX-	NC	NA	-	NC.
P53	GND	GND	NA	Power	Ground.
P54	SPI1_CS0# / ESPI_CS0# / QSPI_CS0#	ECSPI2_SS0	ECSPI2_SS0/AJ22	I, 1.8V CMOS	eCSPI2 Chip Select 0.
P55	SPI1_CS1# / ESPI_CS1# / QSPI_CS1#	NC	NA	-	eCSPI2 Chip Select 1.
P56	SPI1_CK / ESPI_CK / QSPI_CK	ECSPI2_SCLK	ECSPI2_SCLK/AH21	I, 1.8V CMOS	eCSPI2 Clock.
P57	SPI1_DIN / ESPI_IO_1 / QSPI_IO_1	ECSPI2_MISO(I2C4_SCL)	I2C4_SCL/ AF8	IO, 1.8V CMOS	eCSPI2 DATA 0.

Pin No.	SMARC Edge Connector Pin Name	Signal Name	CPU Ball Name/Pin Number	Signal Type/ Termination	Description
P58	SPI1_DO / ESPI_IO_0 / QSPI_IO_0	ECSPI2_MOSI	ECSPI2_MOSI/AJ21	IO, 1.8V CMOS	eCSPI2 DATA 1.
P59	GND	GND	NA	Power	Ground.
P60	USB0+	USB0_DP (Optionally USB_OTG1_DP)	USB1_D_P/D10	IO, USB HS	NC. *Note: USB Port0 Data Positive to USB2.0 OTG connector (J22). Note: This is optional feature in SOM.*
P61	USB0-	NC (Optionally USB_OTG1_D M)	USB1_D_N/E10	IO, USB HS	NC. *Note: USB Port0 Data Negative to USB2.0 OTG connector (J22). Note: This is optional feature in SOM.*
P62	USB0_EN_OC#	NC (Optionally USB1_OTG_OC(GPI O 1_IO13))	GPIO1_IO13/A6	IO, 3.3V CMOS	NC. *Note: USB Port0 PowerEnable/ Over Current Indicator. Note: This is optional feature in SOM.*
P63	USB0_VBUS_DET	NC (Optionally VBUS_OTG 1)	NA	O, 5V Power	NC. *Note: USB Port0 OTGVBUS detection. Note: This is optional feature in SOM.*
P64	USB0_OTG_ID	NC (Optionally USB_OTG1_ID)	USB1_ID/B11	O, 3.3V CMOS	NC. *Note: USB Port0 OTG ID. This is Note: This is optional feature in SOM.*
P65	USB1+	USB_HUB1OUT_DP	NA	IO, USB HS	USB Port1 Data Plus *Note: Connected to USBHub*
P66	USB1-	USB_HUB1OUT_DM	NA	IO, USB HS	USB Port1 Data Minus *Note: Connected to USBHub*
P67	USB1_EN_OC#	USB_HUB1_OC	NA	O, 3.3V CMOS	USB Port1 Power

Pin No.	SMARC Edge Connector Pin Name	Signal Name	CPU Ball Name/Pin Number	Signal Type/ Termination	Description
					Enable/Over Current Indicator *Note: Connected to USB Hub*.
P68	GND	GND	NA	Power	Ground.
P69	USB2+	USB_HUB2OUT_DP	NA	IO, USB HS	USB Port2 Data Plus *Note: Connected to USBHub*
P70	USB2-	USB_HUB2OUT_DM	NA	IO, USB HS	USB Port2 Data Minus *Note: Connected to USB Hub*
P71	USB2_EN_OC#	USB_HUB1_OC	NA	IO, 3.3V CMOS	USB Port2 Power Enable/ Over Current Indicator *Note: Connected to USB Hub*
P71	USB2_EN_OC#	USB_HUB2_OC	NA	O, 3.3V CMOS	USB Port2 Power Enable/Over Current Indicator *Note: Connected to USB Hub*
P72	RSVD4	NC	NA	-	NC.
P73	RSVD5	NC	NA	-	NC.
P74	USB3_EN_OC#	USB1_OTG_OC(GPIO 1_IO13)	GPIO1_IO13/A6	O, 3.3V CMOS	USB Port3 Power Enable/ Over Current Indicator
KEY					
P75	PCIE_A_RST#	GPIO_PCIE_RST(GPI O1_IO12)	GPIO1_IO12/A5	I, 3.3V CMOS	PCIe Reset.
P76	USB4_EN_OC#	USB_HUB3_OC	NA	O, 3.3V CMOS	USB Port4 Power Enable/Over Current Indicator *Note: Connected to USB Hub*
P77	PCIE_B_CKREQ#	NC	NA	NA	NC.
P78	PCIE_A_CKREQ#	NC (Optional PCIE_CLKREQ_B(S AI3_MCLK))	SAI3_MCLK/AJ20	NA	NC. *Note: In SOM Optionally connected to PCIE_CLKREQ_B.*
P79	GND	GND	NA	Power	Ground.
P80	PCIE_C_REFCK+	NC	PCIE_REF_PAD_CLK_ P/D16	-	NC.
P81	PCIE_C_REFCK-	NC	PCIE_REF_PAD_CLK_ N/E16	-	NC.
P82	GND	GND	NA	Power	Ground.
P83	PCIE_A_REFCK+	PCIE_REFCLK_DP	NA	I, PCIe	PCIe Reference Clock Positive.

Pin No.	SMARC Edge Connector Pin Name	Signal Name	CPU Ball Name/Pin Number	Signal Type/ Termination	Description
P84	PCIE_A_REFCK-	PCIE_REFCLK_DM	NA	I, PCIe	PCIe Reference Clock Negative.
P85	GND	GND	NA	Power	Ground.
P86	PCIE_A_RX+	PCIE_RXN_P	PCIE_RXN_P/A14	O, PCIe	PCIe Receive Positive.
P87	PCIE_A_RX-	PCIE_RXN_N	PCIE_RXN_N/B14	O, PCIe	PCIe Receive Negative.
P88	GND	GND	NA	Power	Ground.
P89	PCIE_A_TX+	PCIE_TXN_P	PCIE_TXN_P/A15	I, PCIe	PCIe Transmit Positive.
P90	PCIE_A_TX-	PCIE_TXN_N	PCIE_TXN_N/B15	I, PCIe	PCIe Transmit Negative.
P91	GND	GND	NA	Power	Ground.
P92	HDMI_D2+/DP1_LANE0+	HDMI_TX_D2_P	HDMI_TX2_P/AH27	I, TMDS	HDMI Transceiver 2 Positive to HDMI Connector.
P93	HDMI_D2- /DP1_LANE0-	HDMI_TX_D2_N	HDMI_TX2_N/AJ27	I, TMDS	HDMI Transceiver 2 Negative to HDMI Connector.
P94	GND	GND	NA	Power	Ground.
P95	HDMI_D1+ / DP1_LANE1+	HDMI_TX_D1_P	HDMI_TX1_P/AH26	I, TMDS	HDMI Transceiver 1 Positive to HDMI Connector.
P96	HDMI_D1- / DP1_LANE1-	HDMI_TX_D1_N	HDMI_TX1_N/ AJ26	I, TMDS	HDMI Transceiver 1 Negative to HDMI Connector.
P97	GND	GND	NA	Power	Ground.
P98	HDMI_D0+ / DP1_LANE2+	HDMI_TX_D0_P	HDMI_TX0_P/AH25	I, TMDS	HDMI Transceiver 0 Positive to HDMI Connector.
P99	HDMI_D0- / DP1_LANE2-	HDMI_TX_D0_N	HDMI_TX0_N/AJ25	I, TMDS	HDMI Transceiver 0 Negative to HDMI Connector.
P100	GND	GND	NA	Power	Ground.
P101	HDMI_CK+ / DP1_LANE3+	HDMI_TX_CLK_P	HDMI_TXC_P/AH24	I, TMDS	HDMI Transceiver CLK Positive to HDMI Connector.
P102	HDMI_CK- / DP1_LANE3-	HDMI_TX_CLK_N	HDMI_TXC_N/AJ24	I, TMDS	HDMI Transceiver CLK Negative to HDMI Connector.
P103	GND	GND	NA	Power	Ground.
P104	HDMI_HPD / DP1_HPD	HDMI_TX_HPD	HDMI_HPD/AE22	O, 1.8V CMOS 100K PU	HDMI Hot Plug Detect from HDMI Connector.

Pin No.	SMARC Edge Connector Pin Name	Signal Name	CPU Ball Name/Pin Number	Signal Type/ Termination	Description
P105	HDMI_CTRL_CK / DP1_AUX+	HDMI_TX_DDC_SCL	HDMI_DDC_SCL/ AC22	I, 1.8V CMOS 100K PU	HDMI DDC Clock to HDMI Connector through Voltage Level translator.
P106	HDMI_CTRL_DAT / DP1_AUX-	HDMI_TX_DDC_SDA	HDMI_DDC_SDA/ AF22	IO, 1.8V CMOS	HDMI DDC DATA to HDMI Connector through Voltage Level translator.
P107	DP1_AUX_SEL	NC (Optionally GPIO3_IO28(HDMI _ CEC))	HDMI_CEC /AD22	I, 1.8V CMOS	NC. Note: In SOM Optionally connected to HDMI_CEC.
P108	GPIO0 / CAM0_PWR#	SMARC_GPIO_0_GPIO4_18(SAI1_TXD6)	SAI1_TXD6/AC12	IO, 1.8V CMOS	General Purpose Input/ Output 0. Connected to CAN0 Transceiver Power Down.
P109	GPIO1 / CAM1_PWR#	SMARC_GPIO_1_GPIO4_19(SAI1_TXD7)	SAI1_TXD7/AJ13	IO, 1.8V CMOS	General Purpose Input/ Output 1. Connected to CAN1 Transceiver Power Down.
P110	GPIO2 / CAM0_RST#	SMARC_GPIO_2_GPIO4_0(SAI1_RXFS)	SAI1_RXFS/AJ9	IO, 1.8V CMOS	General Purpose Input/ Output 2. Used for Camera RESET.
P111	GPIO3 / CAM1_RST#	SMARC_GPIO_3_GPIO4_1(SAI1_RXC)	SAI1_RXC/AH8	IO, 1.8V CMOS	General Purpose Input/ Output 3. Connected to A&V Expansion connector.
P112	GPIO4 / HDA_RST#	SMARC_GPIO_4_GPIO4_2(SAI1_RXD0)	SAI1_RXD0/AC10	IO, 1.8V CMOS	General Purpose Input/ Output 4. USB Type C Port selection.
P113	GPIO5 / PWM_OUT	SMARC_GPIO_5_GPIO3_20(SAI5_RXC)	SAI5_RXC/AD14	IO, 1.8V CMOS	General Purpose Input/ Output 5. Connected to M.2 Reset.

Pin No.	SMARC Edge Connector Pin Name	Signal Name	CPU Ball Name/Pin Number	Signal Type/ Termination	Description
P114	GPIO6 / TACHIN	SMARC_GPIO_6_GPIO4_22(SAI2_RXC)	SAI2_RXC/AJ16	IO, 1.8V CMOS	General Purpose Input/ Output 6. Connected to USB Type C Controller interrupt.
P115	GPIO7	SMARC_GPIO_7_GPIO4_21(SAI2_RXFS)	SAI2_RXFS/AH17	IO, 1.8V CMOS	General Purpose Input/ Output 7. Connected to Touch interrupt.
P116	GPIO8	SMARC_GPIO_8_GPIO4_28(SAI3_RXFS)	SAI3_RXFS/AJ19	IO, 1.8V CMOS	General Purpose Input/ Output 8. Connected to Headphone Detect.
P117	GPIO9	SMARC_GPIO_9_GPIO4_3(SAI1_RXD1)	SAI1_RXD1/AF10	IO, 1.8V CMOS	General Purpose Input/ Output 9. Connected to MIPI Display RESET.
P118	GPIO10	SMARC_GPIO_10_GPIO3_21(SAI5_RXFS)	SAI5_RXFS/AC14	IO, 1.8V CMOS	General Purpose Input/ Output 10. Connected to PCIe connector for Wireless disable (active low).
P119	GPIO11	SMARC_GPIO_11_GPIO5_5(SPDIF1_EXT_CLK)	SPDIF_EXT_CLK/ AC18	IO, 1.8V CMOS	General Purpose Input/ Output 11. Connected to MIC Detect.
P120	GND	GND	NA	Power	Ground.
P121	I2C_PM_CK	NC (Optionally I2C1_SCL)	I2C1_SCL/AC8	I, 1.8V CMOS	NC. Note: This is optional feature in SOM.
P122	I2C_PM_DAT	NC (Optionally I2C1_SDA)	I2C1_SDA/AH7	IO, 1.8V CMOS	NC. Note: This is optional feature in SOM.
P123	BOOT_SEL0#	BOOT_SEL0#	NA	O, 1.8V CMOS	Boot Media Select bit 0 from 4bit DIP Switch (SW5).
P124	BOOT_SEL1#	BOOT_SEL1#	NA	O, 1.8V CMOS	Boot Media Select bit 1 from 4bit DIP Switch (SW5).
P125	BOOT_SEL2#	BOOT_SEL2#	NA	O, 1.8V CMOS	Boot Media Select bit

Pin No.	SMARC Edge Connector Pin Name	Signal Name	CPU Ball Name/Pin Number	Signal Type/ Termination	Description
					2 from 4bit DIP Switch (SW5).
P126	RESET_OUT#	GPIO_RESET_OUT_GPIO1_9_1V8	GPIO1_IO08/A8	I, 1.8V CMOS	Reset out from CPU GPIO to all other peripherals.
P127	RESET_IN#	PMIC_RST_B	NA	O, 1.8V CMOS	Hard RESET Input to SOM from Reset Push Button Switch (SW3).
P128	POWER_BTN#	CPU_ON_OFF	ONOFF/ G22	O, 1.8V CMOS	Power ON /OFF Input to SOM from Power Push Button Switch (SW2).
P129	SER0_TX	UART2_TXD	UART2_TXD/AH4	I, 1.8V CMOS	UART2 Transmitter to Data UART Header (J12) through Voltage Level translator.
P130	SER0_RX	UART2_RXD	UART2_RXD/AF6	O, 1.8V CMOS	UART2 Receiver to Data UART Header (J12) through Voltage Level translator.
P131	SER0_RTS#	UART2_CTS_B(SAI3_RXC)	SAI3_RXC/AJ18	0, 1.8V CMOS	UART2 Clear to Send Data UART Header (J12) through Voltage Level translator.
P132	SER0_CTS#	UART2_RTS_B(SAI3_RXD)	SAI3_RXD/AF18	I, 1.8V CMOS	UART2 Request to Send to Data UART Header (J12) through Voltage Level translator.
P133	GND	GND	NA	Power	Ground.
P134	SER1_TX	UART3_TXD	NAND_CE0_B/L26	O, 1.8V CMOS	UART3 Transmitter to Carrier Expansion Connector1.
P135	SER1_RX	UART3_RXD	NAND_ALE/N25	I,1.8V CMOS	UART3 Receiver to Carrier Expansion Connector1
P136	SER2_TX	NC (Optionally UART1_TX)	UART1_TXD/AJ3	O, 1.8V CMOS	NC. Note: In default configuration UART1_TX used for

Pin No.	SMARC Edge Connector Pin Name	Signal Name	CPU Ball Name/Pin Number	Signal Type/ Termination	Description
					on SOM Bluetooth support.
P137	SER2_RX	NC (Optionally UART1_RX)	UART1_RXD/ AD6	I, 1.8V CMOS	NC. Note: In default configuration UART1_RX used for on SOM Bluetooth support.
P138	SER2_RTS#	NC (Optionally UART1_CTS_B)	UART3_RXD/ AE6	O, 1.8V CMOS	NC. Note: In default configuration UART1_CTS_B used for on SOM Bluetooth support.
P139	SER2_CTS#	NC (Optionally UART1_RTS_B)	UART3_TXD/ AJ4	I, 1.8V CMOS	NC. Note: In default configuration UART1_RTS_B used for on SOM Bluetooth support.
P140	SER3_TX	UART4_TXD	UART4_TXD/ AH5	I, 1.8V CMOS	UART4 Transmitter to Debug UART.
P141	SER3_RX	UART4_RXD	UART4_RXD/ AJ5	O, 1.8V CMOS	UART4 Receiver to Debug UART.
P142	GND	GND	NA	Power	Ground.
P143	CAN0_TX	FLEXCAN1_TX(SAI5_RXD1)	SAI5_RXD1/AD16	I, 1.8V CMOS	CAN 0 Transmitter
P144	CAN0_RX	FLEXCAN1_RX(SAI5_RXD2)	SAI5_RXD2/AF16	O, 1.8V CMOS	CAN 0 Receiver
P145	CAN1_TX	FLEXCAN2_TX(SAI5_RXD3)	SAI5_RXD3/AE14	I, 1.8V CMOS	CAN 1 Transmitter
P146	CAN1_RX	FLEXCAN2_RX(SAI5_MCLK)	SAI5_MCLK/AF14	O, 1.8V CMOS	CAN 1 Receiver
P147	VDD_IN	VDD_IN	NA	O, 5V Power	Supply Voltage.
P148	VDD_IN	VDD_IN	NA	O, 5V Power	Supply Voltage.
P149	VDD_IN	VDD_IN	NA	O, 5V Power	Supply Voltage.
P150	VDD_IN	VDD_IN	NA	O, 5V Power	Supply Voltage.
P151	VDD_IN	VDD_IN	NA	O, 5V Power	Supply Voltage.
P152	VDD_IN	VDD_IN	NA	O, 5V Power	Supply Voltage.
P153	VDD_IN	VDD_IN	NA	O, 5V Power	Supply Voltage.
P154	VDD_IN	VDD_IN	NA	O, 5V Power	Supply Voltage.
P155	VDD_IN	VDD_IN	NA	O, 5V Power	Supply Voltage.
P156	VDD_IN	VDD_IN	NA	O, 5V Power	Supply Voltage.

SMARC Secondary Side					
Pin No.	**SMARC MXM Connector Pin Name**	**Signal Name**	**SoC Ball Name/ Pin Number**	**Signal Type/ Termination**	**Description**
S1	CSI1_TX+ / I2C_CAM1_CK	I2C5_SCL(SPDIF_TX)	SPDIF_TX/AE18	I, 1.8V CMOS 4.7k PU	I2C5 Clock.
S2	CSI1_TX- / I2C_CAM1_DAT	I2C5_SDA(SPDIF_RX)	SPDIF_RX/AD18	IO, 1.8V CMOS 4.7k PU	I2C5 Data.
S3	GND	GND	NA	Power	Ground.
S4	RSVD1	NC	NA	-	NC.
S5	CSI0_TX- / I2C_CAM0_CK	I2C3_SCL	I2C3_SCL/AJ7	I, 1.8V CMOS 4.7k PU	I2C3 Clock.
S6	CAM_MCK	CAMERA_CCMCLKO 1(ECSPI2_MISO)	ECSPI2_MISO/ AH20	O, 1.8V CMOS	Master Clock for Camera.
S7	CSI0_TX+ / I2C_CAM0_DAT	I2C3_SDA	I2C3_SDA/AJ6	IO, 1.8V CMOS 4.7k PU	I2C3 Data.
S8	CSI0_CK+	MIPI_CSI1_CLK_P	MIP_CSI1_CLK_P/ D22	O, MIPI	MIPI CSI0 differential Clock positive.
S9	CSI0_CK-	MIPI_CSI1_CLK_N	MIPI_CSI1_CLK_N/ E22	O, MIPI	MIPI CSI1 differential Clock negative.
S10	GND	GND	NA	Power	Ground.
S11	CSI0_RX0+	MIPI_CSI1_D0_P	MIPI_CSI1_D0_P/ D18	O, MIPI	MIPI CSI1 differential data lane 0 positive.
S12	CSI0_RX0-	MIPI_CSI1_D0_N	MIPI_CSI1_D0_N/ E18	O, MIPI	MIPI CSI1 differential data lane 0 negative.
S13	GND	GND	NA	Power	Ground.
S14	CSI0_RX1+	MIPI_CSI1_D1_P	MIPI_CSI1_D1_P/ D20	O, MIPI	MIPI CSI1 differential data lane 1 positive.
S15	CSI0_RX1-	MIPI_CSI1_D1_N	MIPI_CSI1_D1_N/ E20	O, MIPI	MIPI CSI1 differential data lane 1 negative.
S16	GND	GND	NA	Power	Ground.
S17	GBE1_MDI0+	GBE1_MDI0+	NA	IO, GBE	Gigabit Ethernet1 MDI differential pair 0 positiveto top port of Dual Magjack.
S18	GBE1_MDI0-	GBE1_MDI0-	NA	IO, GBE	Gigabit Ethernet1 MDIdifferential pair 0 negative to top port of Dual Magjack.
S19	GBE1_LINK100#	GBE1_LINK100#	NA	I, 3.3V CMOS	Ethernet1 100Mbps link status LED signal to top

Pin No.	SMARC MXM Connector Pin Name	Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
					port of Dual Magjack.
S20	GBE1_MDI1+	GBE1_MDI1+	NA	IO, GBE	Gigabit Ethernet1 MDI differential pair 1 positive to top port of Dual Magjack.
S21	GBE1_MDI1-	GBE1_MDI1-	NA	IO, GBE	Gigabit Ethernet1 MDI differential pair 1 negative to top port of Dual Magjack.
S22	GBE1_LINK1000#	GBE1_LINK1000#	NA	I, 3.3V CMOS	Ethernet1 1000Mbps link status LED signal.
S23	GBE1_MDI2+	GBE1_MDI2+	NA	IO, GBE	Gigabit Ethernet1 MDI differential pair 2 positive to top port of Dual Magjack.
S24	GBE1_MDI2-	GBE1_MDI2-	NA	IO, GBE	Gigabit Ethernet1 MDI differential pair 2 negativeto top port of Dual Magjack.
S25	GND	GND	NA	Power	Ground.
S26	GBE1_MDI3+	GBE1_MDI3+	NA	IO, GBE	Gigabit Ethernet1 MDI differential pair 3 positive to top port of Dual Magjack.
S27	GBE1_MDI3-	GBE1_MDI3-	NA	IO, GBE	Gigabit Ethernet1 MDI differential pair 3 negative to top port of Dual Magjack.
S28	GBE1_CTREF	VPHY1_DVDDL	NA	-	
S29	PCIE_D_TX+	NC (Optionally GBE0_SOP)	NA	-	NC.
S30	PCIE_D_TX-	NC (Optionally GBE0_SON)	NA	-	NC.
S31	GBE1_LINK_ACT#	GBE1_LINK_ACT#	NA	I, 3.3V CMOS	Gigabit Ethernet1 activity status LED signal to top port of Dual Magjack.
S32	PCIE_D_RX+	NC (Optionally GBE0_SIP)	NA	-	NC.
S33	PCIE_D_RX-	NC (Optionally GBE0_SIN)	NA	-	NC.
S34	GND	GND	NA	Power	Ground.

Pin No.	SMARC MXM Connector Pin Name	Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
S35	USB4+	USB_HUB3OUT_DP	NA	IO, USB HS	USB Port4 Data Plus *Note: Connected to USB Hub*
S36	USB4-	USB_HUB3OUT_DM	NA	IO, USB HS	USB Port4 Data Minus *Note: Connected to USB Hub*
S37	USB3_VBUS_DET	VBUS_OTG1	NA	5V, Power	USB Port1 VBUS detection.
S38	AUDIO_MCK	SAI2_MCLK	SAI2_MCLK/AJ15	I, 1.8V CMOS	Master Clock for Audio codec.
S39	I2S0_LRCK	SAI2_TX_SYNC(SAI2_TXFS)	SAI2_TXFS/AJ17	O, 1.8V CMOS	Serial Audio Interface 2 Frame Sync to I2S Audio Codec.
S40	I2S0_SDOUT	SAI2_TX_DATA0(SAI2_TXD0)	SAI2_TXD0/AH16	O, 1.8V CMOS	Serial Audio Interface 2 Data Transmitter to I2S Audio Codec.
S41	I2S0_SDIN	SAI2_RX_DATA0(SAI2_RXD0)	SAI2_RXD0/AJ14	I, 1.8V CMOS	Serial Audio Interface 2 Data Receiver to I2S Audio Codec.
S42	I2S0_CK	SAI2_TX_BCLK(SAI2_TXC)	SAI2_TXC/AH15	O, 1.8V CMOS	Serial Audio Interface 2 Clock to I2S Audio Codec.
S43	ESPI_ALERT0#	NC	NA	NA	NA
S44	ESPI_ALERT1#	NC	NA	NA	NA
S45	MDIO_CLK	ENET1_MDC(SAI1_RXD2)	SAI1_RXD2/AH9	NA	NC
S46	MDIO_DAT	ENET1_MDIO(SAI1_RXD3)	SAI1_RXD3/AJ8	NA	NC
S47	GND	GND	NA	Power	Ground.
S48	I2C_GP_CK	I2C2_SCL	I2C2_SCL/AH6	I, 1.8V CMOS	I2C2 Clock.
S49	I2C_GP_DAT	I2C2_SDA	I2C2_SDA/AE8	IO, 1.8V CMOS	I2C2 Data.
S50	HDA_SYNC / I2S2_LRCK	SAI3_TX_SYNC(SAI3_TXFS)	SAI3_TXFS/AC16	I, 1.8V CMOS	Serial Audio Interface 3 Frame Sync.
S51	HDA_SDO / I2S2_SDOUT	SAI3_TX_DATA0(SAI3_TXD)	SAI3_TXD/AH18	I, 1.8V CMOS	Serial Audio Interface 3 Data Transmitter.
S52	HDA_SDI / I2S2_SDIN	SAI3_RX_DATA0(NAND_DATA00)	NAND_DATA00/ R25	O, 1.8V CMOS	Serial Audio Interface 3 Data Receiver.
S53	HDA_CK / I2S2_CK	SAI3_TX_BCLK(SAI3_TXC)	SAI3_TXC/AH19	I, 1.8V CMOS	Serial Audio Interface 3 Clock.
S54	SATA_ACT#	NC	NA	NA	NA
S55	USB5_EN_OC#	USB_HUB4_OC	NA	O, 3.3V CMOS	USB Port4 Power Enable/ Over Current Indicator

Pin No.	SMARC MXM Connector Pin Name	Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
					Note: Connected to USB Hub
S56	QSPI_IO_2 / ESPI_IO_2	NC	NA	IO, 1.8V CMOS	QSPIB Data2.
S57	QSPI_IO_3 / ESPI_IO_3	NC	NA	IO, 1.8V CMOS	QSPIB Data3.
S58	ESPI_RESET#	NC	NA	O, 1.8V CMOS	QSPIB RESET.
S59	USB5+	USB_HUB4OUT_DP	NA	IO, USB HS	USB Port5 Data Plus *Note: Connected to USB Hub*
S60	USB5-	USB_HUB4OUT_DM	NA	IO, USB HS	USB Port5 Data Minus *Note: Connected to USB Hub*
S61	GND	GND	NA	Power	Ground.
S62	USB3_SSTX+	USB1_TX_P	USB1_TX_P/A10	I, USB SS	USB Port1 Super Speed Transmit Positive to Top Port of Dual Stack USB3.0 TypeA Connector (J17) or TypeC Connector (J20).
S63	USB3_SSTX-	USB1_TX_N	USB1_TX_N/B10	I, USB SS	USB Port1 Super Speed Transmit Negative to Top Port of Dual Stack USB3.0 TypeA Connector (J17) or TypeC Connector (J20).
S64	GND	GND	NA	Power	Ground.
S65	USB3_SSRX+	USB1_RX_P	USB1_RX_P/A9	O, USB SS	USB Port1 Super Speed Receive Positive to Top Port of Dual Stack USB3.0 TypeA Connector (J17) or TypeC Connector (J20).
S66	USB3_SSRX-	USB1_RX_N	USB1_RX_N/B9	O, USB SS	USB Port1 Super Speed Receive Negative to Top Port of Dual Stack USB3.0 TypeA Connector (J17) or TypeC Connector (J20).
S67	GND	GND	NA	Power	Ground.
S68	USB3+	USB_OTG1_DP	USB1_D_P/D10	IO, USB HS	USB Port3 High Speed Data Positive to Top Port of Dual Stack USB3.0 TypeA Connector (J17) or TypeC Connector (J20).

Pin No.	SMARC MXM Connector Pin Name	Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
S69	USB3-	USB_OTG1_DM	USB1_D_N/E10	IO, USB HS	USB Port3 High Speed Data Negative to Top Port of Dual Stack USB3.0 TypeA Connector (J17) or TypeC Connector (J20).
S70	GND	GND	NA	Power	Ground.
S71	USB2_SSTX+	USB2_TX_P	USB2_TX_P/A13	I, USB SS	USB Port2 Super Speed Transmit Positive to bottom Port of Dual Stack USB3.0 TypeA Connector (J17).
S72	USB2_SSTX-	USB2_TX_N	USB2_TX_N/B13	I, USB SS	USB Port2 Super Speed Transmit Negative to bottom Port of Dual Stack USB3.0 TypeA Connector (J17).
S73	GND	GND	NA	Power	Ground.
S74	USB2_SSRX+	USB2_RX_P	USB2_RX_P/A12	O, USB SS	USB Port2 Super Speed Receive Positive to bottom Port of Dual Stack USB3.0 TypeA Connector (J17).
S75	USB2_SSRX-	USB2_RX_N	USB2_RX_N/B12	O, USB SS	USB Port2 Super Speed Receive Negative to bottom Port of Dual Stack USB3.0 TypeA Connector (J17).
KEY					
S76	PCIE_B_RST#	NC	NA	I, 3.3V CMOS	NC. *Note: This is optional feature in SOM.*
S77	PCIE_C_RST#	NC	NA	-	NC.
S78	PCIE_C_RX+	NC (Optionally GBE1_SIP)	NA	-	NC.
S79	PCIE_C_RX- -	NC (Optionally GBE1_SIN)	NA	-	NC.
S80	GND	GND	NA	Power	Ground.
S81	PCIE_C_TX+	NC (Optionally GBE1_SOP)	NA	-	NC.
S82	PCIE_C_TX-	NC (Optionally GBE1_SON)	NA	-	NC.

Pin No.	SMARC MXM Connector Pin Name	Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
S83	GND	GND	NA	Power	Ground.
S84	PCIE_B_REFCK+	NC	NA	-	NC.
S85	PCIE_B_REFCK-	NC	NA	-	NC.
S86	GND	GND	NA	Power	Ground.
S87	PCIE_B_RX+	NC	NA	-	NC.
S88	PCIE_B_RX-	NC	NA	-	NC.
S89	GND	GND	NA	Power	Ground.
S90	PCIE_B_TX+	NC	NA	-	NC.
S91	PCIE_B_TX-	NC	NA	-	NC.
S92	GND	GND	NA	Power	Ground.
S93	DP0_LANE0+	NC	NA	-	NC.
S94	DP0_LANE0-	NC	NA	-	NC.
S95	DP0_AUX_SEL	NC	NA	-	NC.
S96	DP0_LANE1+	NC	NA	-	NC.
S97	DP0_LANE1-	NC	NA	-	NC.
S98	DP0_HPD	NC	NA	-	NC.
S99	DP0_LANE2+	NC	NA	-	NC.
S100	DP0_LANE2-	NC	NA	-	NC.
S101	GND	GND	NA	Power	Ground.
S102	DP0_LANE3+	NC	NA	-	NC.
S103	DP0_LANE3-	NC	NA	-	NC.
S104	USB3_OTG_ID	USB_OTG1_ID	USB1_ID/ B11	-	NC.
S105	DP0_AUX+	NC	NA	-	NC.
S106	DP0_AUX-	NC	NA	-	NC.
S107	LCD1_BKLT_EN	LCD1_BKLT_EN_GPIO3_14 (NAND_DQS)	NAND_DQS/ R26	O, 1.8V CMOS	LCD1 Backlight Enable
S108	LVDS1_CK+ / eDP1_AUX+ / DSI1_CLK+	LVDS1_CLK_P	LVDS1_CLK_P/ A28	-	*LVDS1 differential Clock positive*
S109	LVDS1_CK- / eDP1_AUX- / DSI1_CLK-	LVDS1_CLK_N	LVDS1_CLK_N/ B28	-	*LVDS1 differential Clock negative*
S110	GND	GND	NA	Power	Ground.
S111	LVDS1_0+ / eDP1_TX0+ / DSI1_D0+	LVDS1_D0_P	LVDS1_D0_P/ A26	-	*LVDS1 differential data0 positive*
S112	LVDS1_0- / eDP1_TX0- / DSI1_D0-	LVDS1_D0_N	LVDS1_D0_N/ B26	-	*LVDS1 differential data0 negative*

Pin No.	SMARC MXM Connector Pin Name	Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
S113	eDP1_HPD / DSI1_TE	NC	NA	-	NC.
S114	LVDS1_1+ / eDP1_TX1+ / DSI1_D1+	LVDS1_D1_P	LVDS1_D1_P/ A27	-	*LVDS1 differential data1 positive*
S115	LVDS1_1- / eDP1_TX1- / DSI1_D1-	LVDS1_D1_N	LVDS1_D1_N/ B27	-	*LVDS1 differential data1 negative*
S116	LCD1_VDD_EN	LCD1_VDD_EN_GPIO3_28 (HDMI_CEC)	HDMI_CEC/ AD22	O, 1.8V CMOS	LCD1 Power Enable
S117	LVDS1_2+ / eDP1_TX2+ / DSI1_D2+	LVDS1_D2_P	LVDS1_D2_P/ B29	-	*LVDS1 differential data2 positive*
S118	LVDS1_2- / eDP1_TX2- / DSI1_D2-	LVDS1_D2_N	LVDS1_D2_N/ C28	-	*LVDS1 differential data2 negative*
S119	GND	GND	NA	Power	Ground.
S120	LVDS1_3+ / eDP1_TX3+ / DSI1_D3+	LVDS1_D3_P	LVDS1_D3_P/ C29	-	*LVDS1 differential data3 positive*
S121	LVDS1_3- / eDP1_TX3- / DSI1_D3-	LVDS1_D3_N	LVDS1_D3_N/ D28	-	*LVDS1 differential data3 negative*
S122	LCD1_BKLT_PWM	PWM2_OUT(SAI5_RXD0)	SAI5_RXD0/ AE16	-	Display Back Light Brightness control PWM.
S123	GPIO13	NC	NC	-	NC In SOM Optionally connected to SMARC_GPIO_13_GPIO3_28(HDMI_CEC).
S124	GND	GND	NA	Power	Ground.
S125	LVDS0_0+ / eDP0_TX0+ / DSI0_D0+	LVDS0/DSI0_D0_P	MIPI_DSI1_D0_P/ A16 or LVDS0_D0_P/ D29	I, MIPI	MIPI DSI Differential Data Lane 0 Positive *Note: Optionally connected to LVDS0 differential data0 positive*
S126	LVDS0_0- / eDP0_TX0- / DSI0_D0-	LVDS0/DSI0_D0_N	MIPI_DSI1_D0_N/ B16 or	I, MIPI	MIPI DSI Differential Data Lane 0 Negative

Pin No.	SMARC MXM Connector Pin Name	Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
			LVDS0_D0_N/ E28		*Note: Optionally connected to LVDS0 differential data0 negative*
S127	LCD0_BKLT_EN	LCD0_BKLT_EN_GPIO3_7(NAND_DATA01)	NAND_DATA01/ L25	I, 1.8V CMOS	Display Backlight Enable.
S128	LVDS0_1+ / eDP0_TX1+ / DSI0_D1+	LVDS0/DSI0_D1_P	MIPI_DSI1_D1_P/ A17 or LVDS0_D1_P/ E29	I, MIPI	MIPI DSI Differential Data Lane 1 Positive *Note: Optionally connected to LVDS0 differential data1 positive*
S129	LVDS0_1- / eDP0_TX1- / DSI0_D1-	LVDS0/DSI0_D1_N	MIPI_DSI1_D1_N/ B17 or LVDS0_D1_N/ F28	I, MIPI	MIPI DSI Differential Data Lane 1 Negative. *Note: Optionally connected to LVDS0 differential data1 negative*
S130	GND	GND	NA	Power	Ground.
S131	LVDS0_2+ / eDP0_TX2+ / DSI0_D2+	LVDS0/DSI0_D2_P	MIPI_DSI1_D2_P/ A19 or LVDS0_D2_PP/ G29	I, MIPI	MIPI DSI Differential Data Lane 2 Positive *Note: Optionally connected to LVDS0 differential data2 positive*
S132	LVDS0_2- / eDP0_TX2- / DSI0_D2-	LVDS0/DSI0_D2_N	MIPI_DSI1_D2_N/ B19 or LVDS0_D2_N/ H28	I, MIPI	MIPI DSI Differential Data Lane 2 Negative *Note: Optionally connected to LVDS0 differential data2 negative*
S133	LCD0_VDD_EN	LCD0_VDD_EN_GPIO3_8(NAND_DATA02)	NAND_DATA02/ L24	I, 1.8V CMOS	Display Power Enable.
S134	LVDS0_CK+ / eDP0_AUX+ / DSI0_CLK+	LVDS0/DSI0_CLK_P	MIPI_DSI1_CLK_P/ A18 or LVDS0_CLK_P/ F29	I, MIPI	MIPI DSI Differential Clock Positive *Note: Optionally connected to LVDS0*

Pin No.	SMARC MXM Connector Pin Name	Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
					differential clock positive
S135	LVDS0_CK- / eDP0_AUX- / DSI0_CLK-	LVDS0/DSI0_CLK_N	MIPI_DSI1_CLK_N/ B18 or LVDS0_CLK_N/ G28	I, MIPI	MIPI DSI Differential Clock Negative *Note: Optionally connected to LVDS0 differential clock negative*
S136	GND	GND	NA	Power	Ground.
S137	LVDS0_3+ / eDP0_TX3+ / DSI0_D3+	LVDS0/DSI0_D3_P	MIPI_DSI1_D3_P/ A20 or LVDS0_D3_P/ H29	I, MIPI	MIPI DSI Differential Data Lane 3 Positive *Note: Optionally connected to LVDS0 differential data3 positive*
S138	LVDS0_3- / eDP0_TX3- / DSI0_D3-	LVDS0/DSI0_D3_N	MIPI_DSI1_D3_N/ B20 or LVDS0_D3_N/ J28	I, MIPI	MIPI DSI Differential Data Lane 3 Negative *Note: Optionally connected to LVDS0 differential data3 negative*
S139	I2C_LCD_CK	I2C5_SCL(SPDIF_TX)	SPDIF_TX/ AE18	I, 1.8V CMOS	I2C5 Clock.
S140	I2C_LCD_DAT	I2C5_SDA(SPDIF_RX)	SPDIF_RX/ AD18	IO, 1.8V CMOS	I2C5 Data.
S141	LCD0_BKLT_PWM	PWM1_OUT(I2C4_SDA)	I2C4_SDA/ AD8	I, 1.8V CMOS	Display Back Light Brightness control PWM.
S142	GPIO12	NC	NA	-	NC In SOM Optionally connected to SMARC_GPIO_12_GPIO3_14(NAND_DQS).
S143	GND	GND	NA	Power	Ground.
S144	eDP0_HPD / DSI0_TE	NC	NA	I, 1.8V CMOS	NC.
S145	WDT_TIME_OUT#	GPIO_WDT_OUT	NA	I, 1.8V CMOS	Watchdog Time Out Interrupt.
S146	PCIE_WAKE#	GPIO_PCIe_Wake(GPIO1_IO14)	GPIO1_IO14/A4	O, 3.3V CMOS	PCIe wake up interrupt to host.
S147	VDD_RTC	VRTC_3V0	NA	O, 3V Power	RTC backup power. Connected to RTC battery holder.

Pin No.	SMARC MXM Connector Pin Name	Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
S148	LID#	NC	NA	-	NC.
S149	SLEEP#	NC	NA	-	NC.
S150	VIN_PWR_BAD#	VIN_PWR_BAD#	NA	O, 5V CMOS	Power bad indication.
S151	CHARGING#	NC	NA	-	NC.
S152	CHARGER_PRSNT #	NC	NA	-	NC.
S153	CARRIER_STBY#	CARRIER_STBY#	NA	I, 1.8V CMOS	Carrier Standby
S154	CARRIER_PWR_O N	CARRIER_PWR_ON	NA	I, 1.8V CMOS	Carrier power enable.
S155	FORCE_RECOV#	FORCE_RECOV#	NA	O, 1.8V CMOS	Force Recovery.
S156	BATLOW#	NC	NA	-	NC.
S157	TEST#	TEST#	NA	I, 1.8V CMOS	Connected to 4bit DIP switch (SW6).
S158	GND	GND	NA	Power	Ground.

2.4 Serial Interface Features

2.4.1 Debug UART Port

The i.MX 8M Plus Q/QL/D SMARC Carrier board supports debug interface through i.MX 8M Plus SoC's UART4 interface. This UART4 signals from SMARC MXM connector SER3 port is connected to UART to USB Convertor "FT232RQ" via 1.8V to 3.3V level Translator and to USB Micro AB Connector (J24). This USB Micro AB Connector can be used for Debug purpose which is physically located at the top of the board as shown below.

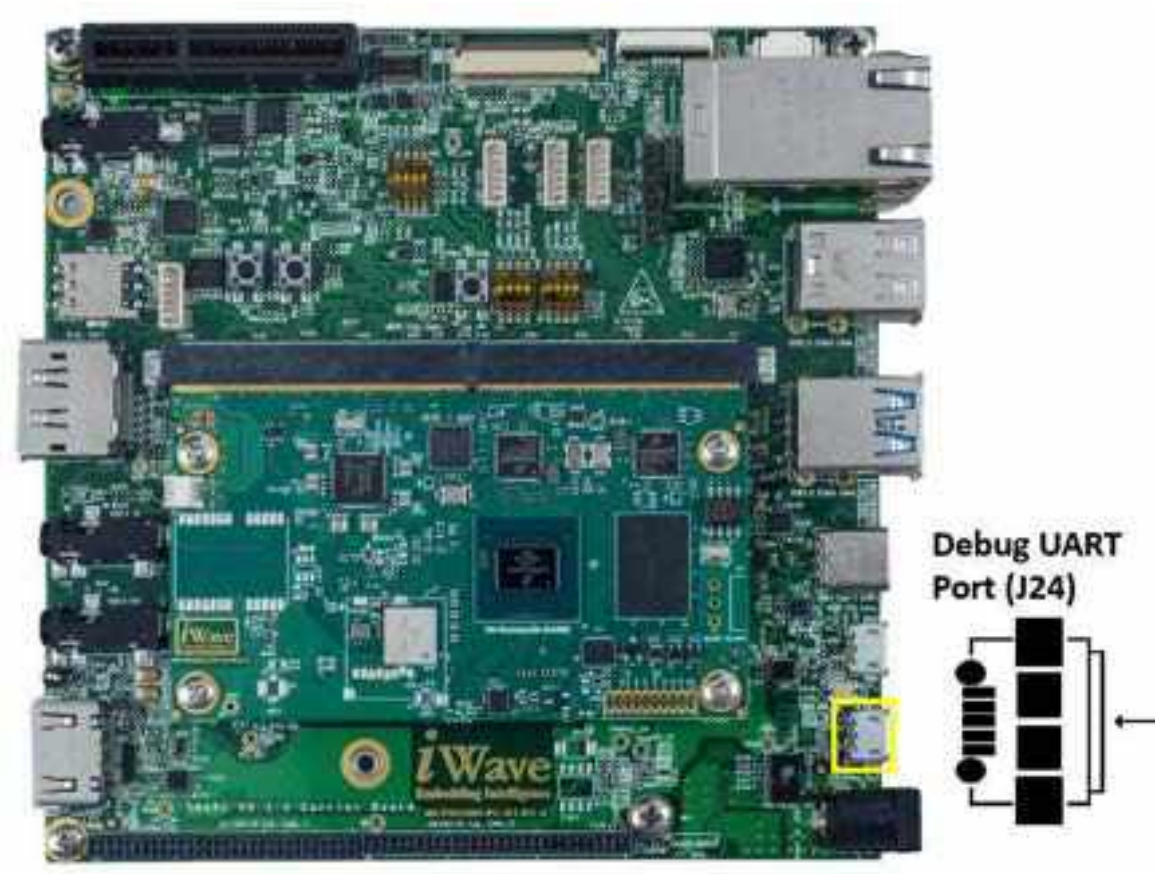


Figure 3: Data UART Header

2.4.2 RS232 UART Interface (Optional)

The i.MX 8M Plus Q/QL/D SMARC Carrier board optionally supports full functional RS232 UART interface through i.MX8 CPU's UART1 interface. This UART1 signals from SMARC MXM connector Connected UART to RS232 Convertor "MAX3232EIPWR" via 1.8V to 3.3V level Translator and MAX3232EIPWR is connected to 6pin Header (J15). This Data RS232 UART header is physically located at the top of the board as shown below.

Number of Pins 6

Connector Part number : 53047-0610 from Molex

Mating Connector Housing : 0510210600 from Molex

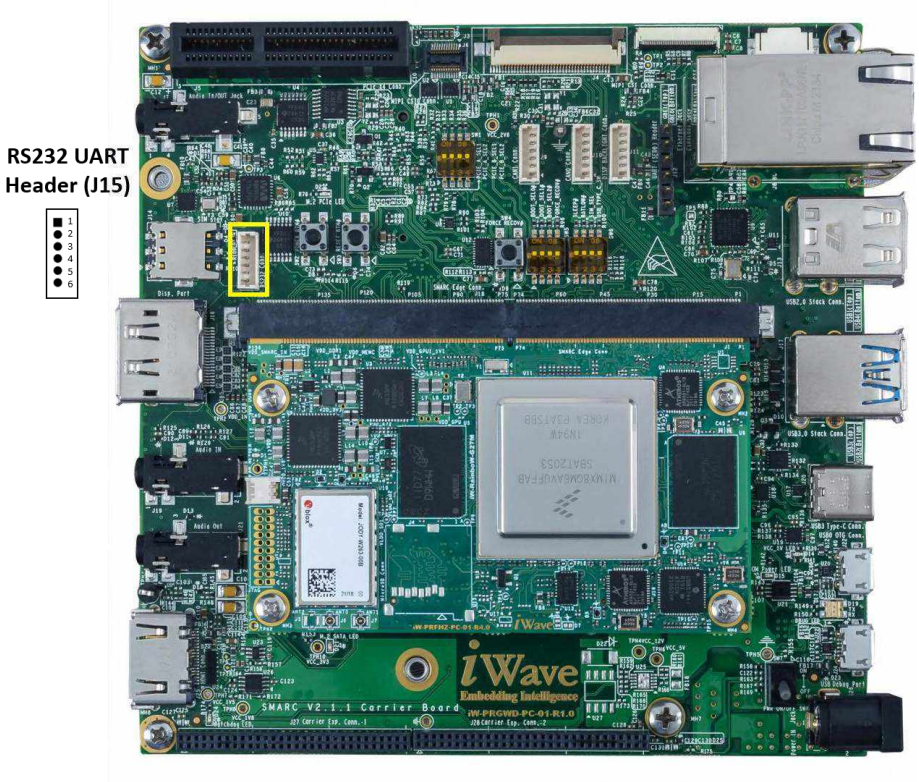


Figure 4: RS232 UART Header

Table 4: RS323 UART Header Pin Out

Pin No	Pin Name	Signal Name	Signal Type/ Termination	Description
1	GND	GND	Power	Ground.
2	CTS	UART1_CTS_B	O, 3.3V CMOS	UART1 interface Clear to Send signal.
3	VCC	NC	O, 3.3V Power	NC. *Note: Optionally connected to VCC_3V3*
4	TXD	UART1_RX	I, 3.3V CMOS	UART1 interface Receive signal.
5	RXD	UART1_TXD	O, 3.3V CMOS	UART1 interface Transmit signal.
6	RTS	UART1_RTS_B	I, 3.3V CMOS	UART1 interface Request to Send signal.

2.4.3 Data UART Header

The i.MX 8M Plus Q/QL/D SMARC Carrier board supports full functional Data UART interface through i.MX 8M Plus SoC's UART2 interface. This UART2 signals from SMARC MXM connector is connected to 6pin Header (J12) via 1.8 to 3.3V voltage level translator. This Data UART header is physically located at the top of the board as shown below.

Number of Pins :6

Connector Part number: 5-146280-6 from TE Connectivity

Mating Connector : 534237-4 from TE Connectivity

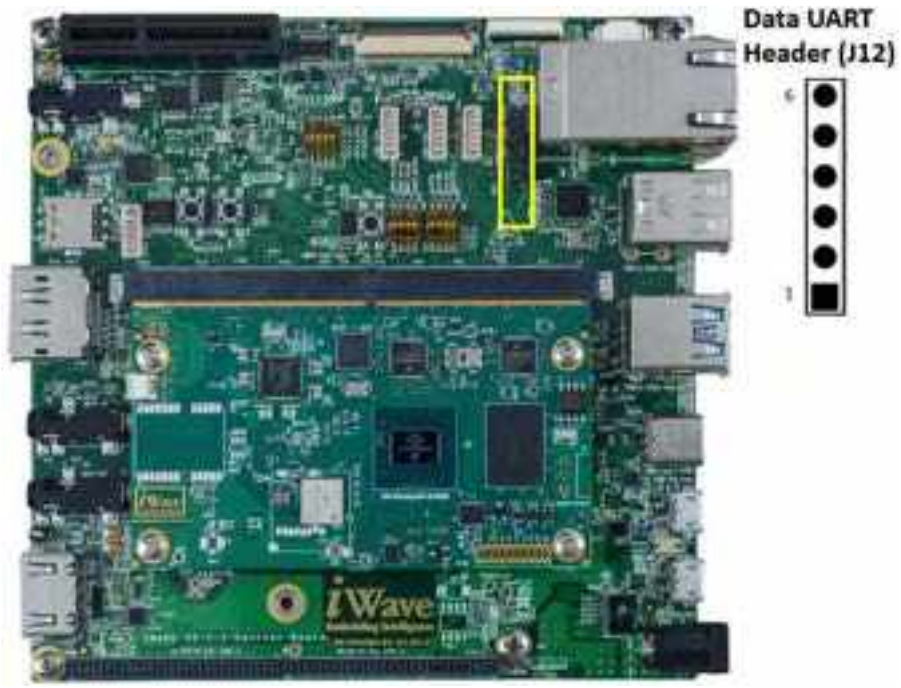


Figure 5: Data UART Header

Table 5: Data UART Header Pin Out

Pin No	Pin Name	Signal Name	Signal Type/ Termination	Description
1	GND	GND	Power	Ground.
2	UART_CTS#	UART2_CTS_B(SAI3_RXC)	O, 3.3V CMOS	UART2 interface Clear to Send signal.
3	VCC_3V3	NC	O, 3.3V Power	NC. *Note: Optionally connected to VCC_3V3*
4	UART_RXD	UART2_RXD	I, 3.3V CMOS	UART2 interface Receive signal.
5	UART_TXD	UART2_TXD	O, 3.3V CMOS	UART2 interface Transmit signal.
6	UART_RTS#	UART2_RTS_B(SAI3_RXD)	I, 3.3V CMOS	UART2 interface Request to Send signal.

2.5 High Speed Interface Features

2.5.1 PCIe Port

The i.MX 8M Plus Q/QL/D SMARC Development platform by default supports one PCIex1 over SMARC PCIe A. PCIe A lane supported through i.MX 8M Plus CPU's PCIe0 Interface.

PCIe A signal of SMARC MXM connector is connected to 1:3 Multiplexer/Demultiplexer switch and the output of the Multiplexer/Demultiplexer switch are connected to PCIex4 connector and M.2 connector. The selection between the connector can be done by setting the 4 bits of Board configuration switch (SW1) to appropriate position. PCIe A reference clock from SMARC MXM connector is connected to 1:2 output clock buffer and then connected to PCIex4 connector and PCIe M.2 connector for clock reference.

Refer Dip Switch (SW1) Settings in "Table 19: Board Configuration Switch" for more details on selecting PCIe connector. **PCIex4 Connector:** PCIeX4 connector (J5) is physically located at the top of the board as shown below

Figure 6: PCIex4 Connector

Table 6: PCIex4 Connector Pin Out

Pin No	Pin Name	Signal Name	Signal Type/ Termination	Description
A1	PRSNT1#	PCIe_HP	O, 3.3V CMOS	Default Grounded.
B1	+12V_1	VCC_12V_PCIe	O, 12V Power	12V Supply Voltage.
A2	+12V_3	VCC_12V_PCIe	O, 12V Power	12V Supply Voltage.
B2	+12V_2	VCC_12V_PCIe	O, 12V Power	12V Supply Voltage.
A3	+12V_4	VCC_12V_PCIe	O, 12V Power	12V Supply Voltage.
B3	RSVD1	VCC_12V_PCIe	O, 12V Power	12V Supply Voltage.
A4	GND6	GND	Power	Ground.
B4	GND1	GND	Power	Ground.
A5	TCK	NC	-	NC.
B5	SMCLK	SMCLK	O, 3.3V CMOS	SMB Clock.
A6	TDI	NC	-	NC.
B6	SMDAT	SMDAT	IO, 3.3V CMOS	SMB Data.
A7	TDO	NC	-	NC.
B7	GND2	GND	Power	Ground.
A8	TMS	NC	-	NC.
B8	+3V3_1	VCC_3V3_PCIe	O, 3.3V Power	3.3V Supply Voltage.
A9	+3V3_2	VCC_3V3_PCIe	O, 3.3V Power	3.3V Supply Voltage.
B9	TRST#	NC	-	NC.
A10	+3V3_3	VCC_3V3_PCIe	O, 3.3V Power	3.3V Supply Voltage.
B10	3V3AUX	VCC_3V3_PCIe	O, 3.3V Power	3.3V Supply Voltage.
A11	PERST#	GPIO_PCIE_RST(GPIO1_IO12)	O, 3.3V CMOS	PCIe PERST#.
B11	WAKE#	GPIO_PCIe_Wake(GPIO1_IO14)	O, 3.3V CMOS	PCIe WAKE#.
A12	GND7	GND	Power	Ground.
B12	RSVD2	NC	-	NC, Reserved Pin.
A13	REFCLK+	PCIE_REFCLK_DP	O, PCIe	PCIe Clock positive.
B13	GND3	GND	Power	Ground.
A14	REFCLK-	PCIE_REFCLK_DN	O, PCIe	PCIe Clock negative.
B14	PETp0	PCIE_TXN_P	O, PCIe	PCIe Port 0 Transmit pair positive. *Note: Refer SW1 setting from Table 17 to support PCIE0_TX.*
A15	GND8	GND	Power	Ground.
B15	PETn0	PCIE_TXN_N	O, PCIe	PCIe Port 0 Transmit pair negative. *Note: Refer SW1 setting from Table 17 to support PCIE0_TX.*
A16	PERp0	PCIE_RXN_P	I, PCIe	PCIe Port 0 Receive pair positive. *Note: Refer SW1 setting from Table 17 to support PCIE0_RX.*
B16	GND4	GND	Power	Ground.

Pin No	Pin Name	Signal Name	Signal Type/ Termination	Description
A17	PERn0	PCIE_RXN_N	I, PCIe	PCIe Port 0 Receive pair negative. *Note: Refer SW1 setting from Table 17 to support PCIE0_RX.*
B17	PRSNT2#_1	NC	-	NC.
A18	GND9	GND	Power	Ground.
B18	GND5	GND	Power	Ground.
A19	RSVD4	NC	-	NC, Reserved Pin.
B19	PETp1	NC	NC	NC
A20	GND16	GND	Power	Ground.
B20	PETn1	NC	NC	NC
A21	PERp1	NC	NC	NC
B21	GND10	GND	Power	Ground.
A22	PERn1	NC	NC	NC
B22	GND11	GND	Power	Ground.
A23	GND17	GND	Power	Ground.
B23	PETp2	NC	NC	NC. *Note: GBE1_SOP Connected optionally.*
A24	GND18	GND	Power	Ground.
B24	PETn2	NC	NC	NC *Note: GBE1_SON Connected optionally.*
A25	PERp2	NC	NC	NC *Note: GBE1_SIP Connected optionally*
B25	GND12	GND	Power	Ground.
A26	PERn2	NC	NC	NC *Note: GBE1_SIN Connected optionally*
B26	GND13	GND	Power	Ground.
A27	GND19	GND	Power	Ground.
B27	PETp3	NC	NC	NC *Note: GBE0_SOP Connected optionally*
A28	GND20	GND	Power	Ground.
B28	PETn3	NC	NC	NC *Note GBE0_SON Connected optionally*
A29	PERp3	NC	NC	NC *Note: GBE0_SIP Connected optionally*
B29	GND14	GND	Power	Ground.
A30	PERn3	NC	NC	NC *Note: GBE0_SIN Connected optionally*
B30	RSVD3	NC	-	NC, Reserved Pin.
A31	GND21	GND	Power	Ground.
B31	PRSNT#2_2	NC	-	NC.
A32	RSVD5	NC	-	NC, Reserved Pin.
B32	**GND15**	**GND**	**Power**	**Ground.**

M.2 Connector: The i.MX 8M Plus SMARC Carrier board supports M.2 Key-B Connector (J32) and is placed at the bottom side of the board.

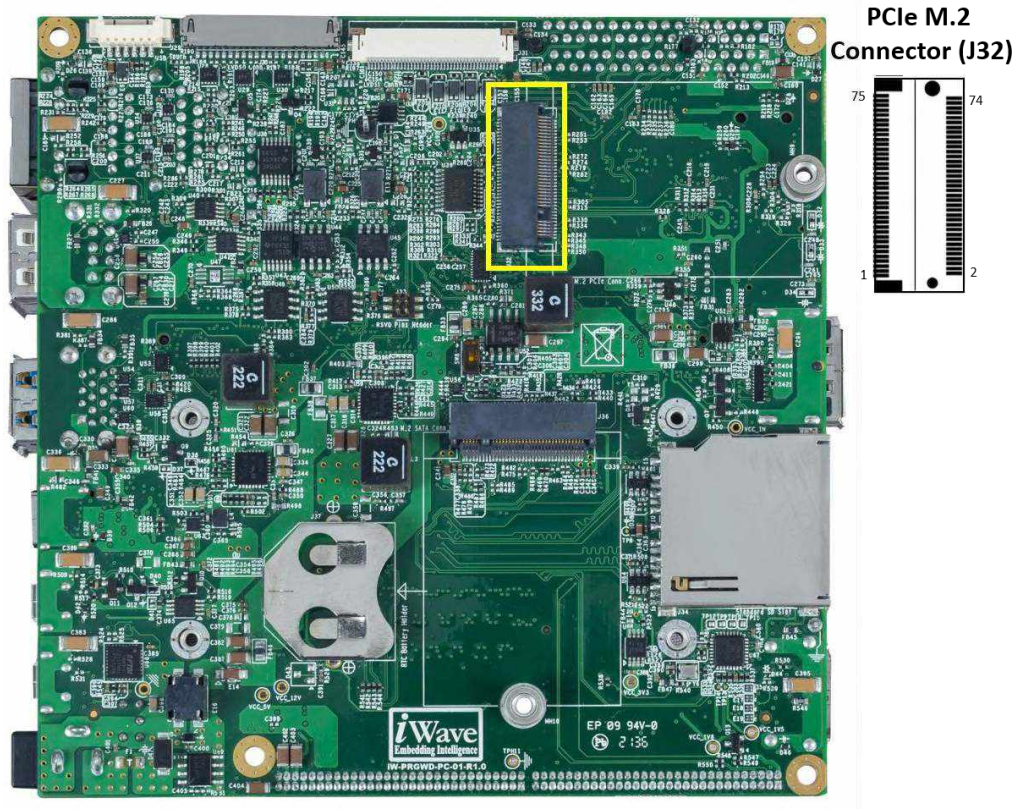


Figure 7: M.2 Connector

Refer below table for M.2 connector pinout details.

Table 7: M.2 Connector Key B-PCIe Pinout

Pin No	Pin Name	Signal Name	Signal Type/ Termination	Description
1	CONFIG_3	1_M.2_CONFIG_3	I, 1.8V CMOS 10K PU	M.2 Configuration Pin 3.
2	VCC_3V3	VCC_3V3	O, 3.3V Power	3.3V Supply Voltage.
3	GND	GND	Power	Ground.
4	VCC_3V3	VCC_3V3	O, 3.3V Power	3.3V Supply Voltage.
5	GND	GND	Power	Ground.
6	FULL_CARD_POWER_OFF# (O)(0/1.8V_3.3V)	1_M.2_PWR_OFF#	O, 3.3V CMOS 10K PU	M.2 Full card Power off Signal.
7	USB_D+	USB5+	IO, USB	USB2.0 Port5 Data Plus.

Pin No	Pin Name	Signal Name	Signal Type/ Termination	Description
8	W_DISABLE1# (O)(0/3.3V)	SMARC_GPIO_10_GPIO3_21(SAI5_RXFS)	O, 3.3V CMOS 10K PU	M.2 Wireless Disable Signal
9	USB_D-	USB5-	IO, USB	USB2.0 Port5 Data Minus.
10	GPIO9(LED1#/DAS_DSS#)(I)(0/3.3V)	1_M.2_LED	O, 3.3V CMOS	Provide status indicators via LED.
11	GND	GND	Power	Ground.
12	B1	NC	NC	NC.
13	B2	NC	NC	NC.
14	B3	NC	NC	NC.
15	B4	NC	NC	NC.
16	B5	NC	NC	NC.
17	B6	NC	NC	NC.
18	B7	NC	NC	NC.
19	B8	NC	NC	NC.
20	GPIO5(AUDIO0/I2S_CLK(I/O)(0/1.8V)	SAI3_TX_BCLK(SAI3_TXC)	IO, 1.8V CMOS	Serial Audio Interface Channel1 Clock
21	CONFIG_0	1_M.2_CONFIG_0	I, 1.8V CMOS 10K PU	M.2 Configuration Pin 0.
22	GPIO6_(AUDIO1/I2S_RX) (I/O)(0/1.8V)	SAI3_RX_DATA0(NAND_DATA00)	I, 1.8V CMOS	Serial Audio Interface Channel1 Data Input
23	GPIO11(WOWWAN#/HSIC_DATA(1.2V))(I/O) (0/1.8V)	SMARC_GPIO_12_GPIO3_21(NAND_DQS)	IO, 1.8V CMOS	M.2 Host Wake. *Note: SMARC_GPIO_12_GPIO3_21(NAND_DQS) Connected Optionally.*
24	GPIO7(AUDIO2/I2S_TX) (I/O)(0/1.8V)	SAI3_TX_DATA0(SAI3_TXD)	O, 1.8V CMOS	Serial Audio Interface Channel1 Data Output
25	DPR (O) (0/1.8V)	1_M.2_DPR	O, 1.8V CMOS	M.2 Dynamic Power Reduction Signal. *Note: SMARC_GPIO_13_GPIO3_28(HDMI_CEC) Connected Optionally.*
26	GPIO10_(W_DISABLE_2#/HSIC_STROBE(1.2V)) (I/O)(0/1.8V)	1_M.2_GPIO10	O, 3.3V CMOS 10K PU	NC.
27	GND	GND	Power	Ground.
28	GPIO8(AUDIO3/I2S_WS)(I/O)(0/1.8V)	SAI3_TX_SYNC(SAI3_TXFS)	IO, 1.8V CMOS	Serial Audio Interface Channel1 Left Right Clock
29	PERN1/USB30_RX-/SSIC_RX-	PCIE_RXN_N	O, PCIe	PCIe1 Receive Negative. *Note: To select PCIe Chanel Refer Table 17*
30	UIM-RESET (I)	SIM_RST1	O, SIM	SIM Card Reset Signal.

Pin No	Pin Name	Signal Name	Signal Type/ Termination	Description
31	PERP1/USB30_RX+/SSIC_RX+	NC	NC	NC.
32	UIM-CLK (I)	SIM_CLK1	I, SIM	SIM Card Clock Signal.
33	GND	GND	Power	Ground.
34	UIM-DATA (I/O)	SIM_DAT1	IO, SIM	SIM Card Data IO Signal.
35	PETN1/USB3.1-TX-/SSIC-TXN	NC	NC	NC.
36	UIM-PWR (I)	M2_UIM_PWR1	O, SIM Power	SIM Card Power.
37	PETP1/USB3.1-TX+/SSIC-TXP	NC	NC	NC.
38	DEVSLP (O)	1_M.2_DESLP	O, 3.3V CMOS 10K PU	NC.
39	GND	GND	Power	Ground.
40	GPIO0(SMB_CLK/GNSS_SCL/SIM_DET2)(I/O)(0/1.8V)	I2C2_SCL	O, 1.8V CMOS	I2C CLK.
41	PERN0/SATA_B+	NC	NC	NC.
42	GPIO1(SMB_DATA/GNSS_SDA/UIM_DAT2)(I/O)/(0/1.8V)	I2C2_SDA	IO, 1.8V CMOS	I2C Data.
43	PERP0/SATA_B-	PCIE_RXP	O, PCIe	PCIe0 Receive Positive. *Note: To select PCIe Chanel Refer Table 17*
44	GPIO2_(ALERT#/GNSS_IRQ/UIM_CLK2)(I)/(0/1.8V)	1_ALERT#	IO, 1.8V CMOS 10K PU	General Purpose Input Output. *Note: GPIO_SMB_ALERT_GPIO5_20 Connected Optionally.*
45	GND	GND	Power	Ground.
46	GPIO3(SYSCLK/GNSS_0/UIM_RST2)(I/O)(0/1.8V)	NC	NA	NC.
47	PETN0/SATA_A-	PCIE_TXN_N	I, PCIe	PCIe0 Transmit Negative. *Note: To select PCIe Chanel Refer Table 17*
48	GPIO4(TX_BLK/GNSS_1/UIM_PWR2)(I/O)(0/1.8V)	NC	NA	NC.
49	PETP0/SATA_A+	PCIE_TXN_P	I, PCIe	PCIe0 Transmit Positive. *Note: To select PCIe Chanel Refer Table 17*
50	PERST# (O)(0/3.3V)	GPIO_PCIE_RST(GPIO1_IO12)	O, 3.3V CMOS 10K PU	PCIe Resets Signal.

Pin No	Pin Name	Signal Name	Signal Type/ Termination	Description
51	GND	GND	Power	Ground.
52	CLKREQ# (I/O)(0/3.3V)	PCIE_CLKREQ_B	IO, 3.3V CMOS 10K PU	M.2 Clock Request Signal. *Note: PCIE_CLKREQ_B is optionally connected*
53	REFCLKN	PCIE_REFCLK_DM	O,PCIe	PCIe Channel Clock Negative.
54	PEWAKE# (I/O)(0/3.3V)	GPIO_PCIe_Wake(GPIO1_IO14)	O, 3.3V CMOS 10K PU	PCIe Wake Signal
55	REFCLKP	PCIE_REFCLK_DP	O,PCIe	PCIe Channel Clock Positive.
56	MFG_DATA	NC	NA	NC.
57	GND	GND	Power	Ground.
58	MFG_CLOCK	NC	NA	NC.
59	ANTCTL0 (I)(0/1.8 V)	NC	NA	NC.
60	COEX3 (I/O)(0/1.8V)	SMARC_GPIO_13_GPIO3_28(HDMI_CEC)	O, 1.8V CMOS	NC. *Note: SMARC_GPIO_13_GPIO3_28(HDMI_CEC) Connected Optionally*
61	ANTCTL1 (I)(0/1.8 V)	NC	NA	NC.
62	COEX_TXD (O)(0/1.8V)	UART3_TXD	I, 1.8V CMOS	NC. *Note: UART3_TXD Connected Optionally*
63	ANTCTL2 (I)(0/1.8 V)	NC	NA	NC.
64	COEX_RXD (I)(0/1.8V)	UART3_RXD	O, 1.8V CMOS	NC. *Note: UART3_RXD Connected Optionally*
65	ANTCTL3 (I)(0/1.8 V)	NC	NA	NC.
66	SIM_DETECT (I)	M.2_SIM_DETECT1	I, 1.8V CMOS 10K PU	NC
67	RESET# (O)(0/1.8V)	1_M.2_RESET#	I, 1.8V CMOS 10K PU	M.2 Reset Signal. *Note: GPIO_5_M2_RST Connected Optionally.*
68	SUSCLK(32KHZ) (O)(0/3.3V)	1_M.2_SUSCLK	I, 3.3V CMOS 33E Series	M.2 Clock *Note: Optionally connected 32.768kHz Clock Oscillator.*
69	CONFIG_1	1_M.2_CONFIG_1	I, 1.8V CMOS 10K PU	M.2 Configuration Pin 1.
70	VCC_3V3	VCC_3V3	O, 3.3V Power	3.3V Supply Voltage.
71	GND	GND	Power	Ground.
72	VCC_3V3	VCC_3V3	O, 3.3V Power	3.3V Supply Voltage.
73	GND	GND	Power	Ground.
74	VCC_3V3	VCC_3V3	O, 3.3V Power	3.3V Supply Voltage.
75	CONFIG_2	1_M.2_CONFIG_2	I, 1.8V CMOS 10K PU	M.2 Configuration Pin 2.

2.5.2 Secondary M.2 Interface (Optional)

Secondary M.2 Key-B Connector is ideal for interfacing USB based M.2 Modules and this M.2 connector is physically located at the bottom of the board.

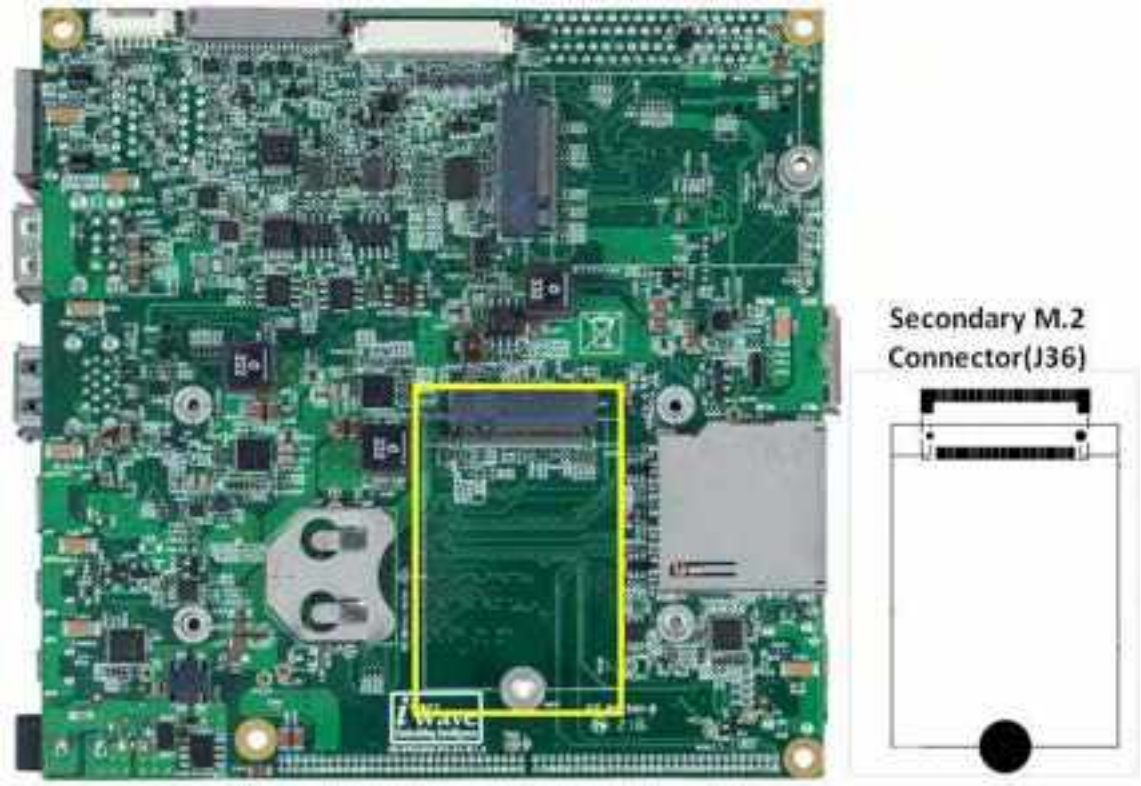


Figure 8: Secondary M.2 Connector

Table 8: Secondary M.2 Connector Pinout

Pin No	Pin Name	Signal Name	Signal Type/ Termination	Description
1	CONFIG_3	2_M.2_CONFIG_3	I, 1.8V CMOS 10K PU	M.2 Configuration Pin 3.
2	VCC_3V3	VCC_3V3	O, 3.3V Power	3.3V Supply Voltage.
3	GND	GND	Power	Ground.
4	VCC_3V3	VCC_3V3	O, 3.3V Power	3.3V Supply Voltage.
5	GND	GND	Power	Ground.
6	FULL_CARD_POWER _OFF# (O)(0/1.8V_3.3V)	2_M.2_PWR_OFF#	O, 3.3V CMOS 10K PU	M.2 Full card Power off Signal.
7	USB_D+	USB_HUBOUT2_DP	IO, USB	USB2.0 Data Plus.

Pin No	Pin Name	Signal Name	Signal Type/ Termination	Description
8	W_DISABLE1# (O)(0/3.3V)	2_M.2_W_DISABLE1#	O, 3.3V CMOS 10K PU	M.2 Wireless Disable Signal *Note: W_DISABLE Connected Optionally.*
9	USB_D-	USB_HUBOUT2_DM	IO, USB	USB2.0 Data Minus.
10	GPIO9(LED1#/DAS_DSS#)(I/0)(0/3.3V)	SATA_ACT#	O, 3.3V CMOS	Provide status indicators via LED. *Note* SATA_ACT# *Connected optionally*
11	GND	GND	Power	Ground.
12	B1	NC	NA	NC.
13	B2	NC	NA	NC.
14	B3	NC	NA	NC.
15	B4	NC	NA	NC.
16	B5	NC	NA	NC.
17	B6	NC	NA	NC.
18	B7	NC	NA	NC.
19	B8	NC	NA	NC.
20	GPIO5(AUDIO0/I2S_CLK(I/O)(0/1.8V)	NC	NA	NC.
21	CONFIG_0	2_M.2_CONFIG_0	I, 1.8V CMOS 10K PU	M.2 Configuration Pin 0.
22	GPIO6_(AUDIO1/I2S_RX) (I/O)(0/1.8V)	NC	NA	NC.
23	GPIO11(WOWWAN#/HSIC_DATA(1.2V))(I/O) (0/1.8V)	GPIO_12_M.2_HOST_WAKE	IO, 1.8V CMOS	M.2 Host Wake.
24	GPIO7(AUDIO2/I2S_TX) (I/O)(0/1.8V)	NC	NA	NC.
25	DPR (O) (0/1.8V)	SMARC_GPIO_13_GPIO3_28(HDMI_CEC)	O, 1.8V CMOS	M.2 Dynamic Power Reduction Signal.
26	GPIO10_(W_DISABLE_2#/HSIC_STROBE(1.2V)) (I/O)(0/1.8V)	2_M.2_GPIO10	O, 3.3V CMOS 10K PU	
27	GND	GND	Power	Ground.
28	GPIO8(AUDIO3/I2S_WS)(I/O)(0/1.8V)	NC	NA	NC.
29	PERN1/USB30_RX-/SSIC_RX-	NC	NA	NC.
30	UIM-RESET (I)	SIM_RST2	O, SIM	SIM Card Reset Signal.
31	PERP1/USB30_RX+/SSIC_RX+	NC	NA	NC.
32	UIM-CLK (I)	SIM_CLK2	I, SIM	SIM Card Clock Signal.
33	GND	GND	Power	Ground.
34	UIM-DATA (I/O)	SIM_DAT2	IO, SIM	SIM Card Data IO Signal.
35	PETN1/USB3.1-TX-	NC	NA	NC.

Pin No	Pin Name	Signal Name	Signal Type/ Termination	Description
	/SSIC-TXN			
36	UIM-PWR (I)	M2_UIM_PWR2	O, SIM Power	SIM Card Power.
37	PETP1/USB3.1-TX+/SSIC-TXP	NC	NA	NC.
38	DEVSLP (O)	2_M.2_DEVSLP	NC	NC.
39	GND	GND	Power	Ground.
40	GPIO0(SMB_CLK/GNSS_SCL/SIM_DET2)(I/O)(0/1.8V)	I2C2_SCL	O, 1.8V CMOS	I2C CLK.
41	PERN0/SATA_B+	NC	NA	NC.
42	GPIO1(SMB_DATA/GNSS_SDA/UIM_DAT2)(I/O)/(0/1.8V)	I2C2_SDA	IO, 1.8V CMOS	I2C Data.
43	PERP0/SATA_B-	NC	NA	NC.
44	GPIO2_(ALERT#/GNSS_IRQ/UIM_CLK2)(I)/(0/1.8V)	GPIO_SMB_ALERT_GPIO5_20	IO, 1.8V CMOS 10K PU	General Purpose Input Output.
45	GND	GND	Power	Ground.
46	GPIO3(SYSCLK/GNSS_0/UIM_RST2)(I/O)(0/1.8V)	NC	NA	NC.
47	PETN0/SATA_A-	NC	NA	NC.
48	GPIO4(TX_BLK/GNSS_1/UIM_PWR2)(I/O)(0/1.8V)	NC	NA	NC.
49	PETP0/SATA_A+	NC	NA	NC.
50	PERST# (O)(0/3.3V)	NC	NA	NC.
51	GND	GND	Power	Ground.
52	CLKREQ# (I/O)(0/3.3V)	NC	NA	NC.
53	REFCLKN	NC	NA	NC.
54	PEWAKE# (I/O)(0/3.3V)	NC	NA	NC.
55	REFCLKP	NC	NA	NC.
56	MFG_DATA	NC	NA	NC.
57	GND	GND	Power	Ground.
58	MFG_CLOCK	NC	NA	NC.
59	ANTCTL0 (I)(0/1.8 V)	NC	NA	NC.
60	COEX3 (I/O)(0/1.8V)	SMARC_GPIO_13_GPIO3_28(HDMI_CEC)	O, 1.8V CMOS	NC. *Note: SMARC_GPIO_13_GPIO3_28(HDMI_CEC) Connected Optionally*

Pin No	Pin Name	Signal Name	Signal Type/ Termination	Description
61	ANTCTL1 (I)(0/1.8 V)	NC	NA	NC.
62	COEX_TXD (O)(0/1.8V)	UART3_TXD	I, 1.8V CMOS	NC. *Note: UART3_TXD Connected Optionally*
63	ANTCTL2 (I)(0/1.8 V)	NC	NA	NC.
64	COEX_RXD (I)(0/1.8V)	UART3_RXD	O, 1.8V CMOS	NC. *Note: UART3_RXD Connected Optionally*
65	ANTCTL3 (I)(0/1.8 V)	NC	NA	NC.
66	SIM_DETECT (I)	NC	NA	NC.
67	RESET# (O)(0/1.8V)	SMARC_GPIO_5_GPIO 3_20(SAI5_RXC)	I, 1.8V CMOS 10K PU	M.2 Reset Signal.
68	SUSCLK(32KHZ) (O)(0/3.3V)	2_M.2_SUSCLK	I, 3.3V CMOS 33E Series	M.2 Clock *Note: Optionally connected 32.768kHz Clock Oscillator.*
69	CONFIG_1	2_M.2_CONFIG_1	I, 1.8V CMOS 10K PU	M.2 Configuration Pin 1.
70	VCC_3V3	VCC_3V3	O, 3.3V Power	3.3V Supply Voltage.
71	GND	GND	Power	Ground.
72	VCC_3V3	VCC_3V3	O, 3.3V Power	3.3V Supply Voltage.
73	GND	GND	Power	Ground.
74	VCC_3V3	VCC_3V3	O, 3.3V Power	3.3V Supply Voltage.
75	CONFIG_2	2_M.2_CONFIG_2	I, 1.8V CMOS 10K PU	M.2 Configuration Pin 2.

2.5.3 USB3.0 Host Interface

The i.MX 8M Plus Q/QL/D SMARC Carrier board supports Super Speed USB3.0 Host interface through on SOM USB3.0 Hub. This USB3.0 signals of SMARC USB2 and USB3 port from MXM connector is directly connected to bottom and top port of dual stack USB3.0 Type-A connector (J17) respectively. Also, USB2.0 signals of USB2 and USB3 Port of SMARC signals are connected to respective connector from 3.0 USB Hub used on SOM. The top port of J17 connector is shared with USB Type-C connector (J20).

The selection between USB Type C connector and top port of dual stack USB3.0 TypeA connector can be done by setting the 4th bit of Board configuration switch (SW6) to appropriate position. If the 4th bit of Board configuration switch (SW6) is set to OFF position, then USB3 port of SMARC MXM connector is connected to USB Type C connector. If the 4th bit of Board configuration switch (SW6) is set to ON position, then USB3 port of SMARC MXM connector is connected to top port of dual stack USB3.0 TypeA connector. Also USB2.0 signals of USB3 Port of SMARC MXM connector is connected to both these connectors.

To support double-way plug in on USB TypeC connector, USB3 signals are connected to FUSB340TMX USB3.0 switch and then connected to USB Type C connector. This USB3.0 switch port connection to Type C connector top or bottom is controlled through GPIO4_2(P112nd pin) of the SMARC MXM connector.

The VBUS power of this USB3.0 connector is connected through current limit power switch and limit is set as 900mA. If connected USB3.0 device takes more than 900mA current, this power switch limits the current to constant mode and sends the over current indication signal to the over current indicator pin of SMARC MXM connector USB2 and USB3 ports. This USB3.0 connector is physically located at the top of the board as shown below.

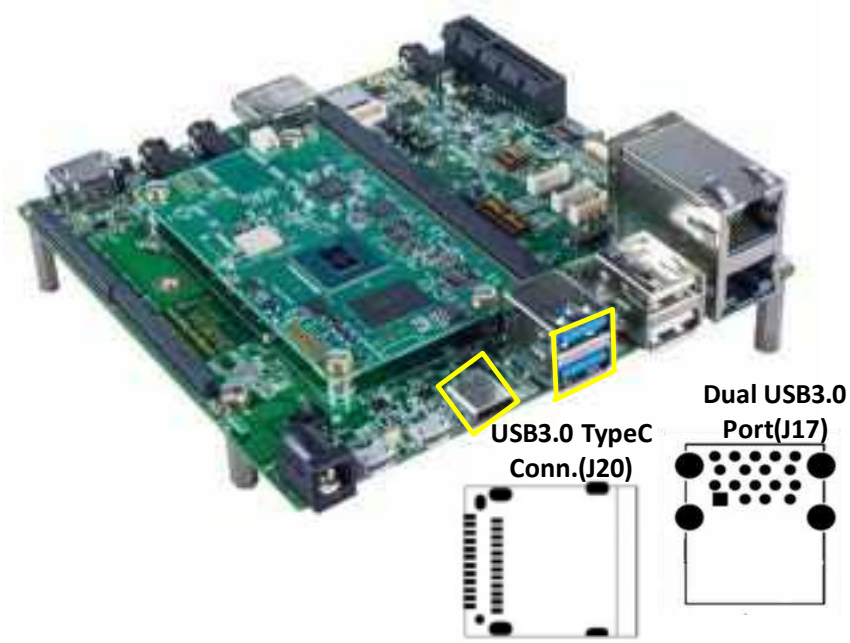


Figure 9: USB3.0 Host

2.6 Communication Interface Features

2.6.1 Dual Gigabit Ethernet Ports

The i.MX 8M Plus Q/QL/D SMARC carrier board supports Dual Ethernet Ports through GBE0 and GBE1 ports of SMARC MXM connector which supports 10/100/1000Mbps Ethernet. The GBE0 and GBE1 signals from SMARC MXM connector are directly connected to Dual Stack RJ45 Magjack (J8) Top & Bottom connector respectively. This RJ45 Magjack combo connector is physically located at the top of the board as shown below.

Figure 10: Dual Stack RJ45 Magjack

2.6.2 USB2.0 Host Port

The i.MX 8 Q/QL/D SMARC carrier board supports additional two USB2.0 Host interface through USB1 and USB4 ports of SMARC MXM connector. USB1 signals from the edge connector is connected to on board 1:4 USB hub. The primary port is directly connected to J13 TOP and secondary port is connected to SATA M.2 connector, 3rd and 4th Port of the USB2.0 HUB are connected to USB Touch header and PCIe M.2 Module (Optional) respectively. Whereas USB4 port from the SMARC edge connector is directly connected to BOTTOM side of J13 connector.

The VBUS power of this USB2.0 connector is connected through current limit power switch and limit is set as 500mA. If connected USB2.0 device takes more than 500mA current, this power switch limits the current to constant mode and sends the over current indication signal to the over current indicator pin of SMARC MXM connector USB1 and USB4 ports. This USB2.0 connector is physically located at the top of the board as shown below

Figure 11: USB2.0 Host Port

2.6.3 USB2.0 OTG Interface(optional)

The i.MX 8M Plus Q/QL/D SMARC Carrier board supports USB2.0 High Speed OTG interface through i.MX8 CPU's USB0 interface. This USB2.0 Port0 signals of SMARC MXM connector is directly connected to USB2.0 MicroAB connector (J22). This port can be used as USB OTG functionality which supports USB host and USB device based on USB ID pin status.This USB2.0 OTG connector is physically located at the top of the board as shown below.

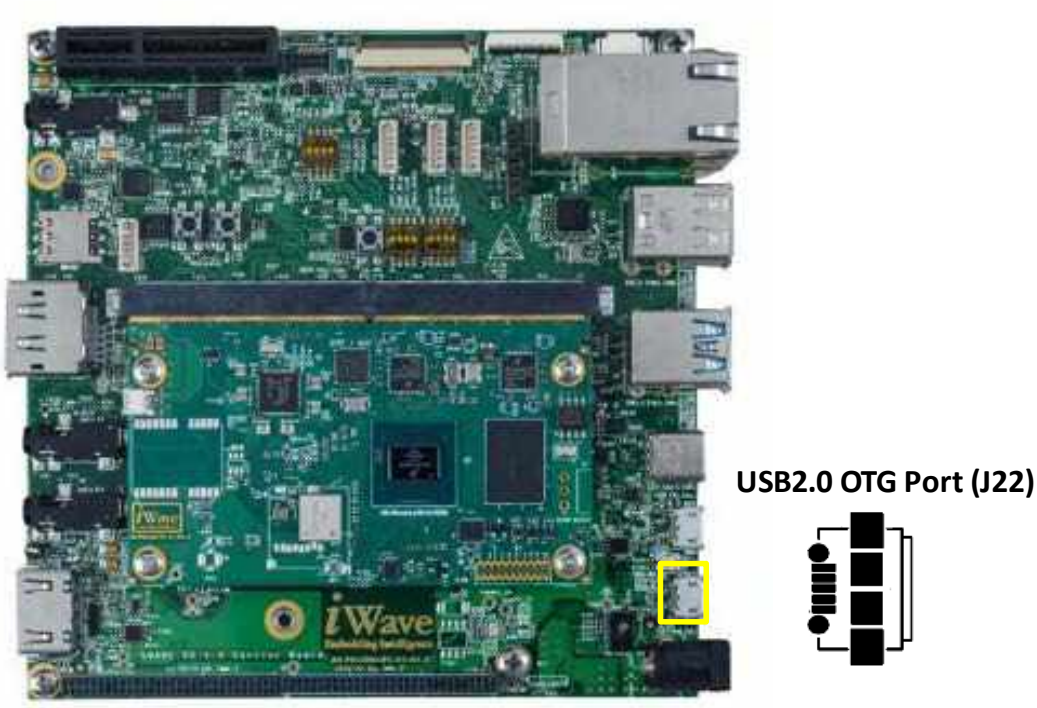


Figure 12: USB2.0 OTG Port

2.6.4 SDIO Interface

The i.MX 8M Plus Q/QL/D SMARC carrier board supports SDIO interface through SoC's uSDHC2 interface. This uSDHC2 signals from SMARC MXM connector is connected to SD connector (J34) to support Standard SD interface. This connector supports up to 4-bit data transfer with card detect and write protect.

The main power to SD/MMC connector is 3.3V and it is connected through power switch to support power enable/disable feature. This power enable/disable is controlled from the SDIO_PWR_EN pin (P37th) of SMARC MXM connector. This SD connector (J34) is physically located at the bottom of the board as shown below.

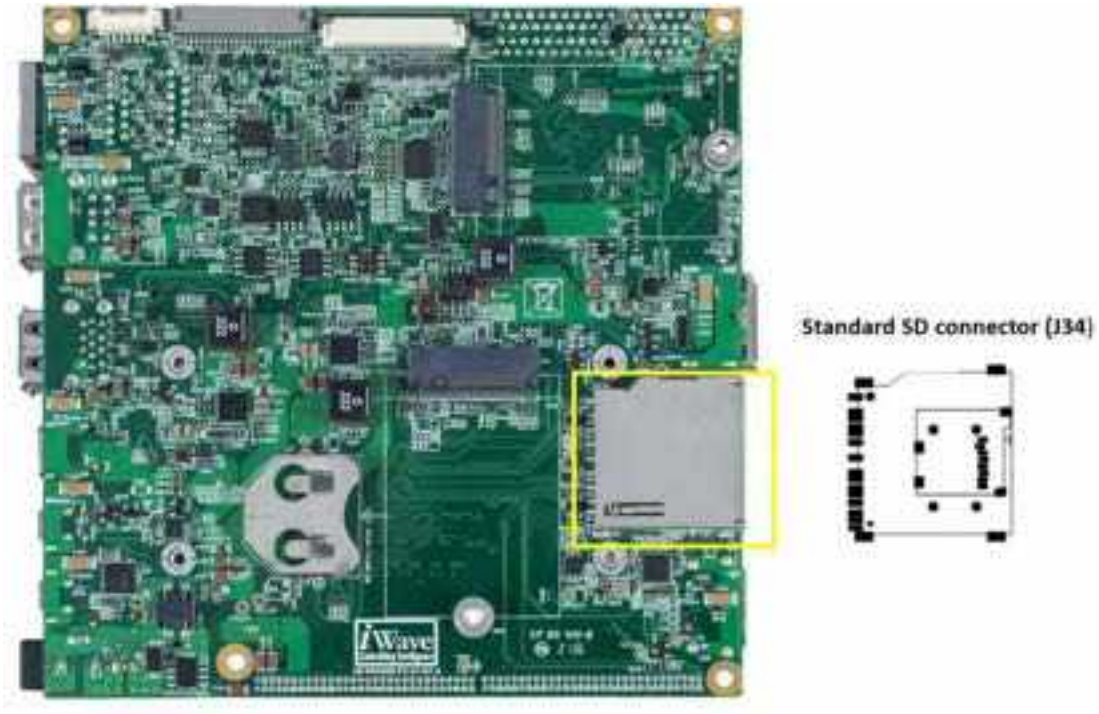


Figure 13: SDIO Port

2.6.5 CAN Interface

The SMARC Carrier Board supports two Control Area Network (CAN) Ports. Both CAN0 and CAN1 from the SMARC Edge connector are connected to MCP2562FD-E/SN CAN Transceiver and CANL & CANH of the transceiver are connected to J9 (CAN1) and J12(CAN0) connectors. Both Connector are placed on Top Side of the Board.

Number of Pins	6
Connector Part number	: 53047-0610 from Molex
Mating Connector Housing	: 0510210600 from Molex

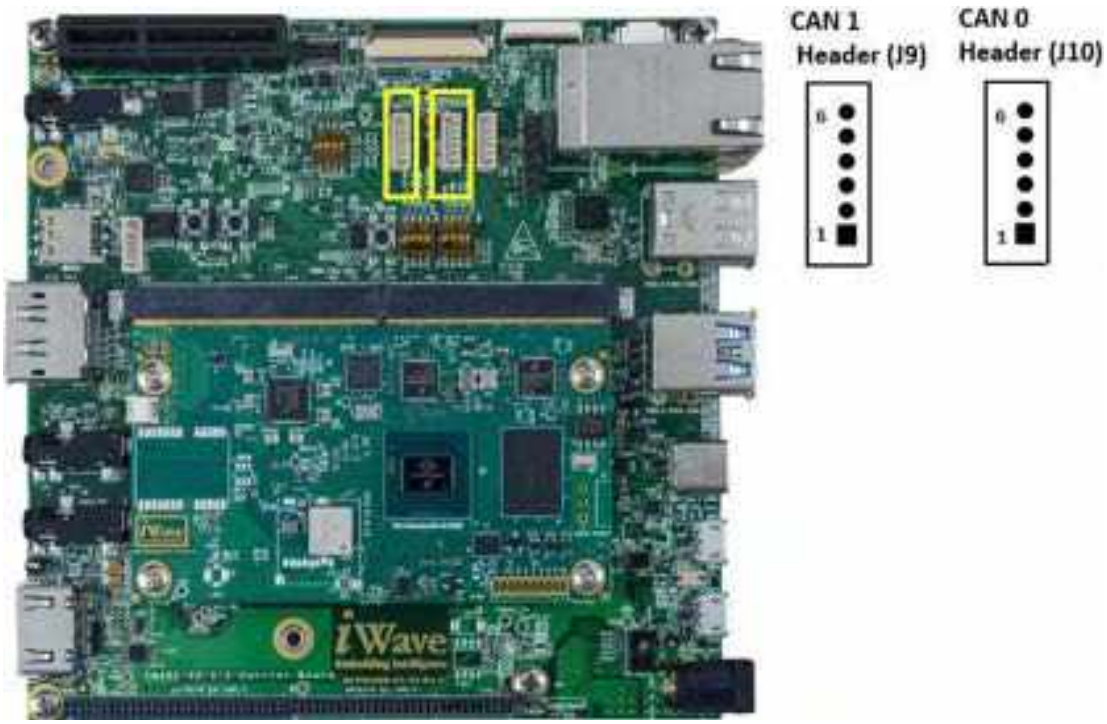


Figure 14: CAN Header

Table 9: CAN0 Header Pinout

Pin No	Pin Name	Signal Name	Signal Type/ Termination	Description
1	VCC_5V	VCC_5V	O, 5V Power	*Note: Optionally connected to 5V supply Voltage.*
2	VCC_12V	NC	NA	*Note: Optionally connected to 12V supply Voltage.*
3	CANL	FLEXCAN1_TX(SAI5_RXD1)	IO, DIFF	CAN0 Low-Level Voltage I/O
4	GND	GND	Power	Ground.
5	CANH	FLEXCAN1_RX(SAI5_RXD2)	IO, DIFF	CAN0 High-Level Voltage I/O
6	GND	GND	Power	Ground.

Table 10: CAN1 Header Pinout

Pin No	Pin Name	Signal Name	Signal Type/ Termination	Description
1	VCC_5V	VCC_5V	O, 5V Power	*Note: Optionally connected to 5V supply Voltage*
2	VCC_12V	NC	NA	*Note: Optionally connected to 12V supply Voltage.*
3	CANL	FLEXCAN2_TX(SAI5_RXD3)	IO, DIFF	CAN1 Low-Level Voltage I/O
4	GND	GND	Power	Ground.
5	CANH	FLEXCAN2_RX(SAI5_MCLK)	IO, DIFF	CAN1 High-Level Voltage I/O
6	GND	GND	Power	Ground.

2.7 Audio & Video Features

2.7.1 I2S Audio Interface

The i.MX 8M Plus Q/QL/D SMARC carrier board supports Audio In and Out through SoC's SAI2 interface which can support I2S format. This four wire I2S signals from SMARC MXM connector is connected to I2S Audio Codec "SGTL5000" to support Headphone Stereo output and Mono Mic input through 3.5mm audio Jack J21 and J19 correspondingly. Also, Headphone detect and Mic detect is supported through GPIO8 (P116th) & GPIO11 (P119th) pin of SMARC MXM connector correspondingly. These Audio Jacks are physically located at the top of the board as shown below.

The i.MX8 SMARC carrier board supports Second Audio IN and OUT through CPU's SAI3 interface which can support I2S format and also SAI3 interface optionally connected to the PCIe M.2 Connector. These four wire I2S signals from SMARC MXM connector is direct connected to I2S Audio Codec "WM8960CGEFL/RV" to support Headphone Stereo output and Mono Mic input through 3.5mm single audio Jack J7. Second Codec is not supported in default BSP, contact iWave support team for enabling second I2S Audio Codec "WM8960CGEFL/RV".

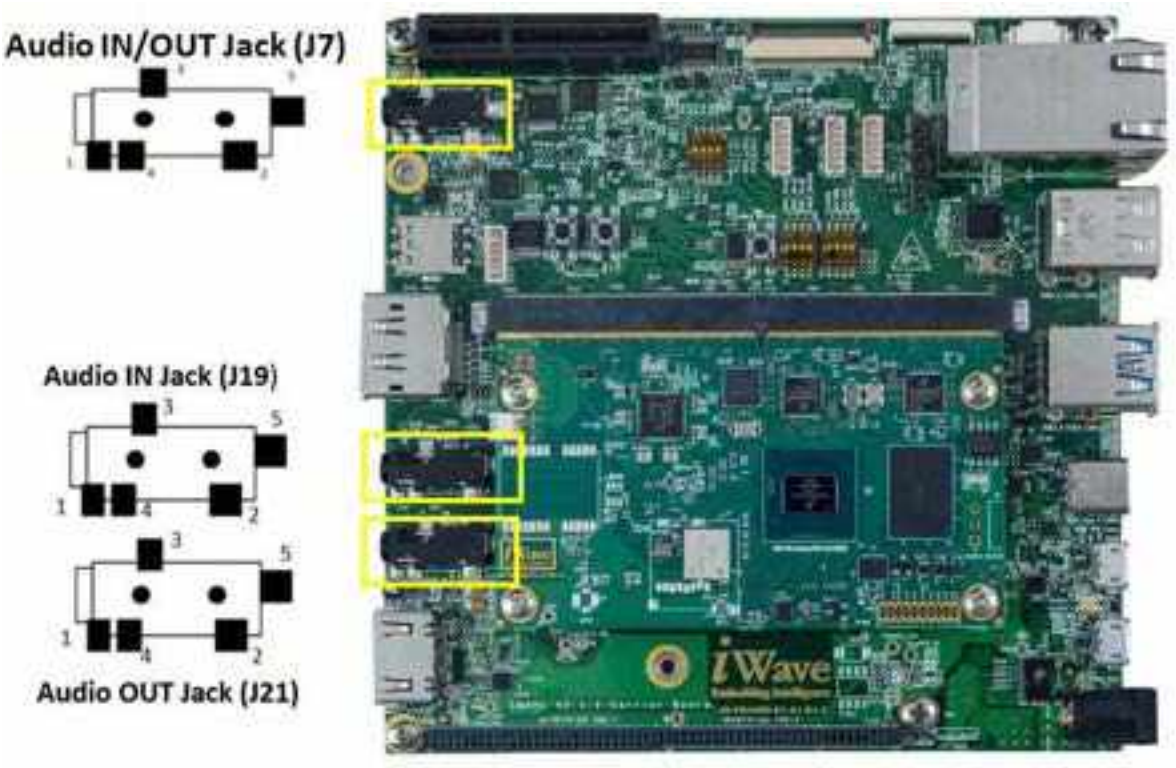


Figure 15: Audio In and Out Ports

2.7.2 MIPI DSI Display

The i.MX 8M Plus Q/QL/D SMARC carrier board supports 4 lane 39 pin MIPI display. i.MX8 CPU's MIPI_DSI0 interface from SMARC MXM connector is used for this LCD interface. This MIPI_DSI0 interface signals are connected to Display connector (J1) via EMI protection circuit and is physically located at the top of board as shown below.

Number of Pins : 39

Connector Part number :5025983993 from Molex

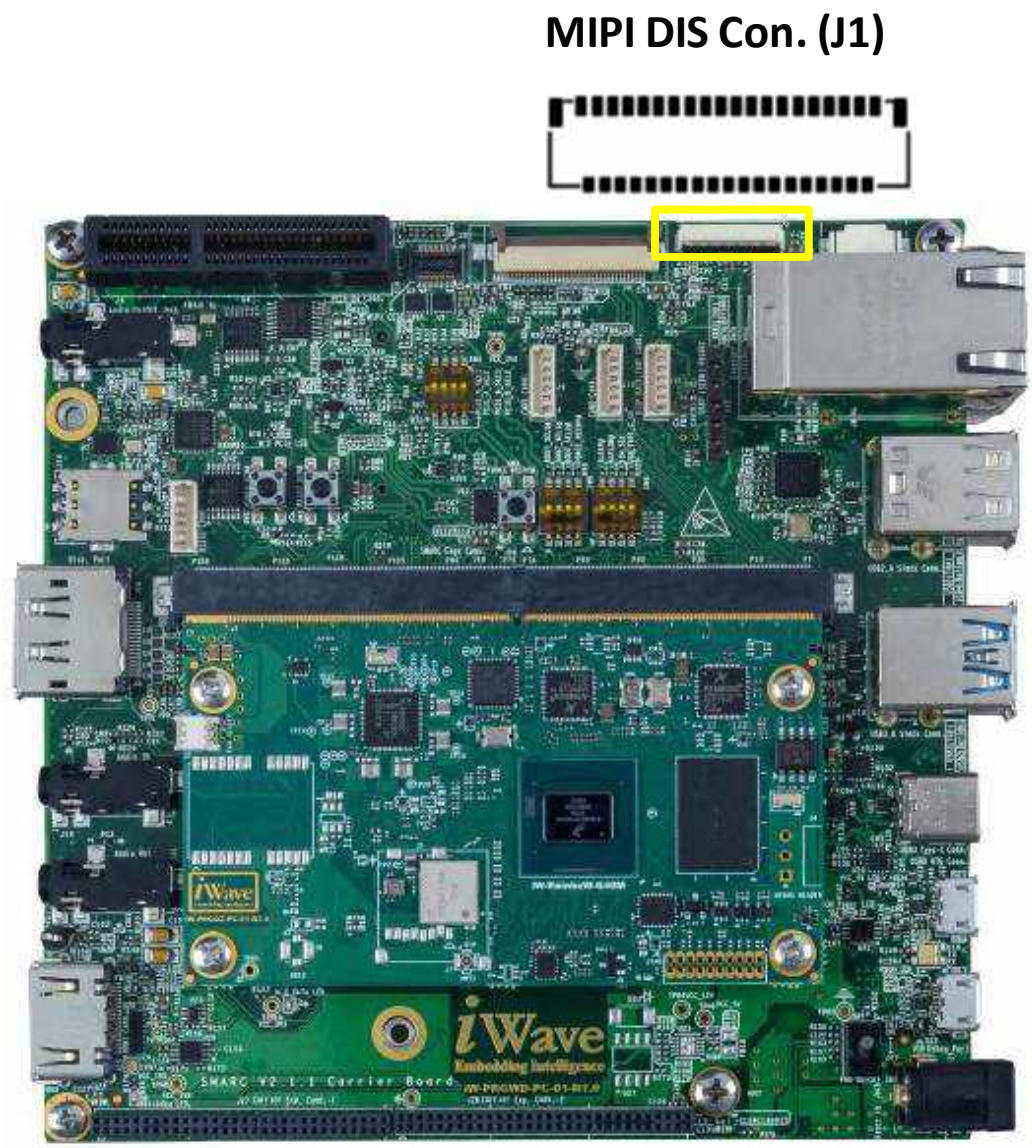


Figure 16: MIPI DSI Display Connector

Table 11: MIPI DSI Display Connector Pin Out

Pin No	Pin Name	Signal Name	Signal Type / Termination	Description
1	GND	GND	Power	Ground.
2	GND	GND	Power	Ground.
3	GND	GND	Power	Ground.
4	VBAT	VCC_3V3_TFT0	O,3.3V Power	3.3V Supply voltage for LED Driver Circuit.
5	VBAT	VCC_3V3_TFT0	O,3.3V Power	3.3V Supply voltage for LED Driver Circuit.
6	VBAT	VCC_3V3_TFT0	O,3.3V Power	3.3V Supply voltage for LED Driver Circuit.
7	VBAT	VCC_3V3_TFT0	O,3.3V Power	3.3V Supply voltage for LED Driver Circuit.
8	VBAT	VCC_3V3_TFT0	O,3.3V Power	3.3V Supply voltage for LED Driver Circuit.
9	GND	GND	Power	Ground.
10	OTPV	NC	NA	NA.
11	NC1	NC	NA	NA.
12	GND	GND	Power	Ground.
13	D3P	MIPI_DSI0_D3_P	O, MIPI	MIPI_DSI DATA Lane3 Positive
14	D3N	MIPI_DSI0_D3_N	O, MIPI	MIPI_DSI DATA Lane3 Negative
15	GND	GND	Power	Ground.
16	D0P	MIPI_DSI0_D0_P	O, MIPI	MIPI_DSI DATA Lane 0 Positive
17	D0N	MIPI_DSI0_D0_N	O, MIPI	MIPI_DSI DATA Lane 0 Negative
18	GND	GND	Power	Ground.
19	DKP	MIPI_DSI0_CLK_P	O, MIPI	MIPI_DSI Clock Positive
20	DKN	MIPI_DSI0_CLK_N	O, MIPI	MIPI_DSI Clock Negative
21	GND	GND	Power	Ground.
22	D1P	MIPI_DSI0_D1_P	O, MIPI	MIPI_DSI DATA Lane 1 Positive
23	D1N	MIPI_DSI0_D1_N	O, MIPI	MIPI_DSI DATA Lane 1 Negative
24	GND	GND	Power	Ground.
25	D2P	MIPI_DSI0_D2_P	O, MIPI	MIPI_DSI DATA Lane2 Positive
26	D2N	MIPI_DSI0_D2_N	O, MIPI	MIPI_DSI DATA Lane2 Negative
27	GND	GND	Power	Ground.

Pin No	Pin Name	Signal Name	Signal Type / Termination	Description
28	RESX	DSI_RST1	O, 1.8V CMOM	RESET
29	VDDIO	VCC_1V8	O, 1.8V Power	1.8V Supply voltage for Display IO Circuit.
30	VCI	VCC_3V3_TFT0	O, 3.3V Power	3.3V Supply voltage for Display Circuit.
31	NC2	NC	NA	NA.
32	GND	GND	Power	Ground.
33	TP_AVDD_3P3V	VCC_3V3_TFT0	O, 3.3V Power	3.3V Supply voltage for Touch driver Circuit.
34	TP_DVDD_1P8V	VCC_1V8	O, 1.8V Power	1.8V Supply voltage for Touch IO Circuit.
35	TP_SDA	I2C5_SDA(SPDIF_RX)	IO, 1.8V CMOS	I2C Data for Capacitive Touch
36	TP_SCL	I2C5_SCL(SPDIF_TX)	O, 1,8V CMOS	I2C Clock for Capacitive Touch
37	TP_RESET	GPIO_RESET_OUT_GPIO1_9_1V8	O, 1.8V CMOS	RESET for Capacitive Touch
38	TP_INT	SMARC_GPIO_7_GPIO4_21(SAI2_RXFS)	I, 1.8V CMOS	Interrupt from Capacitive Touch
39	GND	GND	Power	Ground.

2.7.3 LVDS Connector (Optional)

The i.MX 8M Plus SMARC carrier board supports LVDS Connector (J30) as an optional feature from i.MX 8M Plus SoC. The i.MX 8M Plus processor supports both LVDS and MIPI DSI Display but SMARC Edge connector supports any one display interface. Contact iWave Support team for LVDS based SOM module. The LVDS Connector (J30) connector is placed on Bottom side of the board.

Number of Pins : 20

Connector Part number : DF19G-20P-1H(52) from Hirose

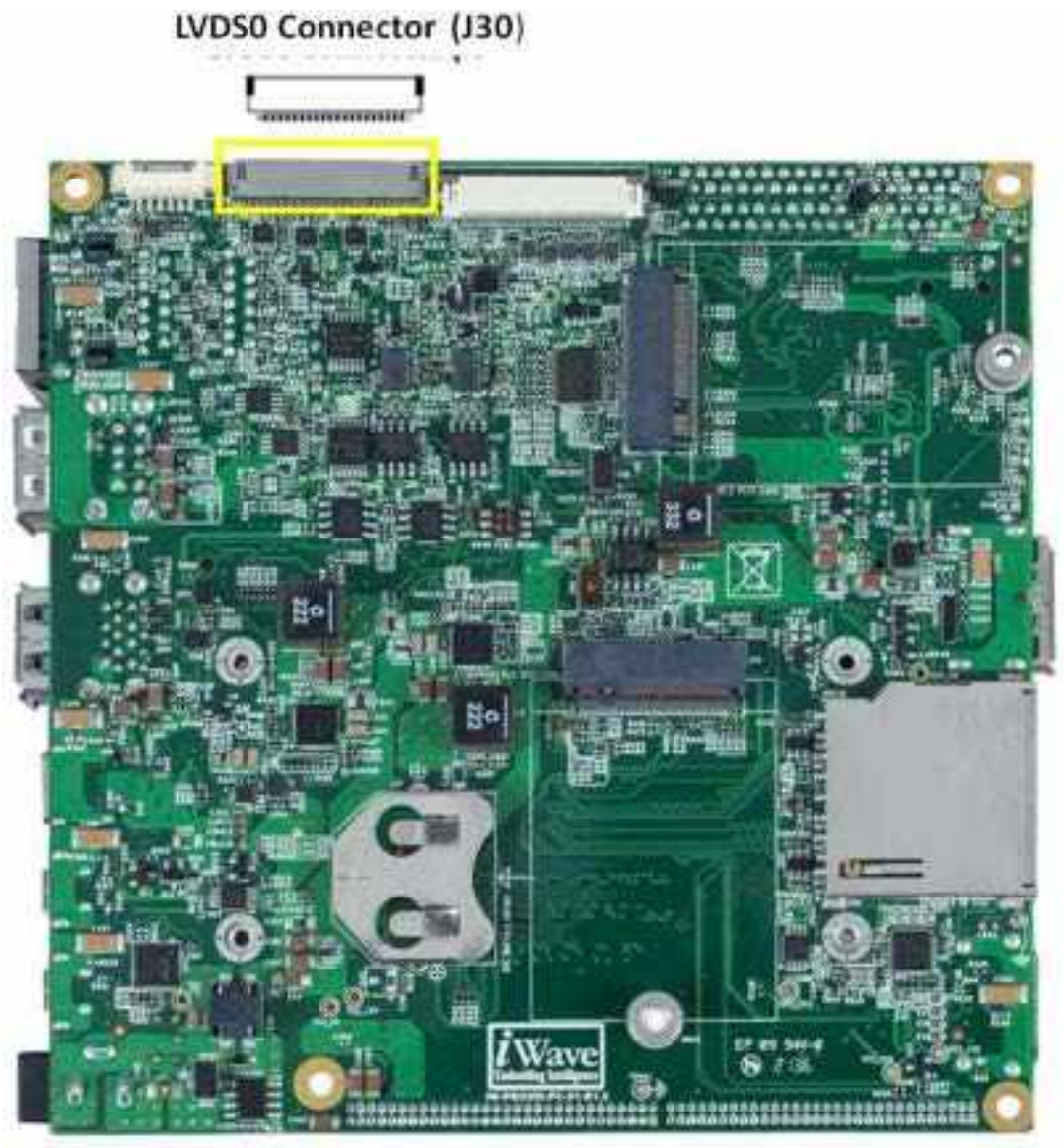


Figure 17: LVDS Display Connector

Table 12: LVDS Connector Pinout

Pin No	Pin Name	Signal Name	Signal Type / Termination	Description
1	VDD1	VCC_3V3_TFT0	Power	3.3V Supply voltage
2	VDD2	VCC_3V3_TFT0	Power	3.3V Supply voltage
3	GND1	GND	Power	Ground
4	GND2	GND	Power	Ground
5	RIN0-	LVDS0/DSI0_D0_N	IO, DIFF	LVDS channel differential pair0 negative
6	RIN0+	LVDS0/DSI0_D0_P	IO, DIFF	LVDS channel differential pair0 positive
7	GND3	GND	Power	Ground
8	RIN1-	LVDS0/DSI0_D1_N	IO, DIFF	LVDS channel differential pair1 negative
9	RIN1+	LVDS0/DSI0_D1_P	IO, DIFF	LVDS channel differential pair1 positive
10	GND4	GND	Power	Ground

Pin No	Pin Name	Signal Name	Signal Type / Termination	Description
11	RIN2-	LVDS0/DSI0_D2_N	IO, DIFF	LVDS channel differential pair2 negative
12	RIN2+	LVDS0/DSI0_D2_P	IO, DIFF	LVDS channel differential pair2 positive
13	GND5	GND	Power	Ground
14	CLKIN-	LVDS0/DSI0_CLK_N	IO, DIFF	LVDS channel differential Clock negative
15	CLKIN+	LVDS0/DSI0_CLK_P	IO, DIFF	LVDS channel differential Clock positive
16	GND6	GND	Power	Ground
17	RIN3-	LVDS0/DSI0_D3_N	IO, DIFF	LVDS channel differential pair3 negative
18	RIN3+	LVDS0/DSI0_D3_P	IO, DIFF	LVDS channel differential pair3 positive
19	GND7	GND	Power	Ground
20	GND8	GND	Power	Ground

2.7.4 HDMI Port

The i.MX 8M Plus Q/QL/D SMARC Carrier board supports HDMI audio/video out through i.MX 8M Plus SoC's HDMI 2.0a interface. HDMI Signals from the SMARC connector is connected to Standard HDMI Type-A connector with ESD protection circuitry. HDMI Output connector (J25) is physically located on top of the board as shown below.

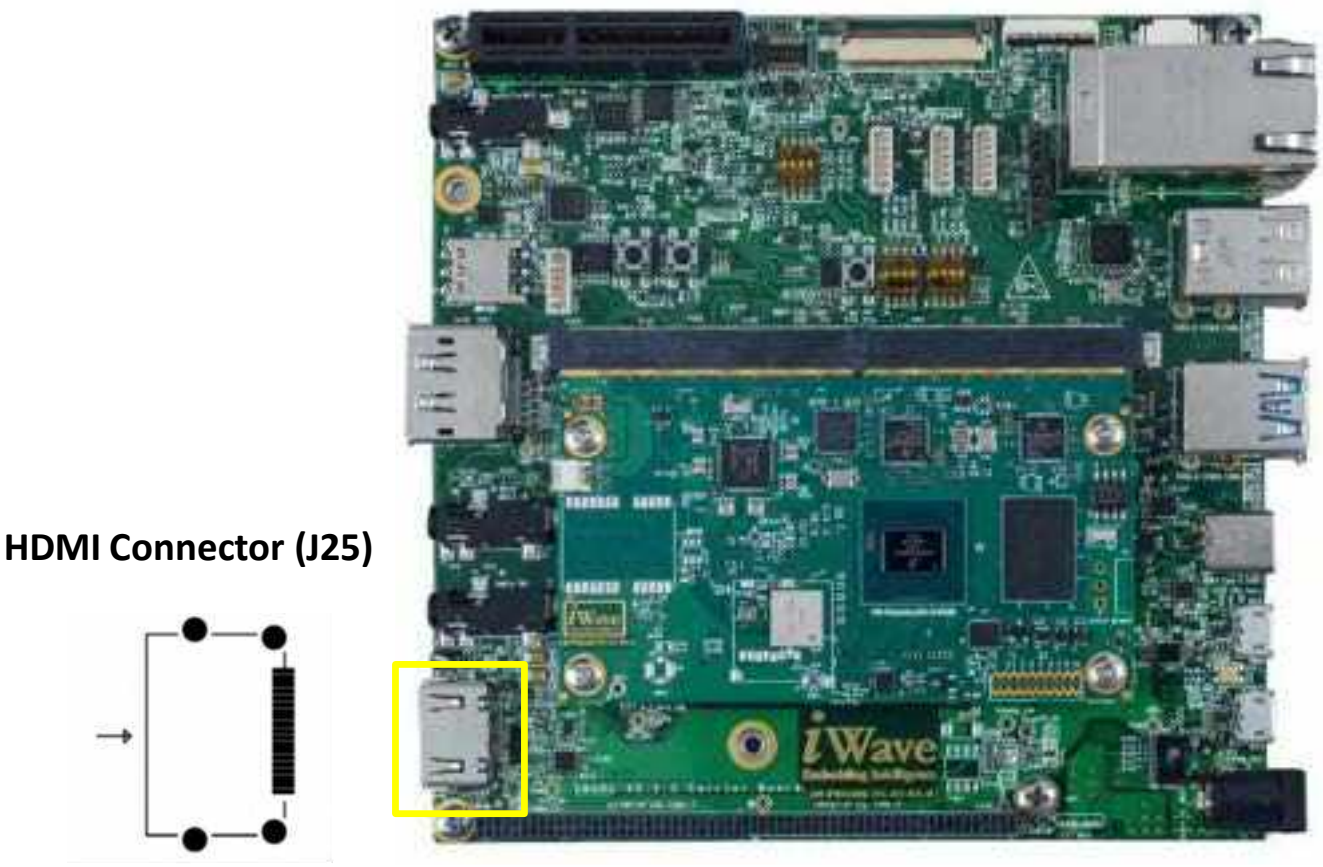


Figure 18: HDMI Port

2.7.5 MIPI CSI Camera

The i.MX 8M Plus Q/QL/D SMARC Carrier board supports OV5640 sensor based MIPI CSI camera which supports 5MP of resolution. i.MX 8M Plus Q/QL/D SoC's dual lane MIPI CSI0 interface from SMARC MXM connector is used for this Camera interface and i.MX 8M Plus CPU's 4 lane MIPI CSI1 interface from SMARC MXM connector is connected to 36 pins FPC Camera connector, This FPC Camera connector can be used to design Custom Camera module or Customer can make use of the iWave Camera module which is already ready to use. This MIPI CSI0 camera connector (J6) and This MIPI CSI1 camera FPC connector (J4) is physically located on top of the board as shown below.

Number of Pins : 24

Connector Part number : AXK724147G from Panasonic

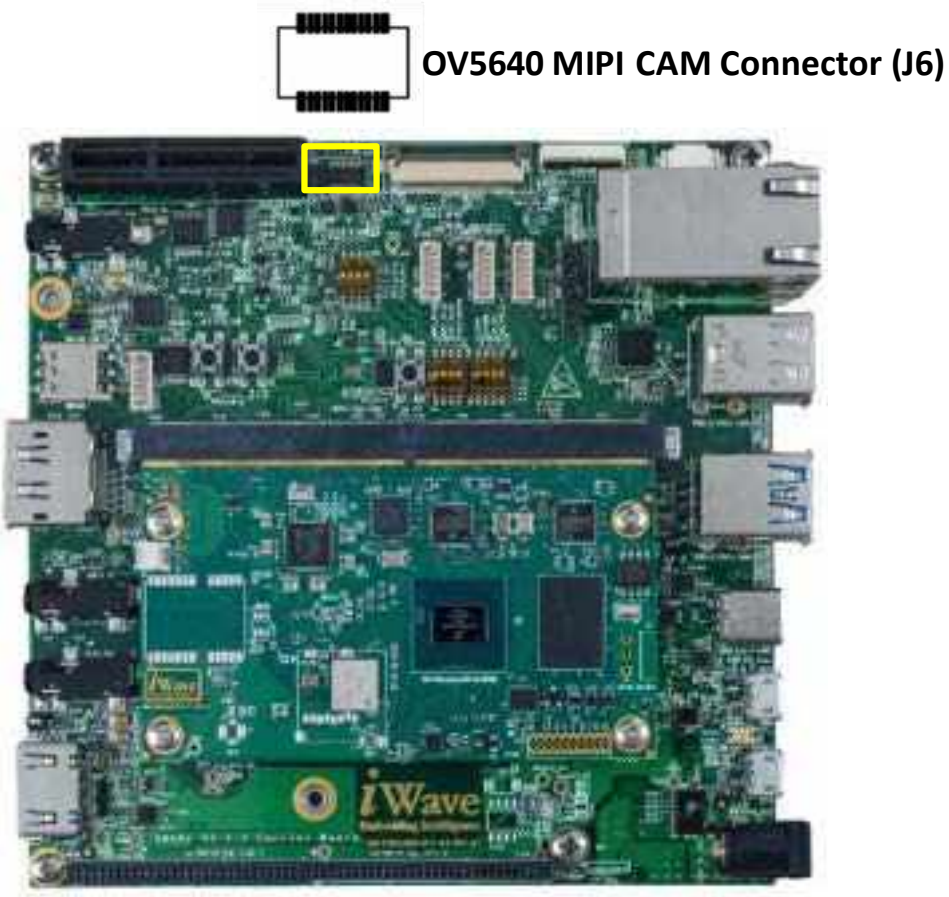


Figure 19: MIPI Camera Connect

Table 13: MIPI Camera Connector Pin Out

Pin No	Pin Name	Signal Name	Signal Type / Termination	Description
1	Strobe	NC	NA	NA
2	AGND	AGND	Power	Analog Ground.
3	SDA	I2C3_SDA	IO, 1.8V OD/4.7K PU	I2C3 Data for Camera

Pin No	Pin Name	Signal Name	Signal Type / Termination	Description
4	AVDD	AVDD	O, Power	2.8V Supply voltage
5	SCL	I2C3_SCL	O, 1.8V OD/ 4.7K PU	I2C3 Clock for Camera
6	RESET	SMARC_GPIO_2_GPIO4_0(SAI1_RXFS)	O, 1.8V CMOS 10k PD	Reset Output GPIO from SoC.
7	NC	NC	NA	NA
8	PWDN	PWDN	O, 1.8V CMOS 10k PD	Power Down Output
9	NC	NC	NA	NA
10	DVDD	DVDD	I, Power	1.5V Supply voltage
11	DOVDD	DOVDD	I, Power	1.8V Supply voltage
12	MDP1	MIPI_CSI1_D1_P	I, MIPI	MIPI_CSI DATA Lane1 Positive
13	XCLK	CAMERA_CCMCLKO1(ECSPI2_MISO)	O, CMOS	Reference Clock to Camera Module
14	MDN1	MIPI_CSI1_D1_N	O, MIPI	MIPI_CSI DATA Lane1 Negative
15	DGND	GND	Power	Ground.
16	MCP	MIPI_CSI1_CLK_P	I, MIPI	MIPI_CSI Clock Positive
17	NC	NC	NA	NA
18	MCN	MIPI_CSI1_CLK_N	I, MIPI	MIPI_CSI Clock Negative
19	NC	NC	NA	NA
20	MDP0	MIPI_CSI1_D0_P	I, MIPI	MIPI_CSI DATA Lane0 Positive
21	NC	NC	NA	NA
22	MDN0	MIPI_CSI1_D0_N	I, MIPI	MIPI_CSI DATA Lane0 Negative
23	AF-VCC	AF-VCC	I, Power	1.8V Supply voltage
24	AF-AGND	AF-AGND	Power	AF Ground.

Number of Pins J4/J3 : 36/40

Connector Part number J4/J3 : FH12A-36S-0.5SH(55) from Hirose/ FH12A40S-0.5SH(55) from Hirose

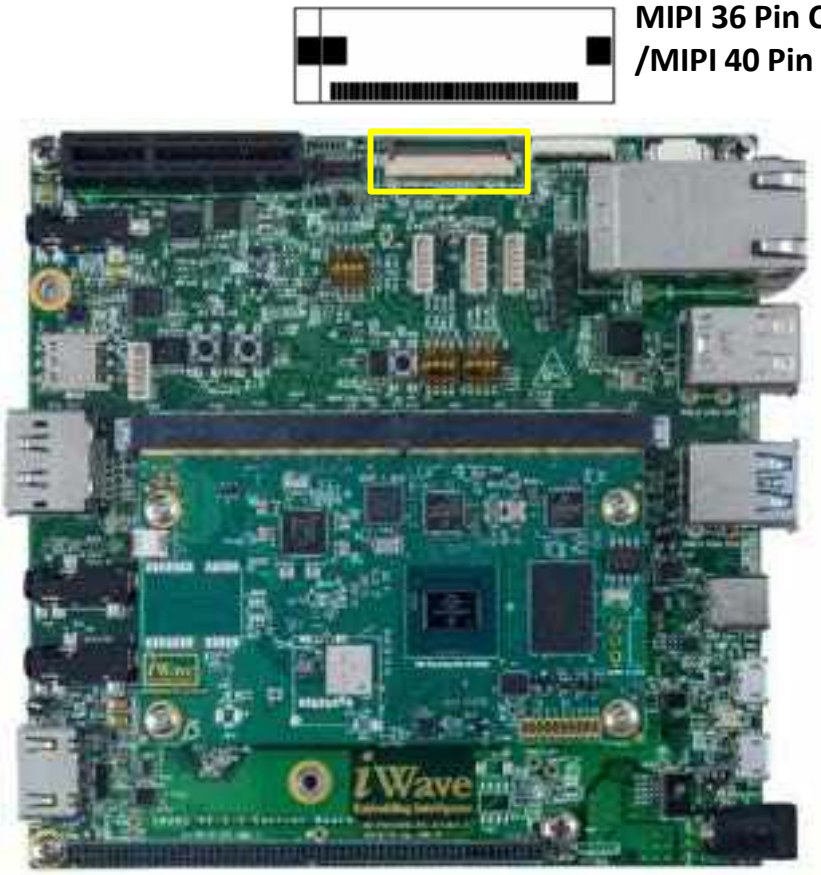


Figure 20: MIPI Camera Connector

Table 14: MIPI CSI FPC Camera 36 Pin Connector Pinout

Pin No.	Pin Name	Signal Name	Signal Type / Termination	Description
1	CAM_PWR	VCC_3V3	Power	3V3 Camera Power
2	CAM_PWR	VCC_3V3	Power	3V3 Camera Power
3	CAM0_CSI_D0+	MIPI_CSI2_D0_P	I, MIPI	MIPI CSI2 differential data lane 0 positive.
4	CAM0_CSI_D0-	MIPI_CSI2_D0_N	I, MIPI	MIPI CSI2 differential data lane 0 negative.
5	GND	GND	Power	Ground.
6	CAM0_CSI_D1+	MIPI_CSI2_D1_P	I, MIPI	MIPI CSI2 differential data lane 1 positive.
7	CAM0_CSI_D1-	MIPI_CSI2_D1_N	I, MIPI	MIPI CSI2 differential data lane 1 negative.
8	GND	GND	Power	Ground.
9	CAM0_CSI_D2+	MIPI_CSI2_D2_P	I, MIPI	MIPI CSI2 differential data lane 2 positive.
10	CAM0_CSI_D2-	MIPI_CSI2_D2_N	I, MIPI	MIPI CSI2 differential data lane 2 negatives.
11	CAM0_RST#	SMARC_GPIO_3(GPIO4_1)	I, 1.8V CMOS 10K PU	MIPI Camera Reset signal

Pin No.	Pin Name	Signal Name	Signal Type / Termination	Description
12	CAM0_CSI_D3+	MIPI_CSI2_D3_P	I, MIPI	MIPI CSI2 differential data lane 3 positives.
13	CAM0_CSI_D3-	MIPI_CSI2_D3_N	I, MIPI	MIPI CSI2 differential data lane 3 negative.
14	GND	GND	Power	Ground.
15	CAM0_CSI_CLK+	MIPI_CSI2_CLK_P	I, MIPI	MIPI CSI2 differential Clock positive.
16	CAM0_CSI_CLK-	MIPI_CSI2_CLK_N	I, MIPI	MIPI CS2 differential Clock negative.
17	GND	GND	Power	Ground.
18	CAM0_I2C_CLK	I2C5_SCL(SPDIF_TX)	I, 1.8V OD/ 4.7K PU	I2C Clock for MIPI CSI2 Camera.
19	CAM0_I2C_DAT	I2C5_SDA(SPDIF_TX)	IO, 1.8V OD/ 4.7K PU	I2C Data for MIPI CSI2 Camera.
20	CAM0_ENA#	NC	NA	NC
21	MCLK	CAMERA_CCMCLKO1(ECSPI 2_MISO)	I, 1.8V CMOS	Master Clock.
22	CAM1_ENA#	NC	NA	NC
23	CAM1_I2C_CLK	I2C3_SCL	I, 1.8V OD/ 4.7k PU	I2C Clock for MIPI_CSI1 Camera.
24	CAM1_I2C_DAT	I2C3_SDA	IO, 1.8V OD/ 4.7k PU	I2C Data for MIPI_CSI1 Camera.
25	GND	GND	Power	Ground.
26	CAM1_CSI_CLK+	MIPI_CSI1_CLK_P	I, MIPI	MIPI CSI1 differential Clock positive.
27	CAM1_CSI_CLK-	MIPI_CSI1_CLK_N	I, MIPI	MIPI CSI1 differential Clock negative.
28	GND	GND	Power	Ground.
29	CAM1_CSI_D0+	MIPI_CSI1_D0_P	I, MIPI	MIPI CSI1 differential data lane 0 positive.
30	CAM1_CSI_D0-	MIPI_CSI1_D0_N	I, MIPI	MIPI CSI1 differential data lane 0 negative.
31	CAM1_RST#	SMARC_GPIO_2_GPIO4_0(S AI1_RXFS)	I, 1.8V CMOS 10K PU	MIPI Camera Reset signal
32	CAM1_CSI_D1+	MIPI_CSI1_D1_P	I, MIPI	MIPI CSI1 differential data lane 1 positive.
33	CAM1_CSI_D1-	MIPI_CSI1_D1_N	I, MIPI	MIPI CSI1 differential data lane 1 negative.
34	GND	GND	Power	Ground.
35	CAM0_GPIO	NC	NA	NC
36	CAM1_GPIO	NC	NA	NC

Table 15: MIPI CSI FPC Camera 40 Pin Connector Pinout (Optional)

Pin No.	Pin Name	Signal Name	Signal Type / Termination	Description
1	CAM_PWR	VCC_3V3	Power	3V3 Camera Power
2	CAM_PWR	VCC_3V3	Power	3V3 Camera Power
3	CAM0_CSI_D0+	MIPI_CSI2_D0_P	I, MIPI	MIPI CSI2 differential data lane 0 positive.
4	CAM0_CSI_D0-	MIPI_CSI2_D0_N	I, MIPI	MIPI CSI2 differential data lane 0 negative.
5	GND	GND	Power	Ground.
6	CAM0_CSI_D1+	MIPI_CSI2_D1_P	I, MIPI	MIPI CSI2 differential data lane 1 positive.
7	CAM0_CSI_D1-	MIPI_CSI2_D1_N	I, MIPI	MIPI CSI2 differential data lane 1 negative.
8	GND	GND	Power	Ground.
9	CAM0_CSI_D2+	MIPI_CSI2_D2_P	I, MIPI	MIPI CSI2 differential data lane 2 positive.
10	CAM0_CSI_D2-	MIPI_CSI2_D2_N	I, MIPI	MIPI CSI2 differential data lane 2 negatives.
11	CAM0_RST#	SMARC_GPIO_3(GPIO4_1)	I, 1.8V CMOS 10K PU	MIPI Camera Reset signal
12	CAM0_CSI_D3+	MIPI_CSI2_D3_P	I, MIPI	MIPI CSI2 differential data lane 3 positives.
13	CAM0_CSI_D3-	MIPI_CSI2_D3_N	I, MIPI	MIPI CSI2 differential data lane 3 negative.
14	GND	GND	Power	Ground.
15	CAM0_CSI_CLK+	MIPI_CSI2_CLK_P	I, MIPI	MIPI CSI2 differential Clock positive.
16	CAM0_CSI_CLK-	MIPI_CSI2_CLK_N	I, MIPI	MIPI CS2 differential Clock negative.
17	GND	GND	Power	Ground.
18	CAM0_I2C_CLK	I2C5_SCL(SPDIF_TX)	I, 1.8V OD/ 4.7K PU	I2C Clock for MIPI CSI2 Camera.
19	CAM0_I2C_DAT	I2C5_SDA(SPDIF_TX)	IO, 1.8V OD/ 4.7K PU	I2C Data for MIPI CSI2 Camera.
20	CAM0_ENA#	NC	NA	NC
21	MCLK	CAMERA_CCMCLKO1(ECSPI 2_MISO)	I, 1.8V CMOS	Master Clock.
22	CAM1_ENA#	NC	NA	NC
23	CAM1_I2C_CLK	I2C3_SCL	I, 1.8V OD/ 4.7k PU	I2C Clock for MIPI_CSI1 Camera.
24	CAM1_I2C_DAT	I2C3_SDA	IO, 1.8V OD/ 4.7k PU	I2C Data for MIPI_CSI1 Camera.

Pin No.	Pin Name	Signal Name	Signal Type / Termination	Description
25	GND	GND	Power	Ground.
26	CAM1_CSI_CLK+	MIPI_CSI1_CLK_P	I, MIPI	MIPI CSI1 differential Clock positive.
27	CAM1_CSI_CLK-	MIPI_CSI1_CLK_N	I, MIPI	MIPI CSI1 differential Clock negative.
28	GND	GND	Power	Ground.
29	CAM1_CSI_D0+	MIPI_CSI1_D0_P	I, MIPI	MIPI CSI1 differential data lane 0 positive.
30	CAM1_CSI_D0-	MIPI_CSI1_D0_N	I, MIPI	MIPI CSI1 differential data lane 0 negative.
31	CAM1_RST#	SMARC_GPIO_2_GPIO4_0(SAI1_RXFS)	I, 1.8V CMOS 10K PU	MIPI Camera Reset signal
32	CAM1_CSI_D1+	MIPI_CSI1_D1_P	I, MIPI	MIPI CSI1 differential data lane 1 positive.
33	CAM1_CSI_D1-	MIPI_CSI1_D1_N	I, MIPI	MIPI CSI1 differential data lane 1 negative.
34	GND	GND	Power	Ground.
35	CAM0_GPIO	NC	NA	NC
36	CAM1_GPIO	NC	NA	NC
37	CAM1_CSI_D2+	NA	NA	NC
38	CAM1_CSI_D2-	NA	NA	NC.
39	CAM1_CSI_D3+	NA	NA	NC
40	CAM1_CSI_D3-	NA	NA	NC.

2.7.6 LVDS1 Connector

The i.MX 8M Plus Q/QL/D SMARC Carrier board has LVDS1 Connector (J31) which placed in the bottom as shown in the image below. It supports 40 pin LVDS Display.

Number of Pins :40

Connector Part number : 541044033 from Molex

LVDS Connector (J31)

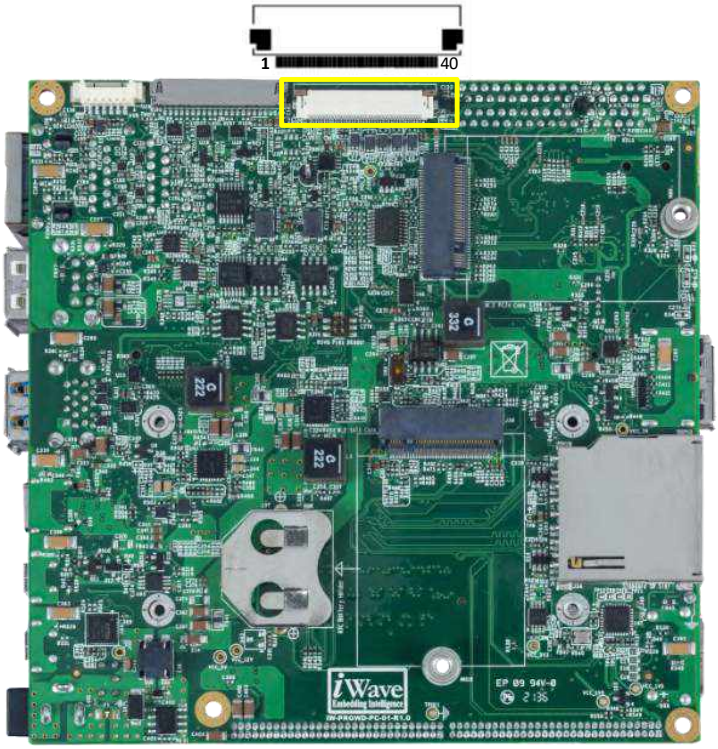


Figure 21: LVDS1 Connector

Table 16: LVDS1 Connector Pinout

Pin No.	Pin Name	Signal Name	Signal Type/ Termination	Description
1	NC1	-	-	NC
2	VDD1	VCC_3V3_TFT1	Power	3.3V Supply Voltage
3	VDD2	VCC_3V3_TFT1	Power	3.3V Supply Voltage
4	NC2	-	-	NC
5	NC3	-	-	NC
6	NC4	-	-	NC
7	NC5	-	-	NC
8	LV0N-	LVDS1_D0_N	I, DIFF	LVDS1 Channel0 negative
9	LV0N+	LVDS1_D0_P	I, DIFF	LVDS1 Channel0 positive
10	GND1	GND	Power	Ground
11	LV1N-	LVDS1_D1_N	I, DIFF	LVDS1 Channel1 negative
12	LV1N+	LVDS1_D1_P	I, DIFF	LVDS1 Channel1 positive
13	GND2	GND	Power	Ground

Pin No.	Pin Name	Signal Name	Signal Type/ Termination	Description
14	LV2N-	LVDS1_D2_N	I, DIFF	LVDS1 Channel2 negative
15	LV2N+	LVDS1_D2_P	I, DIFF	LVDS1 Channel2 positive
16	GND3	GND	Power	Ground
17	LVCLK-	LVDS1_CLK_N	I, DIFF	LVDS1 Channel0 clock negative
18	LVCLK+	LVDS1_CLK_P	I, DIFF	LVDS1 Channel0 clock positive
19	GND4	GND	Power	Ground
20	LV3N-	LVDS1_D3_N	I, DIFF	LVDS1 Channel3 negative
21	LV3N+	LVDS1_D3_P	I, DIFF	LVDS1 Channel3 positive
22	GND5	GND	Power	Ground
23	LED_GND1	GND	Power	Ground
24	LED_GND2	GND	Power	Ground
25	LED_GND3	GND	Power	Ground
26	NC6	-	-	NC
27	LED_PWM	PWM2_OUT(SAI5_RXD0)	O, 3.3V	PWM control signal
28	LED_EN	SMARC_GPIO_12_GPIO3_21(NAND_DQS)	Power	Backlight Enable signal
29	NC7	-	-	NC
30	NC8	-	-	NC
31	LED_VCC1	VCC_12V_LVDS	Power	12V Supply Voltage
32	LED_VCC2	VCC_12V_LVDS	Power	12V Supply Voltage
33	LED_VCC3	VCC_12V_LVDS	Power	12V Supply Voltage
34	NC9	-	-	NC
35	BIST	-	-	NC
36	NC10	-	-	NC
37	NC11	-	-	NC
38	NC12	-	-	NC
39	NC13	-	-	NC
40	NC14	-	-	NC

2.8 Additional Features

2.8.1 RTC Coin Cell Holder

The i.MX 8M Plus Q/QL/D SMARC Carrier board supports Coin Cell Holder to connect "CR 2032" series coin cell. This coin cell voltage is connected to SMARC MXM connector VDD_RTC pin (S147th) for RTC back up voltage when VCC main power is off. This Coin Cell Holder (J37) is physically located on bottom of the board as shown below.

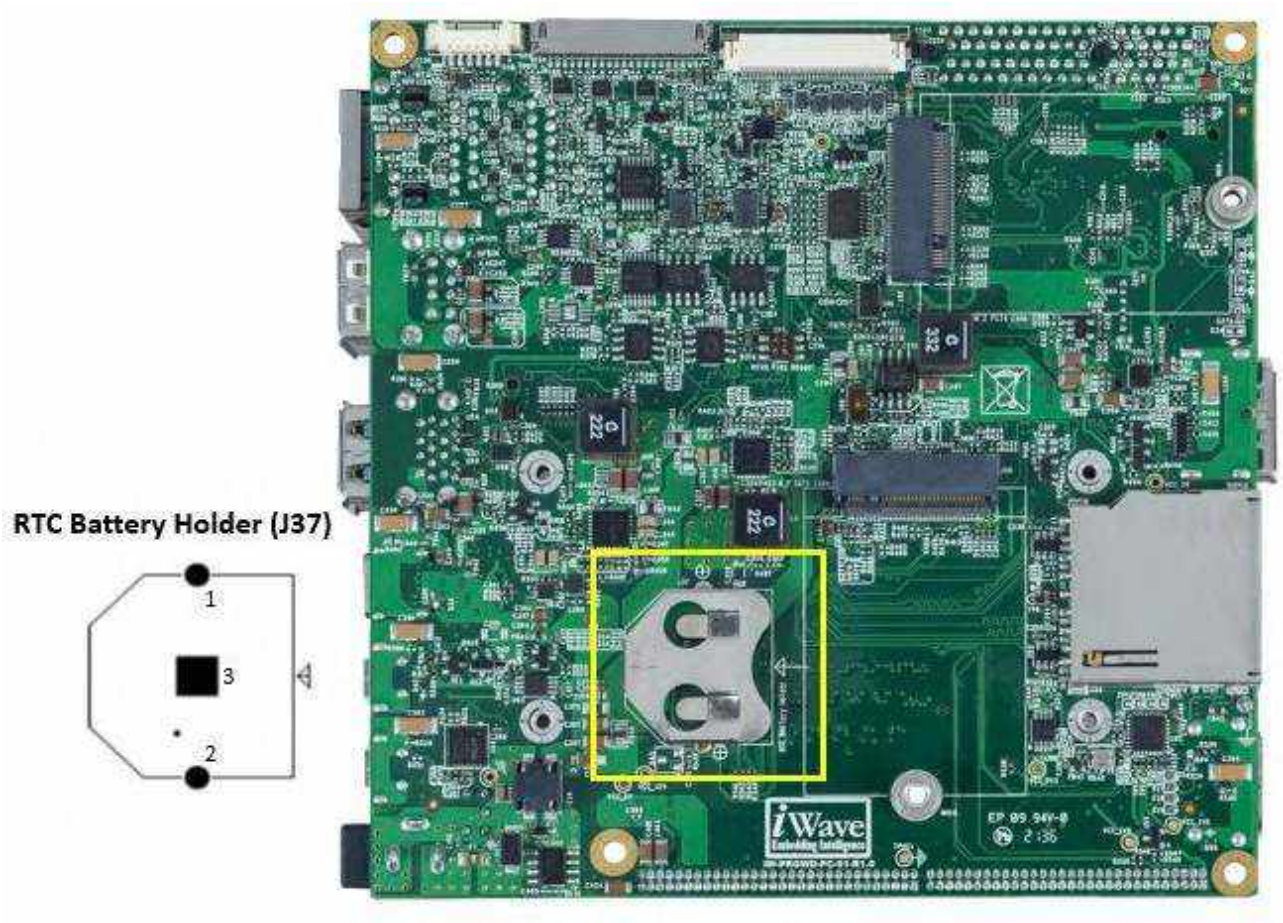


Figure 22: RTC Coin Cell Holder

2.8.2 SPI Flash

The i.MX 8M Plus Q/QL/D SMARC carrier board supports SPI Flash through i.MX 8M Plus SoC's eCSPI1 interface which is connected from SPI0 port of SMARC MXM connector. This SPI interface signals from SMARC MXM connector is connected to SPI Flash "IS25WP016D-JNLE" and operating at 1.8V Level.

2.8.3 QSPI Flash

The i.MX 8M Plus Q/QL/D SMARC carrier board by default supports 2ndSPI Flash(U50) through i.MX8 CPU's SPI2 interface and optionally same IC Can support as QSPI. This SPI interface signals from SMARC MXM connector are connected to SPI Flash "IS25WP016D-JNLE" and operating at 1.8V Level.

2.8.4 Capacitive Touch Connector

The i.MX 8M Plus Q/QL/D SMARC carrier board supports a 10pin capacitive touch connector (J2) which is placed at top side of the board. This connector can be used as general-purpose touch connector using I2C interface.

Figure 23: Capacitive Touch Connector

Table 17: Capacitive Touch Connector

Pin No	Pin Name	Signal Name	Signal Type / Termination	Description
1	VSS1	GND	Ground	GND
2	VDD	VCC_3V3_TFT0	Power	Supply Voltage 3.3V
3	SCL	I2C2_SCL	I, 3.3V CMOS	General purpose I2C Clock
4	NC1	NC	NA	NC
5	SDA	I2C2_SDA	IO, 3.3V CMOS	General purpose I2C data
6	NC	NC2	NA	NC
7	RST#	RST#	O, 3.3V CMOS	Hardware Reset

Pin No	Pin Name	Signal Name	Signal Type /Termination	Description
8	WAKE#	CAP_WAKE#	O, 3.3V CMOS,10K PU	Wake signal
9	INT#	TSC	O, 3.3V CMOS	GPIO_9_TP_INT2 optionally connected
10	VSS1	GND	Ground	Ground

2.8.5 USB2.0 Header

The i.MX 8M Plus Q/QL/D SMARC Carrier board supports a 6-pin USB Header (J29) which is placed at bottom side of the board. This connector can be used as general-purpose touch connector using USB interface.

Number of Pins 6

Connector Part number : 532610671 from Molex

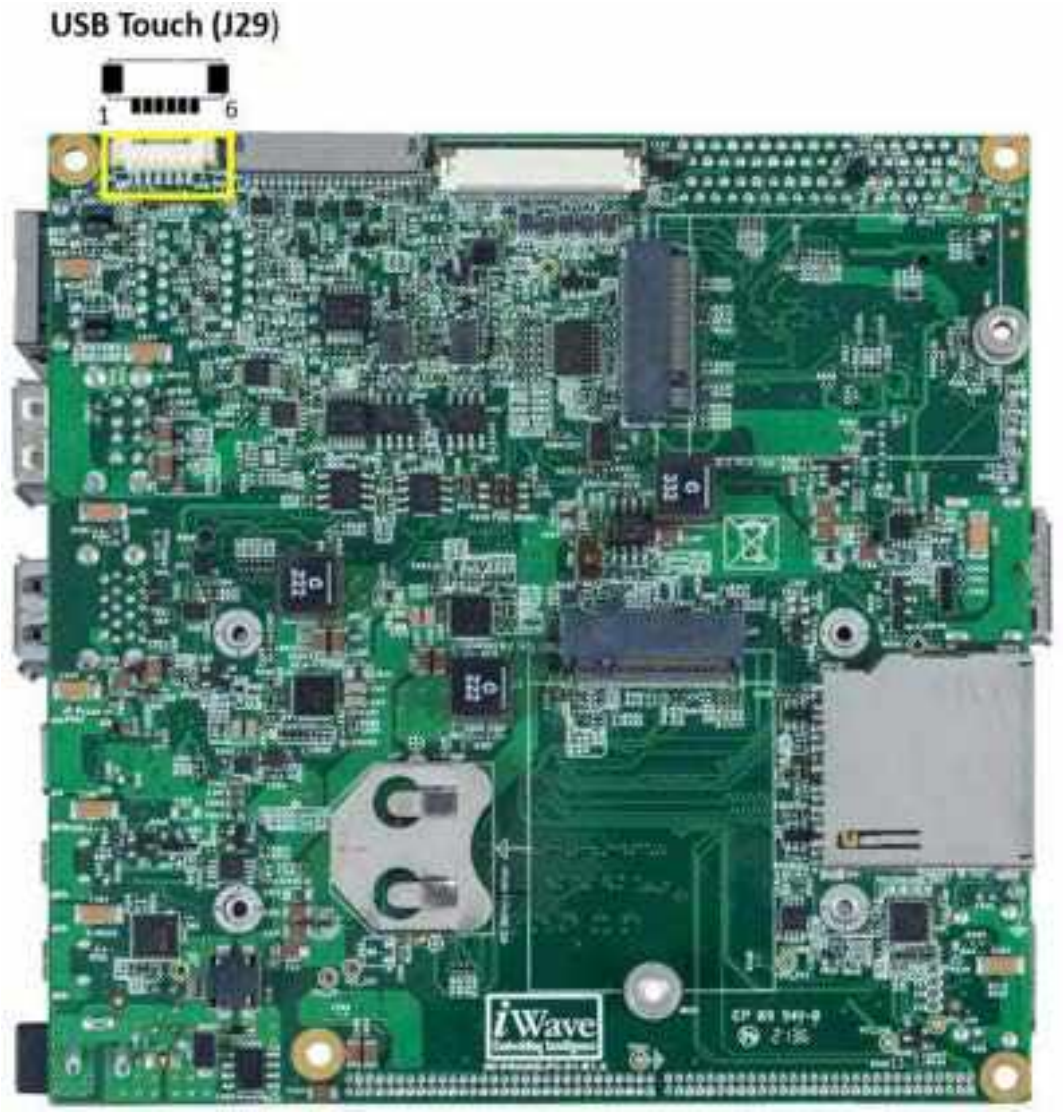


Figure 24: USB2.0 Header

Table 18: USB2.0 Header

Pin No	Signal Name	Signal Type / Termination	Description
1	VBUS_HOST_TP	Power	Supply Voltage 5V
2	USB_HUBOUT3_DM	Power	USB Data Negative
3	USB_HUBOUT3_DP	I, 3.3V CMOS	USB Data Positive
4	NC1	NA	NC
5	GND	Power	Ground
6	NC2	NA	NC

2.8.6 Display Backlight Power Header

The i.MX 8M Plus Q/QL/D SMARC Carrier board supports a 6-pin Backlight Power Header (J11) which is placed at bottom side ofthe board. This connector can be used for Display backlight power.

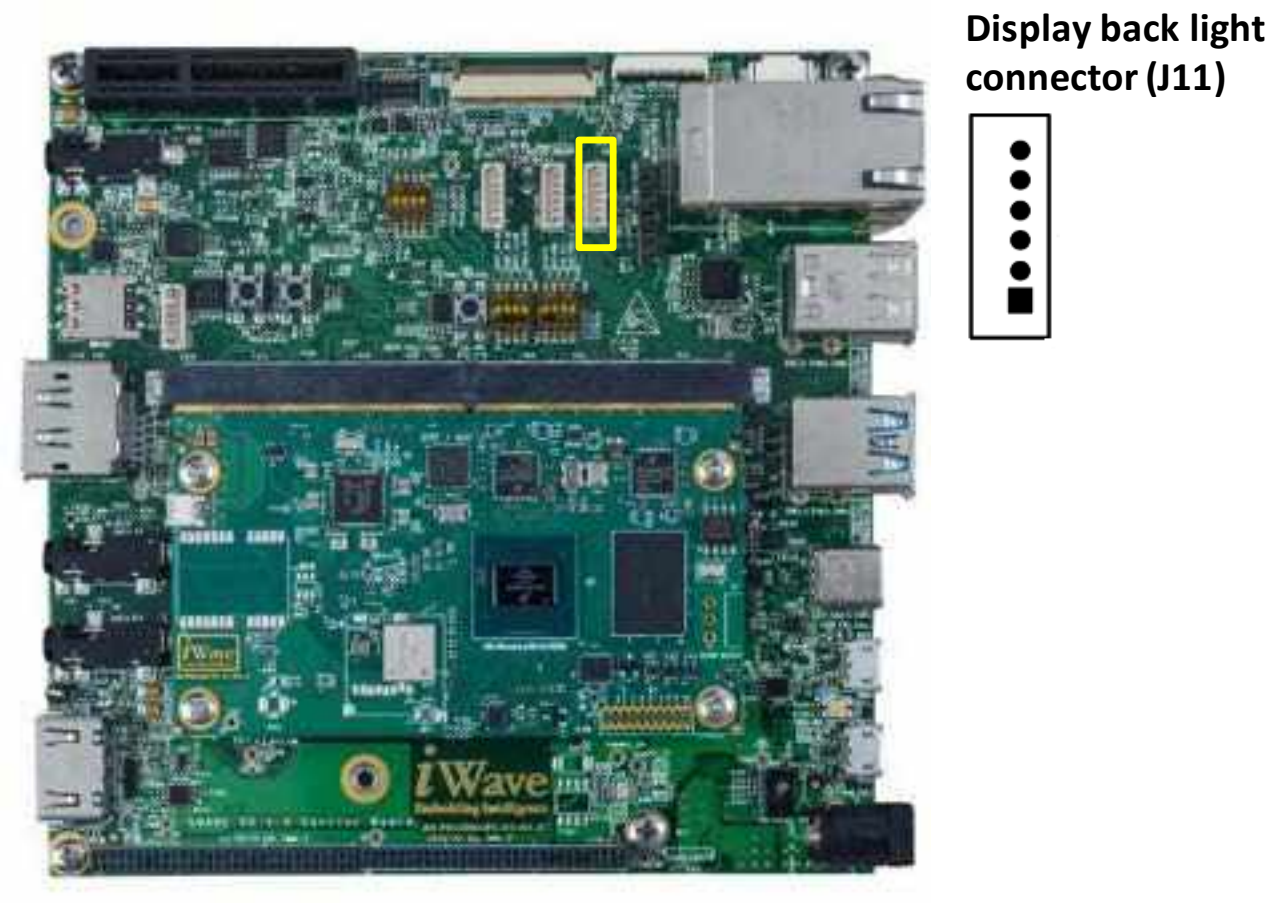


Figure 25: Display Backlight Power Header

Table 19: Display Backlight Power Header

Pin No	Pin Name	Signal Name	Signal Type /Termination
1	VCC_12V	VCC_12V_LVDS0	12V supply
2	GND	GND	Ground
3	EN	BKLT_EN0	Backlight enable

Pin No	Pin Name	Signal Name	Signal Type /Termination
4	PWM	BKLT_PWM0	PWM signal
5	LED_K	NC	NC
6	LED_A	NC	NC

2.9 On Board Settings

The i.MX 8M Plus Q/QL/D SMARC Carrier board has seven Switches on Top side of carrier card to support generic SMARC features. All the seven switches location is highlight in below image and the switch description is given in the following table.

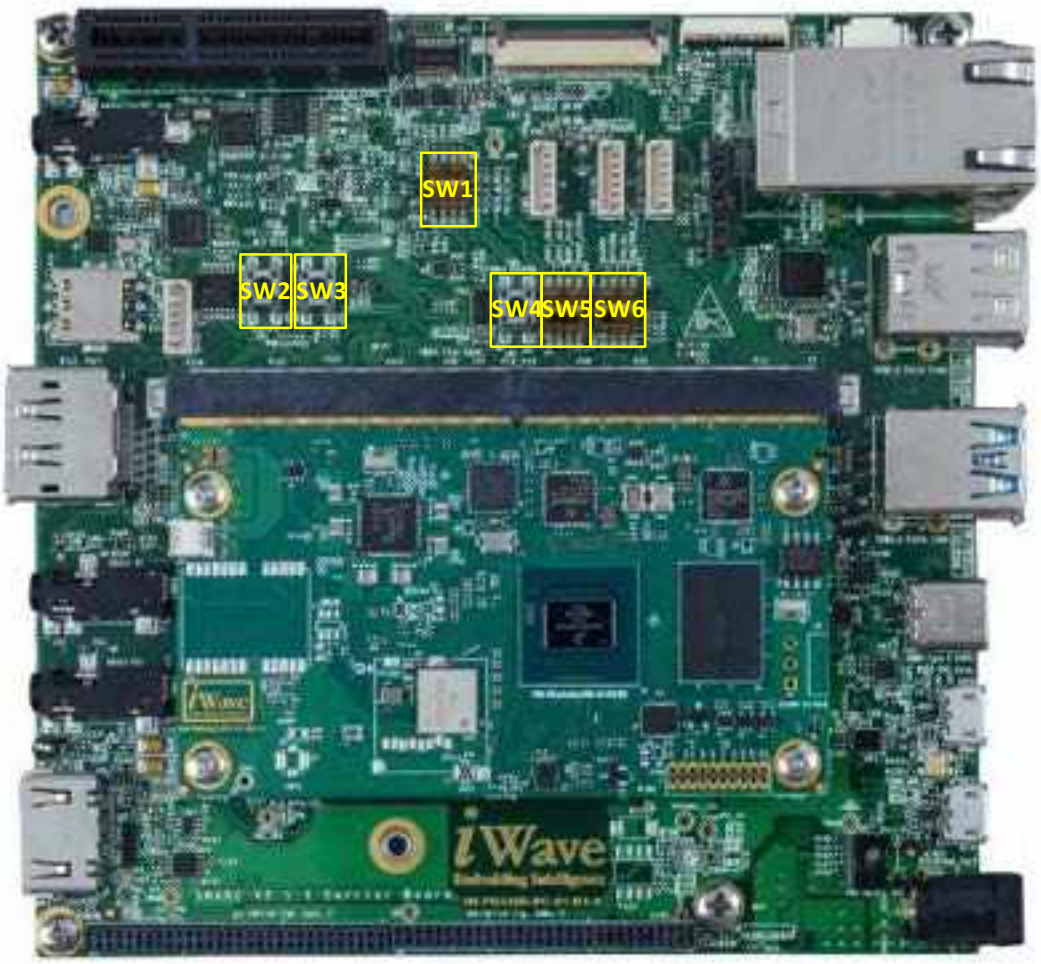


Figure 26: SMARC On Board Switches

Table 20: Board Configuration Switch

<table>
<tr><th>SW Identifier/ (SW Type)</th><th>No. of Bits</th><th>Bit Name</th><th colspan="2">Description</th><th>Remark</th></tr>
<tr><th></th><th></th><th></th><th>ON/Push</th><th>OFF/Release</th><th></th></tr>
<tr><td rowspan="2">SW1 (DIP SW)</td><td>1</td><td>PCIe_A_SEL1</td><td colspan="2" rowspan="2"><u>PCIe Channel 0 Connection:</u>
<table>
<tr><th>State [SEL2,SEL1]</th><th>Select</th><th>Reference image</th></tr>
<tr><td>00</td><td>Hi-Z</td><td> </td></tr>
<tr><td>01</td><td>M.2 Lane0</td><td> </td></tr>
</table></td><td rowspan="2">1-Switch OFF (Pulled High)
0 -Switch ON (GND)

Note: At a time, do not set Both the PCIe Channel A & B neither</td></tr>
<tr><td>2</td><td>PCIe_A_SEL2</td></tr>
</table>

SW Identifier/ (SW Type)	No. of Bits	Bit Name	Description		Remark
			ON/Push	OFF/Release	
			10 M.2 Lane1		*to PCIe x4 nor to M.2 connector.*
			11 PCIe x4(Lane0)		
	3	PCIe_B_SEL1	NC		
	4	PCIe_B_SEL2	NC		
SW2 (Push button)	**1**	POWER_BTN#	SOM Power ON - One Press and release SOM Power OFF - Long Press (above 5sec)		SOM Power ON/OFF Switch
SW3 (Push button)	**1**	RESET_IN#	SOM Reset – While Pressing SOM Out of reset – When release		SOM Reset Switch
SW4 (Push button)	**1**	FORCE_RECOV#	-	-	*Note: Same signal is also connected to SW5 4th bit*
SW5 (DIP SW)	**1**	BOOT_SEL0#	**BOOT_SEL[2:0]#** 100- Boot from Carrier SPI (Optional) 001- Boot from SOM eMMC (Default) 011- Boot from SOM microSD (Optional) 110- Boot from Carrier Board SD		**0**-Switch OFF (Floating) **1** -Switch ON (GND)
	2	BOOT_SEL1#			
	3	BOOT_SEL2#			
	4	FORCE_RECOV#	CPU USB Serial Mode (For programming the SOM boot media)	CPU Normal Boot Mode	*Note: Same signal is also connected to SW4*
SW6 (DIP SW)	**1**	LID#/SLEEP#*	-	-	Not Supported
	2	BATLOW#/CHARGING#*	-	-	Not Supported
	3	TEST#/CHARGER_PRSNT#/SIM_SEL	-	-	By default, SIM Select function is supported
	4	USB_TYPE_C_SW	USB3 port is connected to USB Type A (J17, Top) connector.	USB3 port is connected to USB Type C (J20) connector.	
SW7 (Toggle SW)	**1**	Carrier Power ON/ OFF Switch	Carrier Board Power is ON	Carrier board Power is OFF	Carrier Board Main 12V Power On/Off Switch.

2.10 Carrier Expansion Connectors

The i.MX 8M Plus Q/QL/D SMARC Carrier board have two 80pin Expansion Connectors for expansion purpose. All pins of the First Expansion Connector (J27) are NC. Some signals from the SMARC Edge that cannot be validated directly are connected to the Second Expansion Connector (J28) along with Power. An add-on Module can be designed for utilizing these features. Expansion connectors are physically located at the top of board as shown below.

Connectors Part number : 20021311-00060T4LF from Amphenol ICC (FCI)

Mating Connector : 20021111-00060T4LF from Amphenol ICC (FCI)

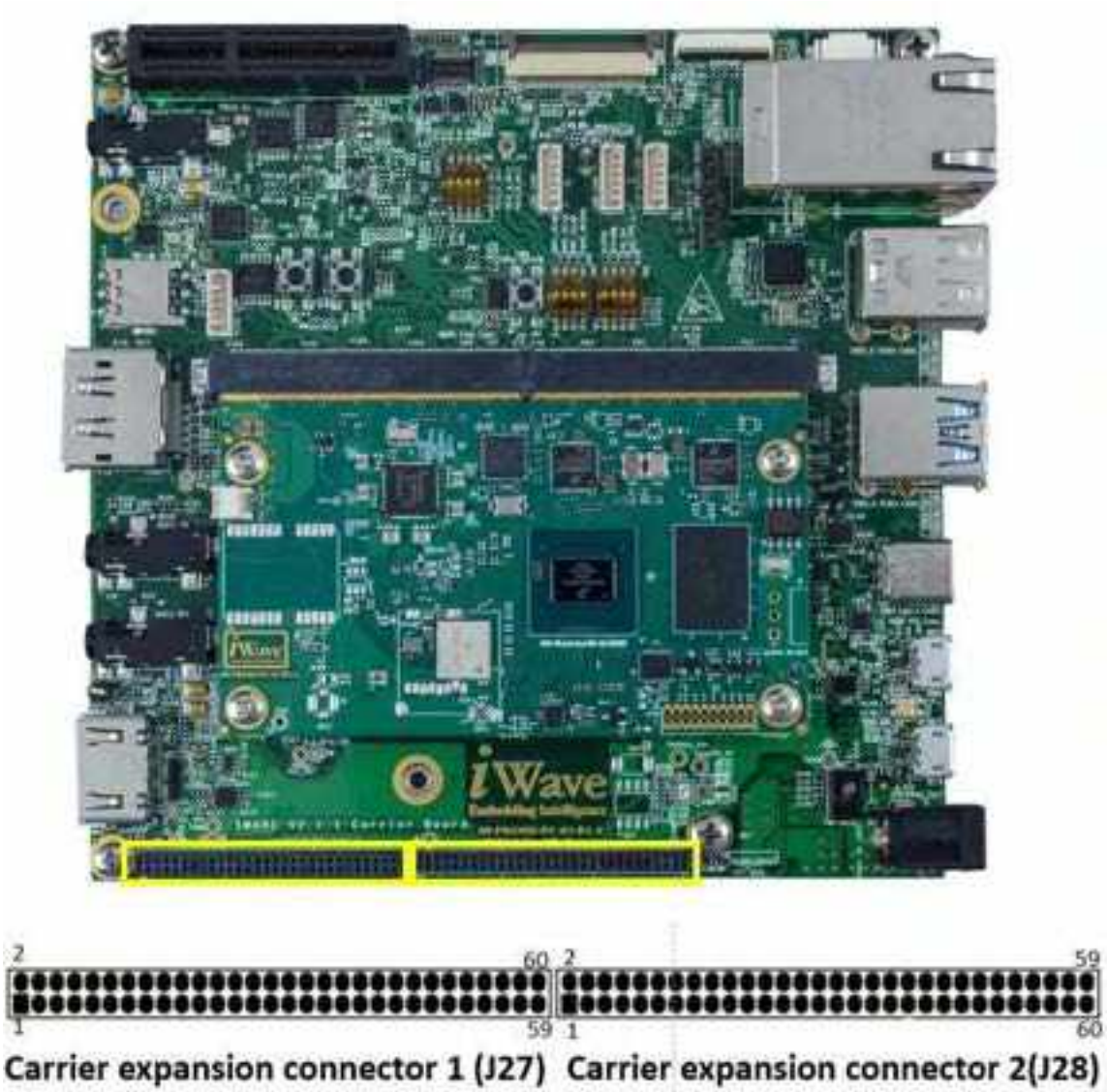


Figure 27: SMARC Expansion Connector

Table 21: Expansion Connector1 Pinout

Pin No	Signal Name	Signal Type / Termination	Description
1	VCC_3V3	Power	Supply Voltage 3.3V
2	VCC_1V8	Power	Supply Voltage 1.8V
3	VCC_5V	Power	Supply Voltage 5V
4	UART3_TXD	O, 1.8V CMOS	*Note: This pin is connected from SMARC Edge connector P134 pin.*
5	GND	Power	Ground.
6	UART3_RXD	I,1.8V CMOS	*Note: This pin is connected from SMARC Edge connector P135 pin*
7	WDT_TIME_OUT#	I, 1.8V CMOS	Watchdog Time Out Interrupt. *Note: This pin is connected from SMARC Edge connector S145 pin*
8	GND	Power	Ground.
9	NC	NC	NC
10	NC	NC	NC
11	NC	NC	NC
12	NC	NC	NC
13	NC	NC	NC
14	NC	NC	NC
15	NC	NC	NC
16	NC	NC	NC
17	NC	NC	NC
18	NC	NC	NC
19	NC	NC	NC
20	NC	NC	NC
21	NC	NC	NC
22	NC	NC	NC
23	NC	NC	NC
24	NC	NC	NC
25	NC	NC	NC
26	NC	NC	NC
27	NC	NC	NC
28	NC	NC	NC
29	NC	NC	NC
30	NC	NC	NC
31	NC	NC	NC
32	NC	NC	NC
33	NC	NC	NC
34	NC	NC	NC
35	NC	NC	NC

Pin No	Signal Name	Signal Type / Termination	Description
36	NC	NC	NC
37	NC	NC	NC
38	NC	NC	NC
39	NC	NC	NC
40	NC	NC	NC
41	NC	NC	NC
42	NC	NC	NC
43	NC	NC	NC
44	NC	NC	NC
45	NC	NC	NC
46	NC	NC	NC
47	NC	NC	NC
48	NC	NC	NC
49	NC	NC	NC
50	NC	NC	NC
51	NC	NC	NC
52	NC	NC	NC
53	NC	NC	NC
54	NC	NC	NC
55	NC	NC	NC
56	NC	NC	NC
56	NC	NC	NC
58	NC	NC	NC
59	NC	NC	NC
60	NC	NC	NC

Table 22: Expansion Connector2 Pinout

Pin No	Signal Name	Signal Type / Termination	Description
1	NC	NC	NC
2	NC	NC	NC
3	NC	NC	NC
4	NC	NC	NC
5	NC	NC	NC
6	NC	NC	NC
7	NC	NC	NC
8	NC	NC	NC
9	NC	NC	NC
10	NC	NC	NC
11	NC	NC	NC
12	NC	NC	NC

Pin No	Signal Name	Signal Type / Termination	Description
13	NC	NC	NC
14	NC	NC	NC
15	NC	NC	NC
16	NC	NC	NC
17	NC	NC	NC
18	NC	NC	NC
19	NC	NC	NC
20	NC	NC	NC
21	NC	NC	NC
22	NC	NC	NC
23	NC	NC	NC
24	NC	NC	NC
25	NC	NC	NC
26	NC	NC	NC
27	I2C2_SCL	I, 1.8V CMOS	I2C2 Clock.
28	NC	NC	NC
29	I2C2_SDA	IO, 1.8V CMOS	I2C2 Data.
30	NC	NC	NC
31	NC	NC	NC
32	NC	NC	NC
33	GND	Power	Ground.
34	NC	NC	NC
35	GND	Power	Ground.
36	NC	NC	NC
37	NC	NC	NC
38	NC	NC	NC
39	NC	NC	NC
40	NC	NC	NC
41	NC	NC	NC
42	NC	NC	NC
43	NC	NC	NC
44	NC	NC	NC
45	NC	NC	NC
46	NC	NC	NC
47	NC	NC	NC
48	NC	NC	NC
49	I2C1_SCL	I, 1.8V CMOS	NC. *Note: This is optional feature in SOM.*
50	GBE0_SDP	O, 3.3V CMOS	NC
51	I2C1_SDA	IO, 1.8V CMOS	NC. *Note: This is optional feature in SOM.*

Pin No	Signal Name	Signal Type / Termination	Description
52	GBE1_PPS_SDP	NA	NA
53	ESPI_RESET#	O, 1.8V CMOS	QSPIB RESET.
54	RESET_IN#	O, 1.8V CMOS	Hard RESET Input to SOM from Reset Push Button Switch (SW3).
55	ESPI_ALERT0#	NA	NA
56	VCC_3V3	Power	Supply Voltage 3.3V
57	ESPI_ALERT1#	NA	NA
58	VCC_1V8	Power	Supply Voltage 1.8V
59	VCC_5V	Power	Supply Voltage 5V
60	GND	Power	Ground.

3. TECHNICAL SPECIFICATION

This section provides detailed information about the i.MX 8M Plus Q/QL/D SMARC Development Platform technical specification with Electrical, Environmental and Mechanical characteristics.

3.1 Power Input Requirement

The i.MX 8M Plus Q/QL/D SMARC Carrier Board is designed to work with a +12V external power and uses on board voltage regulators for internal power management. 12V power input from an external power supply is connected to the SMARC Carrier Board through Power Jack (J26). This 2.5mm x 6.5mm barrel connector Jack should fit standard DC Plugs with an inner dimension of 2.5mm and an outer dimension of 5.5mm. This connector is physically placed at the top of the board as shown below.

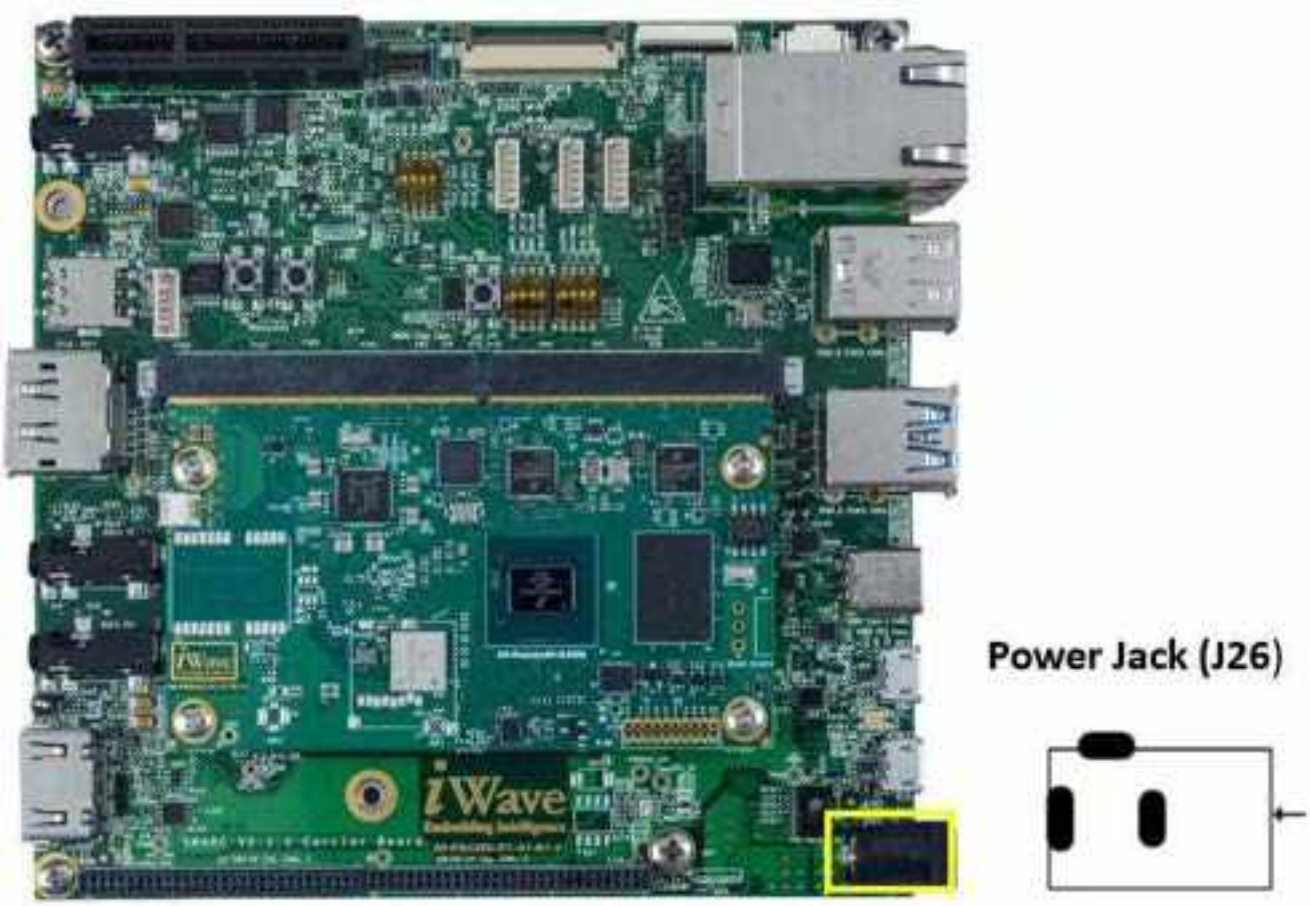


Figure 28: Power Jack

The below table provides the Power Input Requirement of i.MX 8M Plus Q/QL/D SMARC Carrier Board.

Table 23: Power Input Requirement

Sl. No.	Power Rail	Min (V)	Typical (V)	Max(V)	Max Input Ripple
1	VCC_12V[1]	11.75V	12V	12.25V	±50mV
2	VRTC_3V0[2]	2.8V	3V	3.3V	±20mV

[1] SMARC Carrier Board is designed to work with 12V, 2A input power from external Power adapter.

[2] This voltage is from Coin cell holder and used as backup power source to RTC circuit of i.MX 8M Plus Q/QL/D SMARC SOM when SOM VCC is off. This is an optional power and required only if RTC functionality is used.

3.2 Power Output Specification

The i.MX 8M Plus Q/QL/D SMARC Carrier Board has dedicated power regulator to provide +5V power to SMARC SOM for VIN power supply. Also +3V RTC power from coin cell holder is provided to SMARC SOM for Real time clock support.

The i.MX 8M Plus Q/QL/D SMARC carrier board also shares different on-board power to Audio & Video connector and Carrier Expansion connector2 for its Add-On Module power.

Table 24: Power Output Specification

Sl. No.	Power Rail	Min (V)	Typical (V)	Max(V)	Max Output Current (mA)
Power to SMARC SOM (through SMARC MXM connector)					
1	VIN_5V	4.85V	5V	5.15V	5000mA
2	VRTC_3V0	2.8V	3V	3.3V	-
Power to Add-On Module (through Expansion Connector1)					
1	VCC_5V	4.85V	5V	5.15V	1000mA
2	VCC_3V3	3.15	3.3	3.45	1000mA
3	VCC_1V8	1.7	1.8	1.9	1000mA
Power to Add-On Module (through Expansion Connector2)					
1	VCC_5V	4.85V	5V	5.15V	1000mA
2	VCC_3V3	3.15	3.3	3.45	1000mA
3	VCC_1V8	1.7	1.8	1.9	1000mA

3.3 Environmental Characteristics

3.3.1 Environmental Specification

The below table provides the Environment specification of i.MX 8M Plus Q/QL/D SMARC Development Platform.

Table 25: Environmental Specification

Parameters	Min	Max
Operating temperature range[1]	0°C	60°C

[1] *iWave guarantees the component selection for the given operating temperature.*

3.3.2 RoHS Compliance

iWave's i.MX 8M Plus Q/QL/D SMARC Development Platform is designed by using RoHS3 compliant components and manufactured on lead free production process.

3.3.3 Electrostatic Discharge

iWave's i.MX 8M Plus Q/QL/D SMARC Development Platform is sensitive to electro static discharge and so high voltages caused by static electricity could damage some of the devices on board. It is packed with necessary protection while shipping. Do not open or use the SOM and Development Platform except at an electrostatic free workstation.

3.4 Mechanical Characteristics

3.4.1 i.MX 8M Plus Q/QL/D SMARC Carrier Board Mechanical Dimensions

The i.MX 8M Plus Q/QL/D SMARC Development Platform PCB size is 120 mm x 120 mm x 1.6mm. SMARC Carrier card mechanical dimension is shown below. (All dimensions are shown in mm)

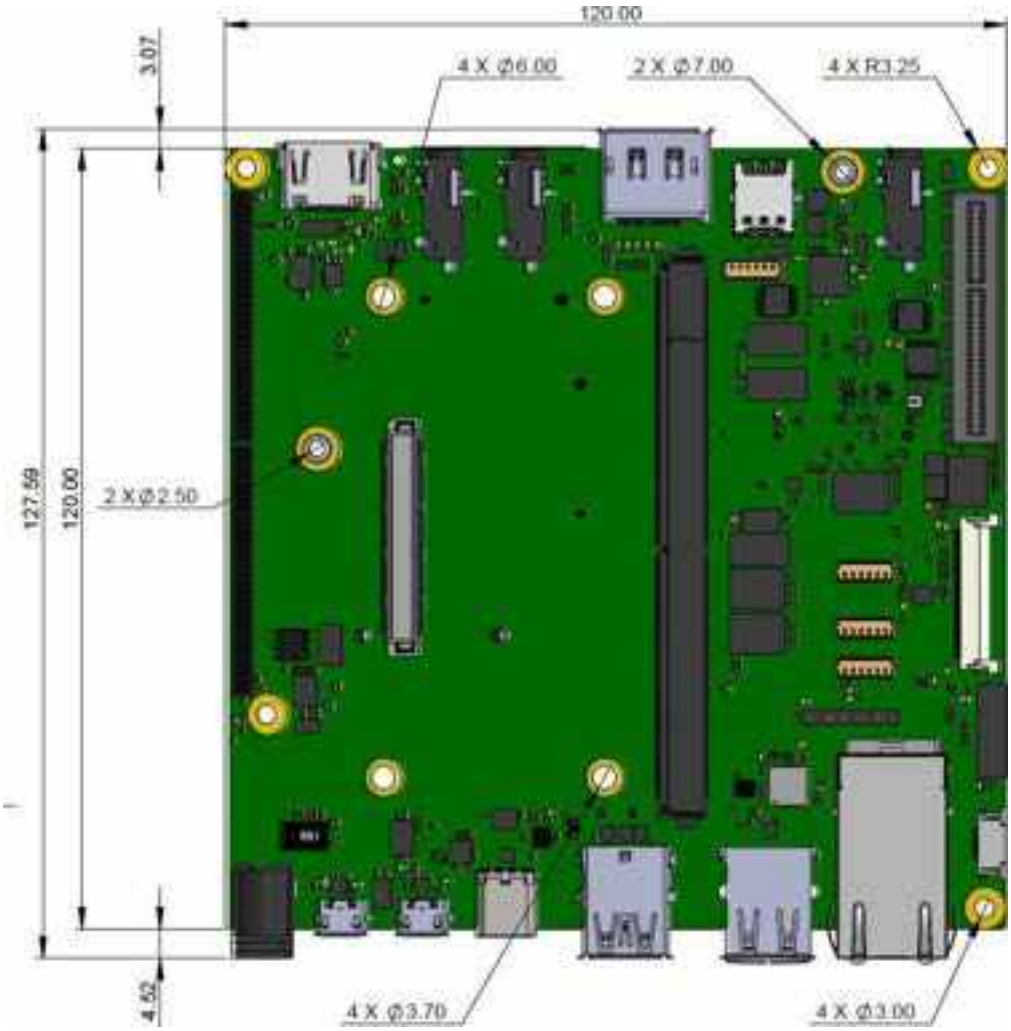


Figure 29: Mechanical dimension of i.MX 8M Plus Q/QL/D SMARC Carrier Board- Top View

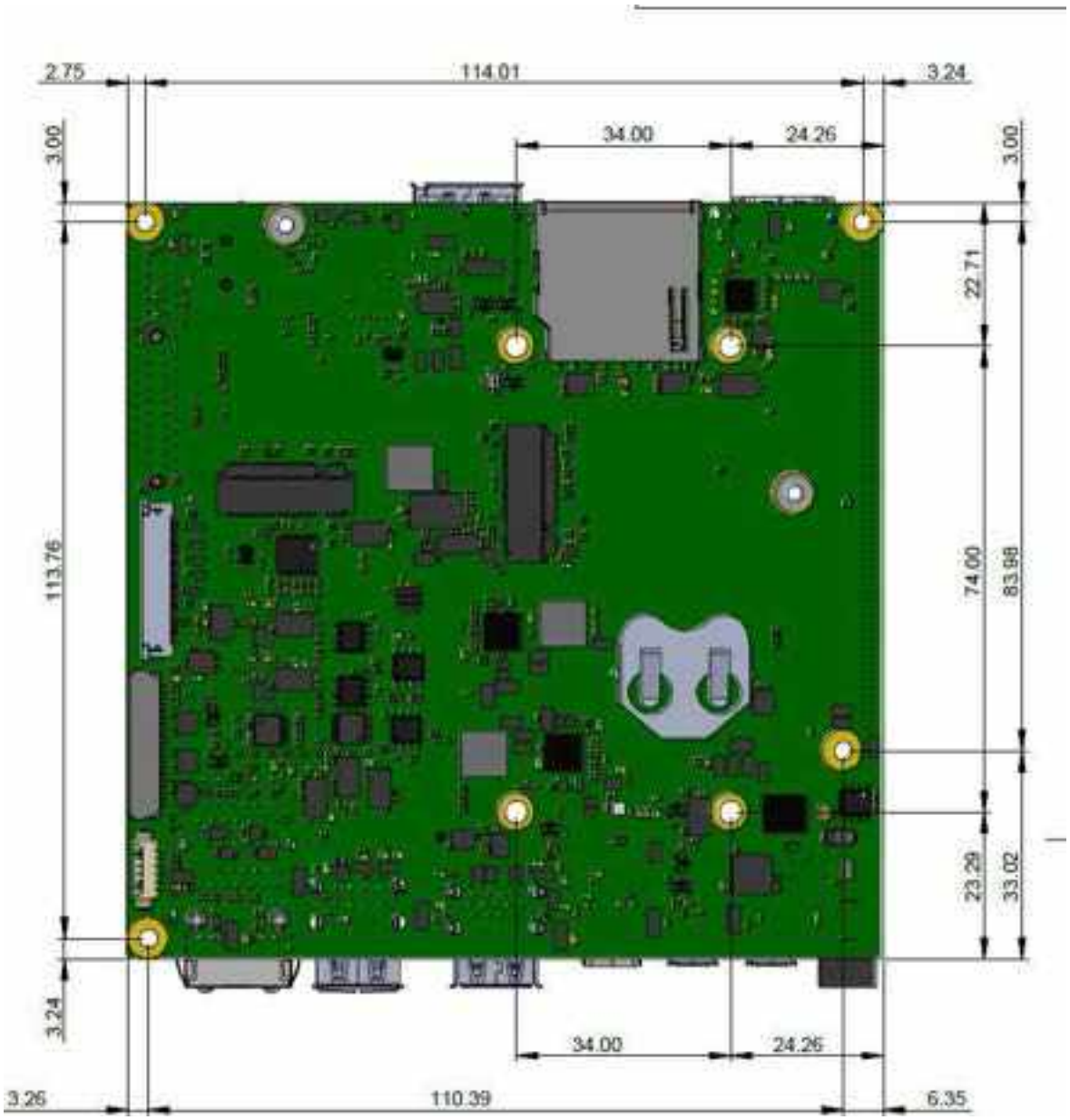


Figure 30: Mechanical dimension of i.MX 8M Plus Q/QL/D SMARC Carrier Board- Bottom View

The i.MX 8M Plus Q/QL/D SMARC Development Platform PCB thickness is 1.6mm±0.16mm, top side maximum height component is connector dual Ethernet Jack J8 (28.58mm) followed by USB3.0 Stack slot J17(15.6mm) and bottom side maximum height component is inductor (7.3mm). Please refer the below figure which gives height details of the i.MX 8M Plus Q/QL/D SMARC Development kit.

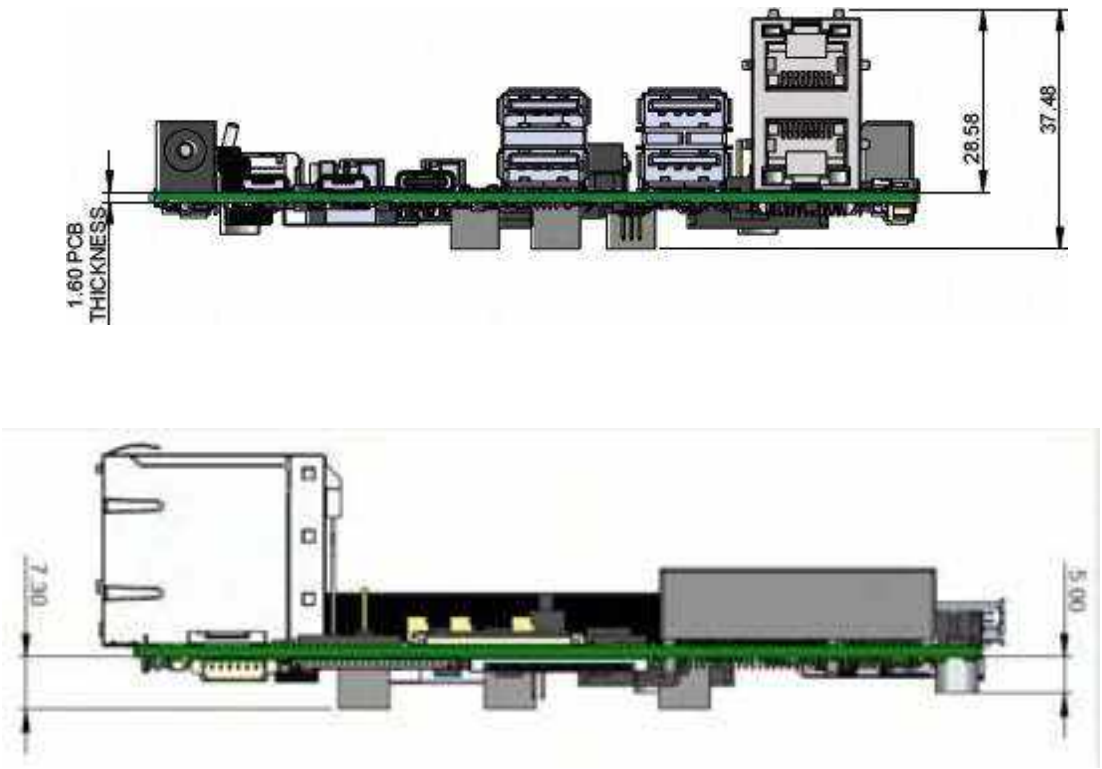


Figure 31: Mechanical dimension of i.MX 8M Plus Q/QL/D SMARC Carrier Board- Side View

3.4.2 Guidelines to insert the SMARC SOM into Carrier Board

- Make sure that power is not provided to the carrier board.
- Insert the SMARC module in to the MXM connector at an angle of 30° as shown in below image.
- Check the Notch position of SMARC module is proper while inserting.
- Once the SMARC module is inserted to the MXM connector properly, press the board vertically down as shown below, such that the board is fixed firmly into the expansion connectors and fix the board by screwing.

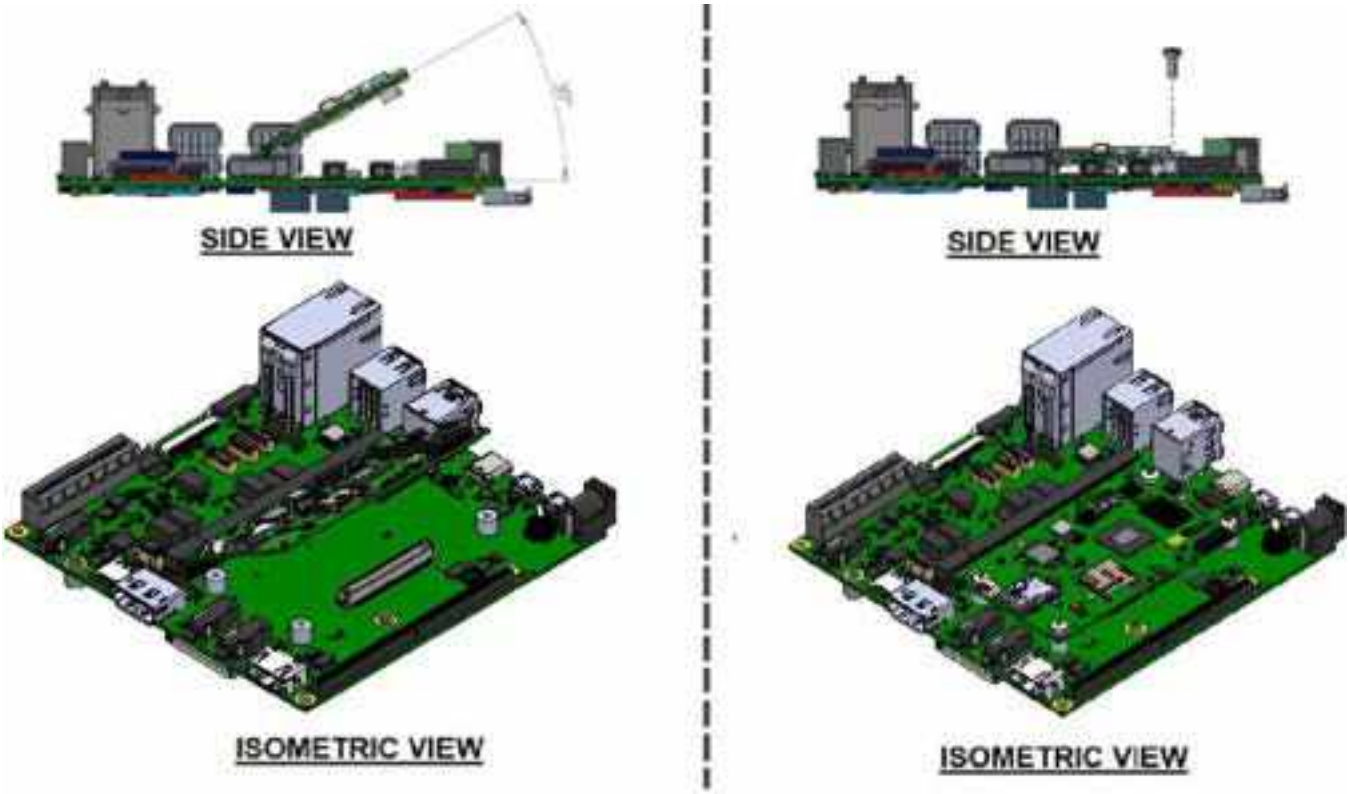


Figure 32: SOM Insertion Guideline

4. ORDERING INFORMATION

The below table provides the standard orderable part numbers for different i.MX 8M Plus Q/QL/D SMARC Development Platform which includes i.MX 8M Plus Q/QL/D SMARC SOM and SMARC carrier board.

Table 26: Orderable Product Part Numbers

Product Part Number	Description	Temperature
iW-G40D-SCPQ-4L002G-E016G-LCD	i.MX 8M Plus Quad CPU, 2GB RAM, 16GB eMMC, Wi-Fi & BT - SMARC development kit -Linux	Commercial
iW-G40D-SCPQ-4L002G-E016G-ACD	i.MX 8M Plus Quad CPU, 2GB RAM, 16GB eMMC, Wi-Fi & BT - SMARC development kit -Android	Commercial
iW-G40D-SCPQ-4L004G-E016G-LCD	i.MX8M Plus Quad CPU, 4GB RAM, 16GB eMMC, Wi-Fi & BT - SMARC development kit-Linux	Commercial
iW-G40D-SCPQ-4L004G-E016G-ACD	i.MX8M Plus Quad CPU, 4GB RAM, 16GB eMMC, Wi-Fi & BT - SMARC development kit-Android	Commercial

Note: For Development platform identification purpose, Product part number is pasted as Label with Barcode readable format.