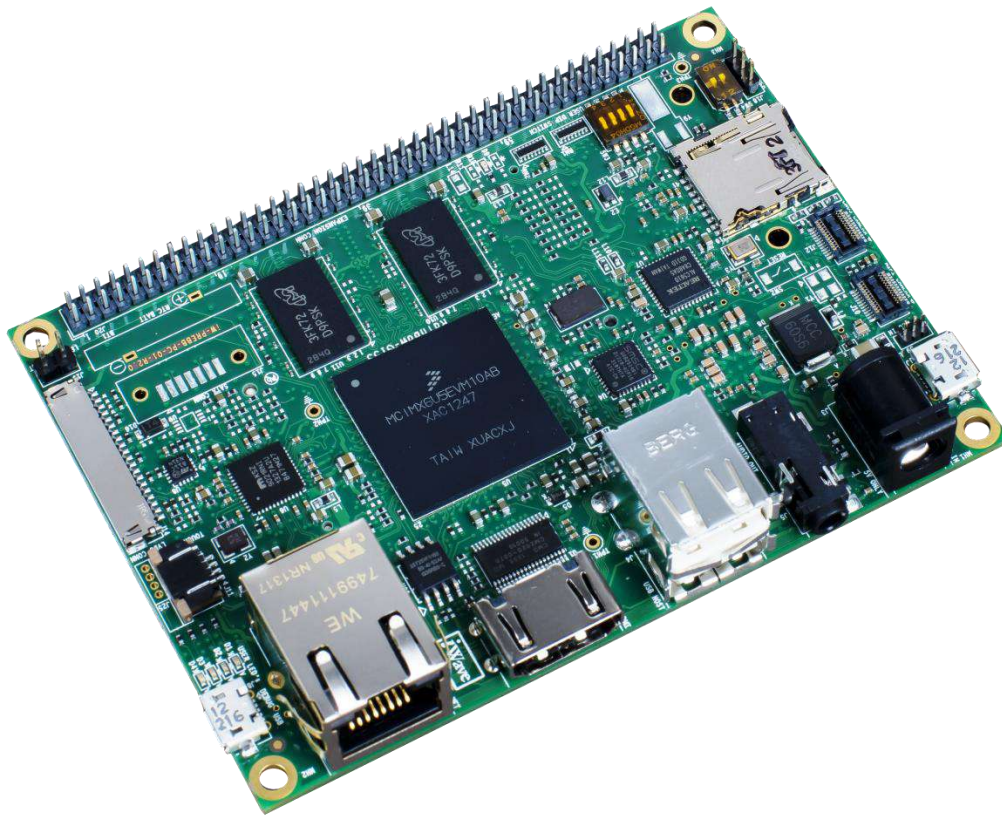


iW-RainboW-G15S

i.MX6 Pico ITX – Single Board Computer Hardware User Guide



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1. INTRODUCTION

1.1 Purpose

This document is the Hardware User Guide for the i.MX6 Pico-ITX SBC which is based on the Freescale's i.MX6 Applications Processor. This board is fully supported by iWave Systems Technologies Pvt. Ltd. This Guide provides detailed information on the overall design and usage of the i.MX6 Pico-ITX SBC from a Hardware Systems perspective.

1.2 Pico ITX Overview

The Pico ITX is a PC mother board form factor. Pico ITX concept is an off-the-shelf, Single-Board-Computer that integrates all the core features of a common PC. Pico ITX modules have a standardized form factor of 100mm x 72mm which is half the area of Nano ITX, and provides the functional requirements for an embedded application.

1.3 List of Acronyms

The following acronyms are used throughout this document.

Table 1: Acronyms & Abbreviations

Acronyms	Abbreviations
AC'97	Audio Codec '97
ARM	Advanced RISC Machine
BOM	Bill Of Materials
C	Celsius/Centigrade
CAN	Controller Area Network
eCSPI	Enhanced Configurable Serial Peripheral Interface
GB	Giga Byte
GBE	Gigabit Ethernet
GPIO	General Purpose Input Output
HDMI	High-Definition Multimedia Interface
I2C	Inter-Integrated Circuit
IC	Integrated Circuit
I/O	Input/output
JTAG	Joint Test Action Group
KB	Kilo Byte
LCD	Liquid Crystal Display
LDO	Low Drop-Out
LED	Light Emitting Diode

LVDS	Low-Voltage Differential Signalling
MB	Mega Byte
Mbps	Megabits per sec
MHz	Mega Hertz
MIPI	Mobile Industry Processor Interface
MMC	Multi Media Card
mm	milli-meter
ms	milli second
OTG	On The Go
PCB	Printed Circuit Board
PCI	Peripheral Controller Interconnect
RJ45	Registered Jack 45
RMII	Reduced Media Independent Interface
ROHS	Restriction of Hazardous Substances
RTC	Real Time Clock
SD	Secure Digital
SPI	Serial Peripheral Interface
UART	Universal Asynchronous Receiver/Transmitters
USB	Universal Serial Bus

1.4 References

- i.MX6 Applications Processors Products Datasheet
- i.MX6 Applications Processor Reference Manual
- iW-RainboW-G15S Quick Start Guide R3.0

1.5 Important Note

In this document, wherever i.MX6 CPU signal name is mentioned, it is followed as per below format.

- If CPU pin functionality name and CPU pad name is same, Signal name is mentioned as
“CPU_Pad_Name”

Example: SD3_DATA2

In this signal, functionality which we are using and CPU Pad name is **SD3_DATA2**.

- If CPU pin functionality name and pad name is different, Signal name is mentioned as
“Functionality_name (CPU_Pad_name)”

Example: UART3_RTS (SD3_RST)

In this signal, **UART3_RTS** is the functionality which we are using and **SD3_RST** is the CPU Pad name.

- If CPU pin functionality is GPIO, Signal name is mentioned as
“GPIONumber_FunctionalityDescription (CPU_Pad_name)”

Example: GPIO7_0_SD1_CD(SD3_DAT5)

In this signal, **GPIO7_0** is the GPIO number, **SD1_CD** (SD1 card detect) is the functionality which we are using and **SD3_DAT5** is the CPU pad name.

Note: The above naming is not applicable for other signals which are not connected to CPU.

2. i.MX6 Pico ITX – SBC Architecture and Design

This section provides detailed information about the i.MX6 Pico-ITX SBC Features and Hardware architecture with high level block diagram. Also this section provides detailed information about Expansion connector's pin assignment and usage.

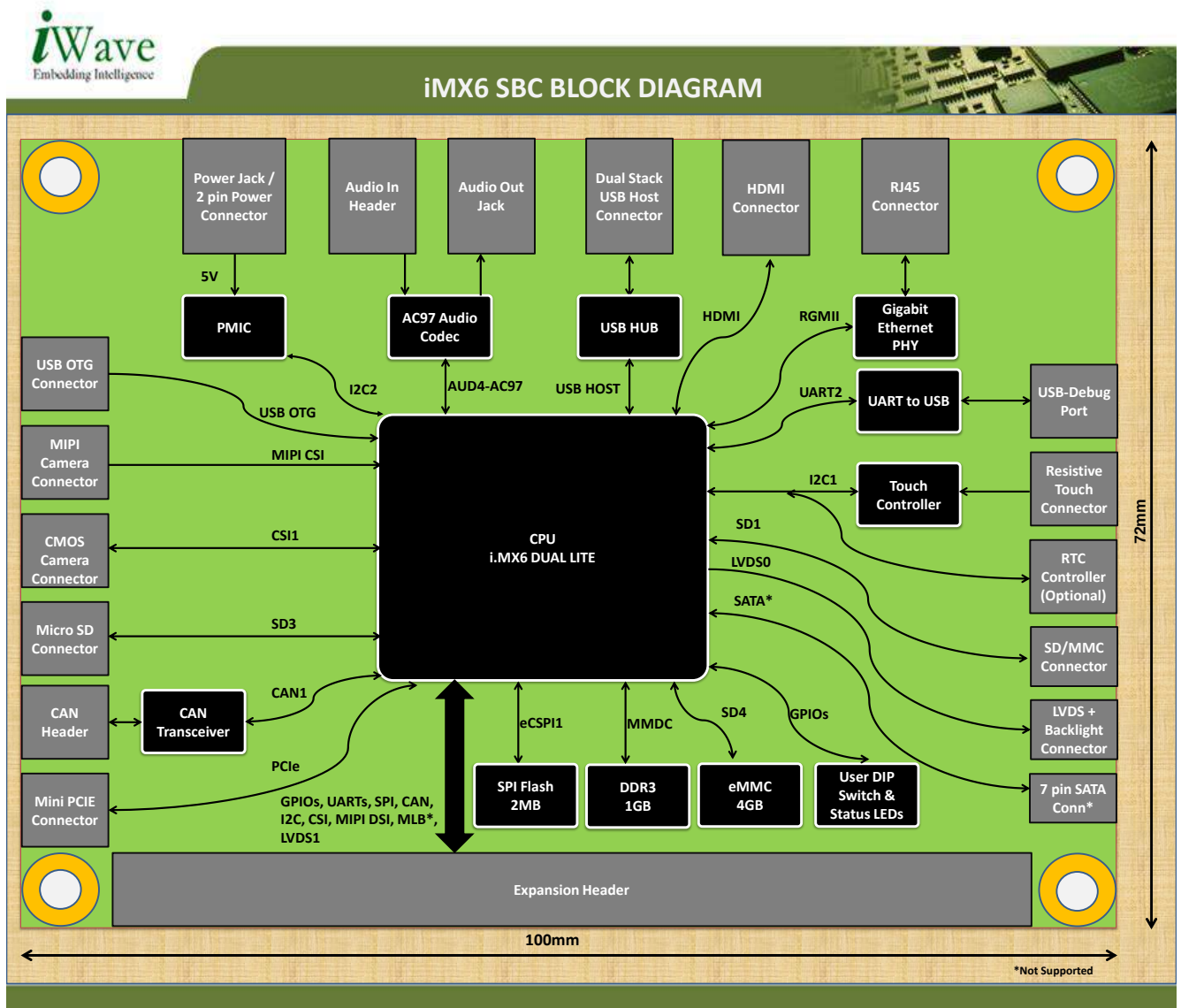


Figure 1: i.MX6 Pico ITX – SBC Block Diagram

2.1 i.MX6 Pico ITX - SBC Features

The i.MX6 Pico ITX - SBC supports the following features.

CPU

- Freescale's i.MX6 DualLite ARM Cortex-A9 core based CPU (Quad/Dual/Solo compatible)

PMIC

- Freescale's PMIC (MMPF0100F0EP)

Boot Mode Setting

- Boot Mode Selection Switch

Memory

- 1GB DDR3 (Expandable)
- SPI Flash (2MB)
- 4GB eMMC Flash
- Micro SD Connector
- Standard SD Connector

Audio/Video Features

- AC'97 Audio Codec with 3.5mm Stereo Head Phone Out Jack & Mic Input Header
- HDMI 1.4Port
- LVDS LCD Connector with Backlight Power Header
- Resistive Touch Connector
- CMOS Camera Connector
- MIPI Camera Connector

Communication Features

- Gigabit Ethernet PHY with RJ45 Magjack
- USB OTG 2.0 through Micro AB Connector
- USB Host 2.0 through Dual Stack Type A Connector
- Half Mini PCIe Gen2.0 Connector(with PCIe & USB interface)
- CAN Header (CAN1 with PHY)

Debug Features

- USB Micro AB Connector through UART to USB convertor for Debug console
- JTAG Connector
- 4bit DIP Switch (through GPIOs)
- 4 Status Indication LEDs (through GPIOs)

Expansion Connector Interfaces

- 2nd LVDS interface (LVDS1)
- MIPI DSI interface
- 8bit Camera interface (CSI0)
- SPI Interface-1 Port
- 2nd CAN Interface (CAN2)
- UART – 3 Ports
- I2C – 3 Ports
- GPIOs
- MLB interface with 6 pin & 3 pin signals*

Optional features

- RTC Controller with Coincell
- SATA Connector*

General specifications

- Power Input - 5V, 2A
- Temperature Supported: -20°C to +85°C
- Form factor: Pico ITX (100 x 72mm)

****Note: MLB & SATA signals will be available only in i.MX6 Quad & Dual CPU.***

2.2 i.MX6 CPU

i.MX6 is based on Freescale's Dual Lite/Solo ARM™ Cortex-A9 core based CPU which can operate up to 800MHz speed/core. i.MX6 CPU is Freescale's latest achievement in integrated multimedia application processors which is part of growing multimedia-focused products that offers high performance processing and are optimized for lowest power consumption. The simplified Block Diagram of i.MX6 CPU is shown below for your reference.

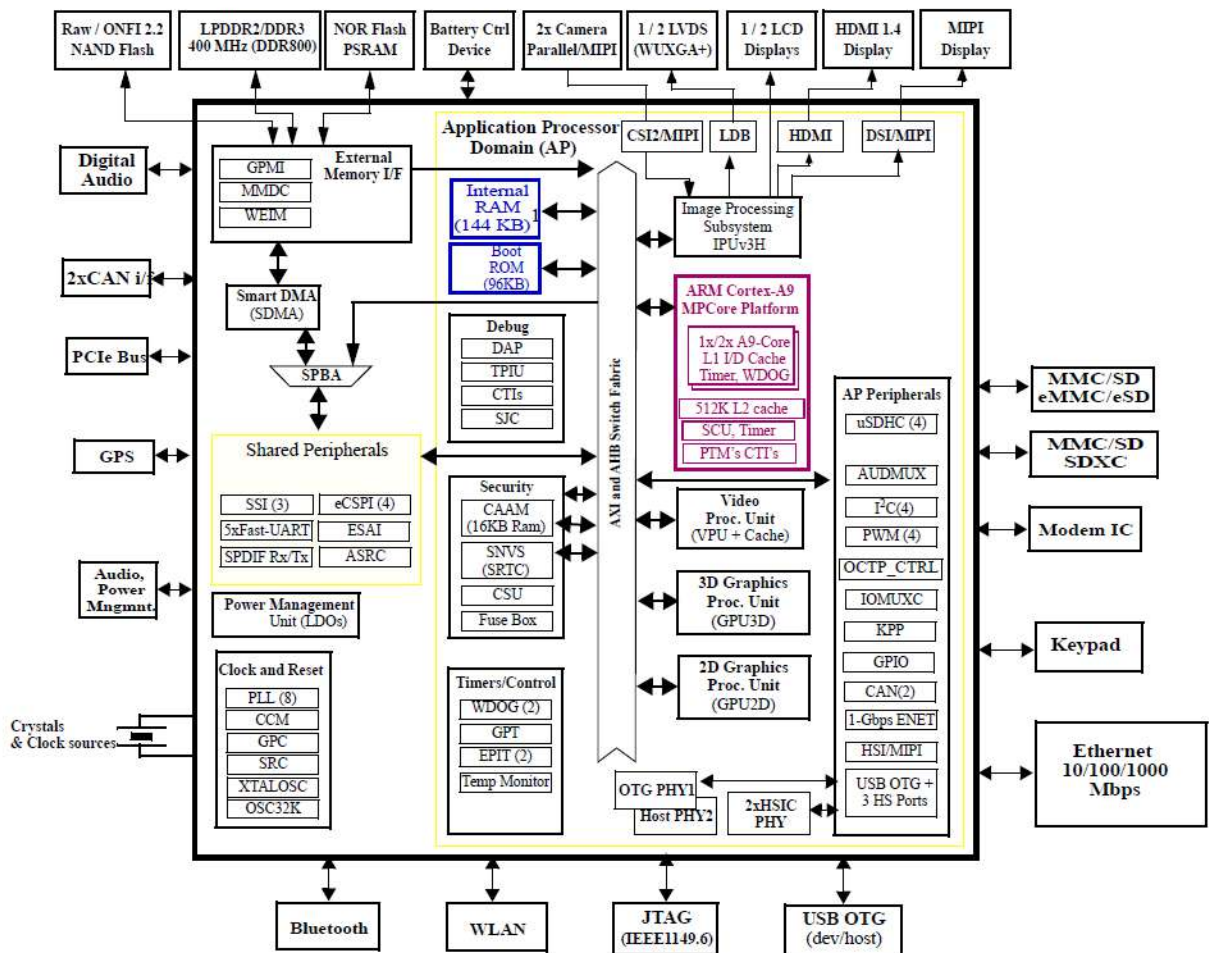


Figure 2: i.MX6 CPU Simplified Block Diagram

Note: Please refer the latest i.MX6 Datasheet & Reference Manual from Freescale website for Electrical characteristics of i.MX6 Application CPU which may be revised from time to time.

2.3 Boot Mode Setting

i.MX6 CPU boot process begins at Power On Reset (POR) where the hardware reset logic forces the ARM core to begin execution starting from the on-chip boot ROM. The i.MX6 Boot ROM code uses the state of the internal register BOOT_MODE [1:0] as well as the state of various eFUSEs and/or GPIO settings to determine the boot flow behaviour of the device.

i.MX6 Pico ITX SBC supports Boot Mode Switch (SW4) which is physically located in the top of the PCB. This Switch is used to select the boot mode setting of i.MX6 CPU as explained in the below table. SPI Flash used as Default Booting Media.

Table 2: Boot Mode Settings Truth Table

Boot Mode Setting On i.MX6 Pico ITX -SBC	Description	Switch (SW4) Position		
		POS 1	POS 2	Image
Internal Boot Mode (Default)	In this mode, i.MX6 boot media is selected by GPIO Pin's settings	OFF	ON	
Boot From eFuses	In this mode, i.MX6 boot media is selected by i.MX6 eFUSE settings <i>Note: i.MX6 eFuse setting is NOT modified by iWave from silicon shipped value.</i>	OFF	OFF	
Serial Downloader Mode	In this mode, i.MX6 boot device can be Programmed through its USB OTG interface using MFG Tool	ON	OFF	
ON – High		OFF - Low		

2.4 Memory

2.4.1 DDR3 SDRAM

i.MX6 Pico ITX – SBC uses four 256MB DDR3 SDRAM ICs to support a total on board RAM memory of 1GB (expandable). These devices will operate at 1.5V voltage level. The DRAM calibration resistor used on board is 240 Ohm 1% resistor. A pair of DDR3 IC is physically located on either side of the board.

2.4.2 SPI NOR Flash Memory

The i.MX6 Pico ITX – SBC supports SPI NOR Flash as default boot device. This is connected to Enhanced Configurable SPI port 1 (eCSPI1) of the i.MX6 CPU and device will operate under 3.3 Voltage level. RainboW-G15S Pico– ITX SBC will be shipped with 2MB SPI Flash on it (expandable). The SPI flash memory is physically located on top side of the Pico ITX – SBC.

2.4.3 eMMC Flash Memory

The i.MX6 Pico ITX – SBC supports 4GB eMMC (expandable) Flash memory as Mass storage also an optional boot device. eMMC is directly connected to the eSDHC Port 4 (SD4) of the i.MX6 CPU and operating under 3.3V Voltage level.

2.4.4 Micro SD Connector

Micro SD Card Connector (J13) is directly connected to the eSDHC channel 3 (SD3) of the i.MX6 CPU. This connector supports up to a 4-bit data transfer along with card detect feature. The main power to Micro SD Card Connector is 3.3V voltage. Micro SD Connector is physically located on top of the i.MX6 Pico ITX – SBC as shown below..

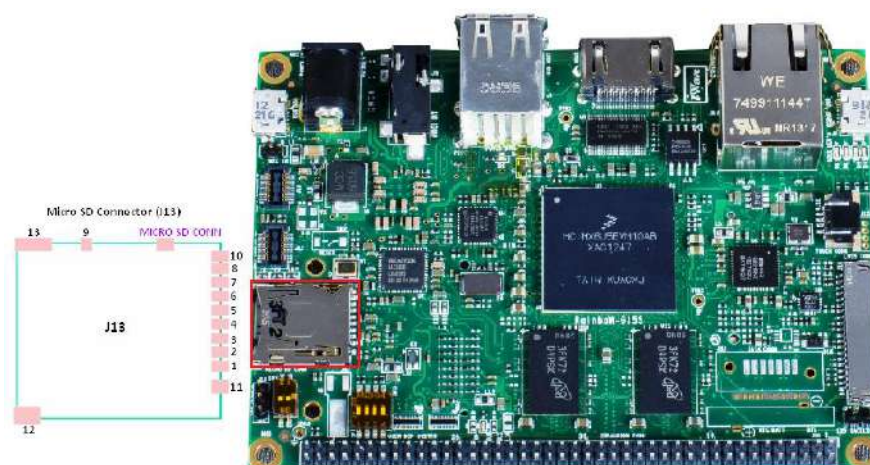


Figure 3: Micro SD Connector

Table 3: Micro SD Connector Pin Assignment

Pin No	Signal Name	Signal Type	Voltage Level/ Termination	Description
1	SD3_DATA2	Input / Output	3.3V CMOS	SD3 Data Line (Bit2)
2	SD3_DATA3	Input / Output	3.3V CMOS	SD3 Data Line (Bit3)
3	SD3_CMD	Input / Output	3.3V CMOS/ 10K Pull-up	SD3 Command Response
4	VCC_3V3	Power	3.3V	Card Supply Voltage
5	SD3_CLK	Output	3.3V CMOS	SD3 Clock
6	VSS	Power	0V	Ground
7	SD3_DATA0	Input / Output	3.3V CMOS	SD3 Data Line (Bit0)
8	SD3_DATA1	Input / Output	3.3V CMOS	SD3 Data Line (Bit1)
9	GPIO7_1_SD3_CD (SD3_DATA4)	Input	3.3V CMOS/ 10K Pull-up	SD3 Card Detect
10,11, 12,13	GND	Power	0V	Ground

2.4.5 Standard SD Connector

The Standard SD Connector (J23) is directly connected to the eSDHC channel 1 (SD1) of the i.MX6 CPU. This connector supports up to 4 bit data transfer along with card detect feature. The main power to the Standard SD connector is 3.3V. Optionally, 8bit data connector footprint is provided in the board and not supported by default.

The Standard SD connector can support SD memory cards, SDIO cards (Wi-Fi, BT etc.) which are designed to fit in a standard SD connector. Standard SD connector is physically located on bottom of the board.

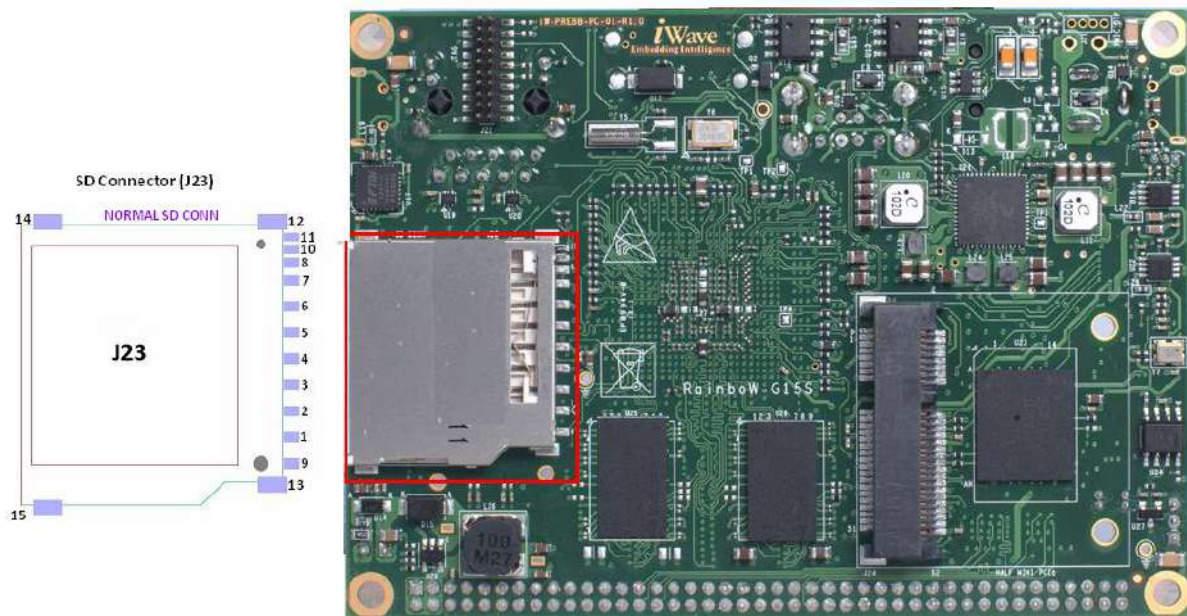


Figure 4: Standard SD Connector

Table 4: Standard SD Connector Pin Assignment

Pin No	Signal Name	Signal Type	Voltage Level/ Termination	Description
1	GPIO6_11_SD1_WP(NANDF_CS0)	Input	3.3V CMOS/ 10K Pull-up	Write Protect
2	GPIO7_0_SD1_CD(SD3_DAT5)	Input	3.3V CMOS/ 10K Pull-up	Card Detect
3	SD1_DAT1	Input / Output	3.3V CMOS	Data Line (bit1)
4	SD1_DAT0	Input / Output	3.3V CMOS	Data Line (bit0)
5	SD1_DAT7(NANDF_D3)	Input / Output	3.3V CMOS	Data Line (bit7) Optional, Not supported by default.
6	VSS1	Power	0V	Ground
7	SD1_DAT6(NANDF_D2)	Input / Output	3.3V CMOS	Data Line (bit6) Optional, Not supported by default.
8	SD1_CLK	Output	3.3V CMOS	Clock

9	VCC/VDD	Power	3.3V	Supply Voltage
10	VSS2	Power	0V	Ground
11	SD1_DAT5(NANDF_D1)	Input / Output	3.3V CMOS	Data Line (bit5) Optional, Not supported by default.
12	SD1_CMD	Input / Output	3.3V CMOS/ 10K Pull-up	Command/ Response
13	SD1_DAT4(NANDF_D0)	Input / Output	3.3V CMOS	Data Line (bit4) Optional, Not supported by default.
14	SD1_DAT3	Input / Output	3.3V CMOS	Data Line (bit3)
15	SD1_DAT2	Input / Output	3.3V CMOS	Data Line (bit2)

2.5 Audio/Video Features

2.5.1 AC'97 audio codec Interface

The Audio CODEC used on the i.MX6 Pico ITX – SBC is ALC5610 from Realtek with inbuilt Headphone amplifier and MIC which is used to provide a complete audio solution for portable products. This Audio codec is connected to AUDMUX channel 3 of the i.MX6 CPU. i.MX6 Pico ITX – SBC supports 3.5mm stereo Headphone Out Jack and 3pin MIC In header which are physically located on top of the board.

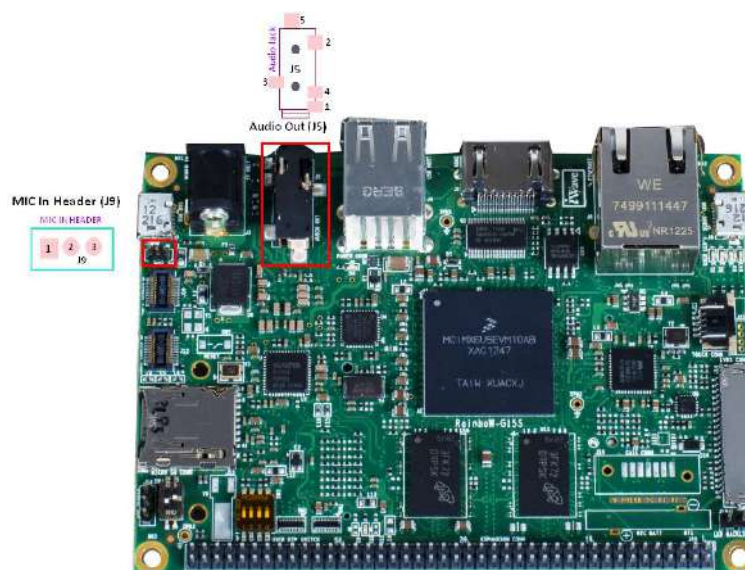


Figure 5: Audio Jack

Table 5: Audio OUT Jack Pin Out

Pin.NO	Signal Name	Signal Type	Voltage Level/ Termination	Description
1	GND	Power	0V	Ground
2	HP_L_ESD	Analog Output	1Vrms	Headphone Left
3	HP_R_ESD	Analog Output	1Vrms	Headphone Right
4	GPIO5_05_HP_DETECT(DISPO_D AT11)	Output	3.3V CMOS	Head Phone Detection
5	NC	-	-	No Connection

Table 6: MIC IN Header Pin Out

Pin.NO	Pin Detail	Signal Type	Voltage Level/ Termination	Description
1	GND	Power	0V	Ground
2	GPIO5_07_MIC_IN_DETECT(DISPO_D DAT13)	Output	3.3V CMOS	Microphone Detection
3	MIC1P_ESD	Analog Input	1Vrms	MIC Positive Input

Number of Pins - 03

Connector Part Number - GRPB031VWVN-RC

Mating Connector - LPPB031NGCN-RC from Sullins Connector Solutions

2.5.2 HDMI interface

HDMI signals from i.MX6 CPU are connected to Standard HDMI port with protection circuitry. HDMI is capable of transferring uncompressed video, audio, and data using a single cable. The video pixel rates are typically from 25 MHz up to 297 MHz (4k x 2k and 3Dvideo modes), but HDMI can support higher rates up to 340 MHz HDMI port is physically located on top of the board.

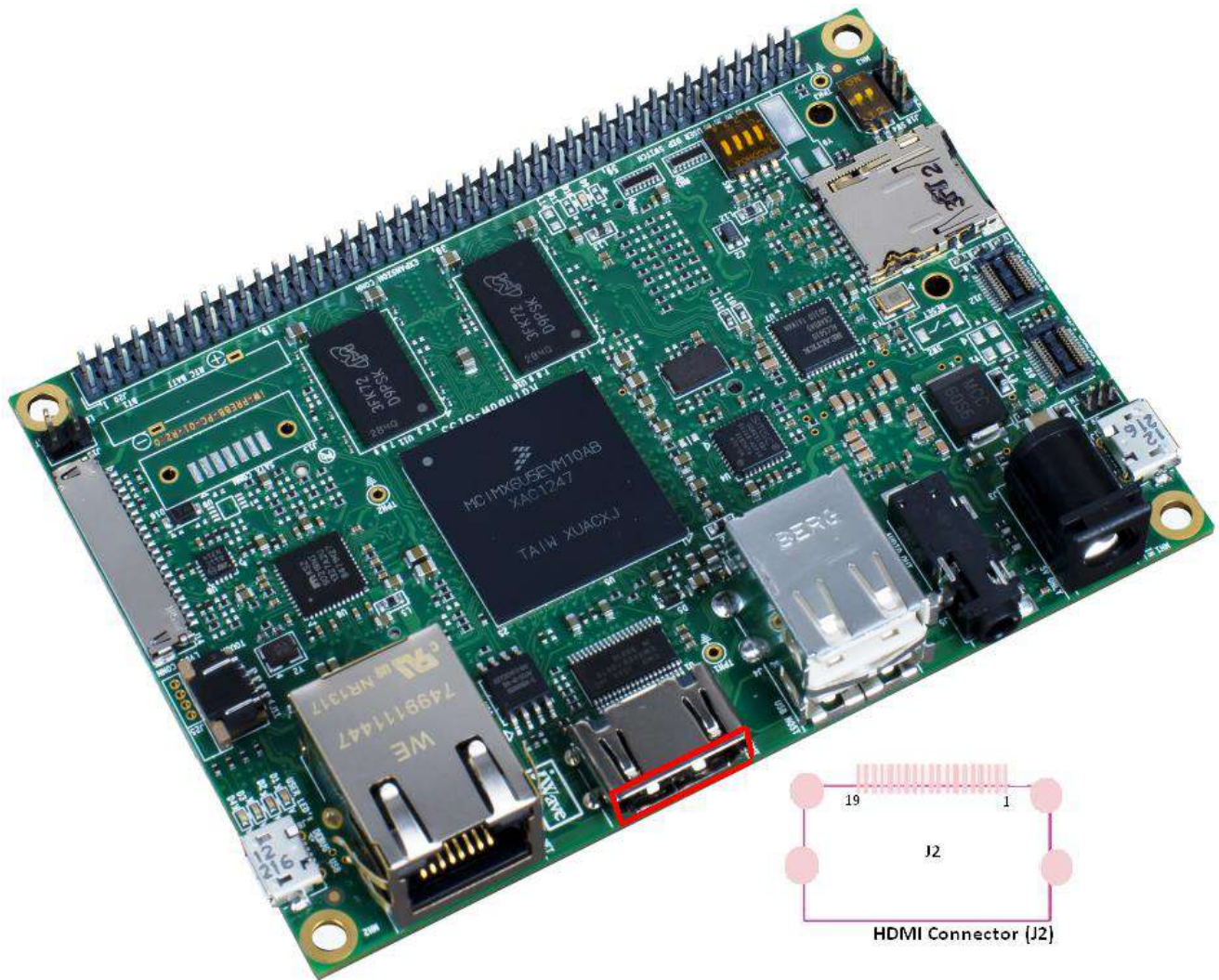


Figure 6: HDMI Port

Table 7: HDMI Port Pin Out

Pin No	Signal Name	Signal Type	Voltage Level/ Termination	Description
1	TMDS_LANE2+	Output	TMDS	Display RED+ differential signal
2	D2_GND	Power	0V	Red Pair Ground
3	TMDS_LANE2-	Output	TMDS	Display RED- differential signal
4	TMDS_LANE1+	Output	TMDS	Display GREEN+ differential signal
5	D1_GND	Power	0V	Green Pair Ground
6	TMDS_LANE1-	Output	TMDS	Display GREEN- differential signal
7	TMDS_LANE0+	Output	TMDS	Display BLUE+ differential signal
8	D0_GND	Power	0V	Blue Pair Ground
9	TMDS_LANE0-	Output	TMDS	Display BLUE- differential signal
10	TMDS_CLK+	Output	TMDS	Display Clock+ differential signal
11	CLK_GND	Power	0V	Clock pair Ground
12	TMDS_CLK-	Output	TMDS	Display Clock- differential signal
13	CEC	Input/Output	3.3V CMOS/ 27K Pull-up	Consumer Electronic Control
14	NC	-	-	No Connection
15	HDMI_SDVO_CTL_CLK	Output	3.3V CMOS/ 4.7K Pull-up	EDID I2C Clock
16	HDMI_SDVO_CTL_DAT	Input/Output	3.3V CMOS/ 4.7K Pull-up	EDID I2C Data
17	GND	Power	0V	Ground
18	VOOUT_5	Power	5V	5V Power Supply
19	HDMI_HPD#	Input	3.3V CMOS/ 15K Pull-down	HDMI Cable Hot plug detect

2.5.3 LVDS Connector

i.MX6 Pico ITX – SBC supports LVDS connector to connect different LVDS LCDs. It also supports backlight connector with 15V 300mA output for LCD backlight. LVDS0 interface from i.MX6 is connected to this 20 pin LVDS connector. LVDS connector (J14) and LVDS Back light connector (J19) are physically located on top of the board.

LVDS LCD Connector:

Number of Pins - 20

Connector Part Number - DF19G-20P-1H(56)/DF19G-20P-1H(54)

Mating Connector - DF19G-20S-1SD(05)/DF19G-20S-1C from Hirose Electric Co. Ltd.

Backlight Connector:

Number of Pins - 02

Connector Part Number - 961102-6404-AR

Mating Connector - 960102-6303-AR from 3M

Compatible LCDs

1. Part Number: OSD104T0571-19TS
Description: 10.4 inch LVDS 6 bits with 800 x 600 (RGB) resolution
Manufacturer Name: OSD Displays
2. Part Number: T-51944D104J-FW-A-ABN
Description: 10.39 inch LVDS 6 bits with 800 x 600 (RGB) resolution
Manufacturer Name: OPTREX Corporation
3. Part Number: TLM-TA40T3130-01
Description: 10.4 inch LVDS 6 bits with 800 x 600 (RGB) resolution
Manufacturer Name: Varitronix

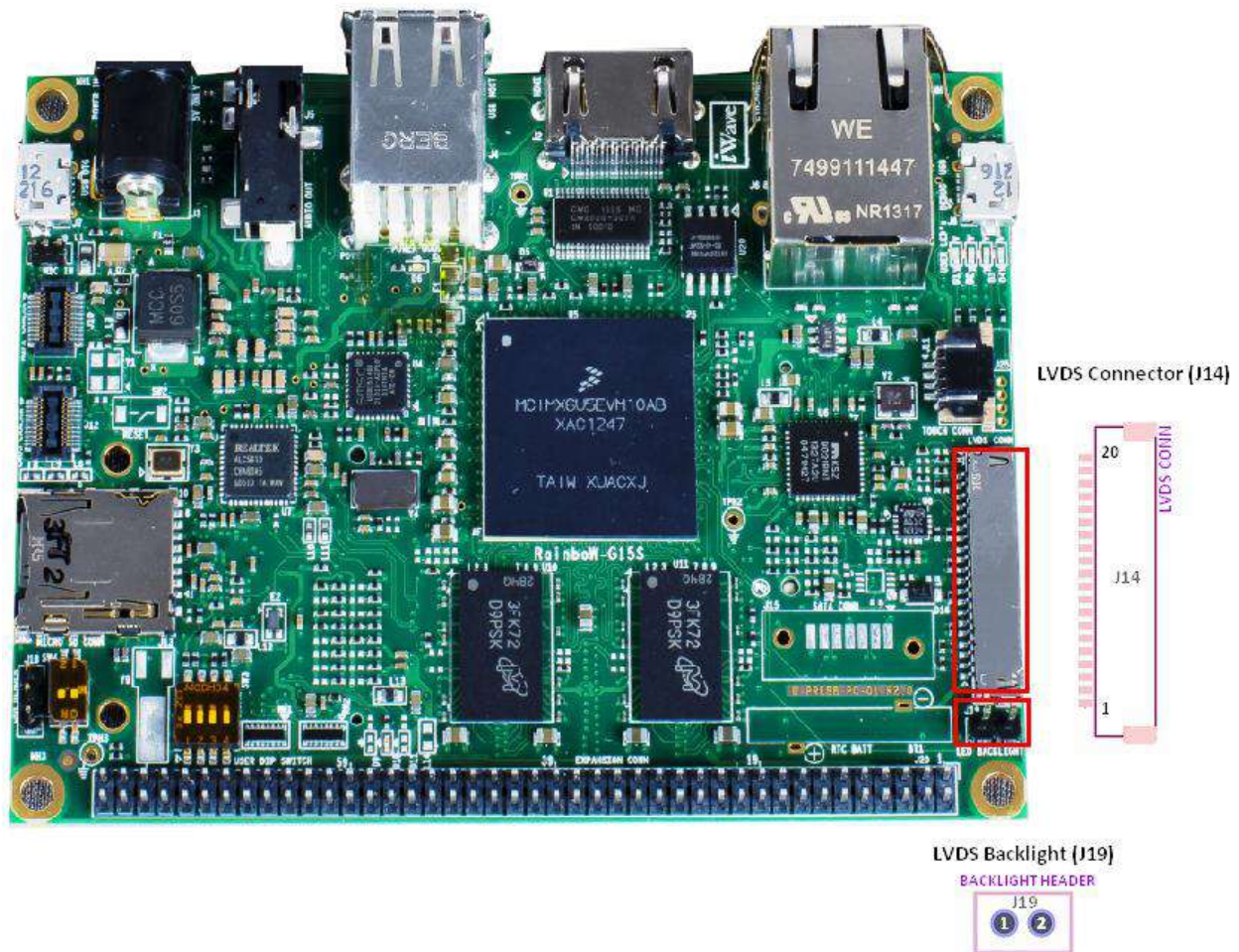


Figure 7: LVDS Connectors

Table 8: LVDS Connector Pin Out

Pin No	Signal Name	Signal Type	Voltage Level/ Termination	Description
1	TFT1_VCC_3V3	Power	3.3V	Supply voltage for TFT
2	TFT1_VCC_3V3	Power	3.3V	Supply voltage for TFT
3	GND	Power	0V	Ground
4	GND	Power	0V	Ground
5	LVDS0_TX0_N	Output	LVDS	LVDS primary channel differential pair 0
6	LVDS0_TX0_P	Output	LVDS	

7	GND	Power	0V	Ground
8	LVDS0_TX1_N	Output	LVDS	LVDS primary channel differential pair 1.
9	LVDS0_TX1_P	Output	LVDS	
10	GND	Power	0V	Ground
11	LVDS0_TX2_N	Output	LVDS	LVDS primary channel differential pair 2.
12	LVDS0_TX2_P	Output	LVDS	
13	GND	Power	0V	Ground
14	LVDS0_CLK_N	Output	LVDS	LVDS primary channel differential pair clock lines.
15	LVDS0_CLK_P	Output	LVDS	
16	GND	Power	0V	Ground
17	LVDS0_TX3_N	Output	LVDS	LVDS primary channel differential pair 3.
18	LVDS0_TX3_P	Output	LVDS	
19	GND	Power	0V	Ground
20	GND	Power	0V	Ground

Table 9: LVDS Backlight Connector Pin Out

Pin No	Signal Name	Signal Type	Voltage Level/ Termination	Description
1	LED_A0	Power	15V	LED Anode
2	LED_K0	Power	0V	LED Cathode

Note: To change the LVDS Backlight LED driver setting,

1. *Change Current sensing resistor **R317 (R_{SET})** by calculating using the below formula*

$$\frac{V_{FB}}{R_{SET}} = I_{LED}$$

Where $V_{FB} = 190mV$, I_{LED} = Current required for LCD backlight LEDs.

2. *Change **D14** Zener Diode from 15V to required voltage.*

(Populated diode part number is BZT52C20-7-F)

Note: For i.MX6 Pico ITX SBC Silkscreen identifier details, refer APPENDIX I

2.5.4 Resistive Touch Connector

i.MX6 Pico ITX – SBC supports a resistive touch interface through resistive touch controller. This resistive touch controller converts the analog touch input values to digital and also generates touch interrupt to i.MX6 CPU. Resistive touch connector is physically located on top of the board.

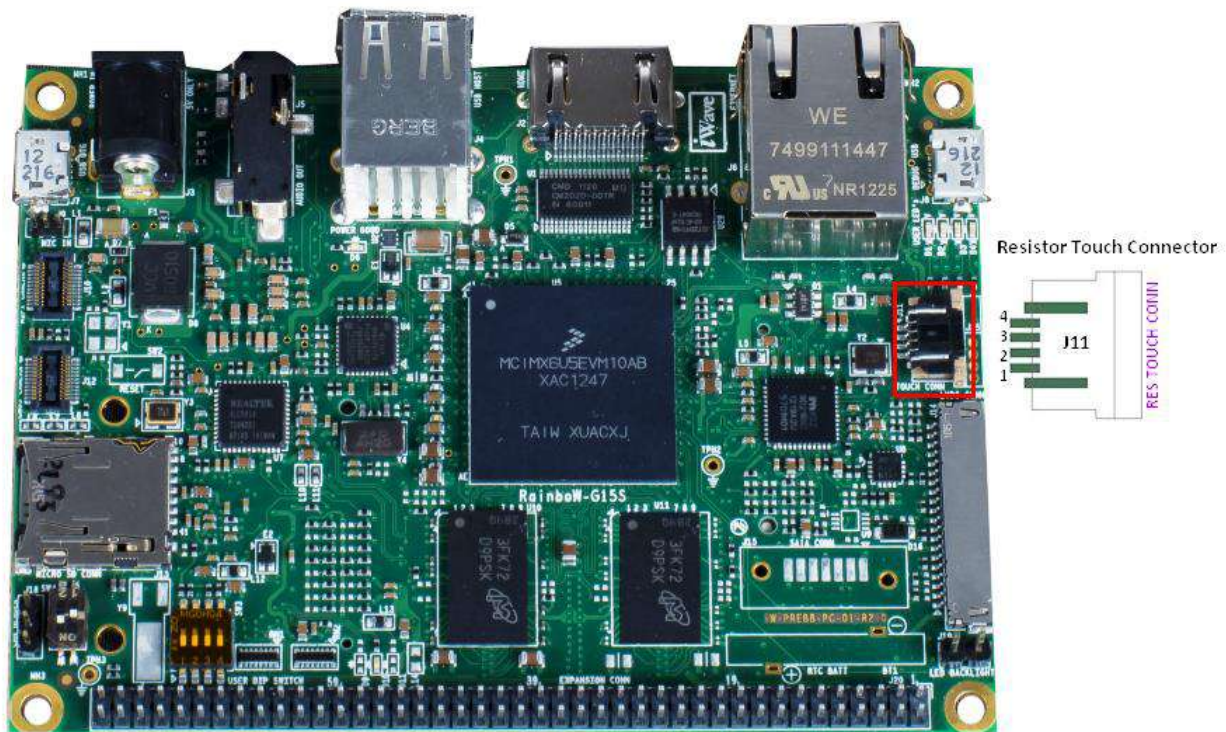


Figure 8: Resistive Touch Connector

Table 10: Resistive Touch Connector Pin Out

Pin No	Signal Name	Signal Type	Voltage Level/ Termination	Description
1	TSC_Y1	Input	Analog	Touch Left Signals
2	TSC_X2	Input	Analog	Touch Up Signals
3	TSC_Y2	Input	Analog	Touch Right Signals
4	TSC_X1	Input	Analog	Touch Down Signals

Number of Pins - 04

Connector Part Number - SFW4R-4STE1LF from FCI

Mating Connector - Touch panel FPC cable with 1mm pitch

2.5.5 CMOS Camera Connector

i.MX6 Pico ITX – SBC supports 8/10bit CMOS Camera Interface through the CSI1 interface from the i.MX6 CPU. External clock for camera is provided using on board Oscillator of frequency 26MHz. The 24-pin Camera connector is physically located on top of board.

Number of Pins - 24

Connector Part Number - AXK724147G

Mating Connector - AXK824245WG from Panasonic Electric Works

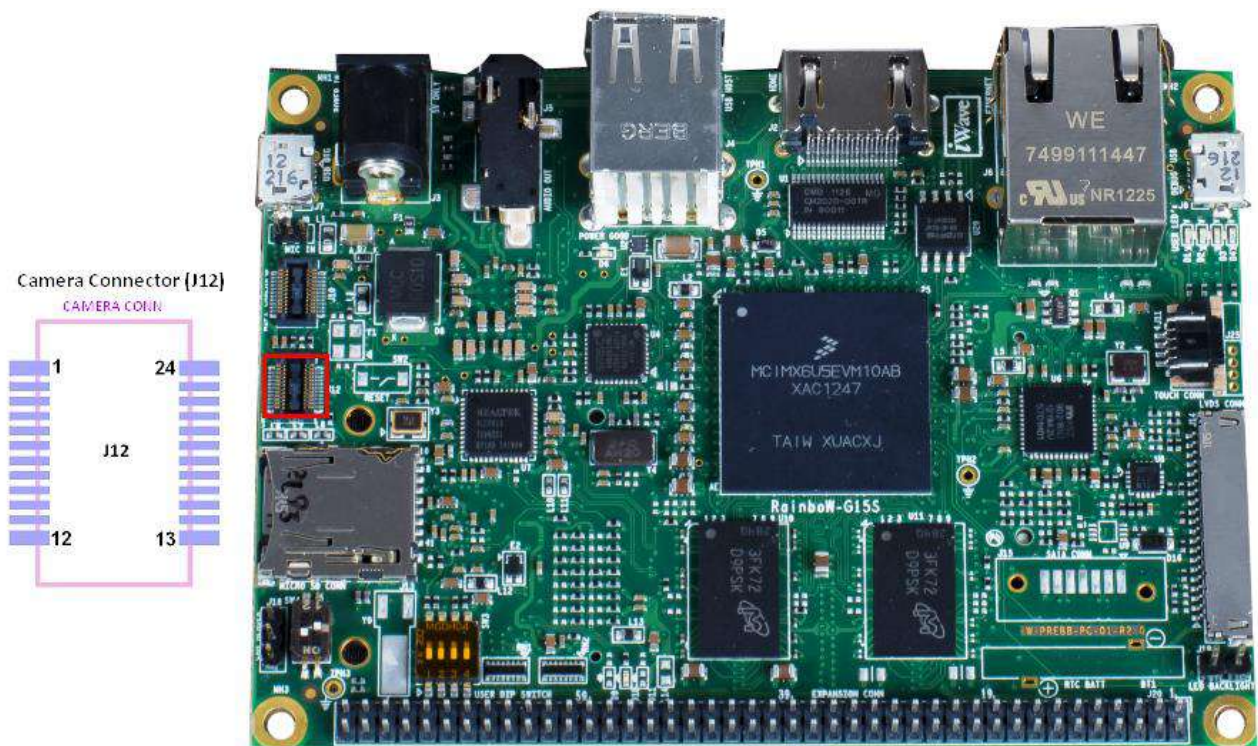


Figure 9: Camera Connector

Table 11: Camera Connector Pin Out

Pin No	Signal Name	Signal Type	Voltage Level/ Termination	Description
1	NC	-	-	No Connection
2	AGND	Power	0V	Analog Ground
3	I2C1_SDA(EIM_D28)	Input/Output	3.3VCMOS/ 4.7K Pull-up	I2C Data
4	VCC_2V8_CAM	Power	2.8V	Analog Power Supply
5	I2C1_SCL(EIM_D21)	Output	3.3VCMOS/ 4.7K Pull-up	I2C Clock
6	GPIO1_11_HDA_RST(S D2_CMD)	Output	3.3V CMOS	Reset In, Active Low 0= Reset asserted
7	CSI1_VSYNC(EIM_D29)	Input	3.3V CMOS	Vertical Synch
8	GPIO4_21_CAM_PWD N(DISP0_DAT0)	Output	3.3V CMOS	Power Down
9	CSI1_HSYNC(EIM_EB3)	Input	3.3V CMOS	Horizontal Synch
10	VCC_1V8	Power	1.8V	Digital Power Supply
11	DOVDD	Power	3.3V	IO Power Supply
12	CSI1_D[19](EIM_A24)	Input	3.3V CMOS	Camera Data9
13	CSI1_MCLK	Input	3.3V CMOS	Camera Clock
14	CSI1_D[18](EIM_A23)	Input	3.3V CMOS	Camera Data8
15	DGND	Power	0V	Digital Ground
16	CSI1_D[17](EIM_A22)	Input	3.3V CMOS	Camera Data7
17	CSI1_PIXCLK(EIM_A16)	Input	3.3V CMOS	Camera Pixel Clock
18	CSI1_D[16](EIM_A21)	Input	3.3V CMOS	Camera Data6
19	CSI1_D[12](EIM_A17)	Input	3.3V CMOS	Camera Data2
20	CSI1_D[15](EIM_A20)	Input	3.3V CMOS	Camera Data5
21	CSI1_D[13](EIM_A18)	Input	3.3V CMOS	Camera Data3
22	CSI1_D[14](EIM_A19)	Input	3.3V CMOS	Camera Data4
23	NC	-	-	No Connection
24	NC	-	-	No Connection

2.5.6 MIPI Camera Connector

i.MX6 Pico ITX – SBC supports MIPI camera connector to connect 5MP OV5640 MIPI camera from Leopard. i.MX6 CPU supports MIPI CSI interface, providing high performance serial interconnect bus for mobile applications connecting camera sensors to the host system. This interface supports from 80 Mbps up to 1Gbps speed per data lane. The CSI receiver core can manage one clock lane and up to two data lanes through the lane management and de-packetization, providing a maximum throughput of 4Gbps transfer rate. This camera connector is physically located on top of the board.

Number of Pins - 24

Connector Part Number - AXK724147G

Mating Connector - AXK824245WG from Panasonic Electric Works

Compatible MIPI Camera:

Part Number - LI-OV5640-MIPI-AF

Description - 5Mega Pixel OV5640 MIPI camera

Manufacturer Name - Leopard

Leopard MIPI Camera Module link: <https://www.leopardimaging.com/LI-OV5640-MIPI-AF.html>

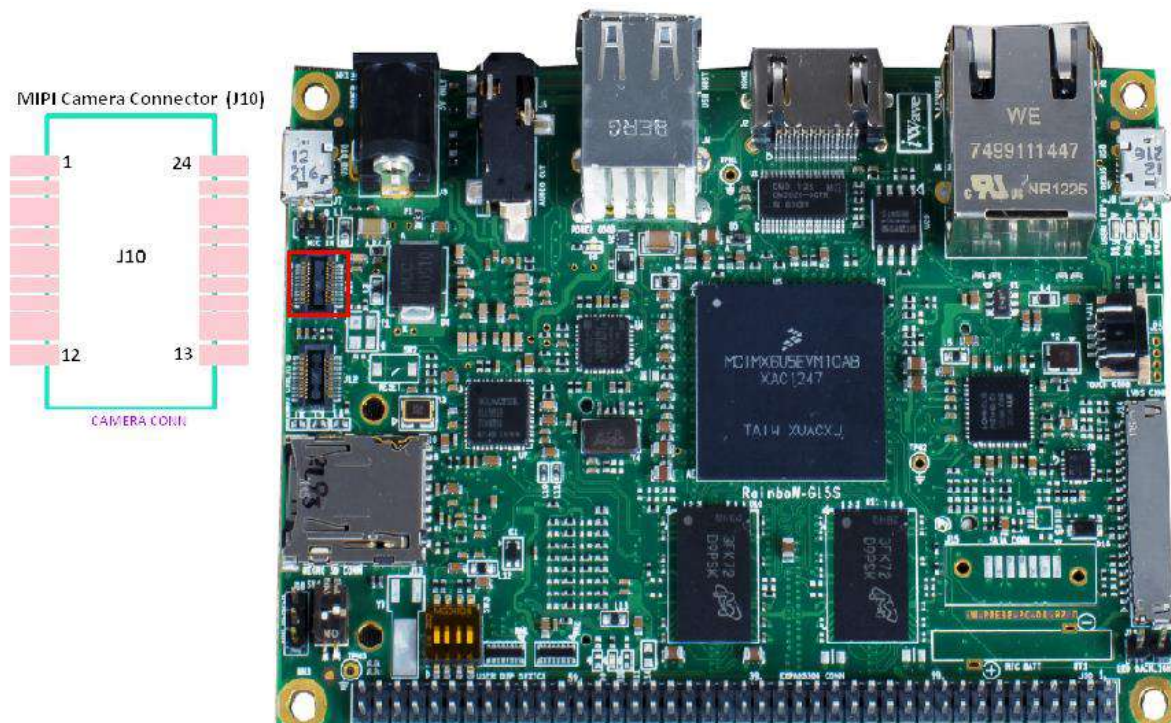


Figure 10: MIPI Camera connector

Table 12: MIPI 5M Camera Interface Pin Out

Pin No	Signal Name	Signal Type	Voltage Level/ Termination	Description
1	NC	-	-	No Connection
2	AGND	Power	0V	Analog Ground
3	I2C1_SDA(EIM_D28)	Input/Output	1.8V CMOS	MIPI CSI I2C Data
4	AVDD	Power	2.8V	Analog Power 2.8V
5	I2C1_SCL(EIM_D21)	Output	1.8V CMOS	MIPI CSI I2C Clock
6	GPIO1_11_HDA_RST(S D2_CMD)	Output	1.8V CMOS	MIPI CSI Reset
7	NC	-	-	No Connection
8	MIPI_CSI_PD	Input	OPEN	MIPI CSI Power Down
9	NC	-	-	No Connection
10	DVDD	Power	1.5V	Digital Power 1.5V
11	DOVDD	Power	1.8V	Digital Power 1.8V
12	CSI_D1P	Input	2.5V CMOS	CSI1 Positive Data
13	MIPI_CSI_MCLK	Output	1.8V CMOS	MIPI CSI Master Clock
14	CSI_D1M	Input	2.5V CMOS	CSI1 Negative Data
15	DGND	Power	0V	Digital Ground
16	CSI_CLK0P	Input	2.5V CMOS	CSI0 Positive Clock
17	NC	-	-	No Connection
18	CSI_CLK0M	Input	2.5V CMOS	CSI0 Negative Clock
19	NC	-	-	No Connection
20	CSI_D0P	Input	2.5V CMOS	CSI0 Positive Data
21	NC	-	-	No Connection
22	CSI_D0M	Input	2.5V CMOS	CSI0 Negative Data
23	MIPI_AF_VDD	Power	1.8V	MIPI AF Power 1.8V
24	AF_GND	Power	0V	Analog Field Ground

2.6 Communication Features

2.6.1 Gigabit Ethernet Interface

i.MX6 Pico ITX – SBC supports Gigabit Ethernet interface using Gigabit Ethernet PHY “KSZ9021RN”. This PHY is interfaced with i.MX6 using RGMII interface. A RJ45 Mag Jack with LED indicators is provided for Gigabit Ethernet interface. This RJ45 Mag jack can work with 10/100/1000 Mbps Ethernet operation and physically located on top of the board.



Figure 11: Gigabit Ethernet Connector

Table 13: RJ45 Magjack Connector Pin Out

Pin No	Signal Name	Signal Type	Voltage Level/ Termination	Description
1	GPHY_ATXRX	Input/Output	MDIO	Media Dependent Interface (MDI) differential pair A
2	GPHY_ATRXM	Input/Output	MDIO	
3	GPHY_BTXX	Input/Output	MDIO	Media Dependent Interface (MDI) differential pair B
4	GPHY_BTXXM	Input/Output	MDIO	
5	VCC_3V3	Power	3.3V	Ref
6	VCC_3V3	Power	3.3V	Ref
7	GPHY_CTXRX	Input/Output	MDIO	Media Dependent Interface (MDI) differential pair C
8	GPHY_CTXRM	Input/Output	MDIO	
9	GPHY_DTXRX	Input/Output	MDIO	Media Dependent Interface (MDI) differential pair D
10	GPHY_DTXRM	Input/Output	MDIO	
11	GPHY_ACTIVITY_LED1	Output	3.3V CMOS/ 1K Pull-down	LED1 Cathode
12	VCC_3V3	Power	3.3V	LED1 Anode
13	VCC_3V3	Power	3.3V	LED2 Anode
14	GPHY_LINK_LED2	Output	3.3V CMOS/1K Pull-down	LED2 Cathode

2.6.2 USB OTG Connector

i.MX6 Pico ITX – SBC supports USB Micro AB connector for USB OTG functionality. USB 2.0 OTG signals from i.MX6 CPU is connected to this USB Micro AB connector. USB 2.0 high speed port supports up to 480 Mbps using i.MX6 integrated High Speed USB PHY. USB OTG connector is physically located on top of the board.

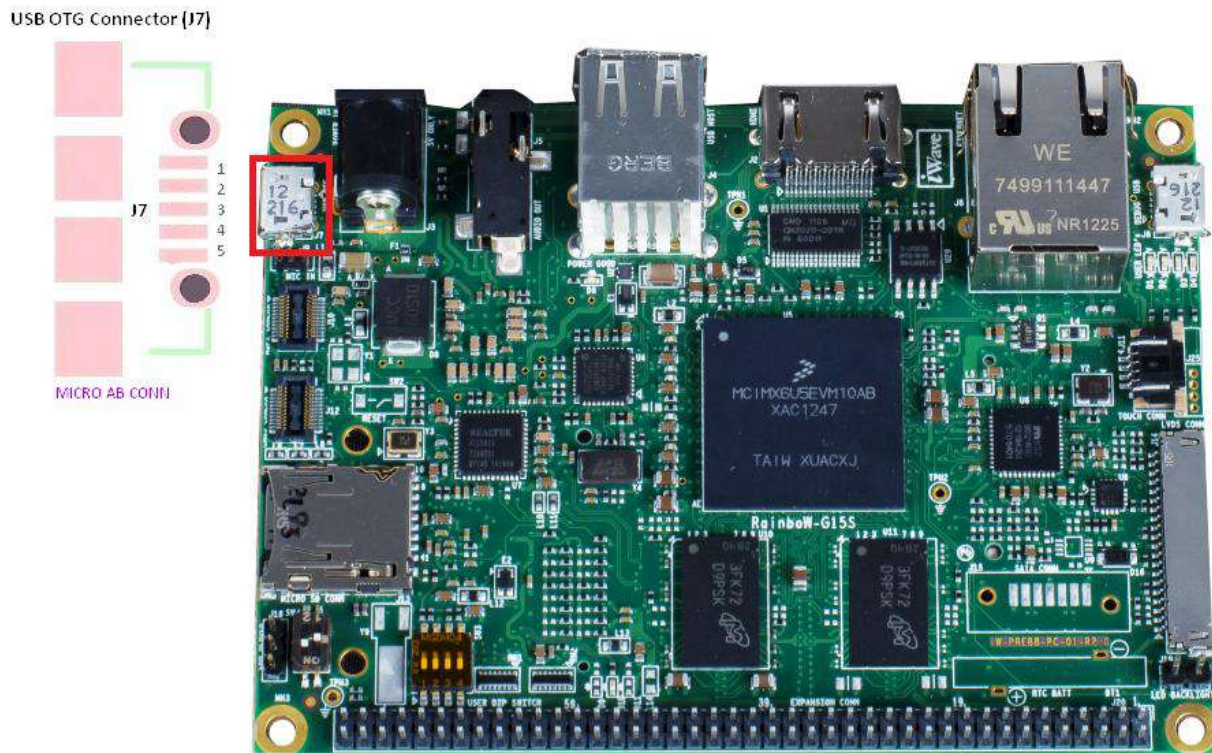


Figure 12: USB1 OTG Connector

Table 14: USB OTG Connector Pin Out

Pin No	Signal Name	Signal Type	Voltage Level/ Termination	Description
1	USB_VBUS1C	Power	5V	USB OTG 5V Power
2	USB_OTG_DN	Input/Output	USB differential Signal	USB OTG Differential data pair
3	USB_OTG_DP	Input/Output	USB differential Signal	
4	USB ID	Input	3.3V CMOS/ 10K Pull-up	USD ID signal Open(float): Device
5	Ground	Power	0V	USB OTG Ground

2.6.3 USB Host Connector

i.MX6 Pico ITX – SBC supports three High Speed (HS) USB 2.0 host. To support 3 USB hosts, the i.MX6 Pico ITX – SBC uses 1 to 4 port USB hub “USB2514Bi”. This USB hub is interfaced with i.MX6 using i.MX6 integrated High Speed USB Host PHY. Two USB Ports from the USB hub are connected to Dual stack Type A connector and 1 USB Port is connected to Mini PCIe. This Dual Stack Connector is located on top of the board as shown below.

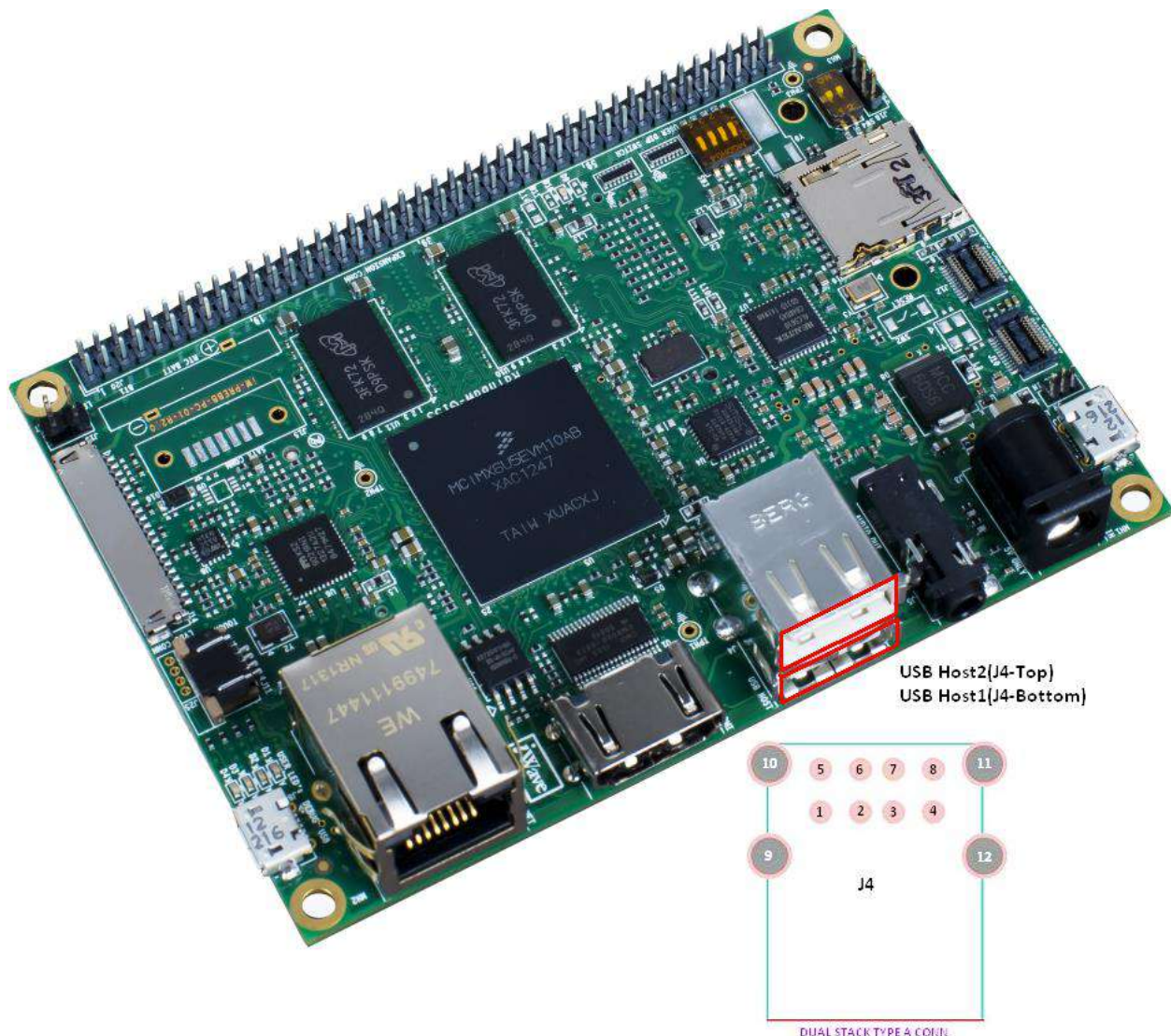


Figure 13: USB Dual Stack Connector

Table 15: USB Host Dual Stack Connector

Pin No	Signal Name	Signal Type	Voltage Level/ Termination	Description
1	USB_VBUS0	Power	5V	USB1 5V Power
2	USB_HUBP1_DM	Input/Output	Differential	USB1 Data negative
3	USB_HUBP1_DP	Input/Output	Differential	USB1 Data Positive
4	GND	Power	0V	USB1 Ground
5	USB_VBUS2	Power	5V	USB2 5V Power
6	USB_HUBP2_DM	Input/Output	Differential	USB2 Data negative
7	USB_HUBP2_DP	Input/Output	Differential	USB2 Data Positive
8	GND	Power	0V	USB2 Ground

2.6.4 Mini PCIe Connector

i.MX6 Pico ITX – SBC supports Mini PCIe connector with PCIe interface and USB interface. i.MX6 CPU supports PCI express (Gen 2.0) dual mode complex supporting Root complex operations and Endpoint operations. PCIe signals from i.MX6 CPU and USB Host signals from USB hub is connected to the Mini PCIe Connector. Mini PCIe Connector is physically located on the bottom of the board.

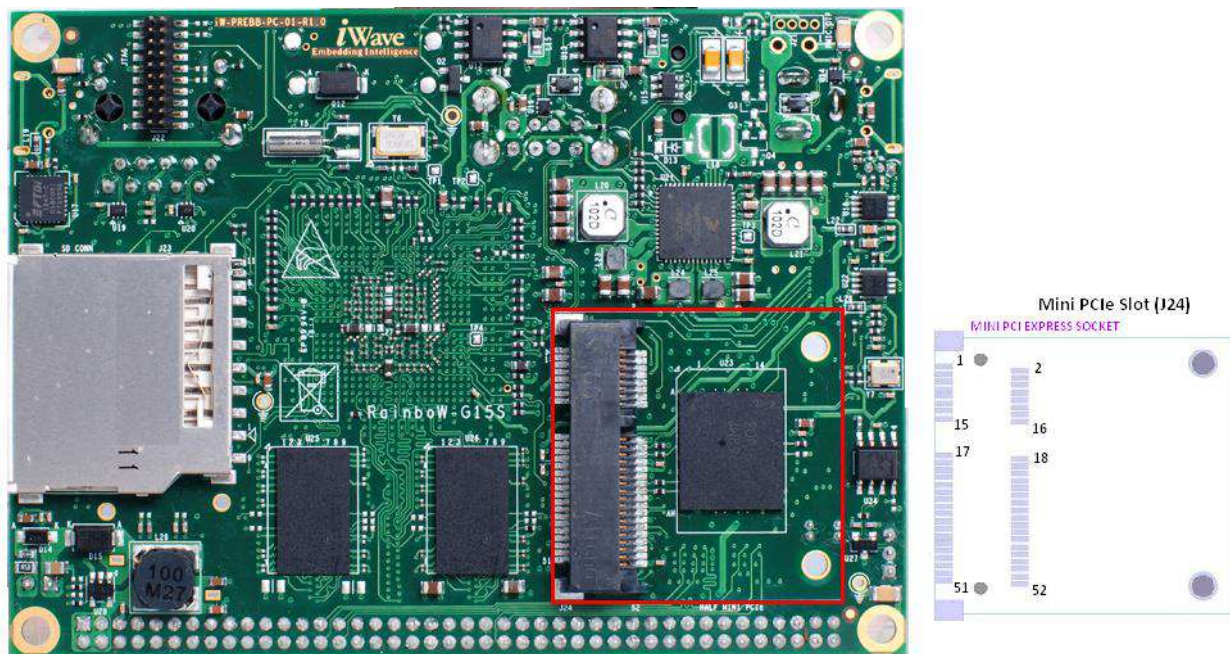


Figure 14: Mini PCIe Slot

Table 16: Mini PCIe Slot Pin Out

Pin No	Signal Name	Signal Type	Voltage Level/ Termination	Description
1	GPIO2_6_PcIe_WAKE(NANDF_D6)	Input	3.3V CMOS	PCie Wake Signal
2	3G_3V3	Power	3.3V	3.3V Power Supply
3	NC	-	-	No Connection
4	GND	Power	0V	Ground
5	NC	-	-	No Connection
6	3G_1V5	Power	1.5V	1.5V Power Supply
7	NC	-	-	No Connection
8	NC	-	-	No Connection
9	GND	Power	0V	Ground
10	NC	-	-	No Connection
11	PCie0_CLK-	Output	Differential/ 0.1uf AC coupling(C122)	PCie reference clock-
12	NC	-	-	No Connection
13	PCie0_CLK+	Output	Differential/ 0.1uf AC coupling(C130)	PCie reference clock+
14	NC	-	-	No Connection
15	GND	Power	0V	Ground
16	NC	-	-	No Connection
17	NC	-	-	No Connection
18	GND	Power	0V	Ground
19	NC	-	-	No Connection
20	GPIO4_28_W_DISABL E(DISPO_DAT7)	Output	3.3V CMOS	Wireless Disable Input
21	GND	Power	0V	Ground
22	GPIO2_07_PcIe_RST(NANDF_D7)	Output	3.3V CMOS	PCie Reset
23	PCie_RXM	Input	Differential/ 0.1uf AC coupling(C366)	PCie Receiver Lane-
24	3G_3V3	Power	3.3V	3.3V Power Supply

25	PCle_RXP	Input	Differential/ 0.1uf AC coupling(C372)	PCle Receiver Lane+
26	GND	Power	0V	Ground
27	GND	Power	0V	Ground
28	3G_1V5	Power	1.5V	1.5V Power Supply
29	GND	Power	0V	Ground
30	I2C2_SCL(KEY_COL3)	Output	3.3V CMOS/ 4.7K Pull-up	I2C2 Clock
31	PCle_TXM	Output	Differential	PCle Transmitter Lane-
32	I2C2_SDA(KEY_ROW3)	Input/Output	3.3V CMOS/ 4.7K pull-up	I2C2 Data
33	PCle_TXP	Output	Differential	PCle Transmitter Lane+
34	GND	Power	0V	Ground
35	GND	Power	0V	Ground
36	USB_HUBP3_DM	Input/Output	Differential	USB Hub3 DATA-
37	GND	Power	0V	Ground
38	USB_HUBP3_DP	Input/Output	Differential	USB Hub3 DATA+
39	3G_3V3	Power	3.3V	3.3V Power Supply
40	GND	Power	0V	Ground
41	3G_3V3	Power	3.3V	3.3V Power Supply
42	LED_WWAN#	Output	3.3V CMOS	LED Connection
43	GND	Power	0V	Ground
44	LED_WLAN#	Output	3.3V CMOS	LED Connection
45	NC	-	-	No Connection
46	LED_WPAN#	Output	3.3V CMOS	LED Connection
47	NC	-	-	No Connection
48	3G_1V5	Power	1.5V	1.5V Power Supply
49	NC	-	-	No Connection
50	GND	Power	0V	Ground
51	NC	-	-	No Connection
52	3G_3V3	Power	3.3V	3.3V Power Supply

2.6.5 CAN Header

i.MX6 CPU has two CAN interface with up to 1 Mbps speed. CAN1 TXD and RXD signals from i.MX6 CPU are connected to CAN transceiver and the output of transceiver is connected to 3pin header. This header is physically located on the bottom of the board.

Number of Pins - 03

Connector Part Number - 951103-8622-AR

Mating Connector - 950503-6102-AR from 3M

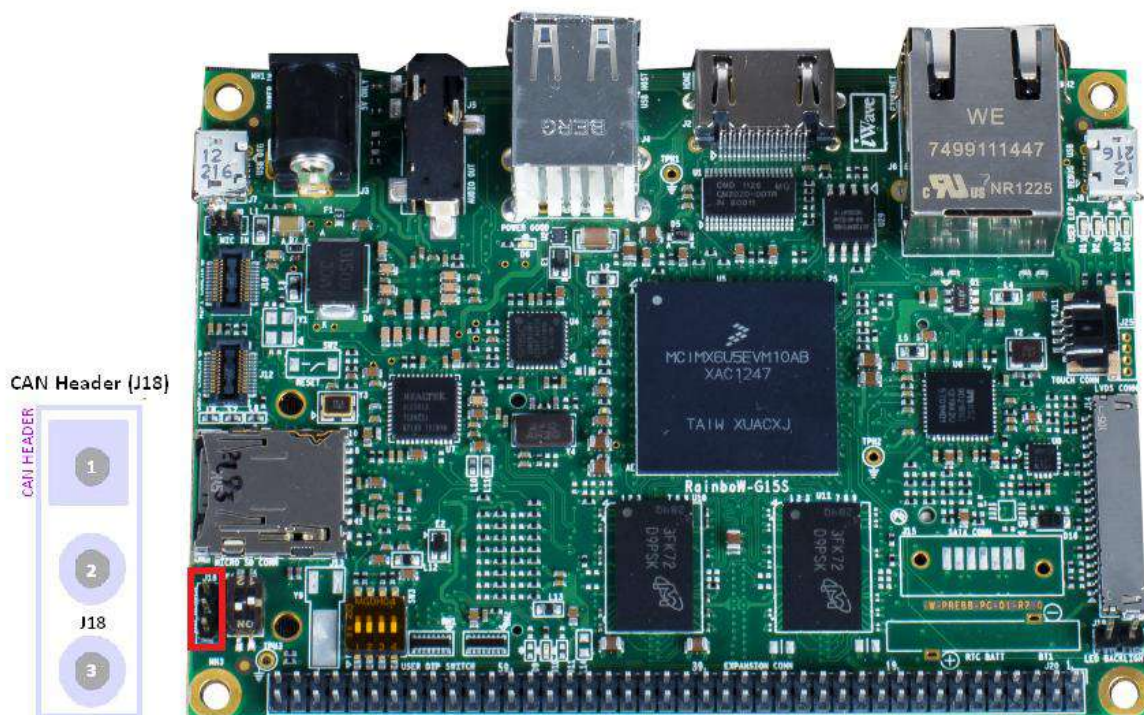


Figure 15: CAN Header

Table 17: CAN Header Pin Out

Pin No	Signal Name	Signal Type	Voltage Level/ Termination	Description
1	GND	Power	0V	Ground
2	CAN0L	Output	CAN Differential	CAN Differential Low Side
3	CAN0H	Output	CAN Differential	CAN Differential High Side

2.7 Debug Features

2.7.1 USB Micro AB Connector for Debug console

i.MX6 Pico ITX – SBC supports debug console port through Micro AB connector. i.MX6 CPU UART2 interface is used for Debug purpose. This is not the full functional UART and supports only Serial TX and RX signals. External UART to USB converter is used to convert the Processor CMOS UART signals into USB signals. This USB signals are connected to a USB Micro AB connector which is physically located on top of the board.

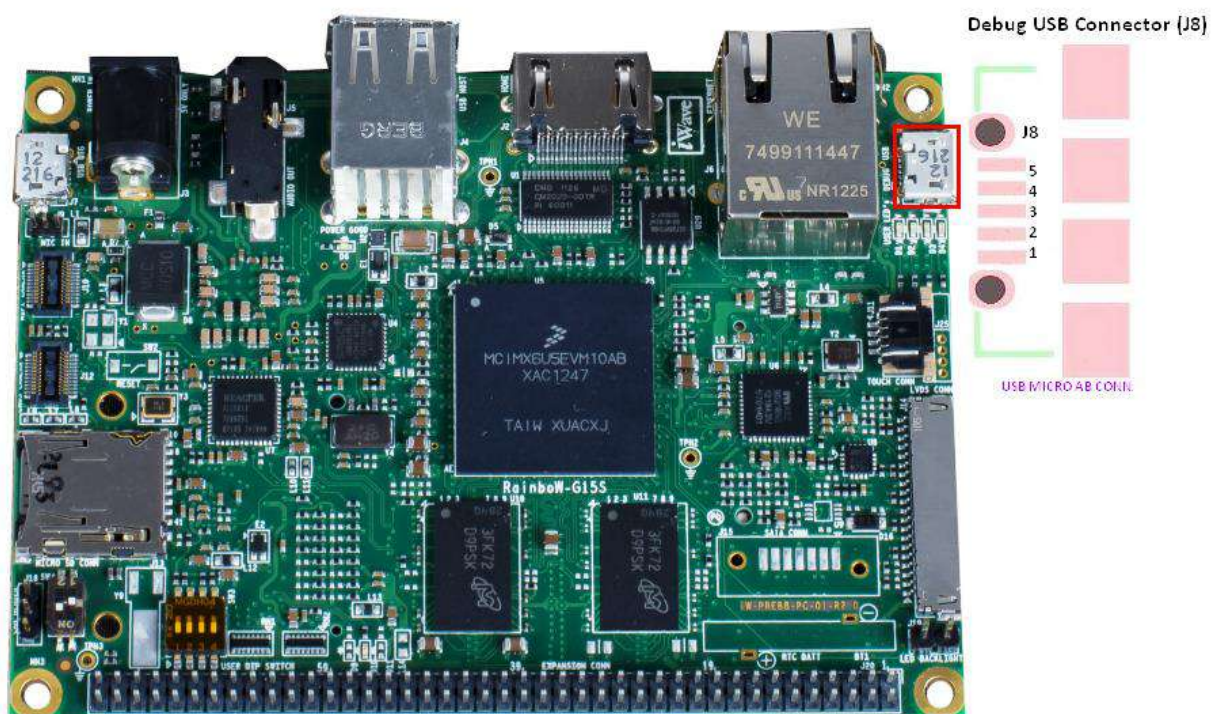


Figure 16: Console Debug USB Micro AB Connector

Table 18: Console Debug USB Micro AB Connector Pin Out

Pin No	Signal Name	Signal Type	Voltage Level/ Termination	Description
1	DEBUG_VBUS	Power	5V	VBUS 5V Power
2	DEBUG_USB_DM	Input/Output	Differential	USB Negative Data
3	DEBUG_USB_DP	Input/Output	Differential	USB Positive Data
4	NC	-	-	USD ID signal
5	GND	Power	0V	Ground

2.7.2 JTAG Connector

A customized 20-pin ARM JTAG connector is available in i.MX6 Pico ITX – SBC for Debug purpose. 3.3V reference power is provided to pin 1 of the connector to allow JTAG tool to automatically configure the logic signals for the right voltage. JTAG connector is physically located on bottom of the board.

Number of Pins - 20

Connector Part Number - GRPB102VWQP-RC

Mating Connector - LPPB102CFFN-RC from Sullins Connector Solutions

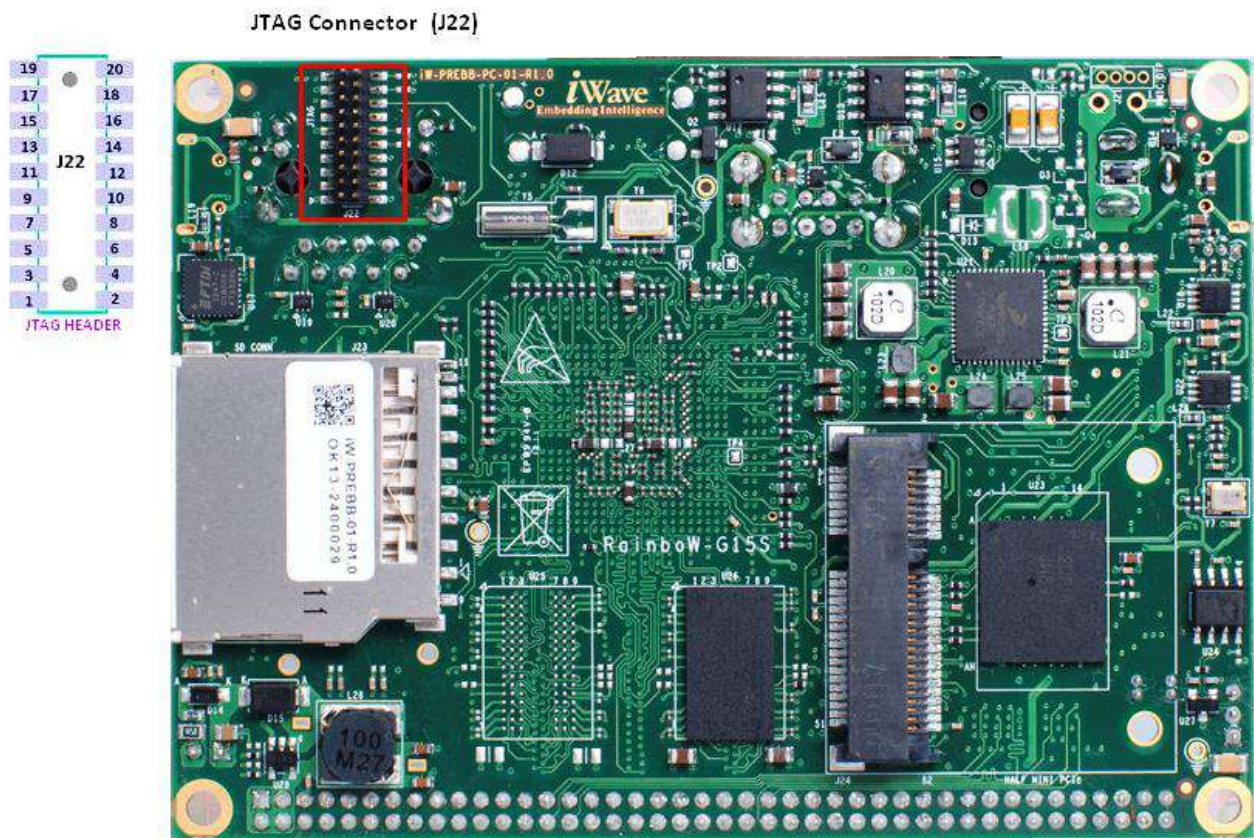


Figure 17: JTAG Connector

Table 19: JTAG Connector Pin Out

Pin No	Signal Name	Signal Type	Voltage Level/ Termination	Description
1	VCC_3V3	Power	3.3V	Supply Voltage
2	VCC_3V3	Power	3.3V	Supply Voltage
3	GND	Power	0V	Ground
4	JTAG_TRSTB	Input	3.3V CMOS	Test Reset Signal
5	GND	Power	0V	Ground
6	JTAG_TDI	Input	3.3V CMOS	Test Data Input
7	GND	Power	0V	Ground
8	JTAG_TMS	Input	3.3V CMOS	Test Mode Select
9	GND	Power	0V	Supply Voltage
10	JTAG_TCK	Input	3.3V CMOS	Test Clock
11	GND	Power	0V	Ground
12	GND	Power	0V	Ground
13	GND	Power	0V	Ground
14	JTAG_TDO	Output	3.3V CMOS	Test Data Output
15	GND	Power	0V	Ground
16	JTAG_RESETB	Input	3.3V CMOS	Reset
17	GND	Power	0V	Ground
18	VCC_3V3	Power	3.3V	Supply Voltage
19	GND	Power	0V	Ground
20	GND	Power	0V	Ground

2.7.3 4bit DIP Switch

i.MX6 Pico ITX – SBC supports 4bit DIP Switch for General Purpose settings. This switch is connected to i.MX6 CPU GPIOs and can be used for any optional setting changes. DIP Switch is physically located at the top of the board.

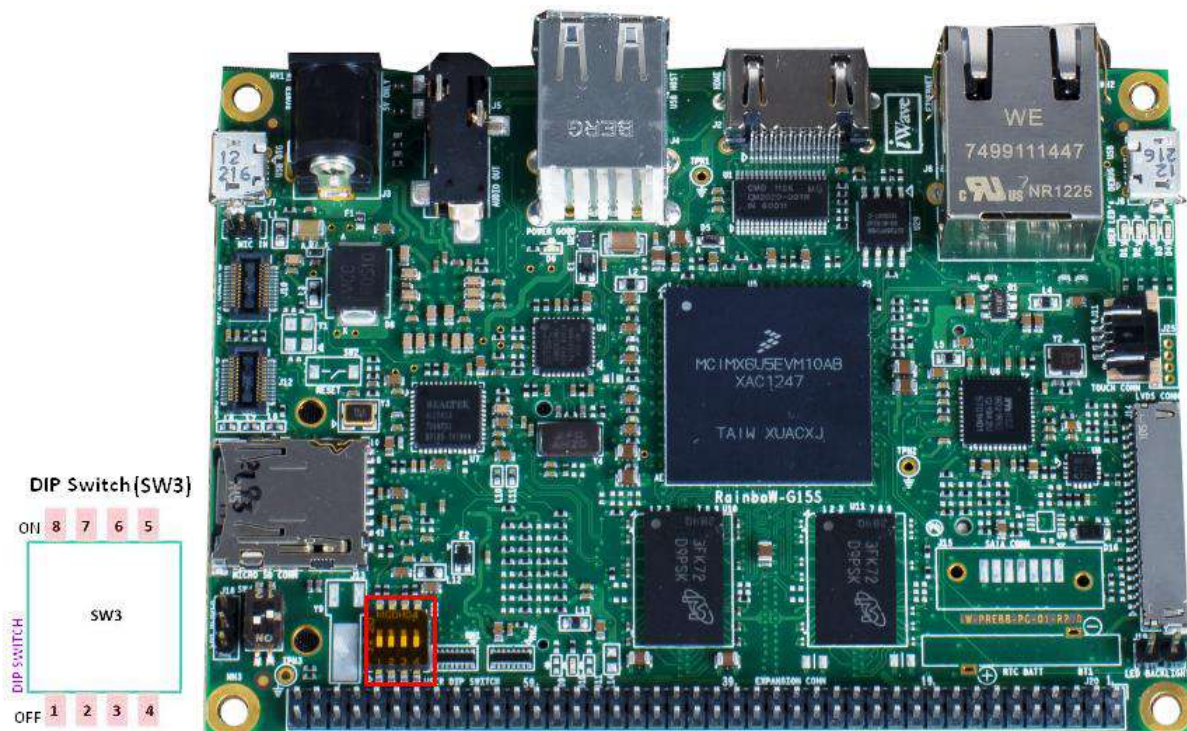


Figure 18: DIP Switch

Table 20: 4bit DIP Switch setting

DIP Switch Bit	Signal Name	Signal Type	Voltage Level/ Termination	Description
Bit 1	GPIO4_24_STAT_PIN1(DI SPO_DAT3)	Input to CPU	3.3V CMOS	On – CPU GPIO Pin will go High Off - CPU GPIO Pin will go Low
Bit 2	GPIO4_25_STAT_PIN2(DI SPO_DAT4)	Input to CPU	3.3V CMOS	
Bit 3	GPIO4_26_STAT_PIN3(DI SPO_DAT5)	Input to CPU	3.3V CMOS	
Bit 4	GPIO4_27_STAT_PIN4(DI SPO_DAT6)	Input to CPU	3.3V CMOS	

2.7.4 Status Indication LEDs

i.MX6 Pico ITX – SBC supports 4 status indication LEDs for status indication purpose. These LEDs are physically located on the top of the board for indication purpose.

Table 21: Status LED setting

LED	Signal Name	Signal Type	Voltage Level/ Termination	Description	Image
D4	GPIO5_12_STA T_LED1(DISPO _DAT18)	Active Low LED Enable	3.3V CMOS	Green colour Status LED1	
D3	GPIO5_13_STA T_LED2(DISPO _DAT19)	Active Low LED Enable	3.3V CMOS	Green colour Status LED2	
D2	GPIO5_14_STA T_LED3(DISPO _DAT20)	Active Low LED Enable	3.3V CMOS	Green colour Status LED3	
D1	GPIO5_15_STA T_LED4(DISPO _DAT21)	Active Low LED Enable	3.3V CMOS	Green colour Status LED4	

2.8 Expansion Connector

i.MX6 Pico ITX –SBC supports one 84pin expansion connector for add-on features. This connector is physically located at the top of the board. Below mentioned interfaces are supported in Expansion Connector.

- LVDS1 Interface
- MIPI DSI Interface
- CSI0 Camera Interface
- CAN Interface
- SPI Interface
- UART Interface x 3ports
- I2C Interface x 3ports
- GPIOs
- MLB 6pin & 3 pin Signals

Note: *MLB is not supported in i.MX6 Dual-Lite & Solo CPU.*

Number of Pins - 84

Connector Part Number - TMM-142-01-T-D (Single 84 pin connector is used)

Mating Connector - M22-3022100 from Harwin Inc (Use single of this 84 Pin connector)

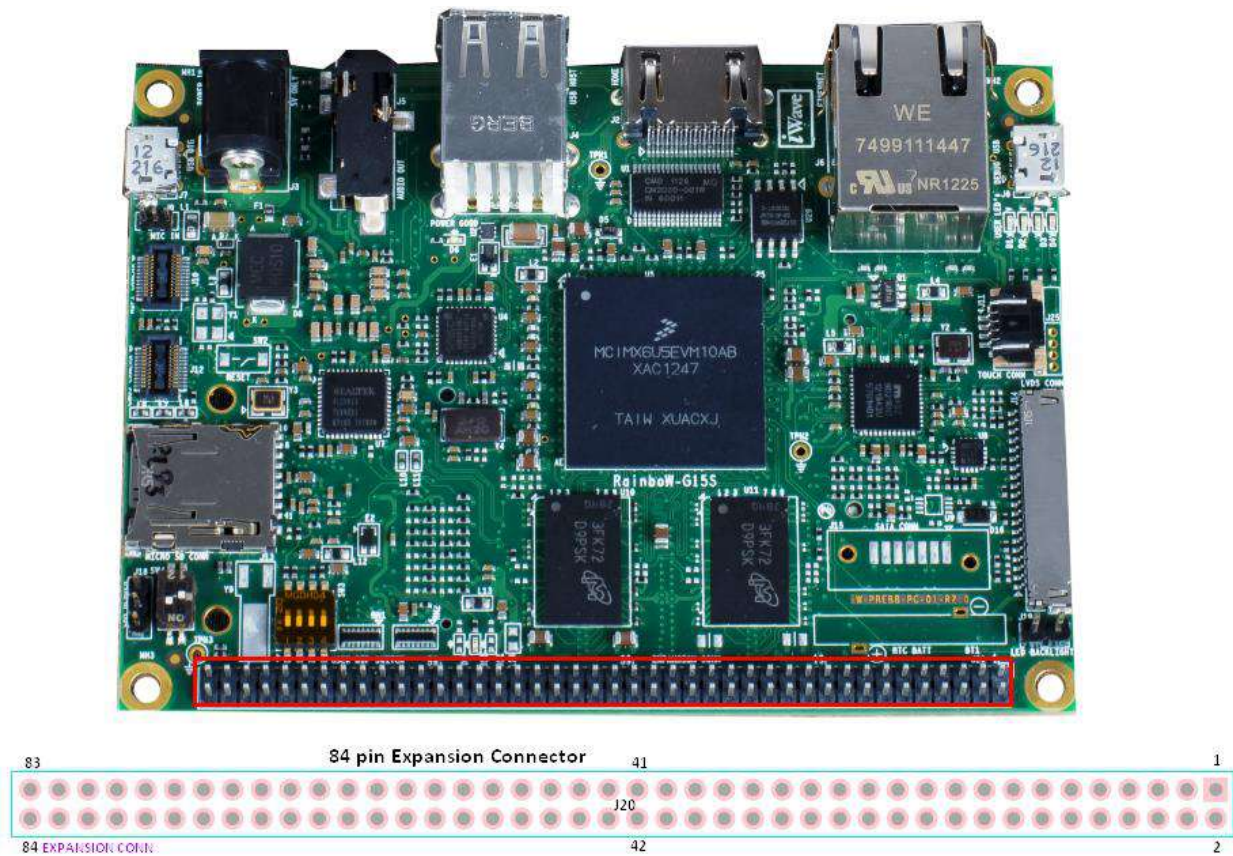


Figure 19: Expansion Connector

Table 22: Expansion Connector Pin Out

Pin No	Signal Name	Signal Type	Voltage Level/ Termination	Description
1	VCC_5V	Power	5V	5V Supply Voltage
2	VCC_5V	Power	5V	5V Supply Voltage
3	VCC_5V	Power	5V	5V Supply Voltage
4	VCC_5V	Power	5V	5V Supply Voltage
5	GND	Power	0V	Ground
6	GND	Power	0V	Ground
7	VCC_3V15	Power	3.15V	3.15Voutput Supply Voltage
8	UART1_RTS(EIM_D20)	Input	3.3V CMOS	UART1 RTS input
9	I2C1_SDA(EIM_D28)	Input/ Output	3.3V CMOS/ 4.7K Pull-up	I2C1 Data signal
10	UART1_CTS(EIM_D19)	Output	3.3V CMOS	UART1 CTS output

11	UART3_RXD(EIM_D25)	Input	3.3V CMOS	UART3 Receive data line
12	UART3_TXD(EIM_D24)	Output	3.3V CMOS	UART3 Transmit data line
13	GPIO4_29(DISP0_DAT8)	Input/ Output	3.3V CMOS	General Purpose Input Output
14	GPIO1_11_HDA_RST(SD2_CMD)	Output	3.3V CMOS	SBC Reset Output
15	GND	Power	0V	Ground
16	GND	Power	0V	Ground
17	GPIO4_30(DISP0_DAT9)	Input/ Output	3.3V CMOS	General Purpose Input Output
18	CAN2_TX(KEY_COL4)	Input	3.3V CMOS	CAN Channel2 Transmit line
19	KEY_ROW1	Output	3.3V CMOS	Keypad Row1
20	KEY_COL1	Input	3.3V CMOS	Keypad Column1
21	UART4_RXD(KEY_ROW0)	Input	3.3V CMOS	UART4 Receive data line
22	UART4_TXD(KEY_COL0)	Output	3.3V CMOS	UART4 Transmit data line
23	CSIO_PIXCLK	Input	3.3V CMOS	Camera0 PIXCLK
24	I2C1_SCL(EIM_D21)	Output	3.3V CMOS/ 4.7K Pull-up	I2C1 Clock signal
25	GND	Power	0V	Ground
26	GND	Power	0V	Ground
27	MLBSIG(GPIO_6)	Output	3.3V CMOS	Media Local Bus single ended signal line
28	MLBDAT(GPIO_2)	Input/ Output	3.3V CMOS	Media Local Bus single ended data line
29	CSIO_DATA_EN	Input	3.3V CMOS	Camera0 data enable
30	CSIO_DAT13	Input	3.3V CMOS	Camera0 data bit1
31	GND	Power	0V	Ground
32	CAN2_RX(KEY_ROW4)	Output	3.3V CMOS	CAN Channel2 Receive line
33	CLKO(GPIO_0)	Output	3.3V CMOS	General purpose configurable clock from CPU
34	UART1_TXD(SD3_DAT7)	Output	3.3V CMOS	UART1 Transmit data line
35	UART1_RXD(SD3_DAT6)	Input	3.3V CMOS	UART1 Receive data line
36	CSIO_HSYNC	Input	3.3V CMOS	Camera0 HSYNC
37	I2C2_SCL(KEY_COL3)	Output	3.3V CMOS/ 4.7K Pull-up	I2C2 clock signal
38	I2C2_SDA(KEY_ROW3)	Input/ Output	3.3V CMOS/ 4.7K Pull-up	I2C2 Data signal

39	GND	Power	0V	Ground
40	ESAI_HCKR(GPIO_3)	Output	3.3V CMOS	Media Local Bus single ended clock line
41	eCSPI2_MISO(CSI0_DAT10)	Input	3.3V CMOS	SPI Master In Slave Out
42	CSI0_DAT12	Input	3.3V CMOS	Camera0 data bit0
43	CSI0_VSYNC	Input	3.3V CMOS	Camera0 VSYNC
44	CSI0_DAT14	Input	3.3V CMOS	Camera0 data bit2
45	eCSPI2_MOSI(CSI0_DAT9)	Output	3.3V CMOS	SPI Master Out Slave In
46	eCSPI2_SS0(CSI0_DAT11)	Output	3.3V CMOS	SPI chip select 0
47	CSI0_DAT17	Input	3.3V CMOS	Camera0 data bit5
48	CSI0_DAT16	Input	3.3V CMOS	Camera0 data bit4
49	CSI0_DAT15	Input	3.3V CMOS	Camera0 data bit3
50	CSI0_DAT19	Input	3.3V CMOS	Camera0 data bit7
51	eCSPI2_SCLK(CSI0_DAT8)	Output	3.3V CMOS	SPI clock output
52	CSI0_DAT18	Input	3.3V CMOS	Camera0 data bit6
53	GND	Power	0V	Ground
54	GND	Power	0V	Ground
55	DSI_CLK0P	Output	Differential	MIPI DSI differential clock positive
56	DSI_CLK0M	Output	Differential	MIPI DSI differential clock negative
57	DSI_D1P	Output	Differential	MIPI DSI differential data1 positive
58	DSI_D1M	Output	Differential	MIPI DSI differential data1 negative
59	DSI_D0P	Output	Differential	MIPI DSI differential data0 positive
60	DSI_D0M	Output	Differential	MIPI DSI differential data0negative
61	GND	Power	0V	Ground
62	GND	Power	0V	Ground
63	CLK2_p	Output	Differential	General purpose high speed differential clock2 positive from CPU.
64	CLK2_n	Output	Differential	General purpose high speed differential clock2 negative from CPU.

65	GND	Power	0V	Ground
66	GND	Power	0V	Ground
67	LVDS1_TX3_N	Output	LVDS	LVDS secondary channel differential pair3 negative
68	LVDS1_TX3_P	Output	LVDS	LVDS secondary channel differential pair3 positive
69	LVDS1_TX2_N	Output	LVDS	LVDS secondary channel differential pair2 negative
70	LVDS1_TX2_P	Output	LVDS	LVDS secondary channel differential pair2positive
71	LVDS1_TX1_P	Output	LVDS	LVDS secondary channel differential pair1positive
72	LVDS1_TX1_N	Output	LVDS	LVDS secondary channel differential pair1negative
73	LVDS1_CLK_N	Output	LVDS	LVDS secondary channel differential clock negative.
74	LVDS1_CLK_P	Output	LVDS	LVDS secondary channel differential clock positive.
75	LVDS1_TX0_P	Output	LVDS	LVDS secondary channel differential pair0 positive
76	LVDS1_TX0_N	Output	LVDS	LVDS secondary channel differential pair0 negative
77	GND	Power	0V	Ground
78	GND	Power	0V	Ground
79	MLB_SP	Output	LVDS	Media Local Bus differential signal line positive
80	MLB_SN	Output	LVDS	Media Local Bus differential signal line negative
81	MLB_DP	Input/ Output	LVDS	Media Local Bus differential data line positive
82	MLB_DN	Input/ Output	LVDS	Media Local Bus differential data line negative
83	MLB_CP	Output	LVDS	Media Local Bus differential clock line positive
84	MLB_CN	Output	LVDS	Media Local Bus differential clock line negative

2.9 Optional Features

2.9.1 RTC Controller with Coin cell

i.MX6 Pico ITX – SBC optionally supports on-board RTC Controller. It has feature of automatic switch over to back up supply from main supply. Its supplied with external crystal oscillator frequency of 32.768Khz. It uses I2C1 lines to interface with the i.MX6 CPU. Also it supports on-board 3V backup Coin cell battery for RTC. This coin cell battery is located at the top of the board and RTC Controller is located at the bottom of the board. This is the optional feature and not populated by default.

The below table provides the RTC Controller & Coin cell BOM which can be used to mount the RTC Controller component in i.MX6 Pico ITX SBC and use it.

Table 23: RTC Controller - BOM

Sl. No.	Part Description	Part Number	Identifier	Package	Quantity
1	IC SRL REAL TIME CLOCK 8SOIC	BQ32000DR	U31	8-SOIC	1
2	CRYSTAL 32.768 KHZ 12.5PF SMD	CMR200T-32.768KDZF-UT	Y9	2Pin,SMD	1
3	3V, 225mAh,BATT LITH COIN CELL PC PINS	CR-2032/VCN	BT1	2Pin Vertical,TH	1
4	RES 0.0 OHM 1/16W 0402 SMD	RC0402JR-070RL	R329,R330	0402	2
5	RES 10.0K OHM 1/16W 5%	RC0402JR-0710KL	R328	0402	1
6	CAP CERAMIC .1UF 10V X5R	CC0402KRX5R6BB104	C422,C423, C418,C424	0402	4
7	CAP THIN FILM 12PF 10V 0402	0402ZJ120GBWTR	C420,C421	0402	2

Note: For i.MX6 Pico ITX SBC Silkscreen identifier details, refer APPENDIX I

2.9.2 SATA Connector

i.MX6 Quad/Dual CPU has one SATA II interface with up to 3.0 Gbps. This can be used to interface with different Hard disk drives. Also this can be used as optional boot source if required. SATA signals from i.MX6 CPU is connected to standard 7pin SATA connector. 7pin SATA connector is physically located on top of the board. This is the optional feature and not populated by default.

Note: SATA is not supported in i.MX6 Dual-Lite & Solo CPU.

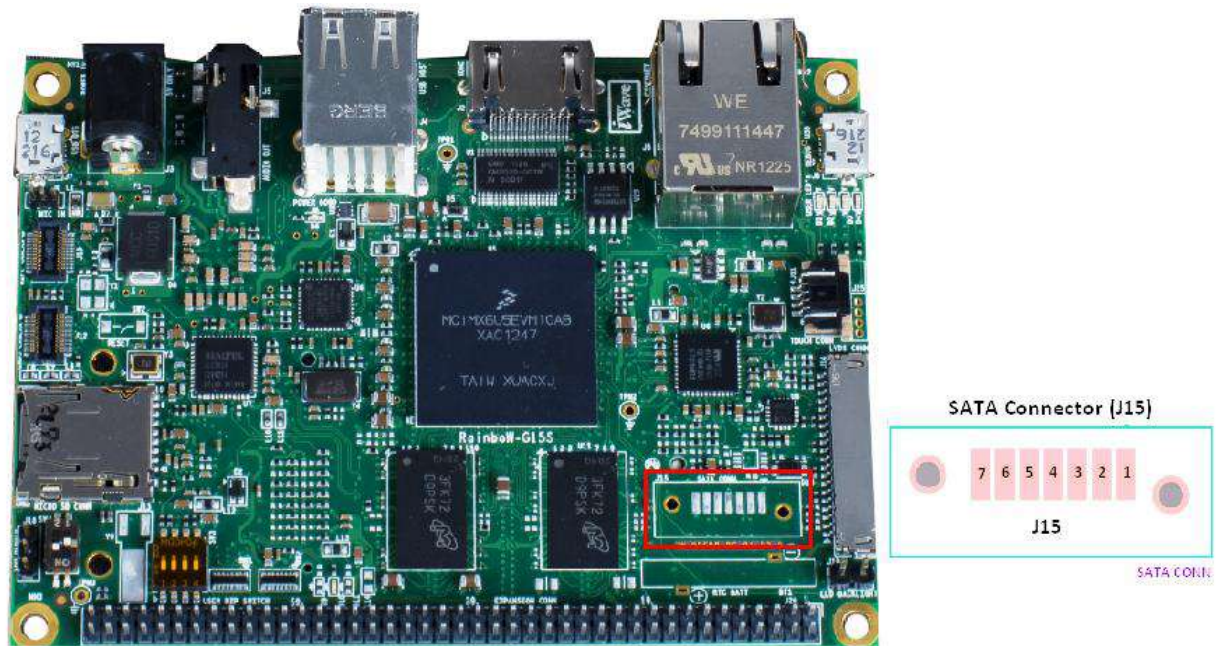


Figure 20: SATA0 22pin Connector

Table 24: SATA Connector Pin Out

Pin No	Signal Name	Signal Type	Voltage Level/ Termination	Description
1	GND	Power	0V	Ground
2	SATA_TXP	Output	Differential/ 0.01uF AC Coupling (C386) & 100E parallel termination between Pair	Serial ATA Transmit Output differential pair
3	SATA_TXM	Output	Differential/ 0.01uF AC Coupling (C387) & 100E parallel termination between Pair	
4	GND	Power	0V	Ground

5	SATA_RXM	Input	Differential/ 0.01uF AC Coupling (C388) & 100E parallel termination between Pair	Serial ATA Receive Input differential pair
6	SATA_RXP	Input	Differential/ 0.01uF AC Coupling (C399) & 100E parallel termination between Pair	
7	GND	Power	0V	Ground

The below table provides the SATA circuit BOM which can be used to mount the SATA components in i.MX6 Pico ITX SBC.

Table 25: SATA Connector - BOM

Sl. No.	Part Description	Part Number	Identifier	Package	Quantity
1	CAP 0.01uF 16V CERAMIC X7R 0402	CC0402KRX7R7BB103	C386,C387, C388,C389	0402	4
2	RES 100 OHM 1/10W 5% 0402 SMD	RC0402JR-07100RL	R306,R307	0402	2
3	CONN HEADER 7POS VERT SMD	0678005001(from Molex)	J15	7Pin SMD	1

Note: For i.MX6 Pico ITX SBC Silkscreen identifier details, refer APPENDIX I

3. Electrical specification

3.1 Power Input Requirement

i.MX6 Pico ITX – SBC supports 5V, 2A Power Jack (J3) for external power supply input and uses on board PMIC regulators for internal power management. Also 2-pin power input connector (J1) option provided for optional power input. Either Power Jack (J3) or Power connector (J1) can be mounted on the board. From the Power input, the 5V supply is directly sent to a 3A fuse (F1) for over current protection. The power input circuit is shown in below Figure.

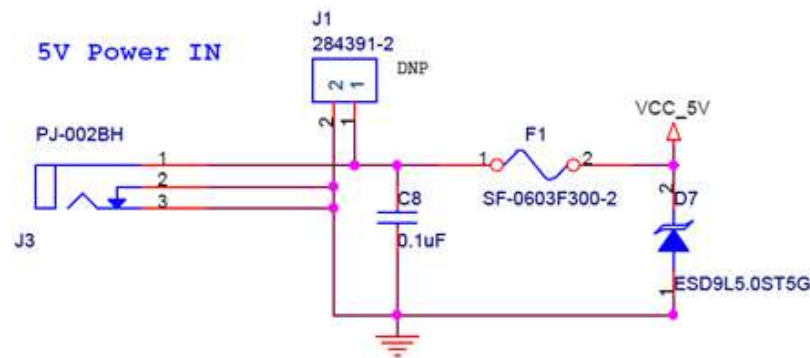


Figure 21: Power In Circuit

3.1.1 Power Jack

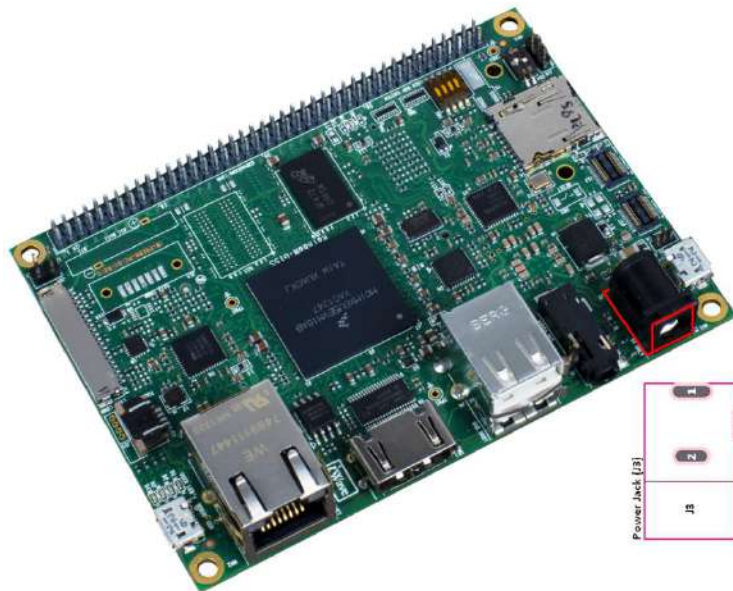


Figure 22: Power Jack

Table 26: Power Jack Pin Out

Sl. No.	Power Rail	Min (V)	Typical (V)	Max(V)	Max Input Ripple
1	5V	4.75V	5V	5.25V	±50mV
2	Ground	NC	NC	NC	NC
3	Ground	NC	NC	NC	NC

Number of Pins - 3
Connector Part Number - PJ -002BH
Mating Connector Diameter - 2.5mm ID, 5.5mm OD

3.1.2 2 Pin Power connector

Power header(J1-Optional)

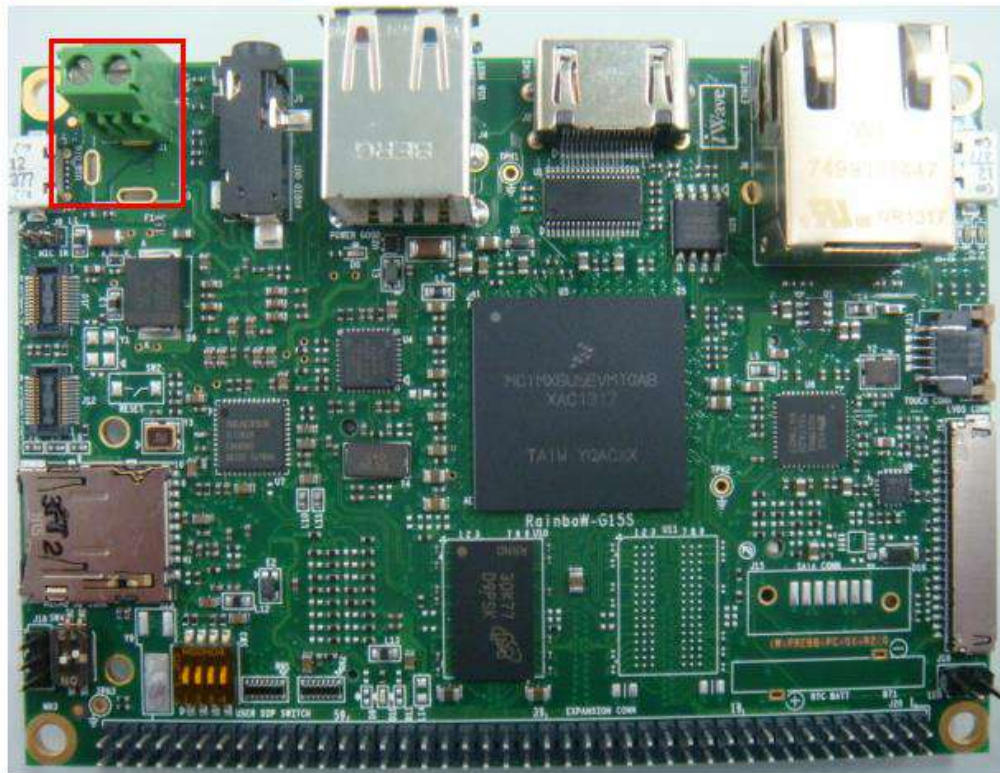


Figure 23: 2Pin Power Connector

Table 27: 2-Pin Power Connector Pin Out (Optional)

Sl. No.	Power Rail	Min (V)	Typical (V)	Max(V)	Max Input Ripple
1	5V	4.75V	5V	5.25V	±50mV
2	Ground	NC	NC	NC	NC

Number of Pins - 2
Connector Part Number - 284391-2
Mating Connector Details - 2Pos Horizontal, 3.5mm Pitch

3.1.3 Power Consumption

Table 28: Power Consumption¹

Task/Status	Power Rail	Current Drawn/Power Consumption
Run Mode Power Consumption		
MP3 audio playback on AUDMUX4	VCC	1.41/7.05W
1080p video playback on LVDS0 (WVGA LCD)	VCC	2.1/10.5W
1080p video playback on HDMI (1080p Monitor)	VCC	2.4/12W
OpenGL graphics application on HDMI	VCC	2.57/12.85W
Dhrystone benchmark application	VCC	2.08/10.4W
Typical Maximum Power: - MP3 audio playback. 1080p video playback on HDMI. - VGA video playback & OpenGL graphics application on LVDS0 - Gigabit Ethernet ping. - USB to Micro SD file transfer. - Dhrystone benchmark application	VCC	3/15W
Low Power Mode Power Consumption		
Deep Sleep Mode	VCC	1.14A/5.7W ²
RTC power when no VCC supply is provided	VCC_RTC	275uA ³

¹ Power consumption measurements have been done in iWave's i.MX6 Quad CPU based (iW-G15S-PI04-3D001G-E004G-LEN) Pico ITX SBC board running iWave's Linux3.10 BSP (iW-PREBB-RN-01-R2.0-REL1.0-Linux3.10).

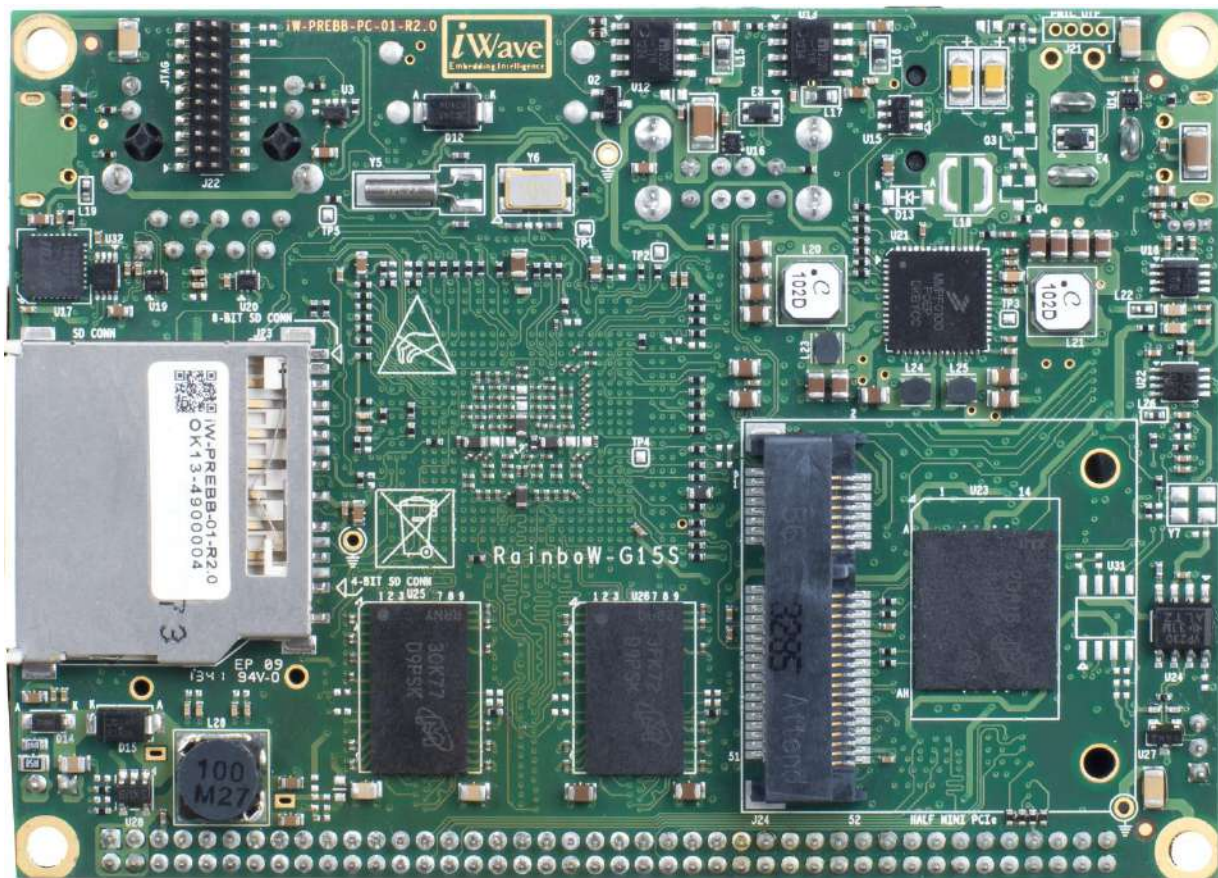
² Only i.MX6 CPU related power management is implemented in the BSP for low power mode.

³ i.MX6 RTC controller draws more power from VCC_RTC coin cell power input and so could drain the coin cell faster.

4. Board Numbering & Revision History

4.1 i.MX6 Pico ITX SBC Numbering

In all i.MX6 Pico ITX SBC, unique number is pasted as a label with Barcode readable format on the bottom side of SBC as shown below.



4.2 i.MX6 Pico ITX SBC Revision History

Table 29: i.MX6 Pico ITX SBC Revision History

Sl. No.	Change Description	i.MX6 Proto SBC	i.MX6 Production SBC
PCB Changes			
1	Boot Mode Setting	For boot mode setting, two Jumper is provided	For boot mode setting, 2bit DIP Switch is provided
2	Boot Media setting	Hardware is fixed to boot Bootloader from on-board eMMC Flash <i>Note: SPI Flash interface is not supported here</i>	Hardware is fixed to boot Bootloader from on-board SPI Flash
3	Resistive touch controller Change	MAX11801ETC+ Touch controller is supported	STMPE811 Touch controller is supported
4	84 Pin Expansion Connector part change	Two 40pin connector (M22-2521005) is used for expansion connector	Single 84pin connector (TMM-142-01-T-D) is used for expansion connector.

5. Mechanical Specification

i.MX6 Pico ITX – SBC is based on standard Pico ITX form factor which is $100 \times 72 \times 17.2$ mm (3.94×2.835 0.68 in) as shown below.

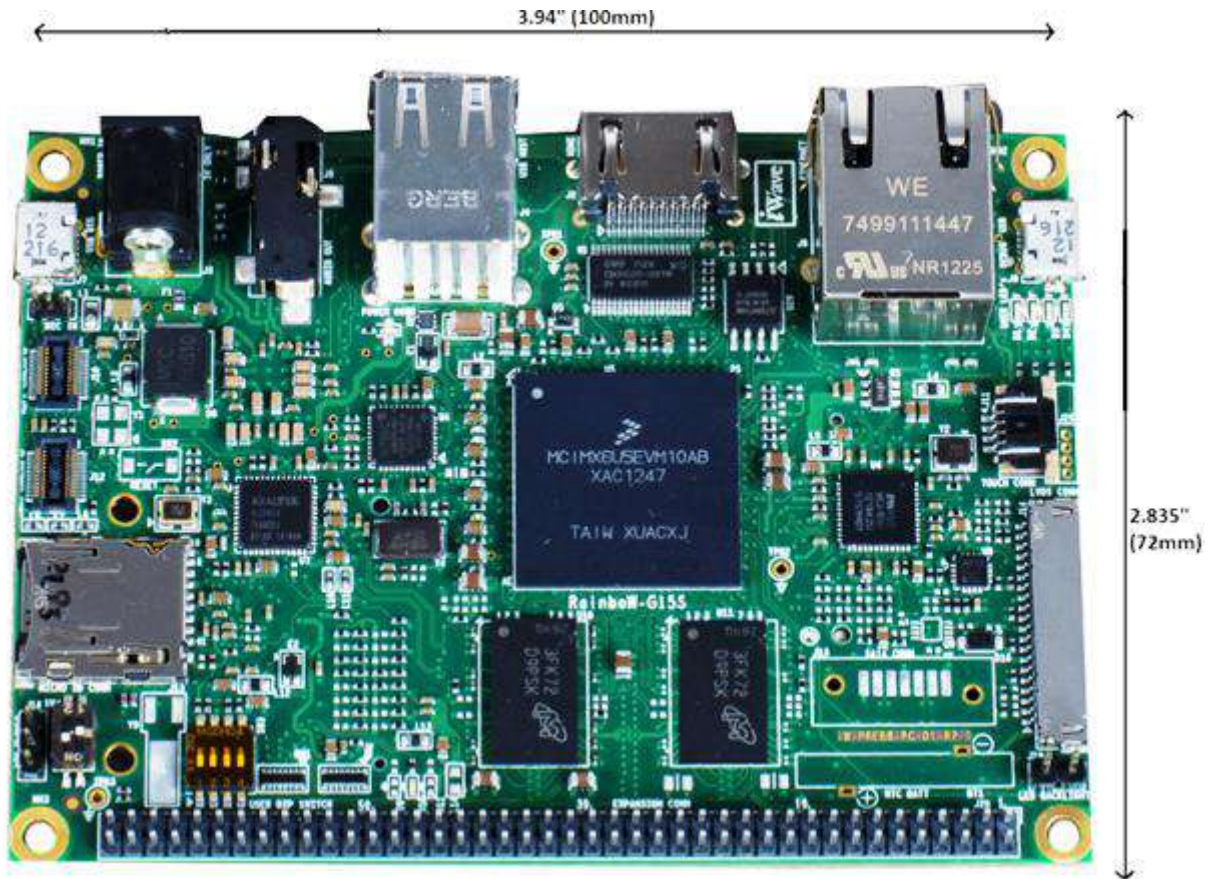


Figure 24: i.MX6 Pico ITX – SBC PCB Dimension

Physical placement dimension of each connector in i.MX6 Pico-ITX SBC is shown in the below Figures.

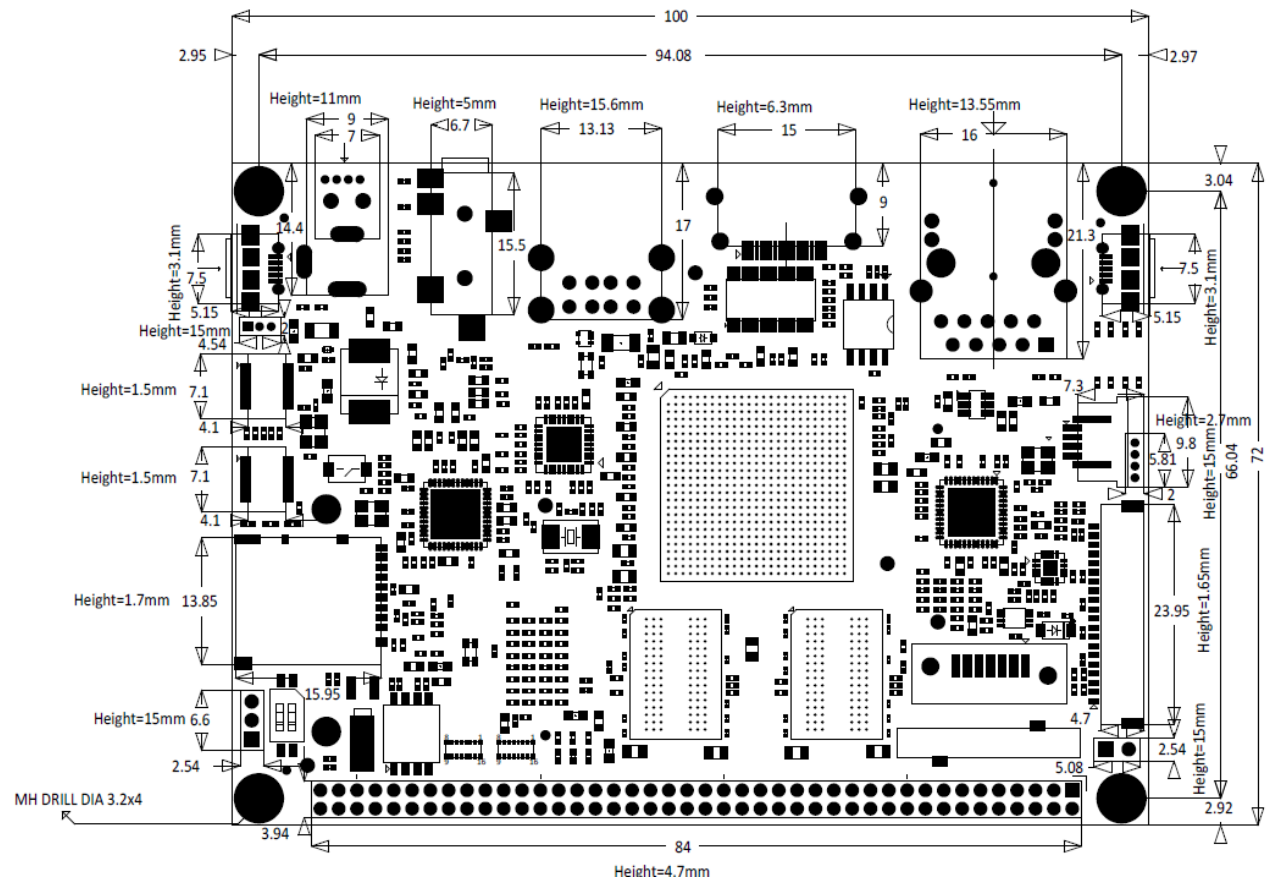


Figure 25: i.MX6 Pico ITX – SBC PCB Dimension Top Side

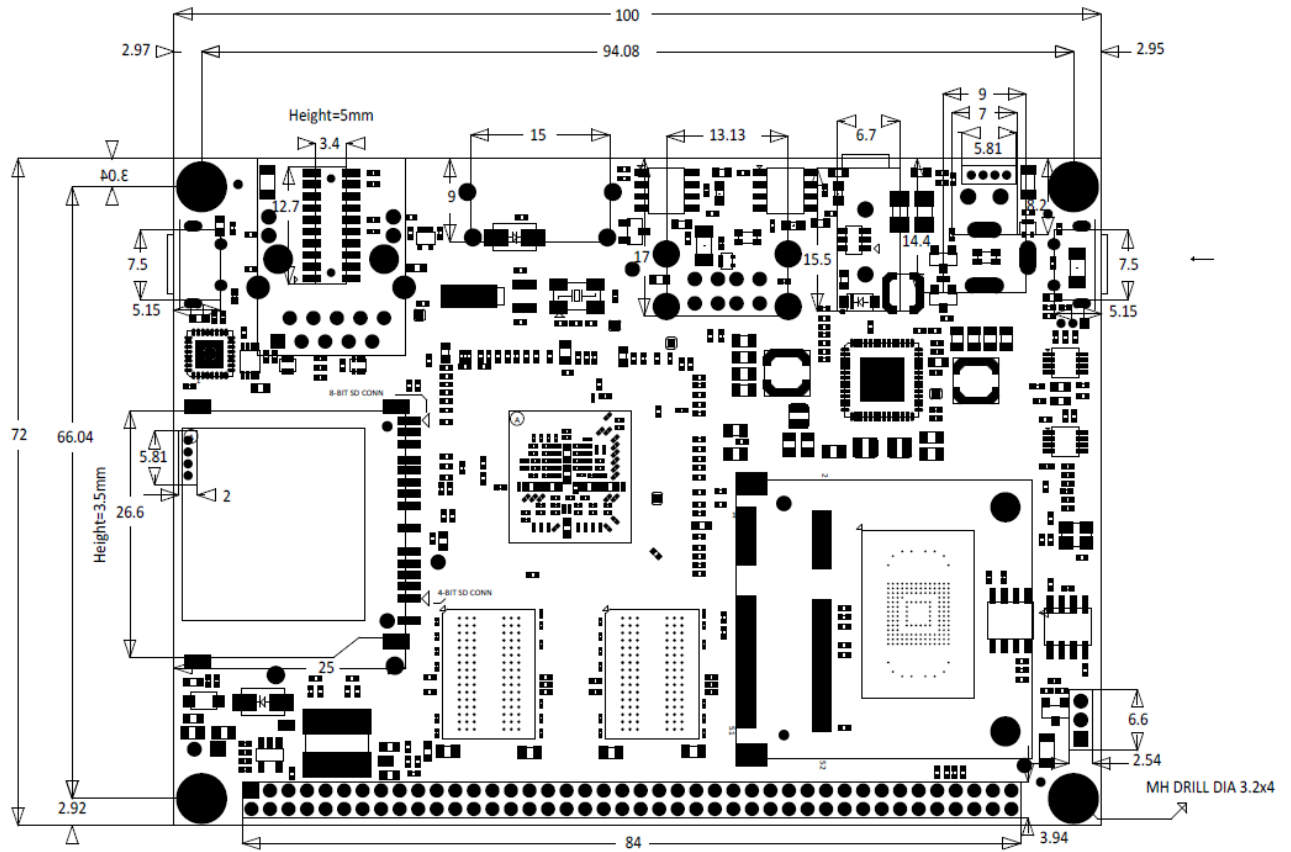


Figure 26: .MX6 Pico ITX – SBC PCB Dimension Bottom Side

6. APPENDIX I

6.1 i.MX6 Pico ITX-SBCSilk Screen

i.MX6 Pico ITX-SBC silkscreen top view and bottom view with Optional Feature's Identifier highlighted are shown in the below Figures. This will be useful while mounting the Optional Features in i.MX6 Pico ITX-SBC.

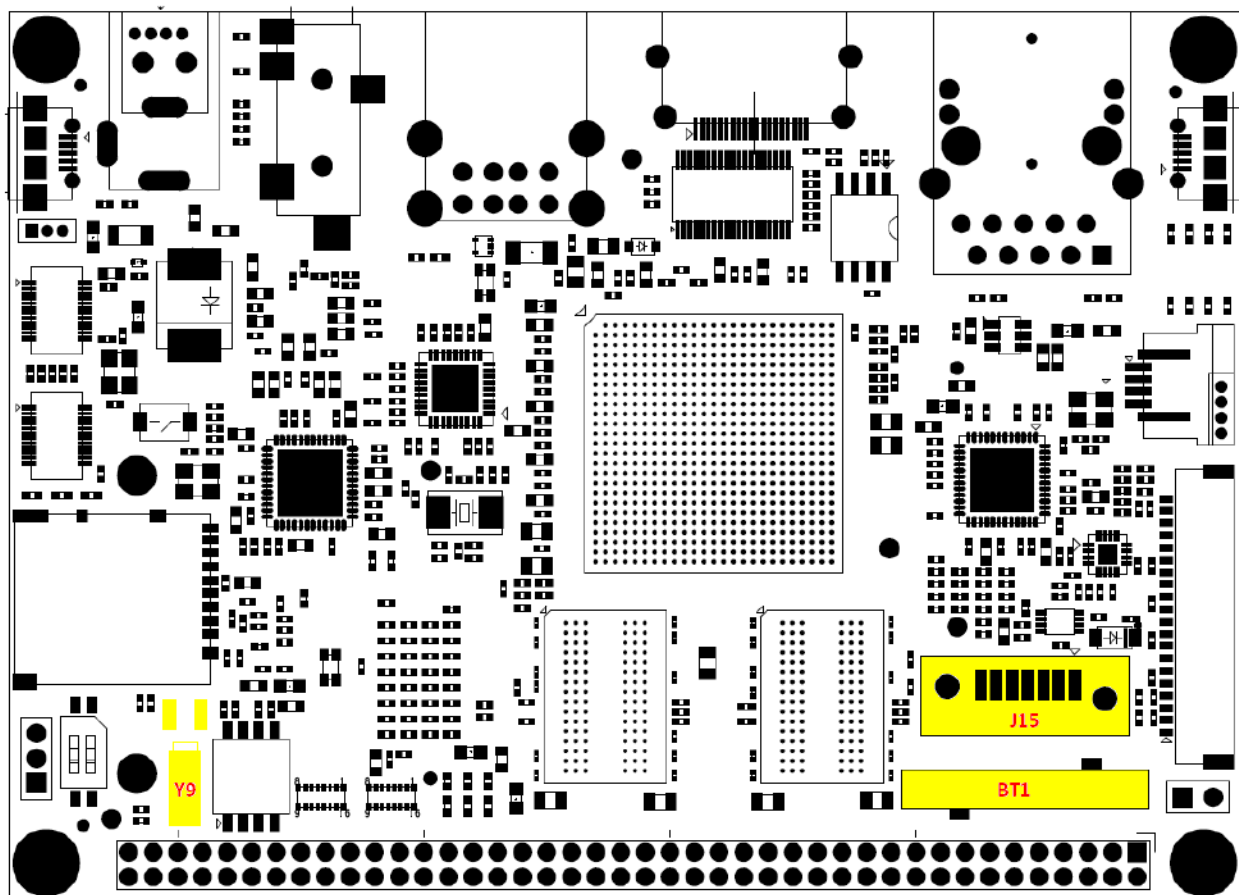


Figure 27: Silk Screen Top View

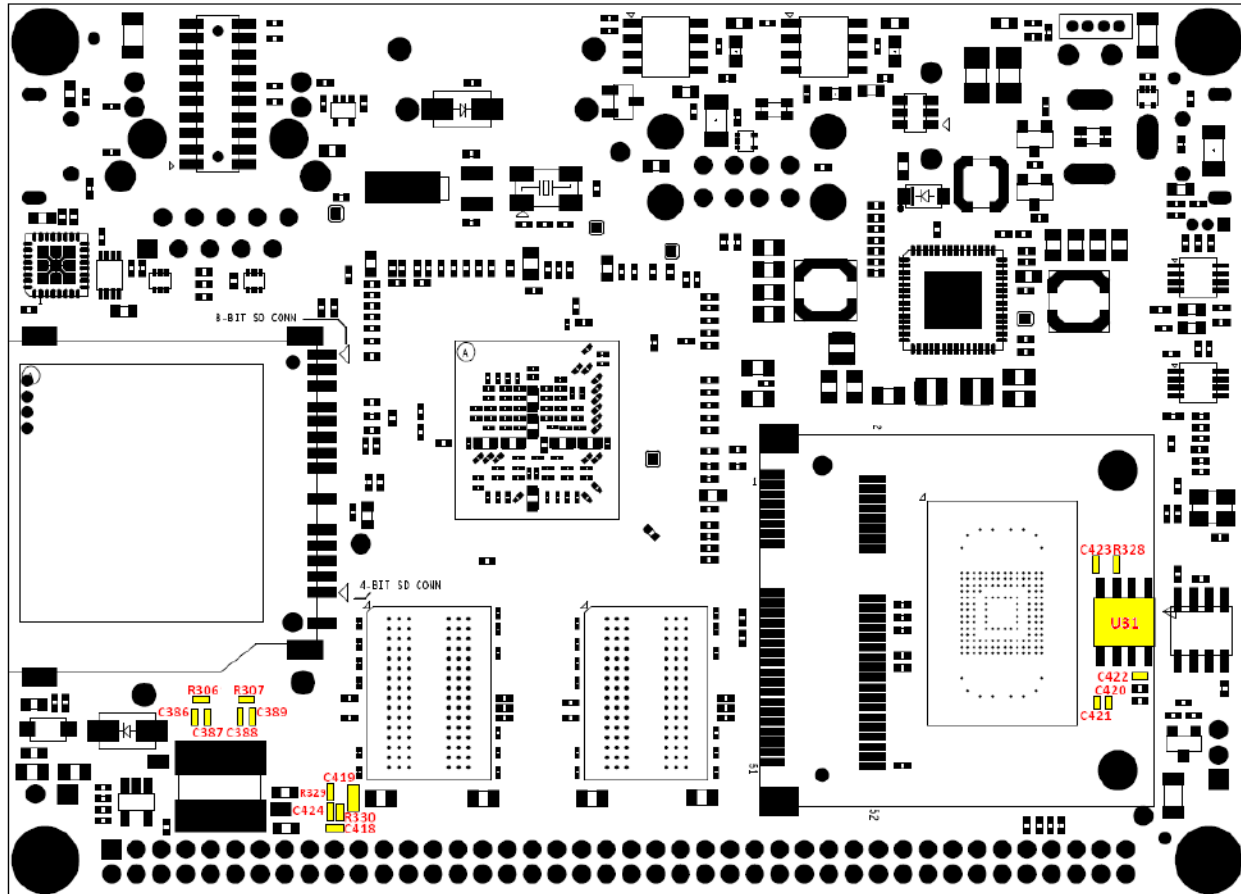


Figure 28: Silk Screen Bottom View