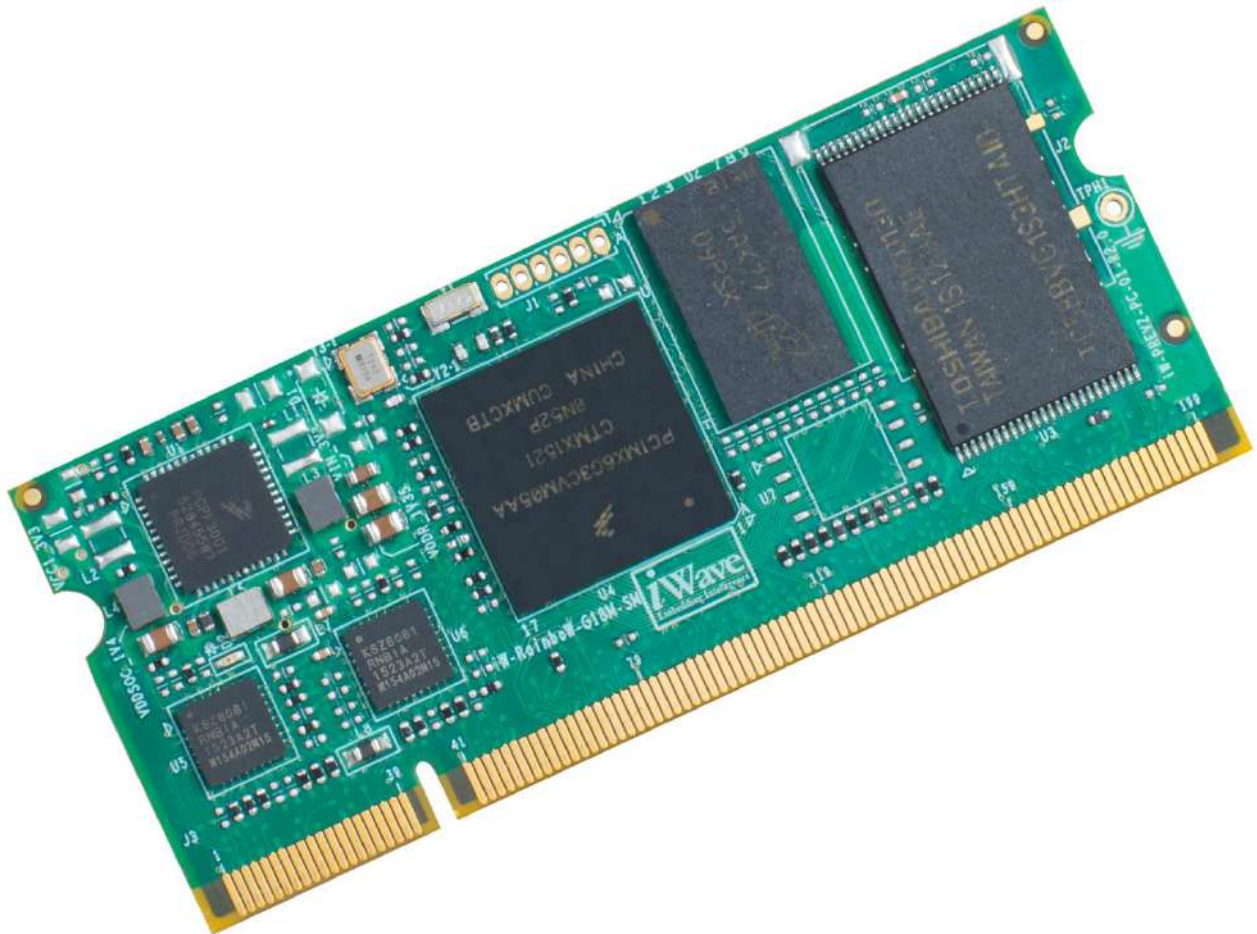


iW-RainboW-G18M

i.MX6UL/i.MX6ULL SODIMM SOM

Hardware User Guide



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1.2	21 st June 2017	- i.MX6ULL support is added throughout the document. - Section 2.6.12 is updated with Important Note. - Pins 47, 68, 73, 86, 133, 134 & 136 details are updated in Table 5. - CPU Pad Name and ALT0 pin details are updated in Table 7 for pins 62, 63, 66, 70, 93, 104, 110 & 120. - Orderable Product Part Numbers are updated in Table 12. - Non substantive changes throughout the document.

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Table of Contents

1. INTRODUCTION	7
1.1 Purpose	7
1.2 SODIMM SOM Overview	7
1.3 List of Acronyms	7
1.4 Terminology Description	9
1.5 References	9
1.6 Important Note	10
2. ARCHITECTURE AND DESIGN	11
2.1 i.MX6UL/i.MX6ULL SODIMM SOM Block Diagram	11
2.2 i.MX6UL/i.MX6ULL SODIMM SOM Features	12
2.3 i.MX6UL/i.MX6ULL CPU	14
2.4 PMIC	16
2.5 Memory	16
2.5.1 DDR3L SDRAM	16
2.5.2 NAND Flash	16
2.6 SODIMM PCB Edge Connector	17
2.6.1 UART Interface	18
2.6.2 CAN Interface	18
2.6.3 SD Interface	18
2.6.4 Parallel RGB Display Interface	18
2.6.5 Parallel Camera Interface	19
2.6.6 I2S Audio Interface	19
2.6.7 JTAG Interface	19
2.6.8 USB 2.0 OTG Interface	20
2.6.9 Dual 10/100Mbps Ethernet	20
2.6.10 I2C Interface	21
2.6.11 PWM Interface	21
2.6.12 Tamper Interface	21
2.6.13 GPIO Interface	21
2.6.14 General Purpose Clock	22
2.6.15 Boot Mode Signals	22
2.6.16 Power Input	23
2.6.17 Reset Signal	23
2.6.18 Power Control Signal	23
2.7 Optional Features	36
2.7.1 eMMC Flash	36
2.7.2 Micro SD Slot	36
2.7.3 QSPI Flash	36
2.7.4 PMIC OTP Header	37
2.8 i.MX6UL/i.MX6ULL Pin Multiplexing on SODIMM Edge	38

3. TECHNICAL SPECIFICATION.....	45
3.1 Electrical Characteristics	45
3.1.1 <i>Power Input Requirement</i>	45
3.1.2 <i>Power Input Sequencing</i>	46
3.1.3 <i>Power Consumption</i>	47
3.2 Environmental Characteristics	48
3.2.1 <i>Environmental Specification</i>	48
3.2.2 <i>RoHS Compliance</i>	48
3.2.3 <i>Electrostatic Discharge</i>	48
3.3 Mechanical Characteristics	49
3.3.1 <i>SODIMM SOM Mechanical Dimensions</i>	49
4. ORDERING INFORMATION	51
5. APPENDIX I.....	53
5.1 Guidelines to insert the SODIMM SOM into Carrier board	53
5.2 Guidelines to remove the SODIMM SOM from Carrier board.....	53
6. APPENDIX II.....	54
6.1 i.MX6UL/i.MX6ULL SODIMM SOM Development Platform.....	54

List of Figures

Figure 1: i.MX6UL/i.MX6ULL SODIMM SOM Block Diagram	11
Figure 2: i.MX6UL Simplified Block Diagram.....	14
Figure 3: i.MX6UL/i.MX6ULL CPU devices comparison	15
Figure 4: SODIMM PCB Edge Connector	17
Figure 5: PMIC OTP Header.....	37
Figure 6: i.MX6UL/i.MX6ULL SODIMM SOM Power Sequence.....	46
Figure 7: Mechanical dimension of SODIMM SOM - Top View	49
Figure 8: Mechanical dimension of SODIMM SOM - Bottom View	49
Figure 9: Mechanical dimension of SODIMM SOM - Side View.....	50
Figure 10: SODIMM SOM Insertion procedure.....	53
Figure 11: SODIMM SOM Removal procedure	53
Figure 12: i.MX6UL/i.MX6ULL SODIMM SOM Development Platform.....	54

List of Tables

Table 1: Acronyms & Abbreviations.....	7
Table 2: Terminology	9
Table 3: Compatible Magnetics	20
Table 4: Boot Mode Pin Settings Truth Table	22
Table 5: 200-Pin PCB Edge Connector Pin Assignment.....	24
Table 6: PMIC OTP Header Pin Assignment	37
Table 7: IOMUX Configuration of i.MX6UL/i.MX6ULL SODIMM SOM Edge Connector interfaces	38
Table 8: Power Input Requirement.....	45
Table 9: Power Sequence Timing	46
Table 10: Power Consumption.....	47
Table 11: Environmental Specification	48
Table 12: Orderable Product Part Numbers	51

1. INTRODUCTION

1.1 Purpose

This document is the Hardware User Guide for the i.MX 6UltraLite (here after mentioned as i.MX6UL)/i.MX6ULL SODIMM System On Module based on the NXP's i.MX6UL/i.MX6ULL Applications Processor with PMIC. This board is fully supported by iWave Systems Technologies Pvt. Ltd. This Guide provides detailed information on the overall design and usage of the i.MX6UL/i.MX6ULL SODIMM System On Module from a Hardware Systems perspective.

1.2 SODIMM SOM Overview

The i.MX6UL/i.MX6ULL SODIMM SOM is extension of i.MX6UL/i.MX6ULL CPU. Also with the SOM approach one can reduce the cost and time required for the development of customised solution on i.MX6UL/i.MX6ULL platform. SODIMM module has a form factor of 67.6mm.x 29mm and provides the functional requirements for an embedded application. A single ruggedized SODIMM connector provides the carrier board interface to carry all the I/O signals to and from the SODIMM module.

1.3 List of Acronyms

The following acronyms will be used throughout this document.

Table 1: Acronyms & Abbreviations

Acronyms	Abbreviations
A	Ampere
ARM	Advanced RISC Machine
BOM	Bill of Material
BPP	Bits Per Pixel
BSP	Board Support Package
CAN	Controller Area Network
CMOS	Complementary Metal-Oxide Semiconductor
CPU	Central Processing Unit
CSI	Camera Serial Interface
DDR3	Double Data Rate 3
eCSPI	Enhanced Configurable Serial Peripheral Interface
eMMC	Enhanced Multi Media Card
FLEXCAN	Flexible Controller Area Network
GB	Giga Byte
Gbps	Gigabits per sec
GPIO	General Purpose Input Output
I2C	Inter-Integrated Circuit
IC	Integrated Circuit
JTAG	Joint Test Action Group

Acronyms	Abbreviations
Kbps	Kilobits per second
LCD	Liquid Crystal Display
MAC	Media Access Controller
MB	Mega Byte
Mbps	Megabits per sec
MHz	Mega Hertz
NC	No Connect
NPTH	Non Plated Through hole
PCB	Printed Circuit Board
PMIC	Power Management Integrated Circuit
PTH	Plated Through hole
PWM	Pulse Width Modulation
PXP	Pixel Pipeline
QSPI	Quad Serial Peripheral Interface
RMII	Reduced Media Independent Interface
ROM	Read-Only Memory
RTC	Real Time Clock
SAI	Synchronous Audio Interface
SD	Secure Digital
SDRAM	Synchronous Dynamic Random Access Memory
SODIMM	Small Outline Dual in-line Memory Module
SOM	System On Module
uA	Micro Ampere
UART	Universal Asynchronous Receiver/Transmitter
UL	Ultra Lite
uSDHC	Ultra Secured Digital Host Controller
USB	Universal Serial Bus
USB OTG	USB On The Go
V	Voltage

1.4 Terminology Description

In this document, wherever Signal Type is mentioned, below terminology is used.

Table 2: Terminology

Terminology	Description
I	Input Signal
O	Output Signal
IO	Bidirectional Input/output Signal
CMOS	Complementary Metal Oxide Semiconductor Signal
DIFF	Differential Signal
TMDS	Transition-Minimized Differential Signalling
OD	Open Drain Signal
OC	Open Collector Signal
Analog	Analog Signal
Power	Power Pin
PU	Pull Up
PD	Pull Down
NA	Not Applicable
NC	Not Connected

Note: Signal Type does not include internal pull-ups or pull-downs implemented by the chip vendors and only includes the pull-ups or pull-downs implemented On-SOM.

1.5 References

- i.MX6UL/i.MX6ULL Applications Processors Datasheet
- i.MX6UL/i.MX6ULL Applications Processors Reference Manual

1.6 Important Note

i.MX6UL/i.MX6ULL SODIMM Edge connector pin name mentioned in **Table 5** is followed as per below format for easy understanding.

- If CPU pin functionality name and CPU pad name is same, Signal name is mentioned as

“CPU Pad Name”

Example: SD1_DATA1

In this signal, functionality which we are using and CPU Pad name is **SD1_DATA1**.

- If CPU pin functionality name and pad name is different, Signal name is mentioned as

“Functionality name (CPU Pad name)”

Example: CAN1_RXD (UART3_RTS_B)

In this signal, **CAN1_RXD** is the functionality which we are using and **UART3_RTS_B** is the CPU Pad name.

- If CPU pin functionality is GPIO, Signal name is mentioned as

“FunctionalityDescription (CPU Pad name)”

Example: PWM4_OUT (GPIO1_IO05)

In this signal, **PWM4_OUT** is the functionality which we are using and **GPIO1_IO05** is the CPU pad name.

Note: The above naming is not applicable for other signals which are not connected to CPU.

2. ARCHITECTURE AND DESIGN

This section provides detailed information about the i.MX6UL/i.MX6ULL SODIMM SOM Features and Hardware architecture with high level block diagram. Also this section provides detailed information about SODIMM edge connector pin assignment and usage.

2.1 i.MX6UL/i.MX6ULL SODIMM SOM Block Diagram

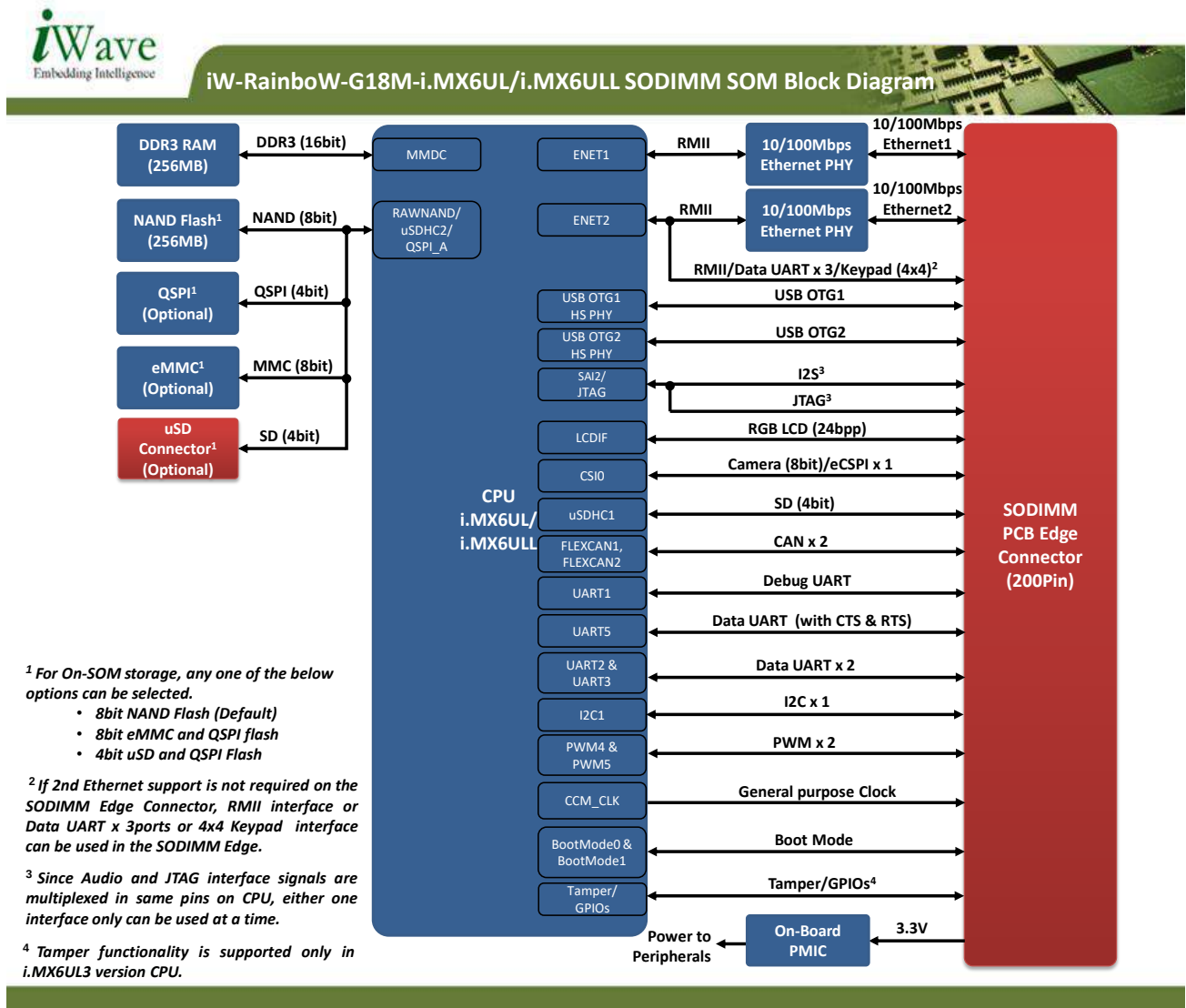


Figure 1: i.MX6UL/i.MX6ULL SODIMM SOM Block Diagram

2.2 i.MX6UL/i.MX6ULL SODIMM SOM Features

The i.MX6UL/i.MX6ULL SODIMM SOM supports the following features.

CPU

- NXP's i.MX6UL/i.MX6ULL ARM Cortex®-A7 core based CPU

PMIC

- NXP's PF3001 PMIC

Memory

- 256MB DDR3L (Expandable)
- 256MB NAND Flash (Expandable)
- 4GB eMMC Flash (Optional)¹
- Micro SD slot (Optional)²
- QSPI Flash (Optional)³

Network & Communication

- 10/100Mbps Ethernet PHY x 2 Ports

SODIMM PCB Edge Interfaces

- Debug UART
- Data UART x 3 Ports
- CAN x 2 Ports
- SD (4bit) x 1 Port
- Parallel RGB Display (24bpp) x 1 Port
- Parallel Camera Interface (8bit) x 1 Port (or eCSPI x 1 Port)
- I2S Audio Interface x 1 Port⁴
- JTAG x 1 Port⁴
- USB OTG x 2 Ports
- 10/100Mbps Ethernet x 2 Ports⁵
- I2C x 1 Port
- PWM x 2 Ports
- Tamper Signals⁶
- General Purpose Clock
- Boot Mode Signals
- Power Control Signals

General Specification

- Power Supply : 3.3V, 1A
- Form Factor : 67.6mm x 29mm

¹Since NAND Flash, eMMC and QSPI are multiplexed in same pins on i.MX6UL/i.MX6ULL CPU, if eMMC flash feature is required in the SOM, NAND flash and Micro SD on SOM cannot be used.

² Since NAND Flash, Micro SD and QSPI are multiplexed in same pins on i.MX6UL/i.MX6ULL CPU, if Micro SD feature is required in the SOM, NAND flash and eMMC on SOM cannot be used.

³ Since NAND Flash and QSPI are multiplexed in same pins on i.MX6UL/i.MX6ULL CPU, if NAND Flash feature is required in the SOM, QSPI on SOM cannot be used.

⁴ Since Audio and JTAG interface signals are multiplexed in same pins on i.MX6UL/i.MX6ULL CPU, either one interface only can be used at a time.

⁵ ENET2 interface is connected to On SOM Ethernet PHY and also optionally connected from i.MX6UL/i.MX6ULL CPU to SODIMM edge connector, either one interface only can be used at a time.

⁶ Only i.MX6UL3 version CPU supports tamper functionality. For all other i.MX6UL/i.MX6ULL CPU versions, tamper pins are used as only GPIOs.

2.3 i.MX6UL/i.MX6ULL CPU

i.MX6UL/i.MX6ULL SODIMM SOM is based on NXP's i.MX6UL/i.MX6ULL high performance, ultra-efficient processor family featuring an advanced implementation of a single ARM® Cortex®-A7 core. The Block Diagram of i.MX6UL CPU from the NXP's i.MX6UL datasheet is shown below for reference.

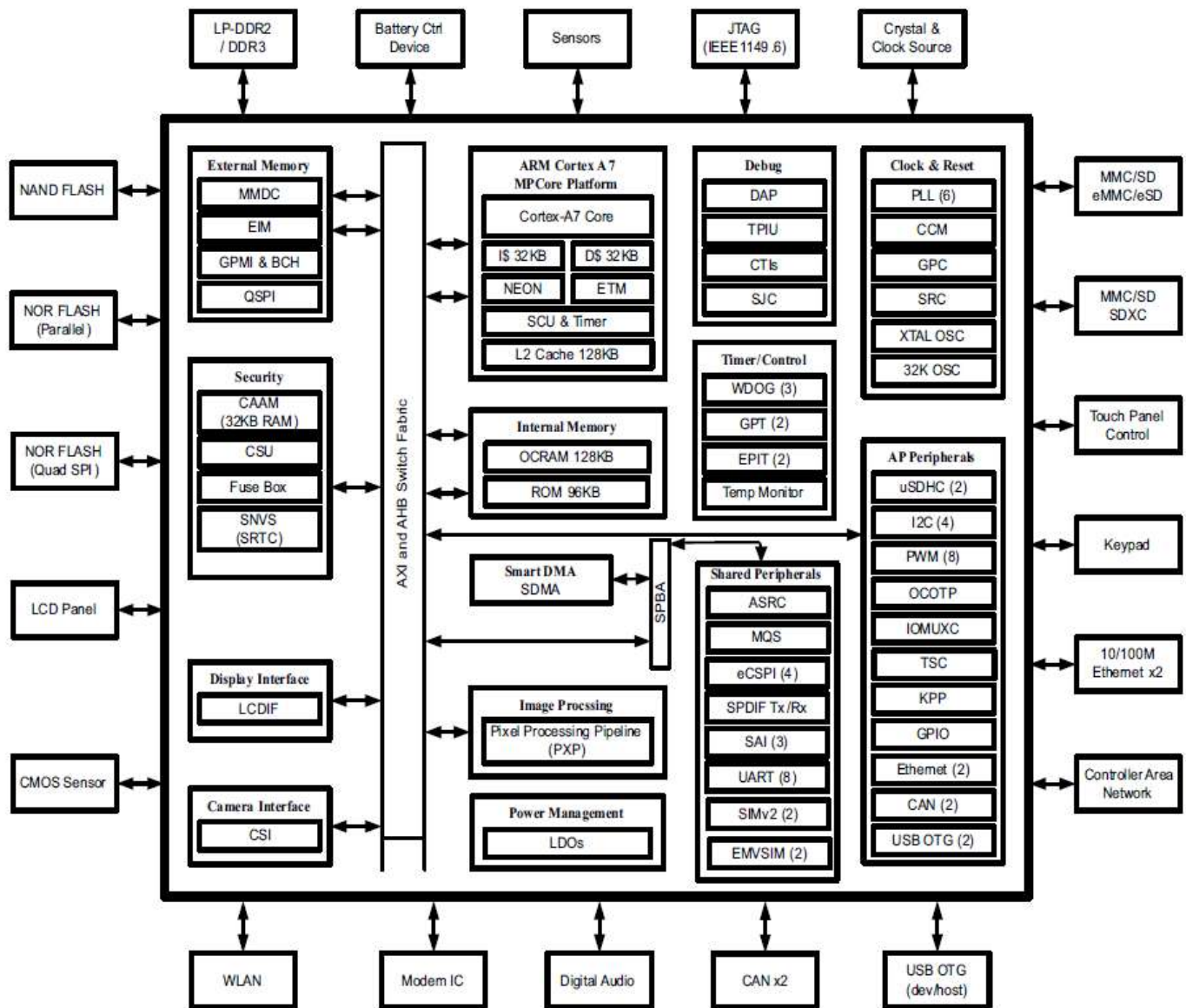


Figure 2: i.MX6UL Simplified Block Diagram

Note: Please refer the latest i.MX6UL/i.MX6ULL Datasheet & Reference Manual from NXP website for Electrical characteristics of i.MX6UL/i.MX6ULL Application CPU which may be revised from time to time.

i.MX6UL/i.MX6ULL SODIMM SOM Hardware User Guide

i.MX6UL CPU has many sub version CPUs i.MX6UL0, i.MX6UL1, i.MX6UL2 & i.MX6UL3. Also i.MX6ULL CPU has many sub version CPUs i.MX6ULL0, i.MX6ULL1 & i.MX6ULL2. The difference between these CPUs from NXP's factsheet is shown below for reference.

i.MX 6UltraLite DEVICE OPTIONS

• Red indicates change from column to the left

Feature	MCIMX6G0	MCIMX6G1	MCIMX6G2	MCIMX6G3
Speed	528 MHz	528 MHz, 696 MHz	528 MHz, 696 MHz	528 MHz
Cache	32 KB-I, 32 KB-D	32 KB-I, 32 KB-D 128 KB L2	32 KB-I, 32 KB-D 128 KB L2	32 KB-I, 32 KB-D 128 KB L2
OCRAM	128 KB	128 KB	128 KB	128 KB
DRAM	16-bit LP-DDR2, DDR3/DDR3L	16-bit LP-DDR2, DDR3/DDR3L	16-bit LP-DDR2, DDR3/DDR3L	16-bit LP-DDR2, DDR3/DDR3L
eFuse for Customer	512-bit	1024-bit	1536-bit	2048-bit
NAND (BCH40)	Yes	Yes	Yes	Yes
Parallel NOR/EBI	Yes	Yes	Yes	Yes
Ethernet	10/100-Mbit/s x 1	10/100-Mbit/s x 1	10/100-Mbit/s x 2	10/100-Mbit/s x 2
USB with PHY	OTG, HS/FS x 1	OTG, HS/FS x 2	OTG, HS/FS x 2	OTG, HS/FS x 2
CAN	0	1	2	2
Security	Basic	TRNG, Crypto Engine (AES/TDES/SHA), Secure Boot	TRNG, Crypto Engine (AES/TDES/SHA), Secure Boot	TRNG, Crypto Engine (AES with DPA/TDES/SHA/RSA), Secure Boot, tamper monitor, PCI4.0 pre-certification, OTF DRAM encryption
Graphic	None	None	PxP	PxP
CSI	None	None	24-bit Parallel CSI	24-bit Parallel CSI
LCD	None	None	24-bit Parallel LCD	24-bit Parallel LCD
Quad SPI	1	1	1	1
SDIO	2	2	2	2
UART	4	8	8	8
I ² C	2	4	4	4
SPI	2	4	4	4
I ² S/SAI	1	3	3	3
S/PDIF	1	1	1	1
Timer/PWM	Timer x 2, PWM x 4	Timer x 4, PWM x 8	Timer x 4, PWM x 8	Timer x 4, PWM x 8
12-bit ADC	1 x 10-ch.	1 x 10-ch.	2 x 10-ch.	2 x 10-ch.

i.MX 6ULL DEVICE OPTIONS

• Red indicates change from column to the left

Feature	MCIMX6Y0	MCIMX6Y1	MCIMX6Y2
Core	ARM® Cortex-A7	ARM Cortex-A7	ARM Cortex-A7
Speed	528 MHz	528 MHz	528 MHz
Cache	32 KB-I, 32 KB-D	32 KB-I, 32 KB-D 128 KB L2	32 KB-I, 32 KB-D 128 KB L2
OCRAM	128 KB	128 KB	128 KB
DRAM	16-bit LP-DDR2, DDR3/DDR3L	16-bit LP-DDR2, DDR3/DDR3L	16-bit LP-DDR2, DDR3/DDR3L
eFuse for customer	256-bit	256-bit	256-bit
NAND (BCH40)	Yes	Yes	Yes
Parallel Nor/EBI	Yes	Yes	Yes
Ethernet	10/100 MB x 1	10/100 MB x 1	10/100 MB x 2
USB with PHY	OTG, HS/FS x 1	OTG, HS/FS x 2	OTG, HS/FS x 2
CAN	0	1	2
Graphic	None	None	PxP
CSI	None	None	16-bit Parallel CSI
LCD	None	None	24-bit Parallel LCD
QSPI	1	1	1
SDIO	2	2	2
UART	4	8	8
IIC	2	4	4
SPI	2	4	4
I ² S/SAI	1	3	3
ESAI	1	1	1
S/PDIF	1	1	1
Timer/PWM	Timer x 2, PWM x 4	Timer x 4, PWM x 8	Timer x 4, PWM x 8
12-bit ADC	1 x 10-ch.	1 x 10-ch.	2 x 10-ch.
Security	None	AES-128, HAB	AES-128, HAB

Figure 3: i.MX6UL/i.MX6ULL CPU devices comparison

2.4 PMIC

i.MX6UL/i.MX6ULL SODIMM SOM supports NXP's PF3001 PMIC for On-SOM power management. The PF3001 is a Power Management Integrated Circuit (PMIC) designed specifically for always ON application with the NXP i.MX6UL/i.MX6ULL application processors. Also i.MX6UL/i.MX6ULL SODIMM SOM can optionally support NXP's PF3000 PMIC which supports Low power and Standby operation too.

The PF3001 PMIC provides all required power to i.MX6UL/i.MX6ULL CPU and all On SOM peripherals. This PMIC supports up to three buck converters, six linear regulators, RTC supply and coin-cell charger. i.MX6UL/i.MX6ULL CPU's I2C1 interface is used for PMIC programming. I2C address for PMIC is 0x08.

2.5 Memory

2.5.1 DDR3L SDRAM

i.MX6UL/i.MX6ULL SODIMM SOM by default supports 256MB DDR3L RAM memory in 16bit mode. To support this, it uses one 256MB DDR3L SDRAM IC. This device operates at 1.35V voltage level. DDR3L IC is physically located on topside of the SODIMM SOM. The RAM size can be expandable up to maximum of 1GB.

2.5.2 NAND Flash

The i.MX6UL/i.MX6ULL SODIMM SOM supports 256MB NAND Flash as default boot device. This is connected to GPMI controller of the i.MX6UL/i.MX6ULL CPU and operates at 3.3 Voltage level. The NAND flash memory is physically located on topside of the SODIMM SOM. The NAND Flash size is expandable.

2.6 SODIMM PCB Edge Connector

i.MX6UL/i.MX6ULL SODIMM SOM Supports JEDEC Physical Standard 200pin DDR SO-DIMM PCB edge connector for interfaces expansion. The interfaces which are available at SODIMM Edge connector are explained in the following sections.



SODIMM Edge Connector (J3)

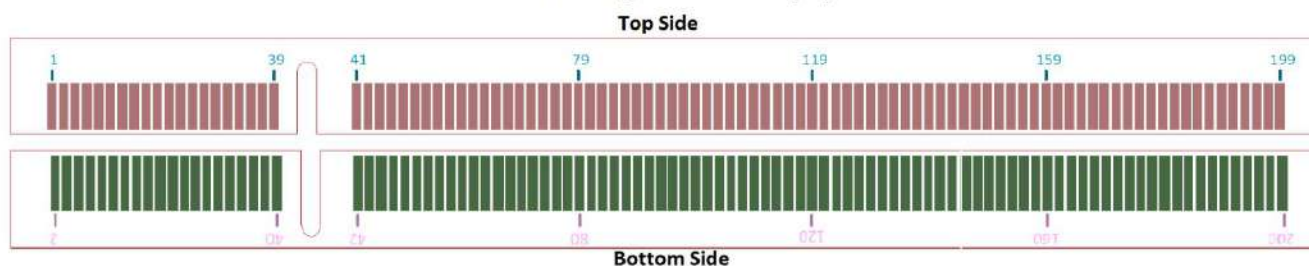


Figure 4: SODIMM PCB Edge Connector

Number of Pins	- 200
Connector Part	- Not Applicable (On Board PCB Edge connector)
Mating Connector	- 1473005-1 from TE Connectivity

Important Note: Some of the interfaces mentioned in the following section are subject to available based on the i.MX6UL/i.MX6ULL CPU device version used in the SODIMM SOM. For more details, refer i.MX6UL/i.MX6ULL documents from NXP or contact iWave.

2.6.1 UART Interface

i.MX6UL/i.MX6ULL SODIMM SOM supports four UART interface on SODIMM Edge connector in which one for Debug UART interface and other three for Data UART interface. i.MX6UL/i.MX6ULL CPU's UART1 controller is used for Debug UART interface and UART2, UART3 & UART5 controller is used for Data UART interface on SODIMM Edge connector. Also i.MX6UL/i.MX6ULL SODIMM SOM supports hardware flow control for request to send and clear to send signals on UART5 interface.

i.MX6UL/i.MX6ULL CPU UART controller supports Serial RS-232NRZ mode, 9-bit RS-485 mode and IrDA mode. It is compatible with High-speed TIA/EIA-232-F (up to 5.0 Mbit/s) with auto baud rate detection (up to 115.2 Kbit/s). It supports 7 or 8 data bits for RS-232 characters (9 bit RS-485 format), 1 or 2 stop bits and programmable parity (even, odd, and no parity).

For more details, refer SODIMM Edge connector pins 117 & 118 for Debug UART, pins 98 & 99 for UART2 interface, pins 7 & 9 for UART3 interface and pins 38, 75, 102 & 103 for UART5 interface on **Table 5**.

2.6.2 CAN Interface

i.MX6UL/i.MX6ULL SODIMM SOM supports two CAN interfaces on SODIMM Edge connector. CPU's FLEXCAN1 and FLEXCAN2 module is used for CAN interface which supports CAN protocol according to the CAN 2.0B protocol specification. It supports programmable bit rate up to 1 Mb/sec with both standard and extended message frames. Also it supports 64 Message Buffers. To connect external CAN module, it is necessary to add transceiver in between.

For more details, refer SODIMM Edge connector pins 176 & 178 for CAN1 interface and pins 175 & 177 for CAN2 interface on **Table 5**.

2.6.3 SD Interface

i.MX6UL/i.MX6ULL SODIMM SOM supports one SD interface port on SODIMM Edge connector. CPU's uSDHC1 controller is used for SD interface which is fully compliant with SD Memory Card Specifications v3.0 including extended-capacity SDHC cards. It supports 1-bit or 4-bit transfer mode for SD and SDIO cards up to UHS-I SDR104 mode.

For more details, refer SODIMM Edge connector pins 105, 107 to 109, 111, 112 & 114 on **Table 5**.

2.6.4 Parallel RGB Display Interface

i.MX6UL/i.MX6ULL SODIMM SOM supports one 24bpp Parallel RGB display interface on SODIMM Edge connector. i.MX6UL/i.MX6ULL CPU's eLCDIF controller is used for display interface which supports upto 24bit data bus (8bits/colour) with up to WXGA (1366x768) resolution at 60Hz. Also CPU's pixel/image processing engine (PXP) is used to perform image processing on image/video buffers before sending to an LCD display,.

For more details, refer SODIMM Edge Connector pins 143 to 146 & 148 to 174 on **Table 5**.

2.6.5 Parallel Camera Interface

i.MX6UL/i.MX6ULL SODIMM SOM supports one 8bit camera interface on SODIMM Edge Connector. i.MX6UL/i.MX6ULL CPU's CSI parallel port is used for camera interface which provides direct connectivity to most relevant CMOS sensors and CCIR656 video interface. The sensor is the master of the pixel clock (PIXCLK) & synchronization signals where synchronization signals can be received using dedicated control signals method (HSYNC & VSYNC) or controls embedded in data stream method (CCIR.656 protocol).

For more details, refer SODIMM Edge connector pins 62, 63, 66, 70, 93, 104, 110, 119 to 123 on **Table 5**.

2.6.6 I2S Audio Interface

i.MX6UL/i.MX6ULL SODIMM SOM supports one SAI audio interface port on SODIMM Edge connector. i.MX6UL/i.MX6ULL CPU's synchronous audio interface (SAI) supports full-duplex serial interfaces with frame synchronization such as I2S, AC97, TDM, and codec/DSP interfaces. The SAI transmitter and receiver support asynchronous free-running bit clocks that can be generated internally from an audio master clock or supplied externally. Also, the SAI transmitter and receiver can be configured to operate with synchronous bit clock and frame sync.

For more details, refer SODIMM Edge connector pins 61, 64, 67, 89 & 90 on **Table 5**.

Important Note: Since Audio and JTAG interface signals are multiplexed in same pins on i.MX6UL/i.MX6ULL CPU, these pins are connected to two places in SODIMM Edge connector and either one interface only can be used at a time.

2.6.7 JTAG Interface

i.MX6UL/i.MX6ULL SODIMM SOM supports one JTAG interface on SODIMM Edge Connector. i.MX6UL/i.MX6ULL CPU implements JTAG Security modes internal to System JTAG Controller. The System JTAG Controller provides debug and test control with the maximum security. The test access port is designed to support features compatible with the IEEE Standard 1149.1 v2001 (JTAG). The SJC module of the processor provides the bridge between external development and test instrumentation and the internal JTAG-accessible debug and test resources.

For more details, refer SODIMM Edge connector pins 191, 193, 195, 197 & 199 on **Table 5**.

Important Note: Since Audio and JTAG interface signals are multiplexed in same pins on i.MX6UL/i.MX6ULL CPU, these pins are connected to two places in SODIMM Edge connector and either one interface only can be used at a time.

2.6.8 USB 2.0 OTG Interface

i.MX6UL/i.MX6ULL SODIMM SOM supports two High Speed USB 2.0 OTG interfaces (USB1 & USB2) on SODIMM Edge connector. i.MX6UL/i.MX6ULL CPU's USB Controller which has two independent USB On-The-Go (OTG) controller cores are used for USB OTG interface. Each USB controller core can operate in High Speed operation (480 Mbps), Full Speed operation (12 Mbps) and Low Speed operation (1.5 Mbps). Also it supports two integrated USB 2.0 PHY macrocells provides a standard UTM interface to connect directly to a USB connector.

For more details, refer SODIMM Edge connector pins 74, 76, 77, 78, 81, 83 & 200 for USB OTG1 interface and pins 39, 140, 141, 188 & 190 for USB OTG2 interface on **Table 5**.

Note: Only USB1 interface can be used in i.MX6UL/i.MX6ULL Serial Downloader Boot Mode and USB2 cannot be used.

2.6.9 Dual 10/100Mbps Ethernet

i.MX6UL/i.MX6ULL SODIMM SOM supports two 10/100Mbps Ethernet interfaces on SODIMM Edge connector through ENET1 and ENET2 interface. The MAC is integrated in the CPU and connected to the external Ethernet PHY on SOM. Since MAC and PHY are supported on SOM itself, only Magnetics are required on the carrier board. i.MX6UL/i.MX6ULL SODIMM SOM also supports Link and Speed indication LED control signals to SODIMM Edge.

i.MX6UL/i.MX6ULL SODIMM SOM supports two "KSZ8081RNB1" Ethernet PHY from Micrel. These PHY's are interfaced with CPU using ENET1 and ENET2 interface correspondingly and works at 3.3V IO voltage level. Since this PHY doesn't require center tap supply to the magnetics, CTREF voltage to SODIMM Edge is not supported on SOM. It is recommended that center tap pins of magnetics should be separated from one another and connected through separate 0.1uF common mode capacitors to ground. The below table provides the compatible magnetics recommended by PHY Manufacturer.

Table 3: Compatible Magnetics

Part Description	Part Number	Manufacturer	Temperature
RJ45 Magjack with Green, Orange – LED's.	0821-1X1T-36-F	Bel Fuse	-40°C to 85°C
RJ45 Magjack with Green, Yellow – LED's.	SI-46001-F	Bel Fuse	-40°C to 85°C
RJ45 Magjack with Green, Yellow – LED's.	HFJ11-E2450E-L12RL	Halo Electronics	-40°C to 85°C
RJ45 Magjack with Green, Yellow – LED's.	JX0011D21BNL	Pulse Electronics	-40°C to 85°C

For more details, refer SODIMM Edge connector pins 2, 4, 6, 8, 11 & 12 for USB ENET1 interface and pins 30, 33 to 37 & 42 to 45 for ENET2 interface on **Table 5**.

Important Note: ENET2 interface is connected to On SOM Ethernet PHY and also optionally connected from CPU to SODIMM edge connector. If ENET2 Ethernet PHY is not used on SOM, the same signals which are optionally connected to SODIMM edge can be used for RMII interface or UART interface (3ports) or Keypad (4x4) interface. Please contact iWave for more details on this support.

2.6.10 I2C Interface

i.MX6UL/i.MX6ULL SODIMM SOM supports one I2C interface on SODIMM Edge connector. i.MX6UL/i.MX6ULL CPU's I2C1.channel is used for General purpose I2C interface which is compatible with the standard NXP I2C bus protocol. It supports standard mode with data transfer rates up to 100kbps and Fast mode with data transfer rates up to 400kbps.

Since flexible I2C standard allows multiple devices to be connected to the single bus, i.MX6UL/i.MX6ULL CPU's I2C1 can be connected to more than one device on the carrier board. This I2C1 interface is also connected to On-SOM PMIC with I2C address 0x08 in the i.MX6UL/i.MX6ULL SODIMM SOM.

For more details, refer SODIMM Edge connector pins 115 & 116 on **Table 5**.

2.6.11 PWM Interface

i.MX6UL/i.MX6ULL SODIMM SOM supports two PWM interface on SODIMM Edge connector. i.MX6UL/i.MX6ULL CPU's PWM4 and PWM5 module is used for PWM interface which has a 16-bit counter and optimized to generate sound from stored sample audio images and it can also generate tones. It uses 16-bit resolution and a 4 x 16 data FIFO.

For more details, refer SODIMM Edge connector pins 138 & 147 on **Table 5**.

2.6.12 Tamper Interface

i.MX6UL3 SODIMM SOM supports upto seven external Tamper detection signals on SODIMM Edge connector. External Tamper Detection is a special mechanism provided through i.MX6UL3 CPU pin to signal when the device encounters unauthorized opening or tampering. Inside the i.MX6UL3 CPU, the received signal is compared with the desired signal level, once unequal, tamper event is found. An always-ON power supply (coin cell battery) should be present in the system.

For more details, refer SODIMM Edge connector pins 47, 68, 73, 86, 133, 134 & 136 on **Table 5**.

Important Note: Only i.MX6UL3 version CPU supports tamper functionality on these pins and doesn't support GPIO functionality. For all other i.MX6UL/i.MX6ULL CPU versions, these tamper pins are used as only GPIOs.

2.6.13 GPIO Interface

Most of the i.MX6UL/i.MX6ULL CPU Pins which are connected to SODIMM Edge connector can be configured as GPIO with interrupt capable (if not used as other interface). i.MX6UL/i.MX6ULL CPU GPIO controller provides dedicated general-purpose pins that can be configured as either inputs or outputs. When configured as an output, it is possible to write to an internal register to control the state driven on the output pin. When configured as an input, it is possible to detect the state of the input by reading the state of an internal register. In addition, the GPIO peripheral can produce Core interrupts.

2.6.14 General Purpose Clock

i.MX6UL/i.MX6ULL SODIMM SOM supports one general purpose differential pair high speed clock input/output on SODIMM Edge connector. This can be used to output internal i.MX6UL/i.MX6ULL CPU clock to outside the CPU as either reference clock or as a functional clock for peripherals. Otherwise this can be used as input to feed external reference clock to the i.MX6UL/i.MX6ULL CPU PLLs and further to the modules inside CPU.

Instead of differential clock, it can also be used as single ended clock also on CLK1_P pin. In this case, corresponding CLK1_N input should be tied to the constant voltage level equal to 1/2 of the input signal swing of CLK1_P. Also termination should be provided in case of high frequency signals.

For more details, refer SODIMM Edge connector pins 135 & 137 on **Table 5**.

2.6.15 Boot Mode Signals

i.MX6UL/i.MX6ULL SODIMM SOM supports two boot mode signals on SODIMM Edge Connector. BOOT_MODE is initialized by sampling the BOOT_MODE0 and BOOT_MODE1 inputs on the rising edge of POR_B. These Boot mode selection signals are connected to SODIMM Edge connector and desired boot mode must be set from the carrier board as explained in the below table.

Table 4: Boot Mode Pin Settings Truth Table

BOOT_MODE [1] (SODIMM Edge Pin 184)	BOOT_MODE [0] (SODIMM Edge Pin 182)	Boot Type	Description
1	0	Internal Boot Mode	In this mode, i.MX6UL/i.MX6ULL boot media is selected by GPIO pin's settings and in i.MX6UL/i.MX6ULL SODIMM SOM, it is fixed to NAND flash by hardware. <i>Note: To support different boot media other than NAND flash, please contact iWave.</i>
0	0	Boot From eFuses	In this mode, i.MX6UL/i.MX6ULL boot media is selected by CPU eFUSE settings. <i>Note: i.MX6 eFuse setting is not modified by iWave from silicon shipped value.</i>
0	1	Serial Downloader Mode	In this mode, i.MX6UL/i.MX6ULL boot media can be Programmed through its USB OTG interface using MFG Tool.

For more details, refer SODIMM Edge connector pins 182 & 184 on **Table 5**.

Important Note: To make i.MX6UL/i.MX6ULL SODIMM SOM boots as expected, make sure to set the desired boot mode from the carrier board.

2.6.16 Power Input

i.MX6UL/i.MX6ULL SODIMM SOM works with single 3.3V power input (VIN_3V3) from SODIMM Edge connector and generates all other required powers internally On-SOM itself. i.MX6UL/i.MX6ULL SODIMM SOM uses VRTC_3V0 coin cell power input from SODIMM Edge connector to CPU's RTC controller for real time clock (when VIN_3V3 is off).

For more details, refer SODIMM Edge connector pins 20, 32, 46, 60, 72, 88, 106, 124, 142, 160, 180 & 192 for 3.3V power input (VIN_3V3) and pin 183 for VRTC_3V0 on **Table 5**.

2.6.17 Reset Signal

i.MX6UL/i.MX6ULL SODIMM SOM supports RSTBTN# for power management on SODIMM Edge connector. RSTBTN# input from SODIMM Edge connector is the active low signal which is connected to CPU's POR pin in i.MX6UL/i.MX6ULL SODIMM SOM. This pin can be used to reset the i.MX6UL/i.MX6ULL CPU by connecting push button in the carrier board.

For more details, refer SODIMM Edge connector pin 187 on **Table 5**.

2.6.18 Power Control Signal

i.MX6UL/i.MX6ULL SODIMM SOM supports ONOFF input from SODIMM Edge connector which is the active low signal and connected to i.MX6 CPU's ONOFF pin. This pin can be used to On/Off the CPU and the entire i.MX6UL/i.MX6ULL SODIMM SOM by connecting push button in the carrier board.

When the board power is On, a button press between 750ms to 5s will send an interrupt to the core to request software to bring down the i.MX6UL/i.MX6ULL safely (if software supports). Otherwise, button press greater than 5s results in a direct hardware power down which is applicable when software is unable to power Off the device. When the i.MX6UL/i.MX6ULL CPU power supply is Off, a button press greater in duration than 750ms asserts an output signal to request power from a power IC to power up the i.MX6UL/i.MX6ULL CPU.

For more details, refer SODIMM Edge connector pins 179 on **Table 5**.

Table 5: 200-Pin PCB Edge Connector Pin Assignment

Pin No.	SODIMM Edge Connector Pin Name	i.MX6UL/i.MX6ULL Ball Name/ Pin Number	Signal Type/ Termination	Description
1	GND	NA	Power	Ground.
2	ETH1_TXM	NA	IO, DIFF	Ethernet transmit differential pair 1 negative.
3	NC	NA	-	NC.
4	ETH1_TXP	NA	IO, DIFF	Ethernet transmit differential pair 1 positive.
5	GND	NA	Power	Ground.
6	ETH1_RXM	NA	IO, DIFF	Ethernet receive differential pair 1 negative.
7	UART3_RX_DATA	UART3_RX_DATA/ H16	I, 3.3V CMOS	UART3 serial data receiver.
8	ETH1_RXP	NA	IO, DIFF	Ethernet receive differential pair 1 positive.
9	UART3_TX_DATA	UART3_TX_DATA/ H17	O, 3.3V CMOS	UART3 serial data transmitter.
10	NC	NA	-	NC.
11	ETH1_LINK_LED0	NA	-	Ethernet link status LED.
12	ETH1_SPEED_LED1	NA	-	Ethernet speed status LED.
13	GND	NA	Power	Ground.
14	NC	NA	-	NC.
15	NC	NA	-	NC.
16	NC	NA	-	NC.
17	NC	NA	-	NC.
18	NC	NA	-	Default NC. <i>Note: UART4_TX_DATA is optionally connected to this pin (for I2C1_SCL) through resistor and default not populated.</i> <i>Note: Same signal is by default connected to SODIMM edge connector 116th pin.</i>
19	NC	NA	-	Default NC. <i>Note: UART4_RX_DATA is optionally connected to this pin (for I2C1_SDA) through resistor and default not populated.</i> <i>Note: Same signal is by default connected to SODIMM edge connector 115th pin.</i>
20	VIN_3V3	NA	I, 3.3V Power	Supply Voltage.
21	NC	NA	-	NC.
22	NC	NA	-	NC.
23	NC	NA	-	NC.
24	NC	NA	-	NC.
25	NC	NA	-	NC.
26	NC	NA	-	NC.
27	GND	NA	Power	Ground.

Pin No.	SODIMM Edge Connector Pin Name	i.MX6UL/i.MX6ULL Ball Name/ Pin Number	Signal Type/ Termination	Description
28	NC	NA	-	NC.
29	NC	NA	-	NC.
30	ETH2_SPEED_LED1	NA	-	Ethernet speed status LED.
31	NC	NA	-	NC.
32	VIN_3V3	NA	I, 3.3V Power	Supply Voltage.
33	ETH2_LINK_LED0	NA	-	Ethernet link status LED.
34	ETH2_TXM	NA	IO, DIFF	Ethernet transmit differential pair 1 negative. <i>Note: ETH2_TXM from Ethernet PHY is connected to this pin through resistor and default populated.</i> <i>Note: ENET2_TX_DATA0 from CPU is optionally connected to this pin through resistor and default not populated.</i>
35	ETH2_RXM	NA	IO, DIFF	Ethernet receive differential pair 1 negative. <i>Note: ETH2_RXM from Ethernet PHY is connected to this pin through resistor and default populated.</i> <i>Note: ENET2_TX_CLK from CPU is optionally connected to this pin through resistor and default not populated.</i>
36	ETH2_TXP	NA	IO, DIFF	Ethernet transmit differential pair 1 positive. <i>Note: ETH2_TXP from Ethernet PHY is connected to this pin through resistor and default populated.</i> <i>Note: ENET2_TX_DATA1 from CPU is optionally connected to this pin through resistor and default not populated.</i>
37	ETH2_RXP	NA	IO, DIFF	Ethernet receive differential pair 1 positive. <i>Note: ETH2_RXP from Ethernet PHY is connected to this pin through resistor and default populated.</i> <i>Note: ENET2_TX_EN from CPU is optionally connected to this pin through resistor and default not populated.</i>
38	UART5_RTS(GPIO1_IO08)	GPIO1_IO08/N17	I, 3.3V CMOS	UART5 ready to send data.
39	USB_OTG2_OC(GPIO1_IO03)	GPIO1_IO08/L17	I, 3.3V CMOS	Over current sense for USB OTG2.
40	GND	NA	Power	Ground.
41	GND	NA	Power	Ground.

i.MX6UL/i.MX6ULL SODIMM SOM Hardware User Guide

Pin No.	SODIMM Edge Connector Pin Name	i.MX6UL/i.MX6ULL Ball Name/ Pin Number	Signal Type/ Termination	Description
42	NC	NA	-	Default NC. <i>Note: ENET2_RX_DATA0 from CPU is optionally connected to this pin through resistor and default not populated.</i>
43	NC	NA	-	Default NC. <i>Note: ENET2_RX_ER from CPU is optionally connected to this pin through resistor and default not populated.</i>
44	NC	NA	-	Default NC. <i>Note: ENET2_RX_DATA1 from CPU is optionally connected to this pin through resistor and default not populated.</i>
45	NC	NA	-	Default NC. <i>Note: ENET2_RX_EN from CPU is optionally connected to this pin through resistor and default not populated.</i>
46	VIN_3V3	NA	I, 3.3V Power	Supply Voltage.
47	GPIO5_IO0(SNVS_TAMPER0)	SNVS_TAMPER0/R10	IO, 3.3V CMOS	Tamper Detection Pin 0 (Or) General purpose input/output. <i>Important Note: In i.MX6UL3 SODIMM SOM, this pin can be used as only Tamper functionality. In all other i.MX6UL/i.MX6ULL CPU version SODIMM SOM, this pin can be used as only GPIO functionality.</i>
48	NC	NA	-	NC.
49	NC	NA	-	NC.
50	NC	NA	-	NC.
51	GND	NA	Power	Ground.
52	NC	NA	-	NC.
53	NC	NA	-	NC.
54	NC	NA	-	NC.
55	NC	NA	-	NC.
56	NC	NA	-	NC.
57	NC	NA	-	NC.
58	NC	NA	-	NC.
59	NC	NA	-	NC.
60	VIN_3V3	NA	I, 3.3V Power	Supply Voltage.
61	JTAG_TCK/SAI2_RX_DATA	JTAG_TCK/M14	I, 3.3V CMOS	Audio receive data. <i>Note: Same signal is also connected to 197th pin of SODIMM edge connector.</i>

Pin No.	SODIMM Edge Connector Pin Name	i.MX6UL/i.MX6ULL Ball Name/ Pin Number	Signal Type/ Termination	Description
62	CSI_DATA01/ECSP12_S0(CSI_DATA01)	CSI_DATA01/E3	I, 3.3V CMOS	Parallel camera data 1.
63	CSI_DATA03/ECSP12_MISO(CSI_DATA03)	CSI_DATA03/E1	I, 3.3V CMOS	Parallel camera data 3.
64	JTAG_TMS/SAI2_MCLK	JTAG_TMS/P14	IO, 3.3V CMOS	Audio Master Clock. <i>Note: Same signal is also connected to 199th pin of SODIMM edge connector.</i>
65	GND	NA	Power	Ground.
66	CSI_DATA00/ECSP12_CLK(CSI_DATA00)	CSI_DATA00/E4	I, 3.3V CMOS	Parallel camera data 0.
67	JTAG_TRST_B/SAI2_TX_DATA	JTAG_TRST_B/N14	O, 3.3V CMOS	Audio Transmit data. <i>Note: Same signal is also connected to 193rd pin of SODIMM edge connector.</i>
68	GPIO5_IO1(SNVS_TAMPER1)	SNVS_TAMPER1/R9	IO, 3.3V CMOS	Tamper Detection Pin 1 (Or) General purpose input/output. <i>Important Note: In i.MX6UL3 SODIMM SOM, this pin can be used as only Tamper functionality. In all other i.MX6UL/i.MX6ULL CPU version SODIMM SOM, this pin can be used as only GPIO functionality.</i>
69	JTAG_MOD	JTAG_MOD/P15	I, 3.3V CMOS/ 10K PD	JTAG controller mode selection pin.
70	CSI_DATA02/ECSP12_MOSI(CSI_DATA02)	CSI_DATA02/E2	I, 3.3V CMOS	Parallel camera data 2.
71	NC	NA	-	Default NC. <i>Note: GPIO1_IO07 is optionally connected to this pin (for ENET_MDC) through resistor and default not populated.</i> <i>Note: Same signal is by default connected to On SOM Ethernet PHY's.</i>
72	VIN_3V3	NA	I, 3.3V Power	Supply Voltage.
73	GPIO5_IO2(SNVS_TAMPER2)	SNVS_TAMPER2/P11	IO, 3.3V CMOS	Tamper Detection Pin 2 (Or) General purpose input/output. <i>Important Note: In i.MX6UL3 SODIMM SOM, this pin can be used as only Tamper functionality. In all other i.MX6UL/i.MX6ULL CPU version SODIMM SOM, this pin can be used as only GPIO functionality.</i>
74	USB_OTG1_CHD_B	USB_OTG1_CHD_B/U16	I, 3.3V CMOS	USB Charge Detect.

i.MX6UL/i.MX6ULL SODIMM SOM Hardware User Guide

Pin No.	SODIMM Edge Connector Pin Name	i.MX6UL/i.MX6ULL Ball Name/ Pin Number	Signal Type/ Termination	Description
75	UART5_CTS(GPIO1_IO09)	GPIO1_IO09/M15	O, 3.3V CMOS	UART5 ready to receive data.
76	USB_OTG1_OC(GPIO1_IO01)	GPIO1_IO01/L15	I, 3.3V CMOS	Over current sense for USB OTG1.
77	USB_OTG1_ID(GPIO1_IO00)	GPIO1_IO00/K13	I, 3.3V CMOS	USB OTG ID to identify Host & Device.
78	USB_OTG1_PWR(GPIO1_IO04)	GPIO1_IO04/M16	O, 3.3V CMOS	Power enable signal to control USB Power switch, to supply VBUS voltage
79	GND	NA	Power	Ground.
80	NC	NA	-	Default NC. <i>Note: GPIO1_IO06 is optionally connected to this pin (for ENET_MDIO) through resistor and default not populated.</i> <i>Note: Same signal is by default connected to On SOM Ethernet PHY's.</i>
81	USB_OTG_DP	USB_OTG_DP/U15	IO, DIFF	USB OTG1 data positive.
82	NC	NA	-	NC.
83	USB_OTG_DN	USB_OTG_DN/T15	IO, DIFF	USB OTG1 data negative.
84	NC	NA	-	NC.
85	NC	NA	-	NC.
86	GPIO5_IO3(SNVS_TAMPER3)	SNVS_TAMPER3/P10	IO, 3.3V CMOS	Tamper Detection Pin 3 (Or) General purpose input/output. <i>Important Note: In i.MX6UL3 SODIMM SOM, this pin can be used as only Tamper functionality. In all other i.MX6UL/i.MX6ULL CPU version SODIMM SOM, this pin can be used as only GPIO functionality.</i>
87	NC	NA	-	NC.
88	VIN_3V3	NA	I, 3.3V Power	Supply Voltage.
89	JTAG_TDO/SAI2_TX_SYNC	JTAG_TDI/N16	O, 3.3V CMOS	Audio transmit frame synchronization. <i>Note: Same signal is also connected to 191st pin of SODIMM edge connector.</i>
90	JTAG_TDI/SAI2_TX_BCLK	JTAG_TDO/N15	O, 3.3V CMOS	Audio transmit clock. <i>Note: Same signal is also connected to 195th pin of SODIMM edge connector.</i>
91	NC	NA	-	Default NC. <i>Note: Boot_Mode0 is optionally connected to this pin (for GPIO) through resistor and default not populated.</i>

Pin No.	SODIMM Edge Connector Pin Name	i.MX6UL/i.MX6ULL Ball Name/ Pin Number	Signal Type/ Termination	Description
92	NC	NA	-	Default NC. <i>Note: Boot_Mode1 is optionally connected to this pin (for GPIO) through resistor and default not populated.</i>
93	CSI_DATA05	CSI_DATA05/ D3	I, 3.3V CMOS	Parallel camera data 05.
94	NC	NA	-	Default NC. <i>Note: UART3_RTS_B is optionally connected to this pin (for UART3 Ready to send data function) through resistor and default not populated.</i>
95	GND	NA	Power	Ground.
96	NC	NA	-	NC.
97	NC	NA	-	Default NC. <i>Note: UART3_CTS_B is optionally connected to this pin (for UART3 Ready to receive data function) through resistor and default not populated.</i>
98	UART2_TX_DATA	UART2_TX_DATA/ J17	O, 3.3V CMOS	UART2 serial data transmitter.
99	UART2_RX_DATA	UART2_RX_DATA/ J16	I, 3.3V CMOS	UART2 serial data receiver.
100	NC	NA	-	Default NC. <i>Note: UART2_CTS_B is optionally connected to this pin (for UART2 Ready to receive data function) through resistor and default not populated.</i>
101	NC	NA	-	Default NC. <i>Note: UART2_RTS_B is optionally connected to this pin (for UART2 Ready to send data function) through resistor and default not populated.</i>
102	UART5_TX_DATA	UART5_TX_DATA/ F17	O, 3.3V CMOS	UART5 serial data transmitter.
103	UART5_RX_DATA	UART5_RX_DATA/ G13	I, 3.3V CMOS	UART5 serial data receiver.
104	CSI_DATA04	CSI_DATA04/ D4	I, 3.3V CMOS	Parallel camera data 4.
105	SD1_CD_B(UART1_RTS_B)	UART1_RTS_B/ J14	I, 3.3V CMOS	SD Card Detect.
106	VIN_3V3	NA	I, 3.3V Power	Supply Voltage.

Pin No.	SODIMM Edge Connector Pin Name	i.MX6UL/i.MX6ULL Ball Name/ Pin Number	Signal Type/ Termination	Description
107	SD1_DATA0	SD1_DATA0/ B3	IO, 3.3V CMOS	SD1 Data0.
108	SD1_CMD	SD1_CMD/ C2	IO, 3.3V CMOS	SD1 command.
109	SD1_CLK	SD1_CLK/ C1	O, 3.3V CMOS	SD1 clock.
110	CSI_DATA06	CSI_DATA06/ D2	I, 3.3V CMOS	Parallel camera data 06.
111	SD1_DATA1	SD1_DATA1/ B2	IO, 3.3V CMOS	SD1 Data1.
112	SD1_DATA2	SD1_DATA2/ B1	IO, 3.3V CMOS	SD1 Data2.
113	GND	NA	Power	Ground.
114	SD1_DATA3	SD1_DATA3/ A2	IO, 3.3V CMOS	SD1 Data3.
115	I2C1_SDA(UART4_RX_DATA)_SODIMM	UART4_RX_DATA/ G16	IO, 3.3V OD/ 4.7K PU	I2C1 data. <i>Note: Same signal is optionally connected to 19th pin of SODIMM Edge connector.</i>
116	I2C1_SCL(UART4_TX_DATA)_SODIMM	UART4_TX_DATA/ G17	O, 3.3V OD/ 4.7K PU	I2C1 clock. <i>Note: Same signal is optionally connected to 18th pin of SODIMM Edge connector.</i>
117	UART1_RX_DATA	UART1_RX_DATA/ K16	I, 3.3V CMOS	UART1 serial data receiver.
118	UART1_TX_DATA	UART1_TX_DATA/ K14	O, 3.3V CMOS	UART1 serial data transmitter.
119	CSIO_PIXCLK	CSIO_PIXCLK/ E5	I, 3.3V CMOS	Parallel camera PIXCLK.
120	CSI_DATA07	CSI_DATA07/ D1	I, 3.3V CMOS	Parallel camera data 07.
121	CSIO_VSYNC	CSIO_VSYNC/ F2	I, 3.3V CMOS	Parallel camera VSYNC.
122	CSIO_MCLK	CSIO_MCLK/ F5	O, 3.3V CMOS	Parallel Camera Master Clock.
123	CSIO_HSYNC	CSIO_HSYNC/ F3	I, 3.3V CMOS	Parallel Camera HSYNC.
124	VIN_3V3	NA	I, 3.3V Power	Supply Voltage.
125	NC	NA	-	NC.
126	GPIO1_IO18(UART1_CTS_B)	UART1_CTS_B/ K15	IO, 3.3V CMOS	General purpose input/output.
127	NC	NA	-	NC.
128	NC	NA	-	NC.

Pin No.	SODIMM Edge Connector Pin Name	i.MX6UL/i.MX6ULL Ball Name/ Pin Number	Signal Type/ Termination	Description
129	NC	NA	-	NC.
130	NC	NA	-	NC.
131	GND	NA	Power	Ground.
132	GPIO3_IO04(LCD_RESET)	LCD_RESET/E9	IO, 3.3V CMOS	General purpose input/output.
133	GPIO5_IO7(SNVS_TAMPER7)	SNVS_TAMPER7/N10	IO, 3.3V CMOS	Tamper Detection Pin 7 (Or) General purpose input/output. <i>Important Note: In i.MX6UL3 SODIMM SOM, this pin can be used as only Tamper functionality. In all other i.MX6UL/i.MX6ULL CPU version SODIMM SOM, this pin can be used as only GPIO functionality.</i>
134	GPIO5_IO8(SNVS_TAMPER8)	SNVS_TAMPER8/N9	IO, 3.3V CMOS	Tamper Detection Pin 8 (Or) General purpose input/output. <i>Important Note: In i.MX6UL3 SODIMM SOM, this pin can be used as only Tamper functionality. In all other i.MX6UL/i.MX6ULL CPU version SODIMM SOM, this pin can be used as only GPIO functionality.</i>
135	CCM_CLK1_P	CCM_CLK1_P/P17	IO, DIFF	Clock Controller Module positive Clock.
136	GPIO5_IO9(SNVS_TAMPER9)	SNVS_TAMPER9/R6	IO, 3.3V CMOS	Tamper Detection Pin 9 (Or) General purpose input/output. <i>Important Note: In i.MX6UL3 SODIMM SOM, this pin can be used as only Tamper functionality. In all other i.MX6UL/i.MX6ULL CPU version SODIMM SOM, this pin can be used as only GPIO functionality.</i>
137	CCM_CLK1_N	CCM_CLK1_N/P16	IO, DIFF	Clock Controller Module negative Clock.
138	NAND_DQS/QSPI_A_S0_B/PWM5_OUT	NAND_DQS/E6	O, 3.3V CMOS	Pulse Width Modulation 5 Output.
139	NC	NA	-	Default NC. <i>Note: GPIO1_IO05 is optionally connected to this pin (for OTG2_ID) through resistor and default not populated.</i>
140	USB_OTG2_PWR(GPIO1_IO02)	GPIO1_IO02/L14	O, 3.3V CMOS	Power enable signal to control USB Power switch, to supply VBUS voltage

Pin No.	SODIMM Edge Connector Pin Name	i.MX6UL/i.MX6ULL Ball Name/ Pin Number	Signal Type/ Termination	Description
141	USB_OTG2_VBUS	USB_OTG2_VBUS/ U12	I, 5V Power	Default NC. <i>Note: USB_OTG2_VBUS is optionally connected to this pin (for OTG2 VBUS) through resistor and default not populated.</i>
142	VIN_3V3	NA	I, 3.3V Power	Supply Voltage.
143	LCD_VSYNC	LCD_VSYNC/ C9	O, 3.3V CMOS	Parallel LCD VSYNC.
144	LCD_HSYNC	LCD_HSYNC/ D9	O, 3.3V CMOS	Parallel LCD HSYNC.
145	LCD_CLK	LCD_CLK/ A8	O, 3.3V CMOS	Parallel LCD Clock.
146	LCD_ENABLE	LCD_ENABLE/ B8	O, 3.3V CMOS	Parallel LCD Enable.
147	PWM4_OUT(GPIO1_IO05)	GPIO1_IO05/ M17	O, 3.3V CMOS	Pulse Width Modulation 4 Output.
148	LCD_DATA16 ¹	LCD_DATA16/ C13	O, 3.3V CMOS/ 10K PD ²	Parallel LCD data 16 (Red data0).
149	LCD_DATA17 ¹	LCD_DATA17/ B13	O, 3.3V CMOS/ 10K PD ²	Parallel LCD data 17 (Red data1).
150	LCD_DATA18 ¹	LCD_DATA18/ A13	O, 3.3V CMOS/ 10K PD ²	Parallel LCD data 18 (Red data2).
151	GND	NA	Power	Ground.
152	LCD_DATA19 ¹	LCD_DATA19/ D14	O, 3.3V CMOS/ 10K PD ²	Parallel LCD data 19 (Red data4).
153	LCD_DATA20 ¹	LCD_DATA20/ C14	O, 3.3V CMOS/ 10K PD ²	Parallel LCD data 20 (Red data5).
154	LCD_DATA21 ¹	LCD_DATA21/ B14	O, 3.3V CMOS/ 10K PD ²	Parallel LCD data 21 (Red data6).
155	LCD_DATA22 ¹	LCD_DATA22/ A14	O, 3.3V CMOS/ 10K PD ²	Parallel LCD data 22 (Red data7).
156	LCD_DATA23 ¹	LCD_DATA23/ B16	O, 3.3V CMOS/ 10K PD ²	Parallel LCD data 23 (Red data8).
157	LCD_DATA08 ¹	LCD_DATA08/ B11	O, 3.3V CMOS/ 10K PD ²	Parallel LCD data 8 (Green data0).
158	LCD_DATA09 ¹	LCD_DATA09/ A11	O, 3.3V CMOS/ 10K PD ²	Parallel LCD data 9 (Green data1).
159	LCD_DATA10 ¹	LCD_DATA10/ E12	O, 3.3V CMOS/ 10K PD ²	Parallel LCD data 10 (Green data2).
160	VIN_3V3	NA	I, 3.3V Power	Supply Voltage.
161	LCD_DATA11 ¹	LCD_DATA11/ D12	O, 3.3V CMOS/ 10K PD ²	Parallel LCD data 11 (Green data3).

Pin No.	SODIMM Edge Connector Pin Name	i.MX6UL/i.MX6ULL Ball Name/ Pin Number	Signal Type/ Termination	Description
162	LCD_DATA12 ¹	LCD_DATA12/ C12	O, 3.3V CMOS/ 10K PD ²	Parallel LCD data 12 (Green data4).
163	LCD_DATA13 ¹	LCD_DATA13/ B12	O, 3.3V CMOS/ 10K PD ²	Parallel LCD data 13 (Green data5).
164	LCD_DATA14 ¹	LCD_DATA14/ A12	O, 3.3V CMOS/ 10K PD ²	Parallel LCD data 14 (Green data6).
165	LCD_DATA15 ¹	LCD_DATA15/ D13	O, 3.3V CMOS/ 10K PD ²	Parallel LCD data 15 (Green data7).
166	LCD_DATA00 ¹	LCD_DATA00/ B9	O, 3.3V CMOS/ 10K PD ²	Parallel LCD data 0 (Blue data0).
167	LCD_DATA01 ¹	LCD_DATA01/ A9	O, 3.3V CMOS/ 10K PD ²	Parallel LCD data 1 (Blue data1).
168	LCD_DATA02 ¹	LCD_DATA02/ E10	O, 3.3V CMOS/ 10K PD ²	Parallel LCD data 2 (Blue data2).
169	GND	NA	Power	Ground.
170	LCD_DATA03 ¹	LCD_DATA03/ D10	O, 3.3V CMOS/ 10K PD ²	Parallel LCD data 3 (Blue data3).
171	LCD_DATA04 ¹	LCD_DATA04/ C10	O, 3.3V CMOS/ 1K PU ²	Parallel LCD data 4 (Blue data4).
172	LCD_DATA05 ¹	LCD_DATA05/ B10	O, 3.3V CMOS/ 10K PD ²	Parallel LCD data 5 (Blue data5).
173	LCD_DATA06 ¹	LCD_DATA06/ A10	O, 3.3V CMOS/ 10K PD ²	Parallel LCD data 6 (Blue data6).
174	LCD_DATA07 ¹	LCD_DATA07/ D11	O, 3.3V CMOS/ 1K PU ²	Parallel LCD data 7 (Blue data7).
175	CAN2_RXD(UART2_RT S_B)	UART2_RTS_B/ H14	I, 3.3V CMOS	Receive input for CAN2 bus.
176	CAN1_RXD(UART3_RT S_B)	UART3_RTS_B/ G14	I, 3.3V CMOS	Receive input for CAN1 bus.
177	CAN2_TXD(UART2_CT S_B)	UART2_CTS_B/ J15	O, 3.3V CMOS	Transmit output for CAN2 bus.
178	CAN1_TXD(UART3_CT S_B)	UART3_CTS_B/ H15	O, 3.3V CMOS	Transmit output for CAN1 bus.
179	ON_OFF	ON_OFF/ R8	I, 3V CMOS	Power button input from Carrier card. <i>Important Note: This pin is directly connected to i.MX6UL/i.MX6ULL CPU's ONOFF pin which has internal pullup and so don't add any external pullup in carrier board on this pin.</i>
180	VIN_3V3	NA	I, 3.3V Power	Supply Voltage.
181	GND	NA	Power	Ground.

Pin No.	SODIMM Edge Connector Pin Name	i.MX6UL/i.MX6ULL Ball Name/ Pin Number	Signal Type/ Termination	Description
182	BOOT_MODE0	BOOT_MODE0/ T10	I, 3.3V CMOS/ 4.7K PU	Boot Mode Select bit0. <i>Important Note: This pin is directly connected to i.MX6UL/i.MX6ULL CPU's BOOT_MODE0 pin with On-SOM pullup and so don't add any external pullup in carrier board on this pin. Make sure to use this pin in carrier board to select desired boot mode by driving only low if required.</i>
183	VRTC_3V0	NA	I, 3V Power	3V backup coin cell input for RTC.
184	BOOT_MODE1	BOOT_MODE1/ U10	I, 3.3V CMOS/ 4.7K PU	Boot Mode Select bit1. <i>Important Note: This pin is directly connected to i.MX6UL/i.MX6ULL CPU's BOOT_MODE1 pin with On-SOM pullup and so don't add any external pullup in carrier board on this pin. Make sure to use this pin in carrier board to select desired boot mode by driving only low if required.</i>
185	GND	NA	Power	Ground.
186	GND	NA	Power	Ground.
187	POR_B	POR_B/ P8	I, 3V CMOS	Active low reset button input. <i>Important Note: This pin is directly connected to i.MX6UL/i.MX6ULL CPU's POR pin which has internal pullup and so don't add any external pullup in carrier board on this pin. Also use this pin only for connecting the reset push button in carrier board.</i>
188	USB_OTG2_DP	USB_OTG2_DP/ U13	IO, 3.3V CMOS	USB OTG2 data positive.
189	NC	NA	-	NC.
190	USB_OTG2_DN	USB_OTG2_DN/ T13	IO, 3.3V CMOS	USB OTG2 data negative.
191	JTAG_TDO/SAI2_TX_S YNC	JTAG_TDO/ N15	O, 3.3V CMOS	JTAG Test Data Output. <i>Note: Same signal is also connected to 89th pin of SODIMM edge connector.</i>
192	VIN_3V3	NA	I, 3.3V Power	Supply Voltage.
193	JTAG_TRST_B/SAI2_TX _DATA	JTAG_TRST_B/ N14	I, 3.3V CMOS	JTAG reset. <i>Note: Same signal is also connected to 67th pin of SODIMM edge connector.</i>
194	NC	NA	-	NC.

Pin No.	SODIMM Edge Connector Pin Name	i.MX6UL/i.MX6ULL Ball Name/ Pin Number	Signal Type/ Termination	Description
195	JTAG_TDI/SAI2_TX_BCLK	JTAG_TDI/ N16	I, 3.3V CMOS	JTAG Test Data Input <i>Note: Same signal is also connected to 90th pin of SODIMM edge connector.</i>
196	NC	NA	-	NC.
197	JTAG_TCK/SAI2_RX_DATA	JTAG_TCK/ M14	I, 3.3V CMOS	JTAG Test Clock. <i>Note: Same signal is also connected to 61st pin of SODIMM edge connector.</i>
198	GND	NA	Power	Ground.
199	JTAG_TMS/SAI2_MCLK	JTAG_TMS/ P14	I, 3.3V CMOS	JTAG Test Mode Select. <i>Note: Same signal is also connected to 64th pin of SODIMM edge connector.</i>
200	USB_OTG1_VBUS	USB_OTG1_VBUS/ T12	I, Power 5V	Input voltage to drive the internal USB LDO. <i>Important Note: It is better to provide the always ON 5V power to this pin for USB block to work properly in i.MX6UL/i.MX6ULL CPU.</i>

¹ Important Note: These signals are also used for i.MX6UL/i.MX6ULL CPU bootstrap setting on SOM and so no external loads or pull-up/pull-down resistors to be connected to these pins which will change the boot configuration.

² Termination value is mentioned based on NAND flash as boot media. If boot media is changed, termination value also may change.

2.7 Optional Features

i.MX6UL/i.MX6ULL SODIMM SOM has PCB footprint option for some features which are not supported by default. These optional features are explained in the following sections.

To add any of these optional features in i.MX6UL/i.MX6ULL SODIMM SOM, please contact iWave.

2.7.1 eMMC Flash

i.MX6UL/i.MX6ULL SODIMM SOM supports an eMMC memory as mass storage and also can be used as boot device. eMMC is directly connected to the uSDHC2 of the i.MX6UL/i.MX6ULL CPU and operating at 3.3V Voltage level. This is the optional feature and will not be populated in default configuration.

Note: If eMMC flash feature is required in the SOM, NAND flash and Micro SD on SOM cannot be used.

2.7.2 Micro SD Slot

i.MX6UL/i.MX6ULL SODIMM SOM supports Micro SD slot to connect Micro SD card for Mass storage and also can be used as Boot device. Micro SD Card Connector (J2) is directly connected to the uSDHC2 of the i.MX6UL/i.MX6ULL CPU. It supports card detect feature. The main power to Micro SD Card Connector is 3.3Voltage. This is the optional feature and will not be populated in default configuration.

Note: If Micro SD feature is required in the SOM, NAND flash and eMMC on SOM cannot be used.

2.7.3 QSPI Flash

The i.MX6UL/i.MX6ULL SODIMM SOM supports QSPI Flash which can be used as boot device. QSPI Flash is connected to QSPI_A interface of the i.MX6UL/i.MX6ULL CPU and operating at 3.3 Voltage level. This is the optional feature and will not be populated in default configuration.

Note: If QSPI Flash feature is required in the SOM, NAND flash on SOM cannot be used.

2.7.4 PMIC OTP Header

By default, i.MX6UL/i.MX6ULL SODIMM SOM supports NXP's PF3001 PMIC. Alternatively i.MX6UL/i.MX6ULL SODIMM SOM can also support NXP's PMIC PF3000 which has programmable output voltage, frequency, start-up sequence and timing.

i.MX6UL/i.MX6ULL SODIMM SOM supports 6Pin PMIC OTP header for PMIC OTP fuse programming. PMIC OTP Header is used to program PF3000 to desired configuration. This is the optional feature and will not be populated in default configuration. PMIC OTP Header is physically located on top side of the SOM as shown below.



Figure 5: PMIC OTP Header

Number of Pins	- 06
Connector Part	- GRPB061VWVN-RC from Sullins Connector Solutions
Mating Connector	- LPPB061NGCN-RC from Sullins Connector Solutions

Table 6: PMIC OTP Header Pin Assignment

Pin No	Signal Name	Signal Type/ Termination	Description
1	VDDOTP	I, Power	Supply voltage to PMIC OTP fuses.
2	VIN_3V3	I, Power	Input Voltage.
3	GND	I, Power	Ground.
4	I2C1_SCL(UART4_TX_DATA)_PMIC	I, 3.3V OD	I2C clock.
5	I2C1_SDA(UART4_RX_DATA)_PMIC	IO, 3.3V OD	I2C data.
6	PWRON	I, Power	Power ON/OFF input from CPU.

2.8 i.MX6UL/i.MX6ULL Pin Multiplexing on SODIMM Edge

The i.MX6UL/i.MX6ULL CPU's IO pins have many alternate functions and can be configured to any one of the alternate functions based on the requirement. Also most of the i.MX6UL/i.MX6ULL CPU's IO pins can be configured as GPIO if required. The below table provides the details of i.MX6UL/i.MX6ULL CPU pin connections to the SOM edge connector with selected pin function and available alternate functions. This table has been prepared by referring NXP's i.MX6UL Applications Processor Reference Manual (Rev0).

Important Note: It is strongly recommended to use the pin function same as selected in the i.MX6UL/i.MX6ULL SODIMM SOM Edge connector for iWave's BSP reusability and to have compatible SODIMM modules in future for upgradability.

Table 7: IOMUX Configuration of i.MX6UL/i.MX6ULL SODIMM SOM Edge Connector interfaces

Interface/ Function	SODIMM Edge Pin No	i.MX6UL/ i.MX6ULL CPU Pad Name	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	ALT8	Default/Reset State
Debug UART (UART1)	117	UART1_RX_D ATA	UART1_RX	ENET1_RDA TA03	I2C3_SDA	CSI_DATA03	GPT1_CLK	GPIO1_IO17			SPDIF_IN	UART1_RX
	118	UART1_TX_D ATA	UART1_TX	ENET1_RDA TA02	I2C3_SCL	CSI_DATA02	GPT1_COMP ARE1	GPIO1_IO16			SPDIF_OUT	UART1_TX
Data UART5	102	UART5_RX_D ATA	UART5_RX	ENET2_COL	I2C2_SDA	CSI_DATA15	CSU_CSU_IN T_DEB	GPIO1_IO31			ECSPI2_MIS O	UART5_RX
	103	UART5_TX_D ATA	UART5_TX	ENET2_CRS	I2C2_SCL	CSI_DATA14	CSU_CSU_AL ARM_AUT00	GPIO1_IO30			ECSPI2_MOS I	UART5_TX
	75	GPIO1_IO09	PWM2_OUT	WDOG1_W DOG_ANY	SPDIF_IN	CSI_HSYNC	USDHC2_RE SET_B	GPIO1_IO09	USDHC1_RE SET_B		UART5_CTS_ B	GPIO1_IO09
	38	GPIO1_IO08	PWM1_OUT	WDOG1_W DOG_B	SPDIF_OUT	CSI_VSYNC	USDHC2_VS ELECT	GPIO1_IO08	CCM_PMIC_ RDY		UART5_RTS_ B	GPIO1_IO08
Data UART2	99	UART2_RX_D ATA	UART2_RX	ENET1_TDA TA03	I2C4_SDA	CSI_DATA07	GPT1_CAPT URE2	GPIO1_IO21		SJC_DONE	ECSPI3_SCLK	UART2_RX
	98	UART2_TX_D ATA	UART2_TX	ENET1_TDA TA02	I2C4_SCL	CSI_DATA06	GPT1_CAPT URE1	GPIO1_IO20			ECSPI3_SS0	UART2_TX

i.MX6UL/i.MX6ULL SODIMM SOM Hardware User Guide

Interface/ Function	SODIMM Edge Pin No	i.MX6UL/ i.MX6ULL CPU Pad Name	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	ALT8	Default/Reset State
Data UART3	7	UART3_RX_D ATA	UART3_RX	ENET2_RDA TA03	SIM2_PORT 0_PD	CSI_DATA00	UART2_RTS_ B	GPIO1_IO25			EPIT1_OUT	UART3_RX
	9	UART3_TX_D ATA	UART3_TX	ENET2_RDA TA02	SIM1_PORT 0_PD	CSI_DATA01	UART2_CTS_ B	GPIO1_IO24		SJC_JTAG_A CT	ANATOP_OT G1_ID	UART3_TX
CAN Port1	178	UART3_CTS_B	UART3_CTS_ B	ENET2_RX_ CLK	FLEXCAN1_ TX	CSI_DATA10	ENET1_1588 _EVENT1_IN	GPIO1_IO26			EPIT2_OUT	UART3_CTS_B
	176	UART3_RTS_B	UART3_RTS_ B	ENET2_TX_ ER	FLEXCAN1_ RX	CSI_DATA11	ENET1_1588 _EVENT1_O UT	GPIO1_IO27			WDOG1_WD OG_B	UART3_RTS_B
CAN Port2	177	UART2_CTS_B	ENET1_CRS	FLEXCAN2_ TX	CSI_DATA0 8	GPT1_COMP ARE2	GPT1_COMP ARE2		GPT1_COMP ARE2	ECSPI3_MOS I	ECSPI3_MOS I	UART2_CTS_B
	175	UART2_RTS_B	ENET1_COL	FLEXCAN2_ RX	CSI_DATA0 9	GPT1_COMP ARE3	GPIO1_IO23		SJC_FAIL	ECSPI3_MIS O	ECSPI3_MIS O	UART2_RTS_B
SD1	109	SD1_CLK	USDHC1_CL K	GPT2_COM PARE2	SAI2_MCLK	SPDIF_IN	EIM_ADDR2 0	GPIO2_IO17			USB_OTG1_ OC	USDHC1_CLK
	108	SD1_CMD	USDHC1_C MD	GPT2_COM PARE1	SAI2_RX_SY NC	SPDIF_OUT	EIM_ADDR1 9	GPIO2_IO16	SDMA_EXT_ EVENT00		USB_OTG1_ PWR	USDHC1_CMD
	107	SD1_DATA0	USDHC1_DA TA0	GPT2_COM PARE3	SAI2_TX_SY NC	FLEXCAN1_T X	EIM_ADDR2 1	GPIO2_IO18			ANATOP_OT G1_ID	USDHC1_DATA 0
	111	SD1_DATA1	USDHC1_DA TA1	GPT2_CLK	SAI2_TX_BC LK	FLEXCAN1_R X	EIM_ADDR2 2	GPIO2_IO19			USB_OTG2_ PWR	USDHC1_DATA 1
	112	SD1_DATA2	USDHC1_DA TA2	GPT2_CAPT URE1	SAI2_RX_D ATA	FLEXCAN2_T X	EIM_ADDR2 3	GPIO2_IO20	CCM_CLKO1		USB_OTG2_ OC	USDHC1_DATA 2
	114	SD1_DATA3	USDHC1_DA TA3	GPT2_CAPT URE2	SAI2_TX_D ATA	FLEXCAN2_R X	EIM_ADDR2 4	GPIO2_IO21	CCM_CLKO2		ANATOP_OT G2_ID	USDHC1_DATA 3
	105	UART1_RTS_B	UART1_RTS_ B	ENET1_TX_ ER	USDHC1_C D_B	CSI_DATA05	ENET2_1588 _EVENT1_O UT	GPIO1_IO19			USDHC2_CD _B	UART1_RTS_B

i.MX6UL/i.MX6ULL SODIMM SOM Hardware User Guide

Interface/ Function	SODIMM Edge Pin No	i.MX6UL/ i.MX6ULL CPU Pad Name	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	ALT8	Default/Reset State
LCD	145	LCDIF_CLK	LCDIF_CLK	LCDIF_WR_RWN	UART4_TX	SAI3_MCLK	EIM_CS2_B	GPIO3_IO00			WDOG1_WDOG_RST_B_DEB	LCDIF_CLK
	166	LCDIF_DATA00	LCDIF_DATA00	PWM1_OUT		ENET1_1588_EVENT2_IN	I2C3_SDA	GPIO3_IO05	SRC_BT_CFG00		SAI1_MCLK	LCDIF_DATA00
	167	LCDIF_DATA01	LCDIF_DATA01	PWM2_OUT		ENET1_1588_EVENT2_OUT	I2C3_SCL	GPIO3_IO06	SRC_BT_CFG01		SAI1_TX_SYNC	LCDIF_DATA01
	168	LCDIF_DATA02	LCDIF_DATA02	PWM3_OUT		ENET1_1588_EVENT3_IN	I2C4_SDA	GPIO3_IO07	SRC_BT_CFG02		SAI1_TX_BCLK	LCDIF_DATA02
	170	LCDIF_DATA03	LCDIF_DATA03	PWM4_OUT		ENET1_1588_EVENT3_OUT	I2C4_SCL	GPIO3_IO08	SRC_BT_CFG03		SAI1_RX_DATA	LCDIF_DATA03
	171	LCDIF_DATA04	LCDIF_DATA04	UART8_CTS_B		ENET2_1588_EVENT2_IN	SPDIF_SRCLK	GPIO3_IO09	SRC_BT_CFG04		SAI1_TX_DATA	LCDIF_DATA04
	172	LCDIF_DATA05	LCDIF_DATA05	UART8_RTS_B		ENET2_1588_EVENT2_OUT	SPDIF_OUT	GPIO3_IO10	SRC_BT_CFG05		ECSP1_SS1	LCDIF_DATA05
	173	LCDIF_DATA06	LCDIF_DATA06	UART7_CTS_B		ENET2_1588_EVENT3_IN	SPDIF_LOCK	GPIO3_IO11	SRC_BT_CFG06		ECSP1_SS2	LCDIF_DATA06
	174	LCDIF_DATA07	LCDIF_DATA07	UART7_RTS_B		ENET2_1588_EVENT3_OUT	SPDIF_EXT_CLK	GPIO3_IO12	SRC_BT_CFG07		ECSP1_SS3	LCDIF_DATA07
	157	LCDIF_DATA08	LCDIF_DATA08	SPDIF_IN		CSI_DATA16	EIM_DATA00	GPIO3_IO13	SRC_BT_CFG08		FLEXCAN1_TX	LCDIF_DATA08
	158	LCDIF_DATA09	LCDIF_DATA09	SAI3_MCLK		CSI_DATA17	EIM_DATA01	GPIO3_IO14	SRC_BT_CFG09		FLEXCAN1_RX	LCDIF_DATA09
	159	LCDIF_DATA10	LCDIF_DATA10	SAI3_RX_SYNC		CSI_DATA18	EIM_DATA02	GPIO3_IO15	SRC_BT_CFG10		FLEXCAN2_TX	LCDIF_DATA10
	161	LCDIF_DATA11	LCDIF_DATA11	SAI3_RX_BCLK		CSI_DATA19	EIM_DATA03	GPIO3_IO16	SRC_BT_CFG11		FLEXCAN2_RX	LCDIF_DATA11
	162	LCDIF_DATA12	LCDIF_DATA12	SAI3_TX_SYNC		CSI_DATA20	EIM_DATA04	GPIO3_IO17	SRC_BT_CFG12		ECSP1_RDY	LCDIF_DATA12
	163	LCDIF_DATA13	LCDIF_DATA13	SAI3_TX_BCLK		CSI_DATA21	EIM_DATA05	GPIO3_IO18	SRC_BT_CFG13		USDHC2_RESET_B	LCDIF_DATA13

i.MX6UL/i.MX6ULL SODIMM SOM Hardware User Guide

Interface/ Function	SODIMM Edge Pin No	i.MX6UL/ i.MX6ULL CPU Pad Name	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	ALT8	Default/Reset State
	164	LCDIF_DATA14	LCDIF_DATA14	SAI3_RX_DATA		CSI_DATA22	EIM_DATA06	GPIO3_IO19	SRC_BT_CFG14		USDHC2_DATA4	LCDIF_DATA14
	165	LCDIF_DATA15	LCDIF_DATA15	SAI3_TX_DATA		CSI_DATA23	EIM_DATA07	GPIO3_IO20	SRC_BT_CFG15		USDHC2_DATA5	LCDIF_DATA15
	148	LCDIF_DATA16	LCDIF_DATA16	UART7_TX		CSI_DATA01	EIM_DATA08	GPIO3_IO21	SRC_BT_CFG24		USDHC2_DATA6	LCDIF_DATA16
	149	LCDIF_DATA17	LCDIF_DATA17	UART7_RX		CSI_DATA00	EIM_DATA09	GPIO3_IO22	SRC_BT_CFG25		USDHC2_DATA7	LCDIF_DATA17
	150	LCDIF_DATA18	LCDIF_DATA18	PWM5_OUT	CA7_MX6UL_EVENTO	CSI_DATA10	EIM_DATA10	GPIO3_IO23	SRC_BT_CFG26		USDHC2_CM D	LCDIF_DATA18
	152	LCDIF_DATA19	LCDIF_DATA19	PWM6_OUT	WDOG1_WDOG_ANY	CSI_DATA11	EIM_DATA11	GPIO3_IO24	SRC_BT_CFG27		USDHC2_CL K	LCDIF_DATA19
	153	LCDIF_DATA20	LCDIF_DATA20	UART8_TX	ECSPI1_SCLK	CSI_DATA12	EIM_DATA12	GPIO3_IO25	SRC_BT_CFG28		USDHC2_DATA0	LCDIF_DATA20
	154	LCDIF_DATA21	LCDIF_DATA21	UART8_RX	ECSPI1_SS0	CSI_DATA13	EIM_DATA13	GPIO3_IO26	SRC_BT_CFG29		USDHC2_DATA1	LCDIF_DATA21
	155	LCDIF_DATA22	LCDIF_DATA22	MQS_RIGHT	ECSPI1_MOSI	CSI_DATA14	EIM_DATA14	GPIO3_IO27	SRC_BT_CFG30		USDHC2_DATA2	LCDIF_DATA22
	156	LCDIF_DATA23	LCDIF_DATA23	MQS_LEFT	ECSPI1_MISO	CSI_DATA15	EIM_DATA15	GPIO3_IO28	SRC_BT_CFG31		USDHC2_DATA3	LCDIF_DATA23
	146	LCDIF_ENABLE	LCDIF_ENABLE	LCDIF_RD_E	UART4_RX	SAI3_TX_SYNC	EIM_CS3_B	GPIO3_IO01			ECSPI2_RDY	LCDIF_ENABLE
	144	LCDIF_HSYNC	LCDIF_HSYNC	LCDIF_RS	UART4_CTS_B	SAI3_TX_BCLK	WDOG3_WDOG_RST_B_DEB	GPIO3_IO02			ECSPI2_SS1	LCDIF_HSYNC
	143	LCDIF_VSYNC	LCDIF_VSYNC	LCDIF_BUSY	UART4_RTS_B	SAI3_RX_DATA	WDOG2_WDOG_B	GPIO3_IO03			ECSPI2_SS2	LCDIF_VSYNC

i.MX6UL/i.MX6ULL SODIMM SOM Hardware User Guide

Interface/ Function	SODIMM Edge Pin No	i.MX6UL/ i.MX6ULL CPU Pad Name	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	ALT8	Default/Reset State
Camera	66	CSI_DATA00	CSI_DATA00	USDHC2_DATA0	SIM1_PORT1_RST_B	ECSPI2_SCLK	EIM_AD00	GPIO4_IO21	SRC_INT_BOOT		UART5_TX	CSI_DATA02
	62	CSI_DATA01	CSI_DATA01	USDHC2_DATA1	SIM1_PORT1_SVEN	ECSPI2_SS0	EIM_AD01	GPIO4_IO22	SAI1_MCLK		UART5_RX	CSI_DATA03
	70	CSI_DATA02	CSI_DATA02	USDHC2_DATA2	SIM1_PORT1_TRXD	ECSPI2_MOSI	EIM_AD02	GPIO4_IO23	SAI1_RX_SYNC		UART5_RTSL_B	CSI_DATA04
	63	CSI_DATA03	CSI_DATA03	USDHC2_DATA3	SIM2_PORT1_PD	ECSPI2_MISO	EIM_AD03	GPIO4_IO24	SAI1_RX_BCLK		UART5_CTS_B	CSI_DATA05
	104	CSI_DATA04	CSI_DATA04	USDHC2_DATA4	SIM2_PORT1_CLK	ECSPI1_SCLK	EIM_AD04	GPIO4_IO25	SAI1_TX_SYNC		USDHC1_WP	CSI_DATA06
	93	CSI_DATA05	CSI_DATA05	USDHC2_DATA5	SIM2_PORT1_RST_B	ECSPI1_SS0	EIM_AD05	GPIO4_IO26	SAI1_TX_BCLK		USDHC1_CDB	CSI_DATA07
	110	CSI_DATA06	CSI_DATA06	USDHC2_DATA6	SIM2_PORT1_SVEN	ECSPI1_MOSI	EIM_AD06	GPIO4_IO27	SAI1_RX_DATA		USDHC1_RESET_B	CSI_DATA08
	120	CSI_DATA07	CSI_DATA07	USDHC2_DATA7	SIM2_PORT1_TRXD	ECSPI1_MISO	EIM_AD07	GPIO4_IO28	SAI1_TX_DATA		USDHC1_VSELECT	CSI_DATA09
	123	CSI_HSYNC	CSI_HSYNC	USDHC2_CMD	SIM1_PORT1_PD	I2C2_SCL	EIM_LBA_B	GPIO4_IO20	PWM8_OUT		UART6_CTS_B	CSI_HSYNC
	122	CSI_MCLK	CSI_MCLK	USDHC2_CDB	RAWNAND_CE2_B	I2C1_SDA	EIM_CS0_B	GPIO4_IO17	SNVS_HP_VIO_5_CTL		UART6_TX	CSI_MCLK
	119	CSI_PIXCLK	CSI_PIXCLK	USDHC2_WP	RAWNAND_CE3_B	I2C1_SCL	EIM_OE	GPIO4_IO18	SNVS_HP_VIO_5		UART6_RX	CSI_PIXCLK
	121	CSI_VSYNC	CSI_VSYNC	USDHC2_CLK	SIM1_PORT1_CLK	I2C2_SDA	EIM_RW	GPIO4_IO19	PWM7_OUT		UART6_RTSL_B	CSI_VSYNC
Audio	61	JTAG_TCK	SJC_TCK	GPT2_COMPARE2	SAI2_RX_DATA		PWM7_OUT	GPIO1_IO14			SIM2_POWER_FAIL	SJC_TCK
	90	JTAG_TDI	SJC_TDI	GPT2_COMPARE1	SAI2_TX_BCLK		PWM6_OUT	GPIO1_IO13	MQS_LEFT		SIM1_POWER_FAIL	SJC_TDI
	89	JTAG_TDO	SJC_TDO	GPT2_CAPTURE2	SAI2_TX_SYNC	CCM_CLKO2	CCM_STOP	GPIO1_IO12	MQS_RIGHT		EPIT2_OUT	SJC_TDO
	64	JTAG_TMS	SJC_TMS	GPT2_CAPTURE1	SAI2_MCLK	CCM_CLKO1	CCM_WAIT	GPIO1_IO11	SDMA_EXT_EVENT01		EPIT1_OUT	SJC_TMS
	67	JTAG_TRST_B	SJC_TRSTB	GPT2_COMPARE3	SAI2_TX_DATA		PWM8_OUT	GPIO1_IO15			CAAM_RNG_OSC_OBS	SJC_TRSTB

i.MX6UL/i.MX6ULL SODIMM SOM Hardware User Guide

Interface/ Function	SODIMM Edge Pin No	i.MX6UL/ i.MX6ULL CPU Pad Name	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	ALT8	Default/Reset State
USB OTG1	81	USB_OTG1_D P										USB_OTG1_DP
	83	USB_OTG1_D N										USB_OTG1_DN
	77	GPIO1_IO00	I2C2_SCL	GPT1_CAPT URE1	ANATOP_O TG1_ID	ENET1_REF_ CLK1	MQS_RIGHT	GPIO1_IO00	ENET1_1588 _EVENT0_IN	SRC_SYSTEM _RESET	WDOG3_WD OG_B	GPIO1_IO00
	76	GPIO1_IO01	I2C2_SDA	GPT1_COM PARE1	USB_OTG1 _OC	ENET2_REF_ CLK2	MQS_LEFT	GPIO1_IO01	ENET1_1588 _EVENT0_O UT	SRC_EARLY_ RESET	WDOG1_WD OG_B	GPIO1_IO01
	78	GPIO1_IO04	ENET1_REF_ _CLK1	PWM3_OUT	USB_OTG1 _PWR		USDHC1_RE SET_B	GPIO1_IO04	ENET2_1588 _EVENT0_IN		UART5_TX	GPIO1_IO04
USB OTG2	188	USB_OTG2_D P										USB_OTG2_DP
	190	USB_OTG2_D N										USB_OTG2_DN
	140	GPIO1_IO02	I2C1_SCL	GPT1_COM PARE2	USB_OTG2 _PWR	ENET1_REF_ CLK_25M	USDHC1_WP	GPIO1_IO02	SDMA_EXT_ EVENT00	SRC_ANY_P U_RESET	UART1_TX	GPIO1_IO02
	39	GPIO1_IO03	I2C1_SDA	GPT1_COM PARE3	USB_OTG2 _OC		USDHC1_CD _B	GPIO1_IO03	CCM_DIO_EX T_CLK	SRC_TESTER _ACK	UART1_RX	GPIO1_IO03
ENET2 – RMII Interface (Optional)	42	ENET2_RX_DA TA0	ENET2_RDA TA00	UART6_TX	SIM1_PORT 0_TRXD	I2C3_SCL	ENET1_MDI O	GPIO2_IO08	KPP_ROW04		USB_OTG1_ PWR	ENET2_RX_DA TA0
	44	ENET2_RX_DA TA1	ENET2_RDA TA01	UART6_RX	SIM1_PORT 0_CLK	I2C3_SDA	ENET1_MDC	GPIO2_IO09	KPP_COL04		USB_OTG1_ OC	ENET2_RX_DA TA1
	45	ENET2_RX_EN	ENET2_RX_ EN	UART7_TX	SIM1_PORT 0_RST_B	I2C4_SCL	EIM_ADDR2 6	GPIO2_IO10	KPP_ROW05		ENET1_REF_ CLK_25M	ENET2_RX_EN
	43	ENET2_RX_ER	ENET2_RX_ ER	UART8_RTS _B	SIM2_PORT 0_SVEN	ECSPI4_SS0	EIM_ADDR2 5	GPIO2_IO15	KPP_COL07		WDOG1_WD OG_ANY	ENET2_RX_ER
	35	ENET2_TX_CL K	ENET2_TX_ CLK	UART8_CTS _B	SIM2_PORT 0_RST_B	ECSPI4_MIS O	ENET2_REF_ CLK2	GPIO2_IO14	KPP_ROW07		ANATOP_OT G2_ID	ENET2_TX_CLK
	34	ENET2_TX_DA TA0	ENET2_TDA TA00	UART7_RX	SIM1_PORT 0_SVEN	I2C4_SDA	EIM_EB_B02	GPIO2_IO11	KPP_COL05			ENET2_TX_DA TA0
	36	ENET2_TX_DA TA1	ENET2_TDA TA01	UART8_TX	SIM2_PORT 0_TRXD	ECSPI4_SCLK	EIM_EB_B03	GPIO2_IO12	KPP_ROW06		USB_OTG2_ PWR	ENET2_TX_DA TA1
	37	ENET2_TX_EN	ENET2_TX_ EN	UART8_RX	SIM2_PORT 0_CLK	ECSPI4_MOS I	EIM_ACLK_F REERUN	GPIO2_IO13	KPP_COL06		USB_OTG2_ OC	ENET2_TX_EN

i.MX6UL/i.MX6ULL SODIMM SOM Hardware User Guide

Interface/ Function	SODIMM Edge Pin No	i.MX6UL/ i.MX6ULL CPU Pad Name	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	ALT8	Default/Reset State
I2C	115	UART4_RX_D ATA	UART4_RX	ENET2_TDA TA03	I2C1_SDA	CSI_DATA13	CSU_CSU_AL ARM_AUT01	GPIO1_IO29			ECSPI2_SS0	UART4_RX_DA TA
	116	UART4_TX_D ATA	UART4_TX	ENET2_TDA TA02	I2C1_SCL	CSI_DATA12	CSU_CSU_AL ARM_AUT02	GPIO1_IO28			ECSPI2_SCLK	UART4_TX_DA TA
PWM	147	GPIO1_IO05	ENET2_REF _CLK2	PWM4_OUT	ANATOP_O TG2_ID	CSI_FIELD	USDHC1_VS ELECT	GPIO1_IO05	ENET2_1588 _EVENT0_O UT		UART5_RX	GPIO1_IO05
	138	NAND_DQS	NAND_DQS	CSI_FIELD	QSPI_A_SS O_B	PWM5_OUT	EIM_WAIT	GPIO4_IO16	SDMA_EXT_ EVENT01		SPDIF_EXT_C LK	NAND_DQS
Tamper/ GPIOs¹	47	SNVS_TAMPE R0	snvs_lp_wra pper0	Reserved	Reserved	Reserved	Reserved	GPIO5_IO00	Reserved	Reserved	Reserved	SNVS_TAMPER 0
	68	SNVS_TAMPE R1	snvs_lp_wra pper1	Reserved	Reserved	Reserved	Reserved	GPIO5_IO01	Reserved	Reserved	Reserved	SNVS_TAMPER 1
	73	SNVS_TAMPE R2	snvs_lp_wra pper2	Reserved	Reserved	Reserved	Reserved	GPIO5_IO02	Reserved	Reserved	Reserved	SNVS_TAMPER 2
	86	SNVS_TAMPE R3	snvs_lp_wra pper3	Reserved	Reserved	Reserved	Reserved	GPIO5_IO03	Reserved	Reserved	Reserved	SNVS_TAMPER 3
	133	SNVS_TAMPE R7	snvs_lp_wra pper7	Reserved	Reserved	Reserved	Reserved	GPIO5_IO07	Reserved	Reserved	Reserved	SNVS_TAMPER 7
	134	SNVS_TAMPE R8	snvs_lp_wra pper8	Reserved	Reserved	Reserved	Reserved	GPIO5_IO08	Reserved	Reserved	Reserved	SNVS_TAMPER 8
	136	SNVS_TAMPE R9	snvs_lp_wra pper9	Reserved	Reserved	Reserved	Reserved	GPIO5_IO09	Reserved	Reserved	Reserved	SNVS_TAMPER 9

¹ Only i.MX6UL3 version CPU supports tamper functionality on these pins and doesn't support GPIO functionality. For all other i.MX6UL/i.MX6ULL CPU versions, these tamper pins are used as only GPIOs.

3. TECHNICAL SPECIFICATION

This section provides detailed information about the i.MX6UL/i.MX6ULL SODIMM SOM technical specification with Electrical, Environmental and Mechanical characteristics.

3.1 Electrical Characteristics

3.1.1 Power Input Requirement

The below table provides the Power Input Requirement of i.MX6UL/i.MX6ULL SODIMM SOM.

Table 8: Power Input Requirement

Sl. No.	Power Rail	Min (V)	Typical (V)	Max(V)	Max Input Ripple
1	VIN_3V3 ¹	3.15	3.3V	3.45	±50mV
2	VRTC_3V0 ²	2.8V	3V	3.3V	±20 mV

¹ i.MX6UL/i.MX6ULL SODIMM SOM is designed to work with VIN_3V3 input power rail from SODIMM Edge connector.

² i.MX6UL/i.MX6ULL SODIMM SOM uses this voltage as backup power source to RTC when VIN_3V3 is off. This is an optional power and required only if RTC functionality is used.

3.1.2 Power Input Sequencing

i.MX6UL/i.MX6ULL SODIMM SOM's Power Input sequence requirement is explained below.

Power up Sequence:

- VRTC_3V0 must come up at the same time or before VIN_3V3 comes up.

Power down Sequence:

- VIN_3V3 must go down at the same time or before VRTC_3V0 goes down.

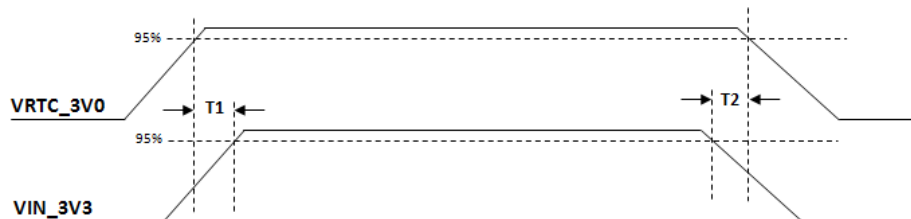


Figure 6: i.MX6UL/i.MX6ULL SODIMM SOM Power Sequence

Table 9: Power Sequence Timing

Item	Description	Value
T1	VRTC_3V0 rise time to VIN_3V3 rise time	≥ 0 ms
T2	VIN_3V3 fall time to VRTC_3V0 fall time	≥ 0 ms

Note: VRTC_3V0 is an optional power and required only if RTC functionality is used.

Important Note: i.MX6UL/i.MX6ULL CPU IO pins should not be externally driven from the carrier board until VIN_3V3 is powered up. Otherwise this can cause internal latch-up and malfunctions due to reverse current flows.

3.1.3 Power Consumption

Table 10: Power Consumption

Task/Status ¹	Power Rail	Current Drawn (A)/ Power Consumption (W)
Run Mode Power Consumption		
MP3 audio playback	VIN_3V3	0.196/0.647W
USB to Micro SD file transfer	VIN_3V3	0.237/0.782W
Dhrystone benchmark application	VIN_3V3	0.164/0.541W
Typical Maximum Power: • MP3 audio playback • USB to Micro SD file transfer • Dhrystone benchmark application • 100Mbps Ethernet ping on ENET1 & ENET2	VIN_3V3	0.265/0.875W
Low Power Mode Power Consumption		
System Idle Mode.	VIN_3V3	0.031/0.102W
Deep Sleep Mode.	VIN_3V3	0.103/0.339W
RTC power when no VIN_3V3 supply is provided	VRTC_3V0	500uA ²

¹ Power consumption measurements have been done in iWave's i.MX6UL3 CPU based SODIMM SOM with iWave's SODIMM Carrier board running iWave's Linux3.14.38 BSP (iW-RainboW-G18M-SM-R2.0-REL1.0-Linux3.14.38-YoctoFido_Deliverables).

² i.MX6UL/i.MX6ULL CPU's RTC controller draws more power from VRTC_3V0 coin cell power input and so could drain the coin cell faster.

3.2 Environmental Characteristics

3.2.1 Environmental Specification

The below table provides the Environment specification of i.MX6UL/i.MX6ULL SODIMM SOM.

Table 11: Environmental Specification

Parameters	Min	Max
Operating temperature range (Industrial) ¹	-40°C	85°C
Operating temperature range (Commercial) ¹	0°C	70°C

¹ iWave guarantees the component selection for the given operating temperature. The operating temperature at the system level will be affected by the various system components like carrier board and its components, system enclosure, air circulation in the system, system power supply etc. Based on the system design, specific heat dissipating approach might be required from system to system. It is recommended to do the necessary system level thermal simulation and find necessary thermal solution in the system before using this board in the end application.

3.2.2 RoHS Compliance

iWave's i.MX6UL/i.MX6ULL SODIMM SOM is designed by using RoHS compliant components and manufactured on lead free production process.

3.2.3 Electrostatic Discharge

iWave's i.MX6UL/i.MX6ULL SODIMM SOM is sensitive to electro static discharge and so high voltages caused by static electricity could damage some of the devices on board. It is packed with necessary protection while shipping. Do not open or use the SOM except at an electrostatic free workstation.

3.3 Mechanical Characteristics

3.3.1 SODIMM SOM Mechanical Dimensions

i.MX6UL/i.MX6ULL SODIMM SOM PCB size is 67.6mm x 29mm x 1mm. SODIMM SOM mechanical dimension is shown below. Please refer the JEDEC Physical standard DDR S.O.DIMM specification for SODIMM Edge connector mechanical details.

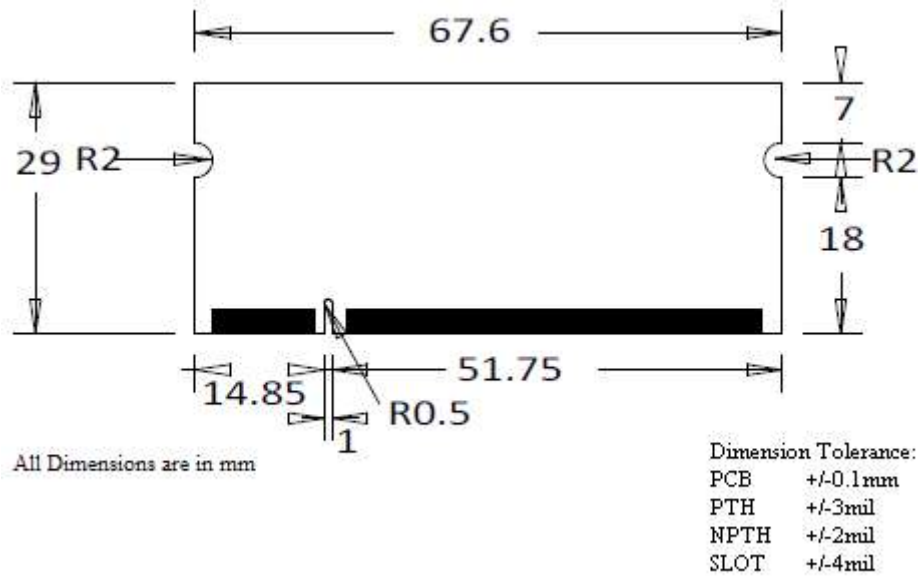


Figure 7: Mechanical dimension of SODIMM SOM - Top View

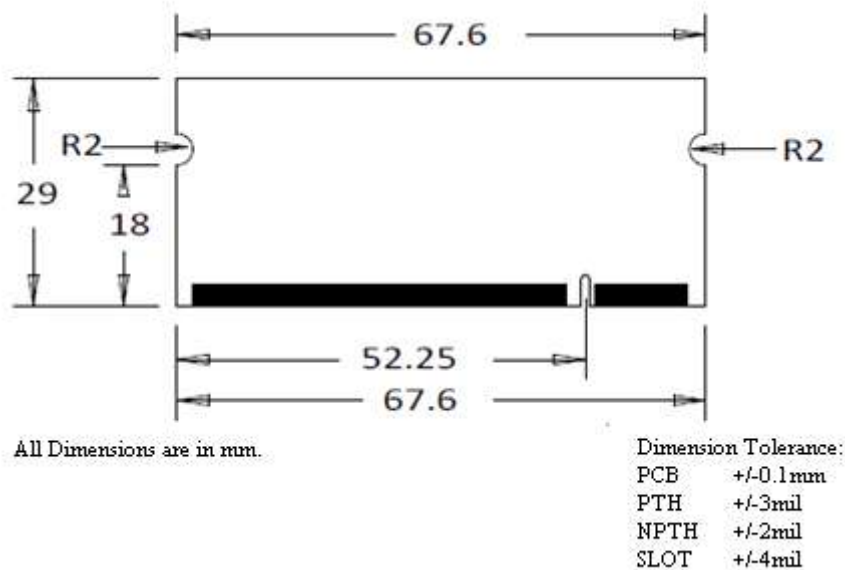


Figure 8: Mechanical dimension of SODIMM SOM - Bottom View

i.MX6UL/i.MX6ULL SODIMM SOM PCB thickness is $1\pm0.1\text{mm}$, top side maximum height component is Capacitor (C22, 1.45mm) followed by CPU (1.32mm) and bottom side maximum height component is Capacitor (C68, 1.45mm) followed by Diode (D3, 1.0mm). Please refer the below figure which gives height details of the i.MX6UL/i.MX6ULL SODIMM SOM.

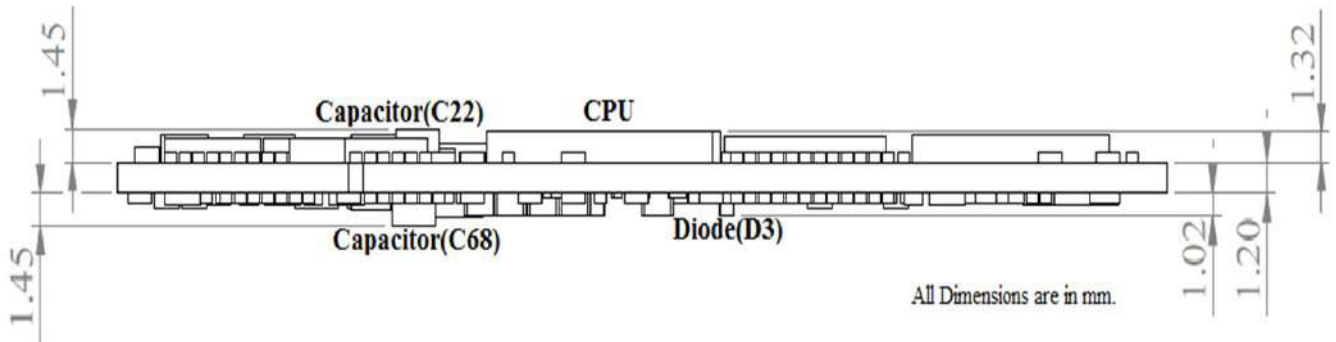


Figure 9: Mechanical dimension of SODIMM SOM - Side View

4. ORDERING INFORMATION

The below table provides the standard orderable part numbers for different i.MX6UL/i.MX6ULL SODIMM SOM variations. If the desired part number is not listed in below table, or if any custom configuration part number is required, please contact iWave.

Also please contact iWave for orderable part number of i.MX6UL/i.MX6ULL SODIMM SOM with higher RAM memory size or Flash memory size configurations.

Table 12: Orderable Product Part Numbers

Product Part Number	Description	Temperature
i.MX6UL3 CPU based SODIMM SOMs		
iW-G18M-SM1S-3D256M-N256M-LI	With i.MX6UL3 Industrial grade CPU, 256MB RAM, 256MB NAND Flash with Linux.	Industrial
iW-G18M-SM1S-3D256M-N256M-BI	With i.MX6UL3 Industrial grade CPU, 256MB RAM, 256MB NAND Flash with Boot Code.	Industrial
iW-G18M-SM1S-3D256M-N256M-LC	With i.MX6UL3 Commercial grade CPU, 256MB RAM, 256MB NAND Flash with Linux.	Commercial
iW-G18M-SM1S-3D256M-N256M-BC	With i.MX6UL3 Commercial grade CPU, 256MB RAM, 256MB NAND Flash with Boot Code.	Commercial
i.MX6UL2 CPU based SODIMM SOMs		
iW-G18M-SM1G-3D256M-N256M-LI	With i.MX6UL2 Industrial grade CPU, 256MB RAM, 256MB NAND Flash with Linux.	Industrial
iW-G18M-SM1G-3D256M-N256M-BI	With i.MX6UL2 Industrial grade CPU, 256MB RAM, 256MB NAND Flash with Boot Code.	Industrial
iW-G18M-SM1G-3D256M-N256M-LC	With i.MX6UL2 Commercial grade CPU, 256MB RAM, 256MB NAND Flash with Linux.	Commercial
iW-G18M-SM1G-3D256M-N256M-BC	With i.MX6UL2 Commercial grade CPU, 256MB RAM, 256MB NAND Flash with Boot Code.	Commercial
i.MX6UL1 CPU based SODIMM SOMs		
iW-G18M-SM1M-3D256M-N256M-LI	With i.MX6UL1 Industrial grade CPU, 256MB RAM, 256MB NAND Flash with Linux.	Industrial
iW-G18M-SM1M-3D256M-N256M-BI	With i.MX6UL1 Industrial grade CPU, 256MB RAM, 256MB NAND Flash with Boot Code.	Industrial
iW-G18M-SM1M-3D256M-N256M-LC	With i.MX6UL1 Commercial grade CPU, 256MB RAM, 256MB NAND Flash with Linux.	Commercial
iW-G18M-SM1M-3D256M-N256M-BC	With i.MX6UL1 Commercial grade CPU, 256MB RAM, 256MB NAND Flash with Boot Code.	Commercial

i.MX6UL/i.MX6ULL SODIMM SOM Hardware User Guide

Product Part Number	Description	Temperature
i.MX6UL0 CPU based SODIMM SOMs		
iW-G18M-SM1B-3D256M-N256M-LC	With i.MX6UL0 Commercial grade CPU, 256MB RAM, 256MB NAND Flash with Linux.	Commercial
iW-G18M-SM1B-3D256M-N256M-BC	With i.MX6UL0 Commercial grade CPU, 256MB RAM, 256MB NAND Flash with Boot Code.	Commercial
i.MX6ULL2 CPU based SODIMM SOMs		
iW-G18M-SMY2-3D256M-N256M-LCA	With i.MX6ULL2 Commercial grade CPU, 256MB RAM, 256MB NAND Flash with Linux.	Commercial
iW-G18M-SMY2-3D256M-N256M-BCA	With i.MX6ULL2 Commercial grade CPU, 256MB RAM, 256MB NAND Flash with Boot Code.	Commercial
i.MX6ULL1 CPU based SODIMM SOMs		
iW-G18M-SMY1-3D256M-N256M-LIA	With i.MX6ULL1 Industrial grade CPU, 256MB RAM, 256MB NAND Flash with Linux.	Industrial
iW-G18M-SMY1-3D256M-N256M-BIA	With i.MX6ULL1 Industrial grade CPU, 256MB RAM, 256MB NAND Flash with Boot Code.	Industrial
iW-G18M-SMY1-3D256M-N256M-LCA	With i.MX6ULL1 Commercial grade CPU, 256MB RAM, 256MB NAND Flash with Linux.	Commercial
iW-G18M-SMY1-3D256M-N256M-BCA	With i.MX6ULL1 Commercial grade CPU, 256MB RAM, 256MB NAND Flash with Boot Code.	Commercial
i.MX6ULL0 CPU based SODIMM SOMs		
iW-G18M-SMY0-3D256M-N256M-LIA	With i.MX6ULL0 Industrial grade CPU, 256MB RAM, 256MB NAND Flash with Linux.	Industrial
iW-G18M-SMY0-3D256M-N256M-BIA	With i.MX6ULL0 Industrial grade CPU, 256MB RAM, 256MB NAND Flash with Boot Code.	Industrial
iW-G18M-SMY0-3D256M-N256M-LCA	With i.MX6ULL0 Commercial grade CPU, 256MB RAM, 256MB NAND Flash with Linux.	Commercial
iW-G18M-SMY0-3D256M-N256M-BCA	With i.MX6ULL0 Commercial grade CPU, 256MB RAM, 256MB NAND Flash with Boot Code.	Commercial

Important Note: Some of the above mentioned Part Number is subject to MOQ purchase. Please contact iWave for further details.

Note: For SOM identification purpose, Product Part Number and SOM Unique Serial Number are pasted as Label with Barcode readable format on SOM.

5. APPENDIX I

5.1 Guidelines to insert the SODIMM SOM into Carrier board

- Make sure that power is not provided to the Carrier board.
- Insert the SODIMM SOM into the socket at a slight angle (approximately 30 degrees). Note that the socket and SOM are both keyed, which means the module can be installed one way only.
- To seat the SODIMM SOM into the socket, apply firm, even pressure to each end of the module until you feel it slip down into the socket.
- With the SODIMM SOM properly seated in the socket, rotate the SOM downward, as indicated in the illustration. Continue pressing downward until the clips at each end of the socket lock into position.
- Once the SOM has been installed, Carrier board can be Powered ON with 5V power supply.

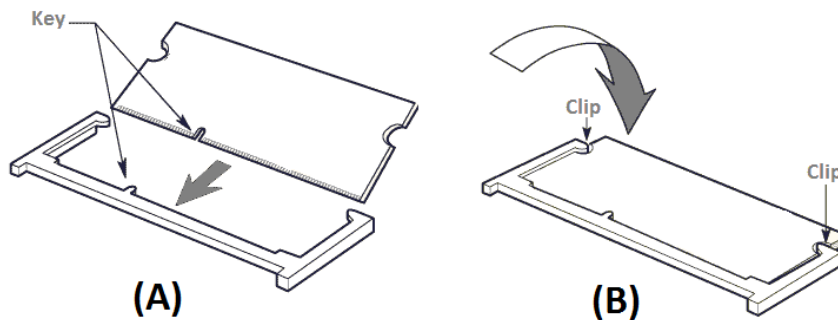


Figure 10: SODIMM SOM Insertion procedure

5.2 Guidelines to remove the SODIMM SOM from Carrier board

- Make sure that power is not provided to the Carrier board.
- When you remove the SODIMM SOM, pull away the retention clips (A) on each side of the SOM.
- The SODIMM SOM pops up. Grasp the edge of the SOM (B) and gently pull the SOM out of the connector.

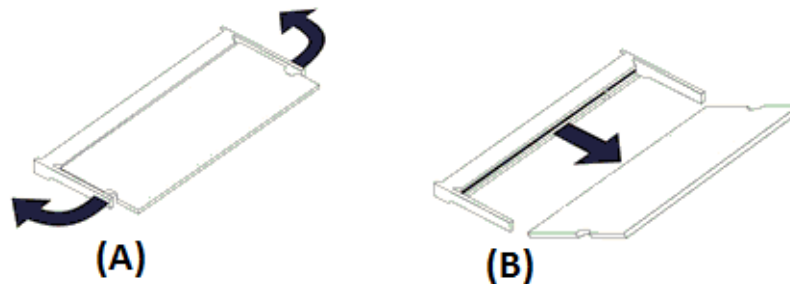


Figure 11: SODIMM SOM Removal procedure

6. APPENDIX II

6.1 i.MX6UL/i.MX6ULL SODIMM SOM Development Platform

iWave Systems supports iW-RainboW-G18D – i.MX6UL/i.MX6ULL SODIMM Development Platform which is targeted for quick validation of i.MX6UL/i.MX6ULL CPU. iWave's i.MX6UL/i.MX6ULL SODIMM Development Board incorporates i.MX6UL/i.MX6ULL SODIMM SOM and SODIMM Carrier board for complete validation of i.MX6UL/i.MX6ULL SODIMM SOM functionality with complete BSP support.

Being a Pico-ITX form factor with 100mmx72mm size, the i.MX6UL/i.MX6ULL SODIMM Development Platform carrier board is highly packed with all the necessary on-board connectors to validate the i.MX6UL/i.MX6ULL CPU features with optional 4.3" resistive display kit. For more details on i.MX6UL/i.MX6ULL SODIMM SOM Development platform, visit the below web links.

<http://www.iwavesystems.com/i-mx6ul-development-kit.html>

<http://www.iwavesystems.com/i-mx6ull-development-board.html>



Figure 12: i.MX6UL/i.MX6ULL SODIMM SOM Development Platform

