SPECIFICATION
FOR
APPROVAL

( ) **Preliminary Specification**

(●) **Final Specification**

Title	83" UHD(QWUXGA) OLED

BUYER	
MODEL	

SUPPLIER	LG Display Co., Ltd.
*MODEL	LE830PQW
SUFFIX	HTE1

APPROVED BY	SIGNATURE DATE
/	
/	
/	

Please return 1 copy for your confirmation with your signature and comments.

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※ Production

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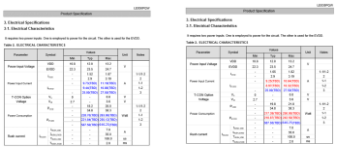
▶ Module site : LG Display in VH (Lot E, Trang Due Industrial zone, Dinh Vu – Cat Hai EZ, Hong Phong commune, An Duong District, Hai Phong City, Vietnam)

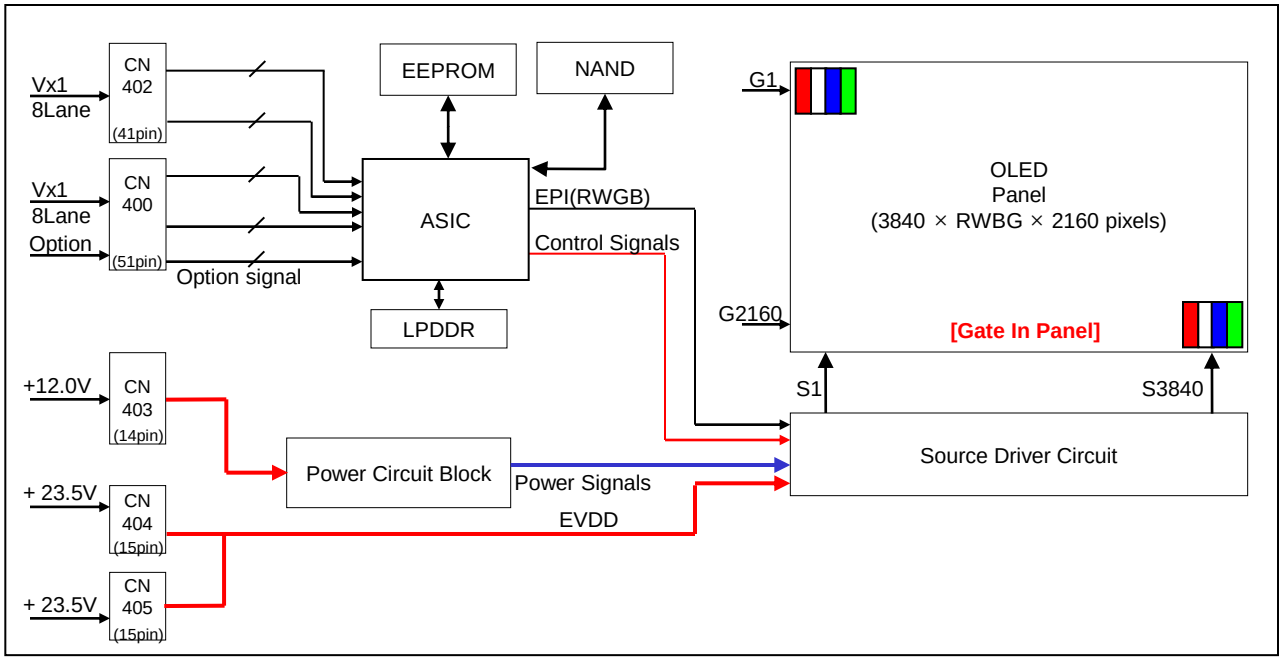
CONTENTS

RECORD OF REVISIONS

Revision No	Revision Date	Page	Before	After	Application Date
0.1	Mar. 07. 2024	-	Preliminary Specification release.		
0.2	Aug. 06. 2024	4,P	Preliminary Specification release.	Electrical Specifications Power Consumption updated Before / After 	
		4, 27	Weight: 5.0 kg	Weight: 4.4 kg	
			Outline Dim Vertical: 1046.45mm	Outline Dim Vertical: 1046.46mm	
0.3	Sep.23,2024	12	-	120Hz VRR Timing Table added	
0.4	Oct.08.2024	38	-	Add content ※ The q'ty and position of oxygen absorber & desiccant can be changed	
0.5	Oct.15.2024	24	CR @ Pritchard 810L (25% APL) Typ : 2,000,000 Min : 1,600,000	CR @ Pritchard 810L (25% APL) Typ : 2,150,000 Min : 1,720,000	
			Response Time_G to G Max : 3	Response Time_G to G Max : 0.5	
		6	PEVDD : Decimal point correction Parameter / Symbol / Values (Min, Typ, Max) Power Consumption / P_{EVDD} - 217.39 250.00 - 210.87 242.50 - 587.50 646.25	PEVDD : Decimal point correction Parameter / Symbol / Values (Min, Typ, Max) Power Consumption / P_{EVDD} - 217.4 250.0 - 210.9 242.5 - 587.5 646.3	
		4	Total 237.19 W (Typ.) [Logic = 19.8W , EVDD = 217.39W] @ IEC62087	Total 237.2 W (Typ.) [Logic = 19.8W , EVDD = 217.4W] @ IEC62087	
	Nov. 7.2024	4	General Description CN8(14Pin) +12.0V → CN8 (14pin)	General Description CN403(14Pin) →correction +12.0V → CN 403 (14pin)	
	Nov. 7.2024	50	■ **ASIC Firmware** : TBD	■ **ASIC Firmware** : key in ■ ASIC Firmware Category / FW version Value / Checksum Value CAS Final / C.0A.01.04.0 / 0F0A1147	
1.0	Nov. 7.2024		-	Final Specification release.	Nov. 7. 2024

1. General Description

The LE830PQW is a Color Active Matrix Organic Light Emitting Diode Display (OLED).
The matrix employs Oxide Thin Film Transistor as the active element. It is a Bottom emission display type.
It has a 83 inch diagonally measured active display area with QWUXGA resolution (2160 vertical by 3840 horizontal pixel array).
Each pixel is divided into Red, Green, Blue and white sub-pixels or dots which are arrayed in vertical stripes.
Gray scale or the luminance of the sub-pixel color is determined with a 10-bit gray scale signal for each dot.
Therefore, it can present a palette of more than 1.07B(true) colors.
It has been designed to apply the 10-bit / 11bit 16-lane V by One interface.
It is intended to support TV where high brightness, super wide viewing angle, high color gamut, high color depth and fast response time are important.



General Features

Active Screen Size	82.51 inch (2095.846 mm) diagonal, 1826.69 x 1027.51 mm
Outline Dimension (Typ.)	1839.49(H) X 1046.46(V) x 0.79 (B)㎜
Pixel Pitch	0.4757 mm x 0.4757 mm
Pixel Format	3840 horiz. by 2160 vert. Pixels, RWBG stripe arrangement
Color Depth	10bit(R), 1.07Billon colors
Luminance, White	650/200 cd/m^2 (Center 1point ,Typ.)
Color Viewing Angle	R/L 120 (min.), U/D 120 (min.) (Δu'v' ≤0.025)
Power Consumption	Total 237.2 W (Typ.) [Logic = 19.8W , EVDD = 217.4W] @ IEC62087
Weight	4.4 kg (Typ., Board Assy only)
Display Mode	Normally black
Surface Treatment	Hard coating(2H), Anti-reflection treatment of the front polarizer (Reflectance Typ. 1.1%)

2. Absolute Maximum Ratings

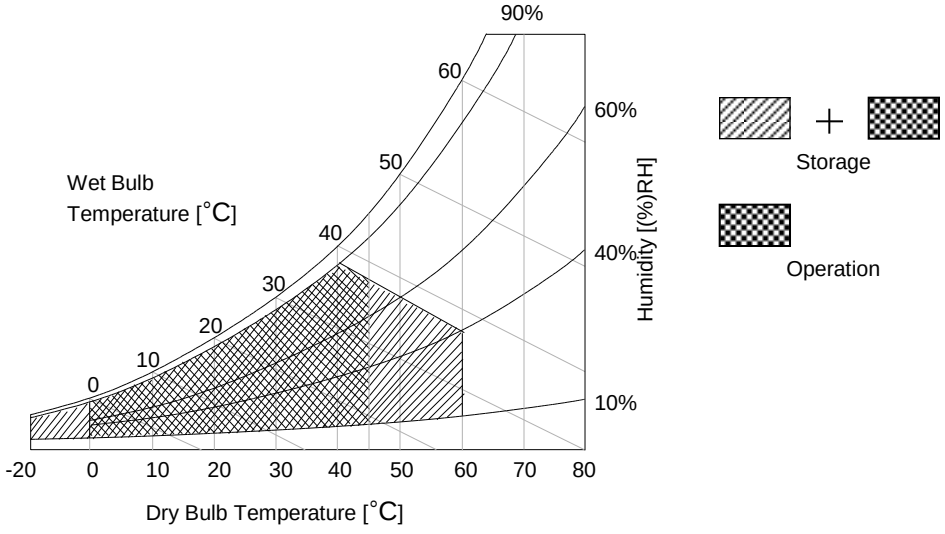
The following items are maximum values which, if exceeded, may cause faulty operation or damage to the OLED module.

Table 1. ABSOLUTE MAXIMUM RATINGS

Parameter		Symbol	Value		Unit	Note
			Min	Max		
Power Input Voltage	Logic	V_{VDD}	-0.3	+14.0	V_{DC}	1
	EVDD	V_{EVDD}	-0.3	+28.5	V_{DC}	
T-Con Option Selection Voltage		V_{LOGIC}	-0.3	+3.7	V_{DC}	
Operating Temperature		T_{OP}	0	+45	°C	2
Storage Temperature		T_{ST}	-20	+60	°C	
Operating Ambient Humidity		H_{OP}	10	90	%RH	2
Storage Humidity		H_{ST}	10	90	%RH	

Note:

1. Ambient temperature condition (Ta = 25 ± 2 °C)
2. Temperature and relative humidity range are shown in the figure below.
   Wet bulb temperature should be Max 39°C, and no condensation of water.



3. Electrical Specifications

3-1. Electrical Characteristics

It requires two power inputs. One is employed to power for the circuit. The other is used for the EVDD.

Table 2. ELECTRICAL CHARACTERISTICS

Parameter	Symbol		Values			Unit	Notes
			Min	Typ	Max		
Power Input Voltage	VDD		10.8	12.0	13.2	V	
	EVDD		22.3	23.5	24.7		
Power Input Current	I_{VDD}		-	1.65	1.82	A	1-1/1-2
			-	2.9	3.19		2
	I_{EVDD}		-	9.25	10.64		1-1
				8.97	10.32		1-2
			-	25.00	27.50		3
T-CON Option Voltage	V_{IL}		0	-	0.8	V	
	V_{IH}		2.7	-	3.6	V	
Power Consumption	P_{VDD}		-	19.8	21.8	Watt	1-1/1-2
			-	34.8	38.3		2
	P_{EVDD}		-	217.4	250.0		1-1
			-	210.9	242.5		1-2
			-	587.5	646.3		3
Rush current	I_{RUSH}	I_{RUSH_VDD}	-	-	7.0	A	
		I_{RUSH_EVDD}	-	-	35.0		
		T_{RUSH_VDD}	-	-	100.0	us	
		T_{RUSH_EVDD}	-	-	2.0	ms	

1-1. The specified current and power consumption are under the VDD=12.0V, EVDD=23.5V Ta=25 ± 2°C, f_V=120Hz condition whereas standard moving picture(IEC62087) is displayed and f_V is the frame frequency.
※ Before measuring the power consumption based on the standard moving picture(IEC62087), the power supplier's input voltage is needed to set the integrated power meter to be the EVDD Typ. value based on 25% APL Pattern.
1-2 The specified current and power consumption are under the VDD=12.0V, EVDD=23.5V Ta=25 ± 2°C, f_V=120Hz condition whereas standard moving picture(CLASP) is displayed and f_V is the frame frequency.
2. The current (I_{VDD}) is specified at the maximum current pattern (1by1 Horizontal Pattern) and under the VDD=12.0V, EVDD=23.5V Ta=25 ± 2°C condition.
3. The current (I_{EVDD}) is specified at the maximum current pattern (Secondary Color Pattern) and under the VDD=12.0V, EVDD=23.5V Ta=25 ± 2°C condition.

3-2. Interface Connections

This OLED module employs two kinds of interface connection, 51-pin connector and 41-pin connector are used for the module signals and two 15-pin connectors and one 14-pin connector are used for the module powers.

3-2-1. OLED Module (Signals)

- Module Connector(CN400): 05030WR-H51B (Yeonho) or GT05S-51S-H38(LSM)
- Mating Connector : FI-RE51HL(JAE) or compatible

Table 3-1. MODULE CONNECTOR(CN400) PIN CONFIGURATION

Pin No.	Symbol	Description	Pin No.	Symbol	Description
1	NC (Reserved)	No Connection (Reserved)	27	GND	Ground
2	NC (Reserved)	No Connection (Reserved)	28	Rx0n	V-by-One HS Data Lane 0
3	NC (Reserved)	No Connection (Reserved)	29	Rx0p	V-by-One HS Data Lane 0
4	NC (Reserved)	No Connection (Reserved)	30	GND	Ground
5	NC (Reserved)	No Connection (Reserved)	31	Rx1n	V-by-One HS Data Lane 1
6	NC (Reserved)	No Connection (Reserved)	32	Rx1p	V-by-One HS Data Lane 1
7	NC (Reserved)	No Connection (Reserved)	33	GND	Ground
8	NC (Reserved)	No Connection (Reserved)	34	Rx2n	V-by-One HS Data Lane 2
9	NC (Reserved)	No Connection (Reserved)	35	Rx2p	V-by-One HS Data Lane 2
10	JB&Off -RS Power_off done	JB&Off-RS&Power _off Done(H), Set←Module	36	GND	Ground
11	AC_DET	AC_DET (H= On), Set → Module	37	Rx3n	V-by-One HS Data Lane 3
12	Error Detection	H=Error, L=Normal (note 4)	38	Rx3p	V-by-One HS Data Lane 3
13	I2C-SDA1	I2C for Customer	39	GND	Ground
14	I2C-SCL1		40	Rx4n	V-by-One HS Data Lane 4
15	Data format 0	Data Format[1:0] (Note5, Default : 00) 00:1-div, 01:2-div, 10:4-div, 11:8-div	41	Rx4p	V-by-One HS Data Lane 4
16	Data format 1		42	GND	Ground
17	TPC	H=TPC, L=Normal	43	Rx5n	V-by-One HS Data Lane 5
18	I2C-SDA	I2C for Customer	44	Rx5p	V-by-One HS Data Lane 5
19	I2C-SCL		45	GND	Ground
20	EVDD Det	EVDD reset, Set ← Module	46	Rx6n	V-by-One HS Data Lane 6
21	NC (Reserved)	No Connection (Reserved)	47	Rx6p	V-by-One HS Data Lane 6
22	GND	AGP0 (note 6)	48	GND	Ground
23	GND	AGP1 (note 6)	49	Rx7n	V-by-One HS Data Lane 7
24	GND	Ground	50	Rx7p	V-by-One HS Data Lane 7
25	HTPDN	Hot plug detect	51	GND	Ground
26	LOCKN	Lock detect	-	-	-

Notes :
1. All GND (ground) pins should be connected together.
2. All Input levels of V-by-One signals are based on the V-by-One HS Standard.
3. Specific pin No. #10 is used for compensation when power turn off.
4. Specific pin No. #12 is used for “Power Error detection” of the OLED module.
5. Specific pins No. #15 and #16 are Vx1 Input Format. This module can support 1~8 division mode (Please see the Appendix VI for more information.)
6. Specific pins No. #22 and #23 are used for “No signal detection” of system signal interface. It should be GND for NSB (No Signal Black) while the system interface signal is not. If this pin is “H”, OLED module displays AGP (Auto Generation Pattern).

- Module Connector (CN402) : 05030WR-H41B5 (Yeonho) or GT05S-41S-H38(LSM)
- Mating Connector : FI-RE41HL(JAE) or compatible

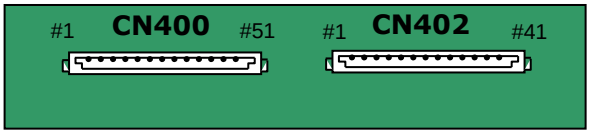
Table 3-2. MODULE CONNECTOR(CN402) PIN CONFIGURATION

No	Symbol	Description
1	GND	Ground
2	Rx8n	V-by-One HS Data Lane 8
3	Rx8p	V-by-One HS Data Lane 8
4	GND	Ground
5	Rx9n	V-by-One HS Data Lane 9
6	Rx9p	V-by-One HS Data Lane 9
7	GND	Ground
8	Rx10n	V-by-One HS Data Lane 10
9	Rx10p	V-by-One HS Data Lane 10
10	GND	Ground
11	Rx11n	V-by-One HS Data Lane 11
12	Rx11p	V-by-One HS Data Lane 11
13	GND	Ground
14	Rx12n	V-by-One HS Data Lane 12
15	Rx12p	V-by-One HS Data Lane 12
16	GND	Ground
17	Rx13n	V-by-One HS Data Lane 13
18	Rx13p	V-by-One HS Data Lane 13
19	GND	Ground
20	Rx14n	V-by-One HS Data Lane 14
21	Rx14p	V-by-One HS Data Lane 14

No	Symbol	Description
22	GND	Ground
23	Rx15n	V-by-One HS Data Lane 15
24	Rx15p	V-by-One HS Data Lane 15
25	GND	Ground
26	NC	No Connection
27	NC	No Connection
28	NC	No Connection
29	NC	No Connection
30	NC	No Connection
31	NC	No Connection
32	NC	No Connection
33	NC	No Connection
34	NC	No Connection
35	NC	No Connection
36	NC	No Connection
37	P-CLK_Sel (EN_891)	Clock Selection (H:84.24M, L or NC :74,25M)
38	Vx1 Byte mode	Vx1 4/5Byte mode(H:5byte, L or NC: 4byte)
39	QSMEN	QSMEN (Set → Module)
40	ON_RF	ON_RF_DONE (Set ← Module)
41	NC	No Connection
-		

Notes : 1. All GND (ground) pins should be connected together.
2. #26~#36 NC (No Connection) : These pins are used only for LGD (Do not connect)

◆ **Rear view of OLED Module**



< Top view of PCB >

3-2-2. OLED Module (Powers)

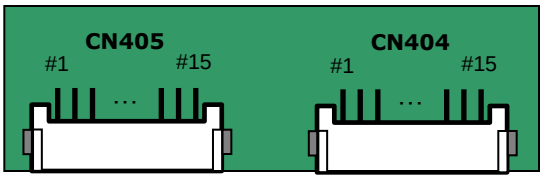
- EVDD Connector (CN404, CN405): 20022WR-H15B2(manufactured by YeonHo)
- Mating Connector : 20022HS-15B2(BK)(manufactured by YeonHo)

Table 4. EVDD CONNECTOR (CN404, CN405) PIN CONFIGURATION

No	Symbol	Description
1	EVSS	OLED Panel Ground
2	EVSS	OLED Panel Ground
3	EVSS	OLED Panel Ground
4	EVSS	OLED Panel Ground
5	EVSS	OLED Panel Ground
6	EVSS	OLED Panel Ground
7	EVSS	OLED Panel Ground
8	EVDD	OLED Panel Power Supply +23.5V
9	EVDD	OLED Panel Power Supply +23.5V
10	EVDD	OLED Panel Power Supply +23.5V
11	EVDD	OLED Panel Power Supply +23.5V
12	EVDD	OLED Panel Power Supply +23.5V
13	EVDD	OLED Panel Power Supply +23.5V
14	EVDD	OLED Panel Power Supply +23.5V
15	EVDD	OLED Panel Power Supply +23.5V

No	Symbol	Description
1	EVSS	OLED Panel Ground
2	EVSS	OLED Panel Ground
3	EVSS	OLED Panel Ground
4	EVSS	OLED Panel Ground
5	EVSS	OLED Panel Ground
6	EVSS	OLED Panel Ground
7	EVSS	OLED Panel Ground
8	EVDD	OLED Panel Power Supply +23.5V
9	EVDD	OLED Panel Power Supply +23.5V
10	EVDD	OLED Panel Power Supply +23.5V
11	EVDD	OLED Panel Power Supply +23.5V
12	EVDD	OLED Panel Power Supply +23.5V
13	EVDD	OLED Panel Power Supply +23.5V
14	EVDD	OLED Panel Power Supply +23.5V
15	EVDD	OLED Panel Power Supply +23.5V

◆ **Rear view of OLED Module**



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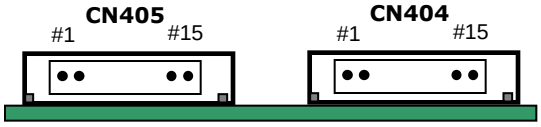


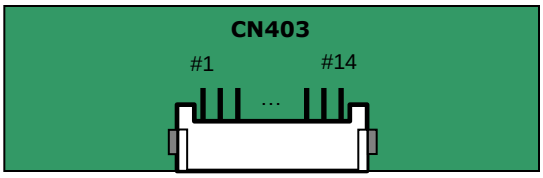
< Side view of PCB >

- VDD Connector (CN403) : 20022WR-H14B2(manufactured by YeonHo)
- Mating Connector : 20022HS-14B2(BK)(manufactured by YeonHo)

Table 403. VIN CONNECTOR (CN403) PIN CONFIGURATION

No	Symbol	Description
1	GND	Ground
2	GND	Ground
3	GND	Ground
4	GND	Ground
5	GND	Ground
6	GND	Ground
7	VDD	Power Supply +12V
8	VDD	Power Supply +12V
9	VDD	Power Supply +12V
10	VDD	Power Supply +12V
11	VDD	Power Supply +12V
12	VDD	Power Supply +12V
13	NC	Not Connection
14	NC	Not Connection

◆ **Rear view of OLED Module**



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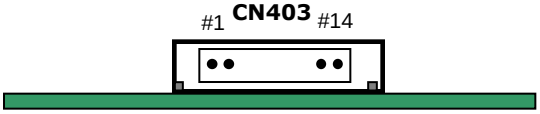

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3-3. Signal Timing Specifications

Table 6 shows the signal timing required at the input of the V-by-One transmitter. All of the interface signal timings should be satisfied with the following specification for normal operation.

Table 6-1. Timing Table(DE Only Mode)

ITEM		Symbol		Min	Typ	Max	Unit	Note
Horizontal	Display Period	t_{HV}		240 (248)	240 (248)	240 (248)	tCLK	3840 / 16 (11Bit)
	Blank	t_{HB}		70 (62)	72 (64)	72 (64)	tCLK	1 (11bit)
				0.823 (0.729)	0.855 (0.760)	0.863 (0.767)	us	3 (11bit)
	Total	t_{HP}		310	312	312	tCLK	
Vertical	Display Period	t_{VV}		2160	2160	2160	Lines	
	Blank	tVB	NTSC	89	90	121	Lines	1
			PAL	(512)	(540)	(673)		
			NTSC	326.5	333.3	449.5	us	3
			PAL	(1878.6)	(2000)	(2500)		
	Total	t_{VP}		2249 (2672)	2250 (2700)	2281 (2833)	Lines	

ITEM		Symbol	Min	Typ	Max	Unit	Note
Frequency	DCLK	f_{CLK}	83.99	84.24	84.49	MHz	1347.84 / 16
	Horizontal	f_H	269.20	270.00	272.55	KHz	1
	Vertical	f_V	118 (95)	120 (100)	121 (102)	Hz	2 NTSC (PAL)

Note: 1. The input of HSYNC & VSYNC signal does not have an effect on normal operation (DE Only Mode). If you use spread spectrum of EMI, add some additional clock to minimum value for clock margin.

2. The performance of the electro-optical characteristics may be influenced by variance of the vertical refresh rate and the horizontal frequency.

3. If you change the DCLK, must satisfy the minimum horizontal & vertical blank time.

※ This OLED module supports Spread Spectrum Clocking tolerance with up to 30kHz/ ±0.5%

※ Timing should be set based on clock frequency.

Table 6-2. Timing Table(Only Gaming mode : VRR Mode)

ITEM		Symbol	Min	Typ	Max	Unit	Note
Horizontal	Display Period	t_{HV}	240 (248)	240 (248)	240 (248)	tCLK	3840 / 16 (11Bit)
	Blank	t_{HB}	70 (62)	72 (64)	72 (64)	tCLK	(11bit)
			0.823 (0.731)	0.855 (0.760)	0.858 (0.765)	us	(11bit)
	Total	t_{HP}	310	312	312	tCLK	
Vertical	Display Period	t_{VV}	2160	2160	2160	Lines	
	Blank	t_{VB}	89	90	4610	Lines	
	Total	t_{VP}	2249	2250	6770	Lines	

ITEM		Symbol	Min	Typ	Max	Unit	Note
Frequency	DCLK	f_{CLK}	83.99	84.24	84.49	MHz	1347.84 / 16
	Horizontal	f_H	270	270	272.55	KHz	
	Vertical	f_V	40	120	121.19	Hz	

Note:
1. Only applicable to Gaming mode with VRR operation

Table 6-3. Timing Table(Only Gaming mode : VRR Mode)

ITEM		Symbol	Min	Typ	Max	Unit	Note
Horizontal	Display Period	t_{HV}	240 (248)	240 (248)	240 (248)	tCLK	3840 / 16 (11Bit)
	Blank	t_{HB}	19 (11)	20 (12)	20 (12)	tCLK	(11bit)
			0.225 (0.130)	0.237 (0.142)	0.238 (0.143)	us	(11bit)
	Total	t_{HP}	259	260	260	tCLK	
Vertical	Display Period	t_{VV}	2160	2160	2160	Lines	
	Blank	t_{VB}	87	90	5964	Lines	
	Total	t_{VP}	2247	2250	8100	Lines	

ITEM		Symbol	Min	Typ	Max	Unit	Note
Frequency	DCLK	f_{CLK}	83.99	84.24	84.49	MHz	1347.84 / 16
	Horizontal	f_H	324	324	325.25	KHz	
	Vertical	f_V	40	144	144.7	Hz	

Note:
1. Only applicable to Gaming mode with VRR operation

3-4. V by One Signal Specifications

3-4-1. V by One Eye Mask Specification

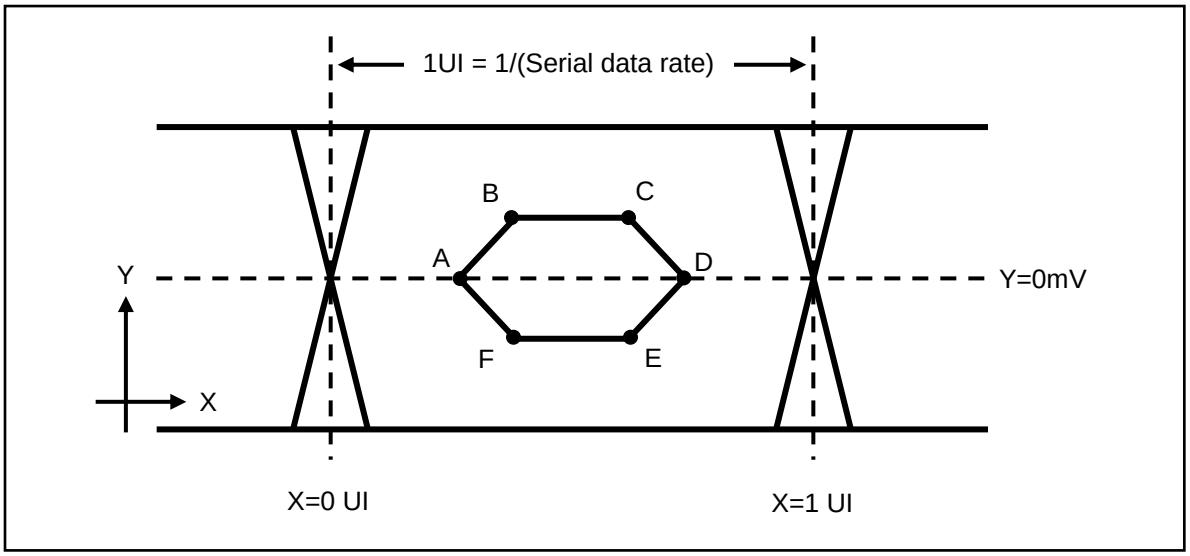
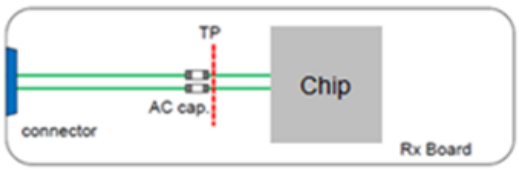


Table 7. Eye Mask Specification

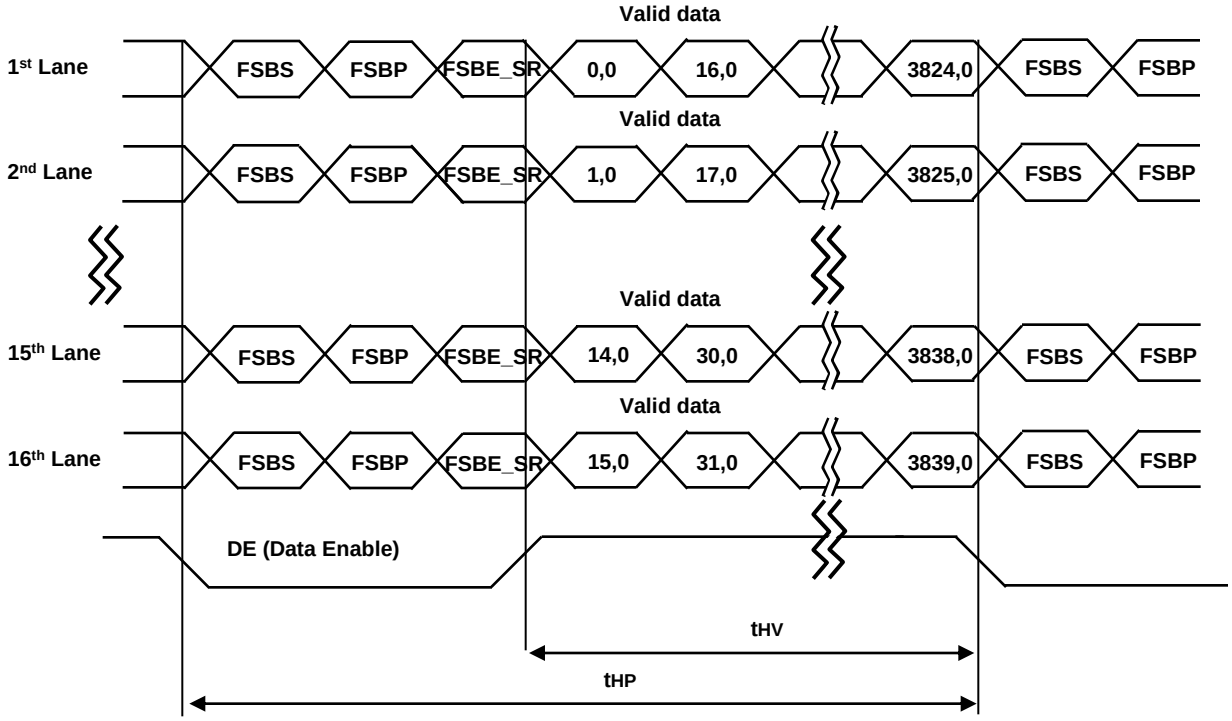
	X [UI]	Note	X [UI]	Note
A	0.25 (max)	2	0	-
B	0.30 (max)	2	50	3
C	0.70 (min)	3	50	3
D	0.75 (min)	3	0	-
E	0.70 (min)	3	|-50|	3
F	0.30 (max)	2	|-50|	3

Notes: 1.1 All Input levels of V by One signals are based on the V by One HS Standard.
1.2 When using the Tx's Pre-Emphasis function to be set to a minimum value that meets the EYE mask spec.
2. This is allowable maximum value.
3. This is allowable minimum value.
4. The eye diagram is measured by the oscilloscope and receiver CDR characteristic must be emulated.
- PLL Type : 2nd Order
- PLL bandwidth : 10Mhz
- Damping Factor : 2

5. EYE mask measuring point

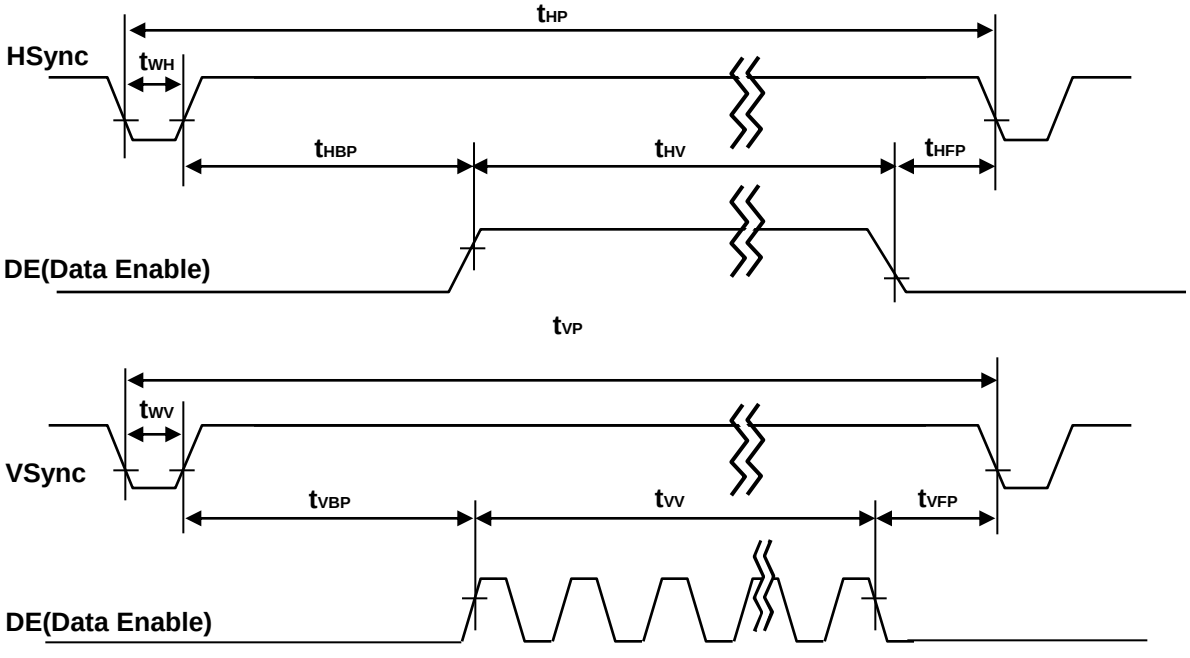


3-4-2. V by One Input Signal Timing Diagram



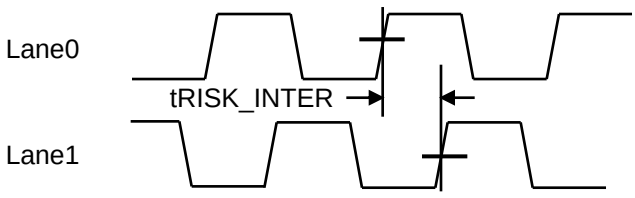
* Reference: Sync. Relation

* $t_{HB} = t_{HFP} + t_{WH} + t_{HBP}$
* $t_{VB} = t_{VFP} + t_{WV} + t_{VBP}$

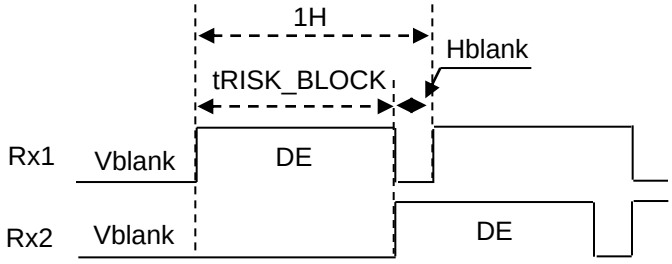


3-4-3. V by One Input Signal Characteristics

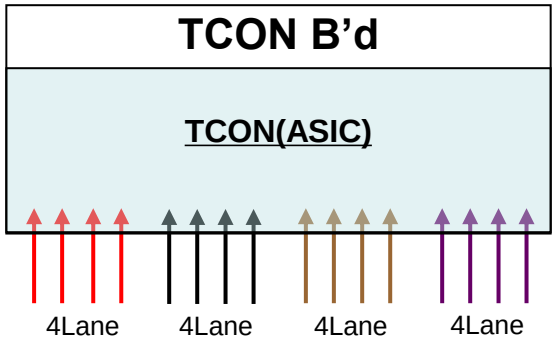
1) AC Specification



<Inter-pair skew between two lanes>



<Inter-pair skew between two sub-blocks>



<V by One Brief Diagram >

Description	Symbol	Min	Max	Unit	Note
Allowable inter-pair skew between lanes	tRISK_INTER	-	5	UI	1, 3
Allowable inter-pair skew between sub-blocks	tRISK_BLOCK	-	1	DE	1, 4

Notes: 1.1UI = 1/serial data rate

2. it is the time difference between the true and complementary single-ended signals.
3. it is the time difference of the differential voltage between any two lanes in one sub block.
4. it is the time difference of the differential voltage between any two blocks in one IP.
5. APL packet of Vx1 Input

5-1) APL data transmission should be completed between after 5H from frame last DE falling and 10H before next frame DE rising.

5-2) APL data transmission should be inputted only one time during V blank period.

3-5. Color Data Reference

The brightness of each primary color (red, green, blue) is based on the 10 or 11 bit gray scale data input for the color. The higher binary input, the brighter the color. Table 8 provides a reference for color versus data input.

Table 8. Color data Reference

Packer input & Unpacker output		30bpp (10bit)	33bpp (11bit)	33bpp (11bit)_4byte								
		RGB	RGB	RGB	Dummy CLK1	Dummy CLK2	Dummy CLK3	Dummy CLK4	Dummy CLK5	Dummy CLK6	Dummy CLK7	Dummy CLK8
Byte0	D[0]	R[2]	R[4]	R[3]	R0[0]	R32[0]	R64[0]	R96[0]	R128[0]	R160[0]	R192[0]	R224[0]
	D[1]	R[3]	R[5]	R[4]	R1[0]							
	D[2]	R[4]	R[6]	R[5]	R2[0]							
	D[3]	R[5]	R[7]	R[6]	R3[0]							
	D[4]	R[6]	R[8]	R[7]	R4[0]							
	D[5]	R[7]	R[9]	R[8]	R5[0]							
	D[6]	R[8]	R[10]	R[9]	R6[0]							
	D[7]	R[9]	-	R[10]	R7[0]							
Byte1	D[8]	G[2]	G[4]	G[3]	R8[0]							
	D[9]	G[3]	G[5]	G[4]	R9[0]							
	D[10]	G[4]	G[6]	G[5]	R10[0]							
	D[11]	G[5]	G[7]	G[6]	R11[0]							
	D[12]	G[6]	G[8]	G[7]	R12[0]							
	D[13]	G[7]	G[9]	G[8]	R13[0]							
	D[14]	G[8]	G[10]	G[9]	R14[0]							
	D[15]	G[9]	-	G[10]	R15[0]							R239[0]
Byte2	D[16]	B[2]	B[4]	B[3]	R16[0]							don't use
	D[17]	B[3]	B[5]	B[4]	R17[0]							
	D[18]	B[4]	B[6]	B[5]	R18[0]							
	D[19]	B[5]	B[7]	B[6]	R19[0]							
	D[20]	B[6]	B[8]	B[7]	R20[0]							
	D[21]	B[7]	B[9]	B[8]	R21[0]							
	D[22]	B[8]	B[10]	B[9]	R22[0]							
	D[23]	B[9]	-	B[10]	R23[0]							
Byte3	D[24]	Don't care	Don't care	B[0]	R24[0]							
	D[25]	Don't care	Don't care	G[0]	R25[0]							
	D[26]	B[0]	B[2]	B[1]	R26[0]							
	D[27]	B[1]	B[3]	B[2]	R27[0]							
	D[28]	G[0]	G[2]	G[1]	R28[0]							
	D[29]	G[1]	G[3]	G[2]	R29[0]							
	D[30]	R[0]	R[2]	R[1]	R30[0]							
	D[31]	R[1]	R[3]	R[2]	R31[0]	R63[0]	R95[0]	R127[0]	R159[0]	R191[0]	R223[0]	
Byte4	D[24]	-	-									
	D[25]	-	-									
	D[26]	-	B[0]									
	D[27]	-	B[1]									
	D[28]	-	G[0]									
	D[29]	-	G[1]									
	D[30]	-	R[0]									
	D[31]	-	R[1]									

Notes 1. 30bpp RGB (10bit), 33bpp RGB(11bit)_4byte are 4 byte mode, 33bpp RGB(11bit) is 5byte

3-6. Power Sequence

3-6-1. OLED Driving circuit

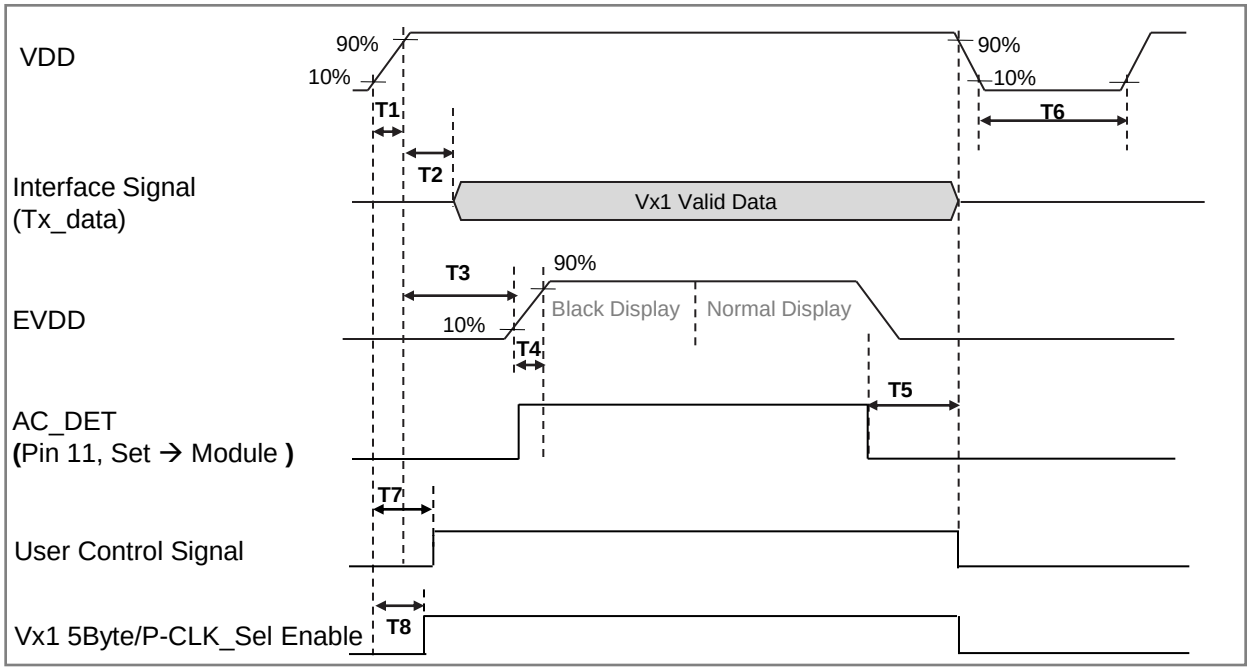


Table 9. POWER SEQUENCE

Parameter	Value			Unit	Notes
	Min	Typ	Max		
T1	1	-	20	ms	1
T2	58	-	-	ms	
T3	0.54	-	-	sec	2
T4	5	-	50	ms	
T5	30	-	-	ms	
T6	1.5	-	-	sec	3
T7	0	-	T1+T2	ms	4
T8	-	-	58	ms	

Note : 1. The T3 is recommended value, the case when failed to meet a minimum specification, abnormal display would be shown. There is no reliability problem. T3 should be larger than T2.

2. T6 should be measured after the module has been fully discharge between power off and on period.

3. If the on time of signals (Interface signal and user control signals) precedes the on time of Power(VDD) it will be happened abnormal display. When T7 is NC status, T7 doesn't need to be measured

4. I2C is able to be accessed from 54**0ms(**after VDD 90% rising.

※ Black pattern is displayed during black display period before normal display. (ON RF Time **2.7s)**

※ When the power for logic (VDD) **turns on** , EVDD should be less than 5V.
But, it does not matter if there is no garbage image.

3-6-2. OFF RS compensation operation

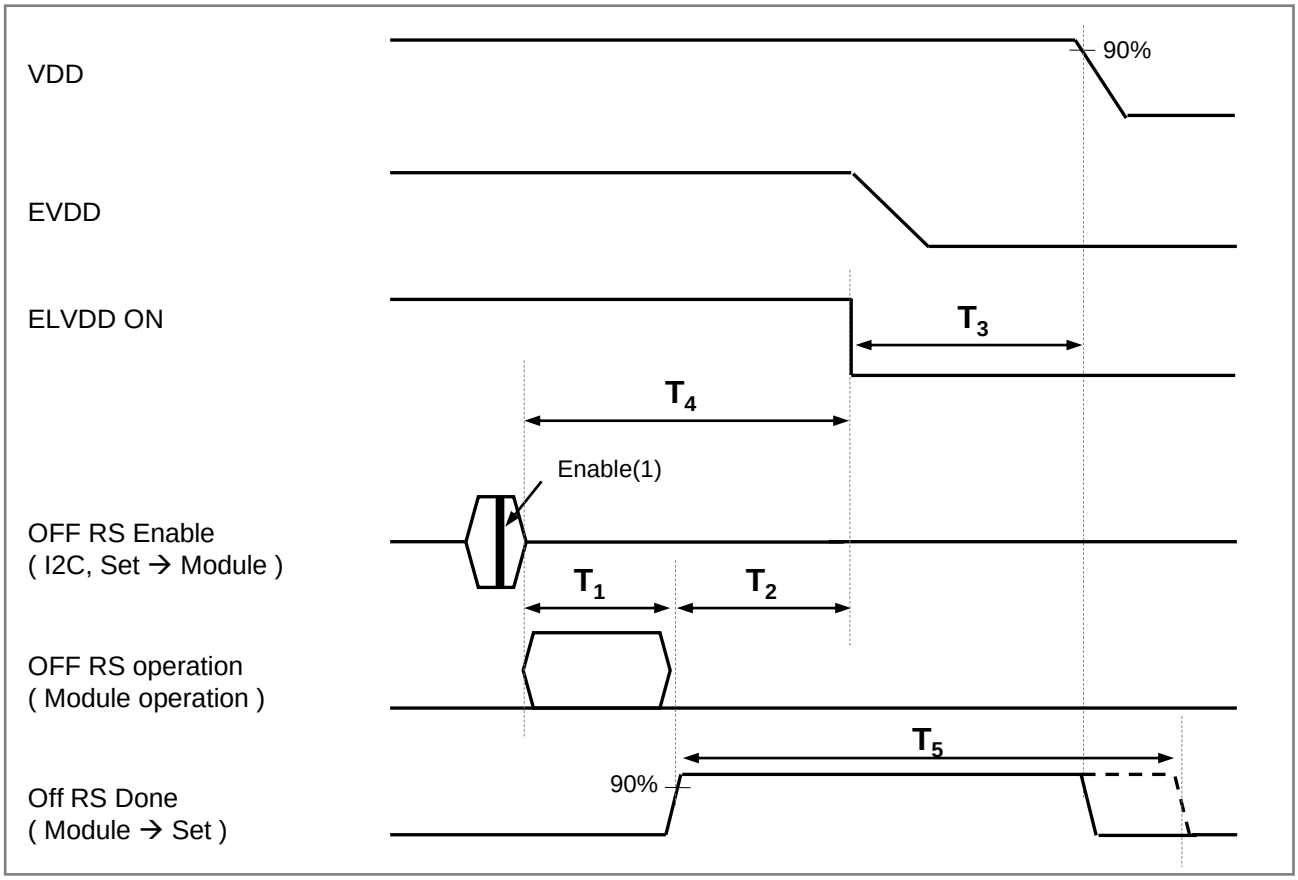


Table 10. Off-RS Power Sequence

Parameter	Value			Unit	Notes
	Min	Typ	Max		
T1	270		370	sec	1
T2	0	-	10	sec	
T3	30	-	-	ms	
T4	270	-	380	sec	2-1
	380		500	sec	2-2
T5	0.5	7	10	sec	

Note : 1. It is the actual RS sensing time. This timing is determined according to the characteristics of the panel. (LGD Internal timing)

2-1. When Off-RS Done Signal is transferred normally.

2-2. When Off-RS Done Signal is not transferred.

※ When there is power on action before completing OFF RS operation, don't change OFF RS enable signal (1→0). Just do power off and power on.

※ Off RS Enable is only available during Normal Display period.

※ In order to prevent mura defects, it is recommended that customer do Off-RS in their lines.

3-6-3. JB compensation operation

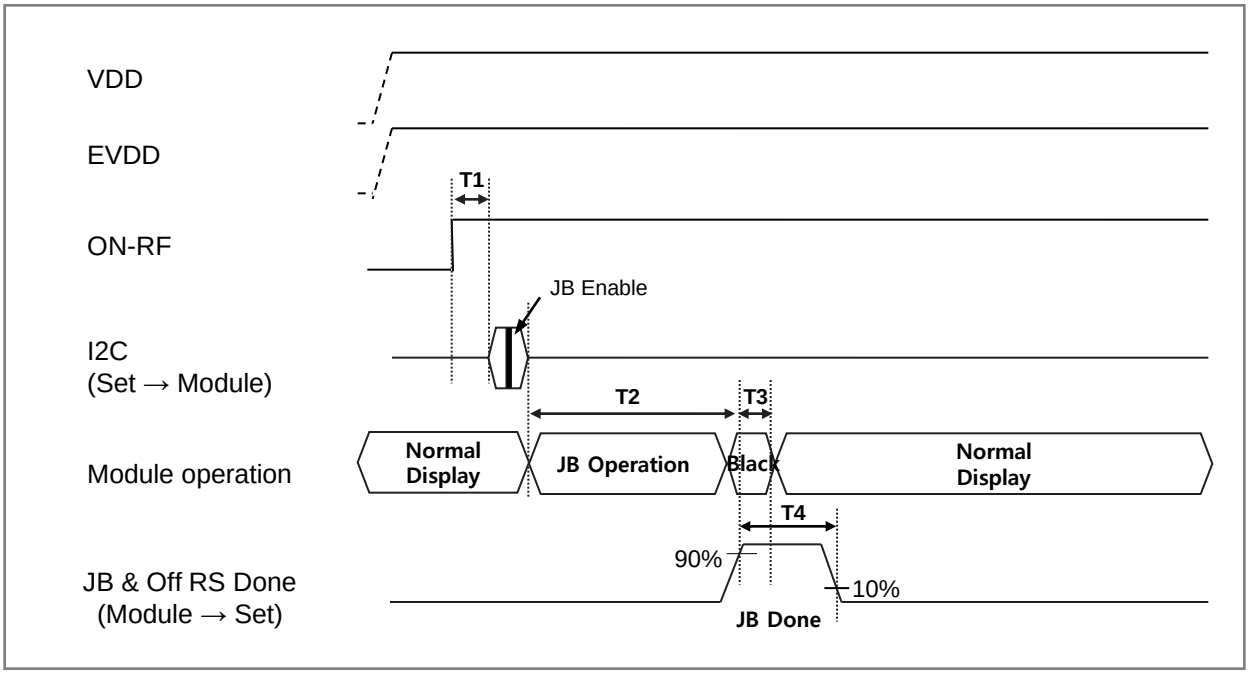


Table 11. JB Power Sequence

Parameter	Value			Unit	Notes
	Min	Typ	Max		
T1	200	-	-	ms	
T2	-	-	21	sec	
T3	415.6	-	508.0	ms	Black PTN
T4	0.5	7	10	sec	

Note : ※ At VRR mode, T3 can change by adaptive sync timing(T3 need 19 frame) (VRR Only)
※ T3 can change by adaptive sync timing(T3 need 19 frame) (VRR Only)
※ T2 is the actual JB sensing time. This timing is determined according to the characteristics of the panel. (LGD Internal timing)

3-6-4. QSM Operation

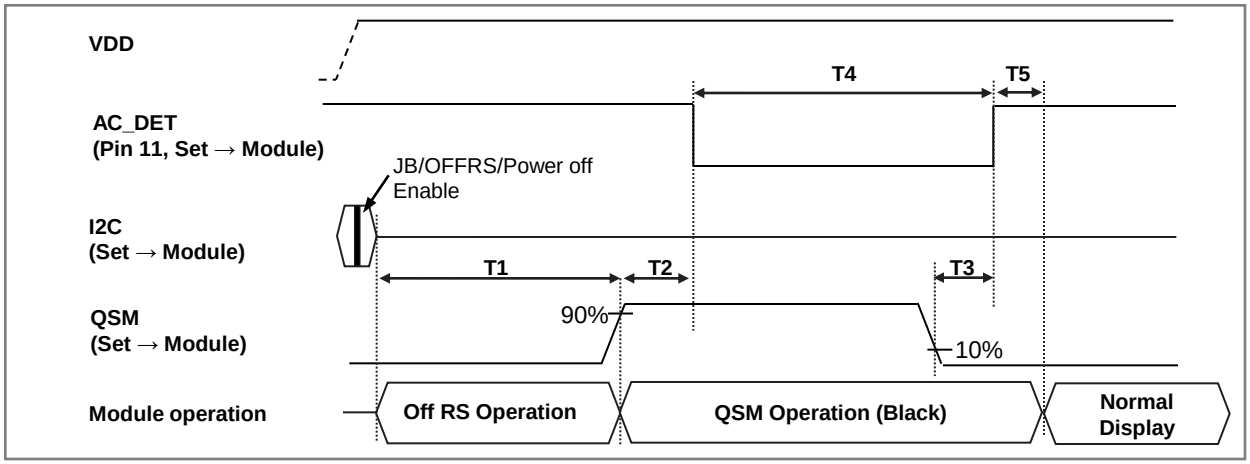


Table 12. QSM Sequence

Parameter	Value			Unit	Notes
	Min	Typ	Max		
T1	1	-	-	sec	JB/OFFRS POWER OFF
T2	75	-	-	ms	NOTE
T3	10	-	-	ms	NOTE
T4	1	-	-	sec	
T5	-	-	500	ms	

Note : 1. QSM EN pulse width should be more than 1s.

2. QSM EN & AC DET sequence should meet following order.
(QSM Rising → AC DET Falling →QSM Falling →AC DET Rising)

3-6-5. DPC Operation

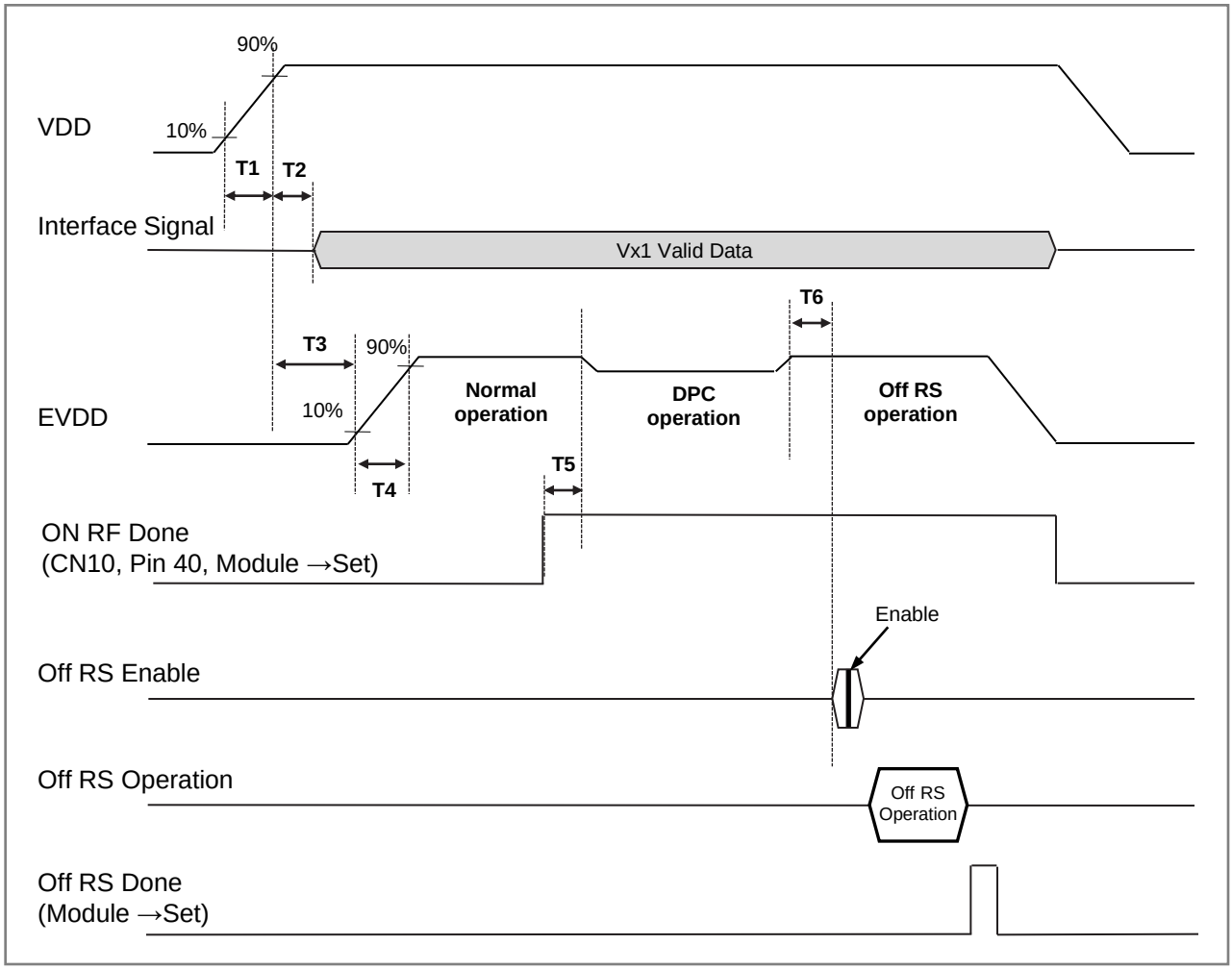


Table 13. DPC Sequence

Parameter	Value			Unit	Notes
	Min	Typ	Max		
T1	1	-	20	ms	
T2	58	-	-	ms	
T3	0.54	-	-	sec	
T4	5	-	50	ms	
T5	0.2	**-**		sec	1
T6	0.5	**-**		sec	2

Note : 1. T5 should be guaranteed for ON RF operation with black pattern before switching to DPC mode.

2. Refer to 3.6.1. OLED Driving Circuit in case of DPC power off without OFF-RS.

3. EVDD input recommend voltage range : 22.3V ~ 24.7V

※ EVDD UVLO voltage : ON (14.3V), OFF (13.2V)

3-6-6. Power off sequence

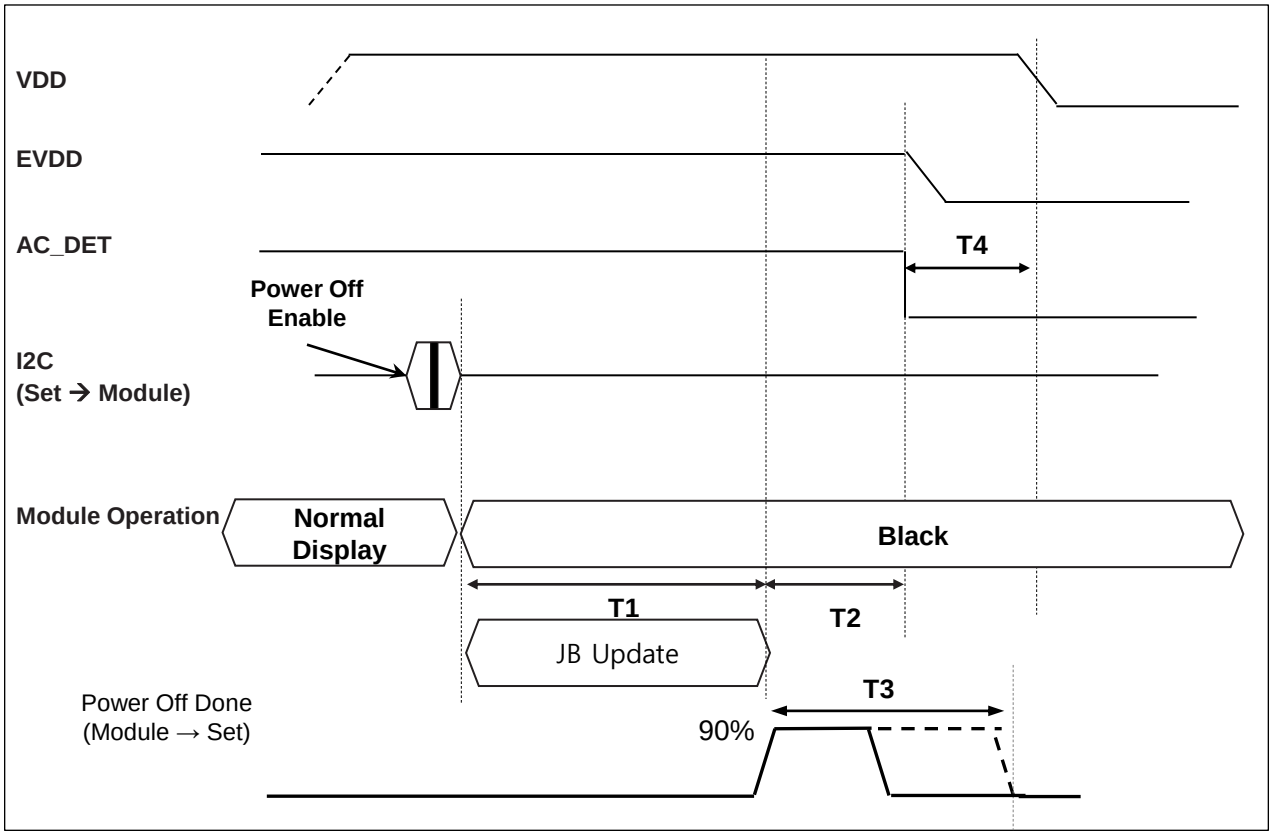


Table 8. POWER SEQUENCE

Parameter	Value			Unit	Notes
	Min	Typ	Max		
T1	-	-	16.5	Sec	
T2	30	-	-	ms	
T3	5	7	10	sec	
T4	30	-	-	ms	

4. Optical Specification

Optical characteristics are determined after the unit has been 'ON' and stable in a dark environment at 25±2°C. The values are specified at distance 50cm from the OLED surface at a viewing angle of Φ and θ equal to 0 °. FIG. 1 shows additional information concerning the measurement equipment and method.

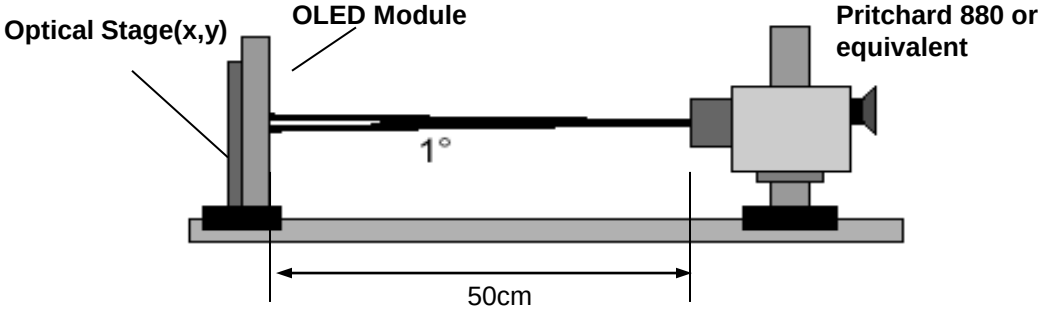


FIG. 1 Optical Characteristic Measurement Equipment and Method

Table 14. OPTICAL CHARACTERISTICS Ta= 25±2°C, VDD=12V, EVDD=23.5V, fv=120Hz, Dclk=84.24MHz

Parameter		Symbol			Value Min	Value Typ	Value Max	Unit	Note
Contrast Ratio		CR @ Pritchard 880			160,000	200,000	-		1
		CR @ Pritchard 810L (25% APL)			1,720,000	2,150,000			
Surface Luminance, white		L_{WH}	2D	Normal	160	200	-	cd/m²	2
				Peak	520	650	-		
				HDR 10%	960	1200	-		
				HDR 3%	1200	1500	-		
Luminance Uniformity		δ_{WHITE}	9P		75	85	-	%	3
Response Time		G to G			-	0.1	0.5	ms	4
		MPRT			-	6	12	ms	5
Color Coordinates [CIE1931]	RED	Rx			Typ - 0.02	0.678	Typ + 0.02		
		Ry				0.320			
	GREEN	Gx				0.267			
		Gy				0.678			
	BLUE	Bx				0.147			
		By				0.049			
	WHITE	Wx			Typ - 0.015	0.281	Typ + 0.015		
		Wy				0.288			
Color Temperature						10,000		K	
Color Gamut (DCI)					94.0	98.5		%	
Color Viewing Angle	θ=60º Φ=0º, 90º, 180º, 270º	Δu′v′			-	0.015	0.025		6
Life Time (B10)		Hrs				30,000			7
Gray Scale					-	2.2	-		8

Note : 1. Contrast Ratio(CR) is defined mathematically as :

$$\text{Contrast Ratio} = \frac{\text{Surface Luminance with all white pixels}}{\text{Surface Luminance with all black pixels}}$$

It is measured at center 1-point.

2. Normal full white luminance is determined with 100% APL after 30 minutes 'ON' with APL 100%(Full white) pattern in a dark environment at 25±2°C . It is the luminance value at center 1-point across the OLED surface 50cm from the surface with all pixels displaying white. For additional measurement, OLED module need to power-off for 2 minutes(min). Peak luminance is determined with 25% APL after 1.5 minutes at least 'ON' with 25% white window box. HDR luminance is determined with 10% APL after 60 seconds at least 'ON' with 10% white window box. For more information, see the Fig. 2.

※ Normal : APL 100% (Full white) / Peak : APL 25% / HDR : APL 10% / HDR : APL 3%

3. The variation in surface luminance , δ WHITE is defined as :
   δ WHITE(9P) = Minimum(L_{on1},.... L_{on9}) / Maximum(L_{on1}..... L_{on9})
   Where L_{on1} to L_{on9} are the luminance with all pixels displaying white at 9 locations .
   For more information, see the FIG. 2.
4. Response time is the time required for the display to transit from G(N) to G(M) (Rise Time, Tr_R) and from G(M) to G(N) (Decay Time, Tr_D). For additional information, see the FIG. 3. (N<M)
   ※ G to G Spec stands for average value of all measured points.
   Photo Detector : RD-80S / Field : 2°
5. MPRT is defined as the 10% to 90% blur-edge width Bij(pixels) and scroll speed U(pixels/frame) at the moving picture. For more information, see FIG 4
6. Viewing Angle Color Shift (VACS) is defined as follows after measuring color coordinates at each angle.; VACS = sqrt(du2+dv2) (@ CIE (u', v') color space) For more information, see the FIG. 6.
7. Test Condition : IEC62087 standard video with OFF-RS every 4 hours at room temperature 25℃ (If the cumulative time of usage is over 4 hours, OFF-RS compensation should be performed.)
8. Gray scale specification.
   Gamma Value is approximately 2.2. For more information, see the Table 15.

Table 15. Gray Scale Specification

Gray Level	Luminance [%] (Typ)
L0	0.001
L63	0.20
L127	0.97
L191	2.42
L255	4.61
L319	7.59
L383	11.4
L447	16.0
L511	21.6
L575	28.0
L639	35.4
L703	43.7
L767	53.0
L831	63.2
L895	74.5
L959	86.7
L1023	100

Measuring point for surface luminance & measuring point for luminance variation.

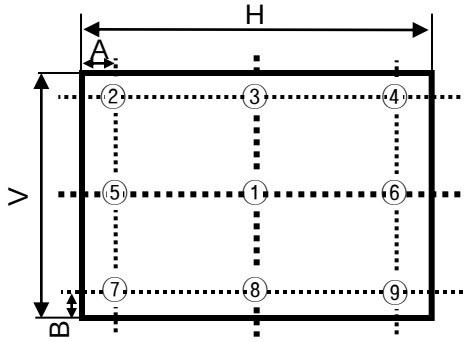


FIG. 2-1 9 Points for Luminance Measure with 100% APL

A: H/9 B: V/9 @ H,V: Active Area

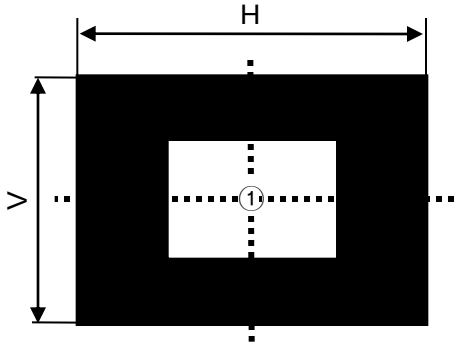


FIG. 2-2. 1 Point for peak luminance measure with 25% APL

@ H,V: Active Area

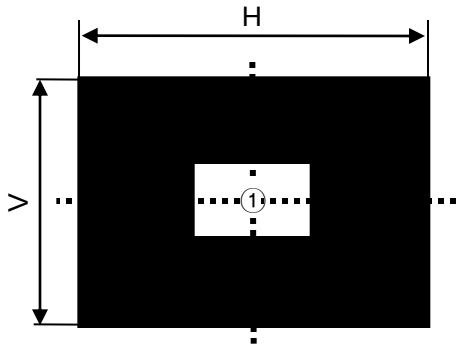


FIG. 2-3. 1 Point for peak luminance measure with 10% APL

@ H,V: Active Area

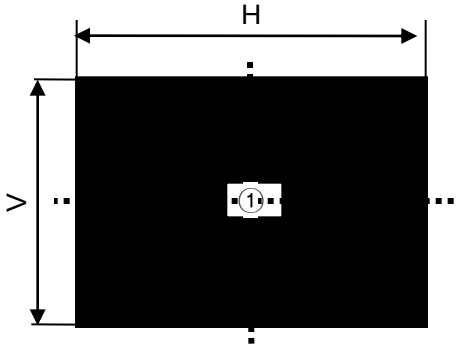
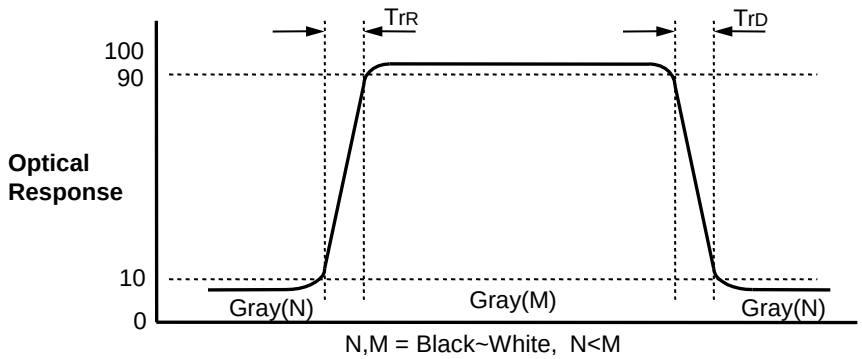


FIG. 2-4. 1 Point for peak luminance measure with 3% APL

@ H,V: Active Area

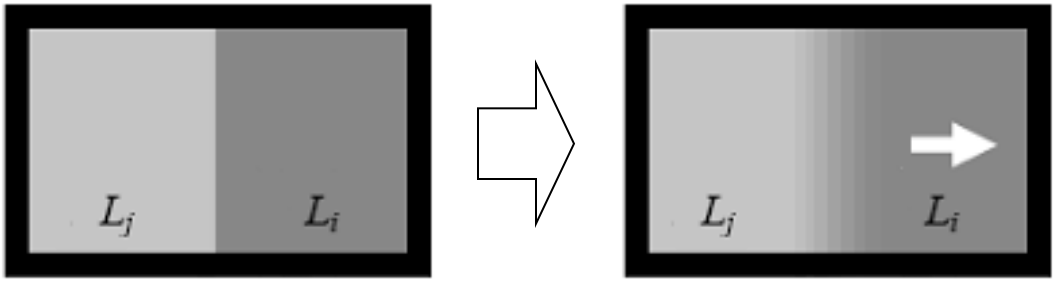
Response time is defined as the following figure and shall be measured by switching the input signal for "Gray(N)" and "Gray(M)".



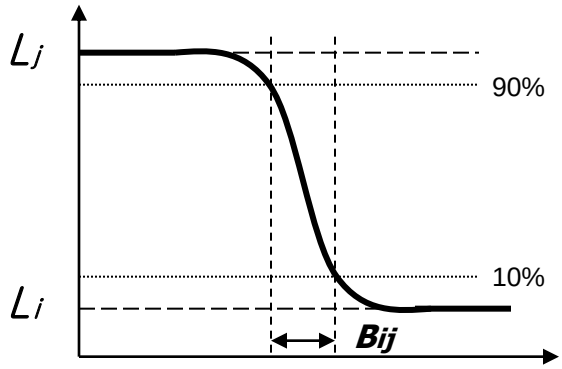
N,M = Black~White, N<M

FIG. 3 Response Time

MPRT is defined as the 10% to 90% blur-edge with Bij(pixels) and scroll speed U(pixels/frame)at the moving picture.



$$M = \frac{1}{U} Bij \ (i \neq j)$$



Example) Bij = 12pixels, U = 10pixels / 120Hz
M = 12pixels / (10pixels / 120Hz)
= 12pixels / {10pixels / (1/120)s}
= 12 / 1,200 s
= 10 ms

FIG. 4 MPRT

Dimension of viewing angle range

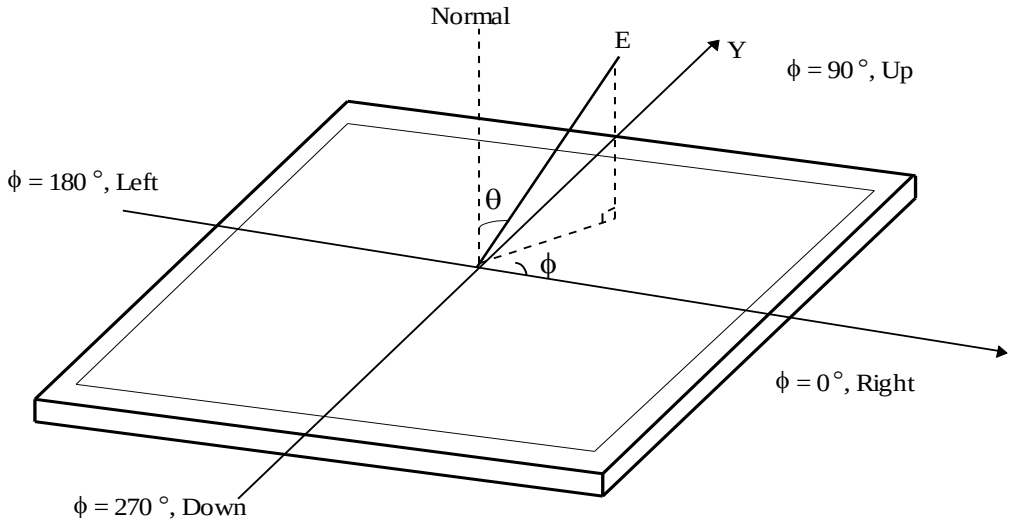


FIG. 5 Viewing Angle

5. Mechanical Characteristics

Table 16. MECHANICAL CHARACTERISTICS

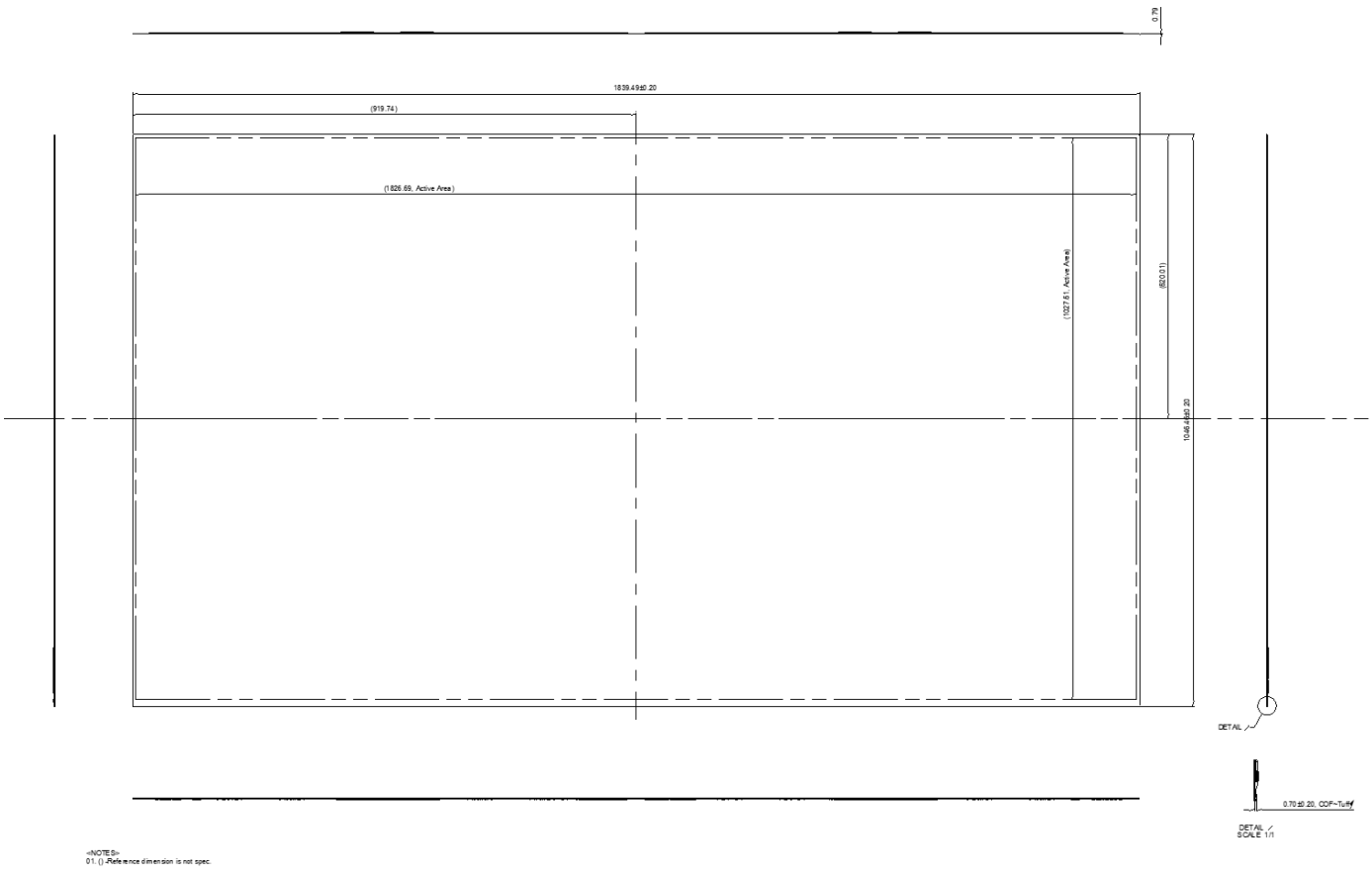
Item	Value	
Outline Dimension (Straight Length)	Horizontal	1839.49㎜
	Vertical	1046.46㎜
	Depth	0.79㎜
Active Display Area	Horizontal	1826.69㎜
	Vertical	1027.51㎜
Weight	4.4 kg (Typ. Board Ass'y only)	

Note : Please refer to a mechanical drawing in terms of tolerance at the next page.

Table 17. MECHANICAL CHARACTERISTICS

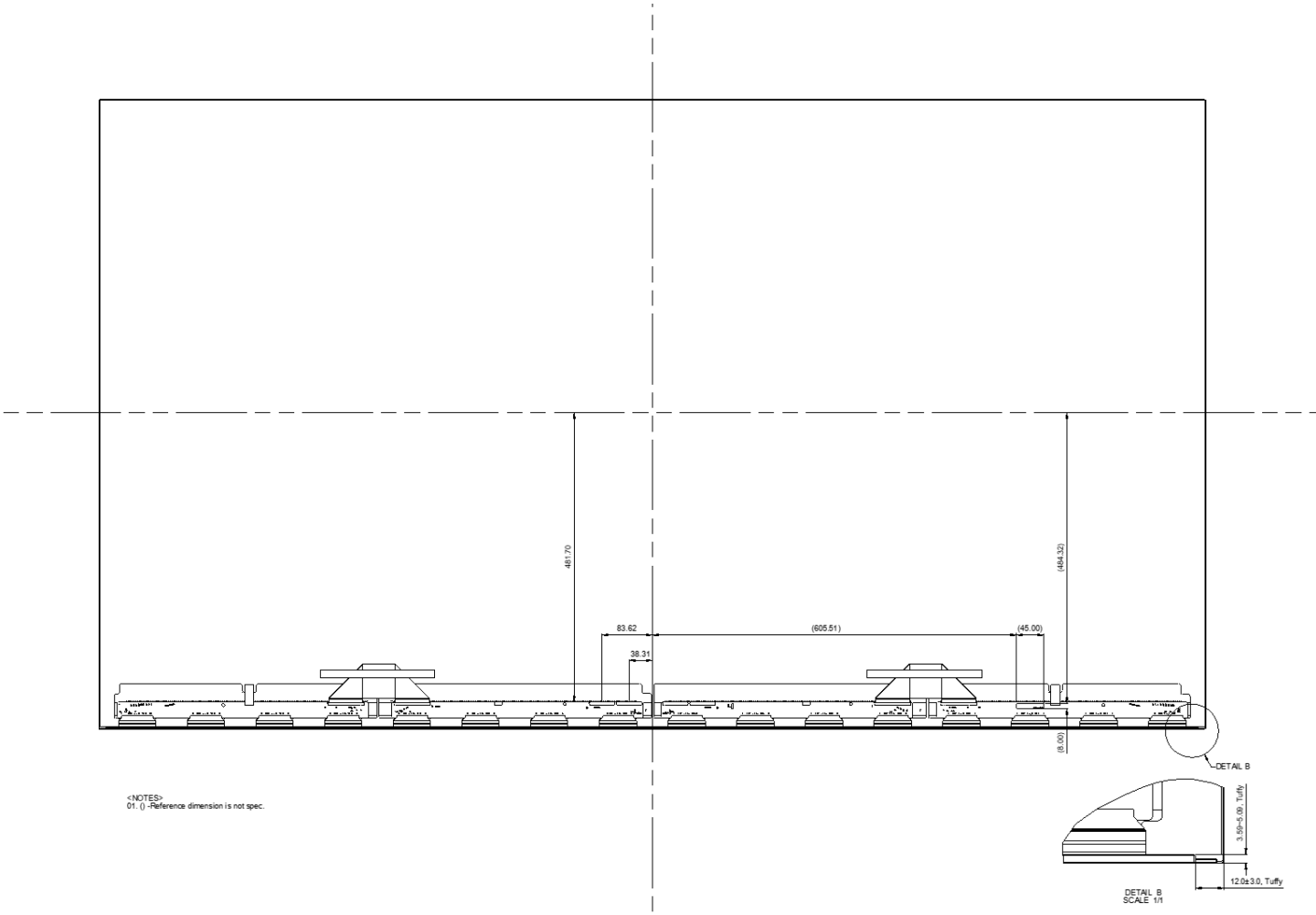
Item	Value	
On Bezel (Active Area ~ Edge of Module)	Horizontal	6.4mm (Left) / 6.4mm (Right)
	Vertical	6.25mm (Top) / 12.7 mm (Bottom)

[FRONT VIEW]

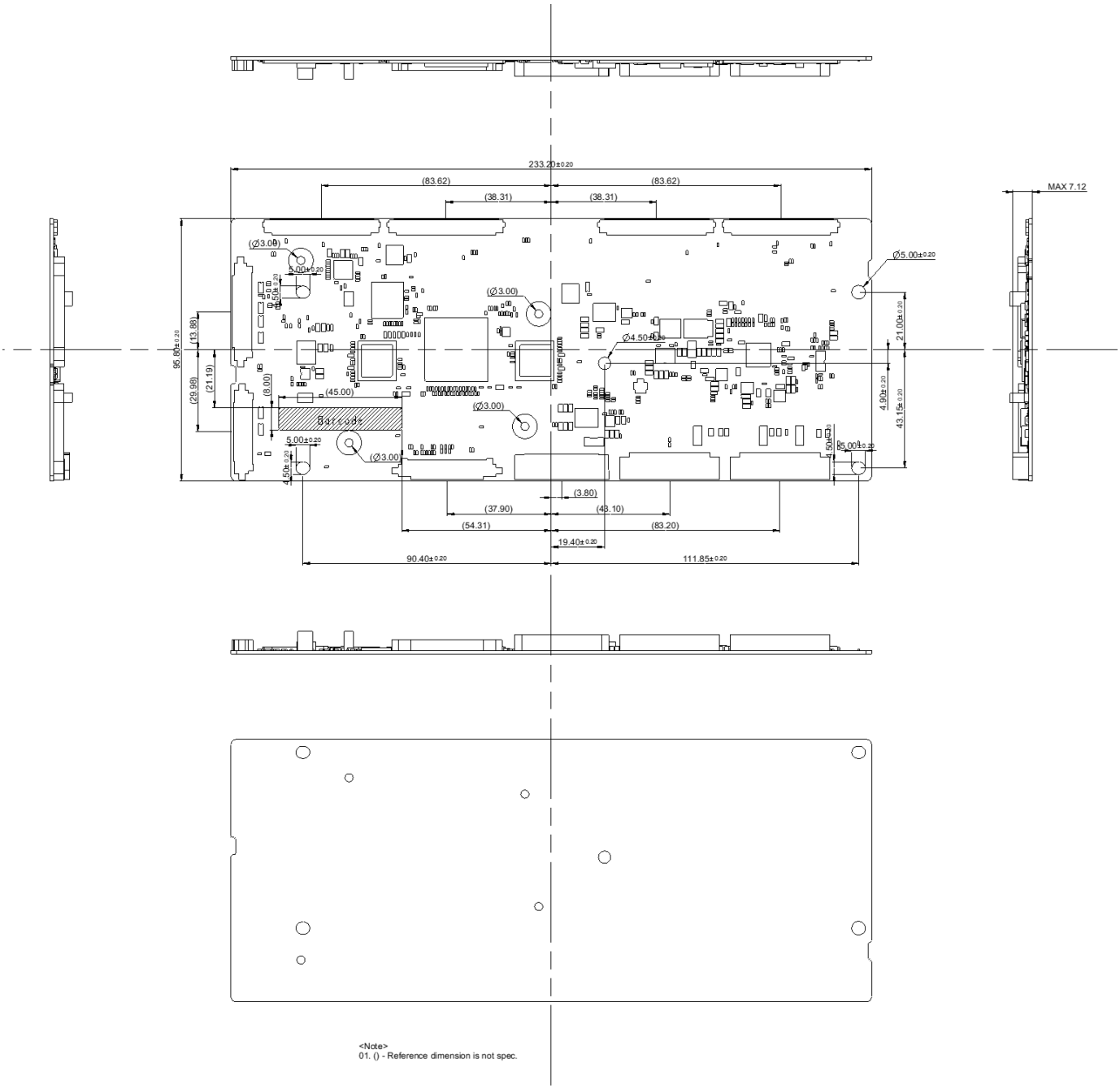


<NOTE S>
01. ( ) -Reference dimension is not spec.

[Rear VIEW]


461.70
(484.32)
83.62
(605.51)
(45.00)
38.31
(8.00)
DETAIL B
3.09±0.09, Tuffy
12.0±3.0, Tuffy
DETAIL B
SCALE 1/1
<NOTES>
01. ( ) -Reference dimension is not spec.

[Control Board Assembly Dimension]



<Note>
01. () - Reference dimension is not spec.

6. Reliability

Table 18. ENVIRONMENT TEST CONDITION

No.	Test Item	Condition
1	High temperature storage test	Ta= 60°C 240h
2	Low temperature storage test	Ta= -20°C 240h
3	High temperature operation test	Ta= 50°C 50%RH 240h
4	Low temperature operation test	Ta= 0°C 240h
5	Pallet Packing Vibration test (non-operating)	Wave form : random Vibration level : 1.15Grms Bandwidth : 1-200Hz Duration : Z, 60 min
6	Humidity condition Operation	Ta= 40 °C ,90%RH
7	Altitude operating storage / shipment	0 - 15,000 ft 0 - 40,000 ft

Note : 1. Before and after Reliability test, OLED Module should be operated with normal function.
(After Reliability test, some OLED Module need to do OFF-RS before function check)

7. International Standards

7-1. Safety

1) IEC 62368-1, The International Electro-technical Commission(IEC).
Audio/video, Information and Communication Technology Equipment - Safety - Safety Requirements.

2) EN 62368-1, European Committee for Electro-technical Standardization (CENELEC)
Audio/video, Information and Communication Technology Equipment - Safety Requirements

3) UL 62368-1, UL LLC.
Audio/video, Information and Communication Technology Equipment - Safety Requirements

4) CAN/CSA C22.2 No.62368-1, Canadian Standards Association (CSA).
Audio/video, Information and Communication Technology Equipment - Safety Requirements

5) IEC 60065, The International Electro-technical Commission (IEC).
Audio, Video and Similar Electronic Apparatus - Safety Requirements

7-2. Environment

(1) RoHS, Commission Delegated Directive (EU) 2015/863 of 31 March 2015 amending Annex II to Directive 2011/65/EU of the European Parliament and of the Council

8. Packing

8-1. Information of OLED Module Label

a) Lot Mark

A	B	C	D	E	F	G	H	I	J	K	L	M

A,B,C : SIZE(INCH)
D : YEAR
E : MONTH
F ~ M : SERIAL NO.

Note

1. YEAR

Year	2020	2021	2022	2023	2024	2025	2026	2027	2028	2029
Mark	K	L	M	N	P	Q	R	S	T	U

2. MONTH

Month	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
Mark	1	2	3	4	5	6	7	8	9	A	B	C

b) Location of Lot Mark

Serial NO. is printed on the label. The label is attached to the backside of the OLED module.
This is subject to change without prior notice.

8-2. Packing Form

a) Package quantity in one Pallet : 12 pcs

b) Pallet Size : 2,260 mm(W) X 1,520 mm(D) X 1,194 mm(H)

9. Precautions

Please pay attention to the followings when you use this OLED Board Assy.

9.1 Operating Precautions

(1) The spike noise causes the mis-operation of circuits. It should be lower than following voltage :
V=±200mV(Over and under shoot voltage)
(2) Response time depends on the temperature.(In lower temperature, it becomes longer.)
(3) Be careful for condensation at sudden temperature change. Condensation makes damage to polarizer or electrical contacted parts. And after fading condensation, smear or spot will occur.
(4) When fixed patterns are displayed for a long time, Image Retention is likely to occur.
- If the fixed image remains stationary, it is recommended to apply luminance reduction or screen protection function to the set to prevent from image sticking
- Please contact us in advance if you plan to use the display with the same pattern for an extended
(5) Module has high frequency circuits. Sufficient suppression to the electromagnetic interference shall be done by system manufacturers. Grounding and shielding methods may be important to minimized the interference.
(6) Please do not give any mechanical and/or acoustical impact to Module. Otherwise, Module can't be operated its full characteristics perfectly.
(7) A screw which is fastened up the steels should be a machine screw.
(if not, it can causes conductive particles and deal Module a fatal blow)
(8) Please do not set OLED on its edge.

9-2. Electrostatic Discharge Control

Since a module is composed of electronic circuits, it is not strong to electrostatic discharge. Make certain that treatment persons are connected to ground through wrist band etc. And don't touch interface pin directly.

9-3. Precautions for Strong Light Exposure

Strong light exposure causes degradation of polarizer and color filter.

9-4. Storage Precautions

When storing Board Ass'y as spares for a long time, the following precautions are recommended.

Storage conditions for packing

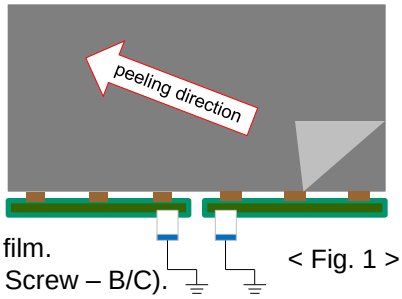
Item	Temperature	Humidity	Period
Storage Standard	5~35℃	35~75%	12months

(1) It is recommended to store in an environment equipped with a dark and air conditioning / ventilation system and a room in controlling specific condition.
(2) It must be stored in a space composed of general air atmosphere.
(3) Do not expose the module to sunlight or fluorescent light.
(4) Contact with humid spaces, rainy environments, high humid atmosphere, moisture and condensation within package is prohibited.
(5) Storing products in outside environment and out door is prohibited.
(6) If products are stored in specified conditions over more than 3 months, it is recommended to check the product packaging condition.

9-5. Handling Precautions for Protection Film

(1) The protection film is attached to the bezel with a small masking tape.
When the protection film is peeled off, static electricity is generated between the film and polarizer.
This should be peeled off slowly and carefully by people who are electrically grounded and with well ion-blown equipment or in such a condition, etc.
(2) When the module with protection film attached is stored for a long time, sometimes there remains a very small amount of glue still on the bezel after the protection film is peeled off.
(3) You can remove the glue easily. When the glue remains on the bezel surface or its vestige is recognized, please wipe them off with absorbent cotton waste or other soft material like chamois soaked with normal-hexane.

9-7. Handling Precautions for Protection Film

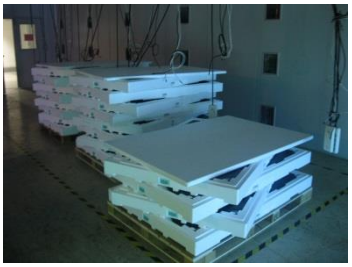


< Fig. 1 >

(1) Please don't remove the protection film before assembly.
(2) Please peel off the protection film slowly.
(3) Please peel off the protection film just like shown in the Fig.1
(4) Ionized air should be blown over during the peeling.
(5) Source PCB should be connected to the ground when peel off the protection film.
Normal assembled ground path will be no problem(S-PCB – FFC – C-PCB – Screw – B/C).
(6) The protection film should not be contacted to the source D-IC during peeling it off.
(7) When handling the polarizer, in particular, please be aware of the following precautions.
- Please do not damage on the edge of the polarizer in any form.
- Peeling off the protection film must be done only with the adhesive tape, not with other means by fingers, tweezers and so on.
- It is recommended to peel off the protection film as slowly as possible at an initial step.
- Refer to Appendix – XVI for more details

9-8. B/A Box Pretreatment Precautions

In winter season , in particular, please be aware of the following precautions.
(1) Before putting B/A boxes on the line, aging process is required to make the temperature of products similar to the temperature of workplace.
(2) Place the lid open on the B/A box and allowed to stand for 24 hours in the similar environment of work place. It was shown in Fig.2



< Fig. 2 >

9-9. Packing Precautions

Product assembled into module should be stored in the Al-bag(cover case).

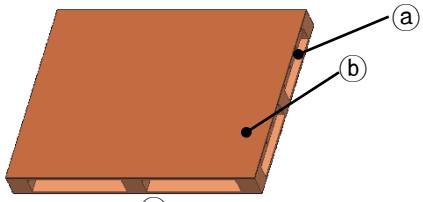
APPENDIX - I

■ Pallet Ass'y

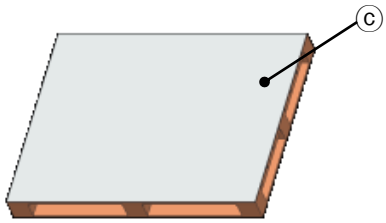
a) B/Ass'y Qty + PE Sheet / Box : 12pcs + 13pcs
b) B/Ass'y Qty / Pallet : 72pcs
c) Oxygen Absorber + Desiccant / Box : 10ea + 20ea
d) Oxygen Absorber + Desiccant / Pallet : 60ea + 120ea
e) Box Qty / Pallet : 6Box

※ The q'ty and position of oxygen absorber & desiccant can be changed.

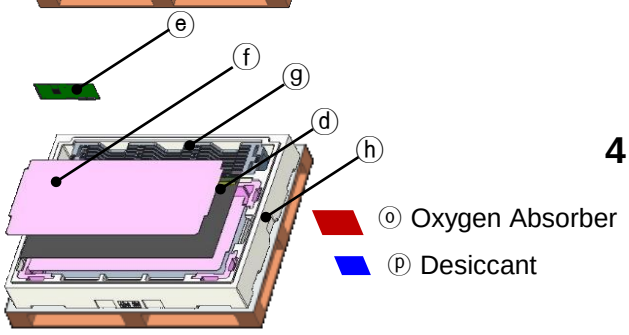
1



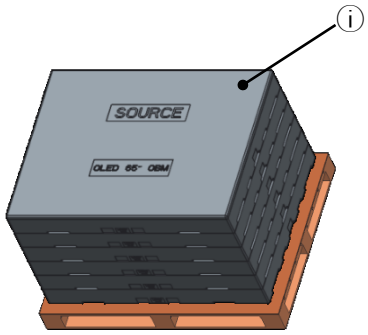
2



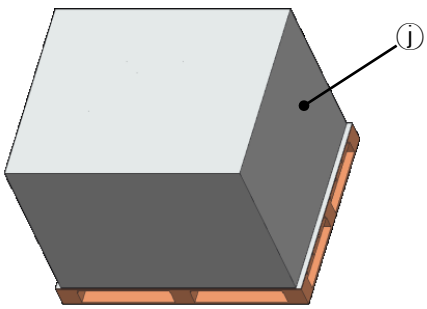
3



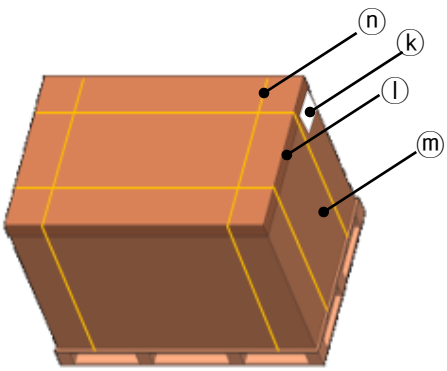
4



5



6

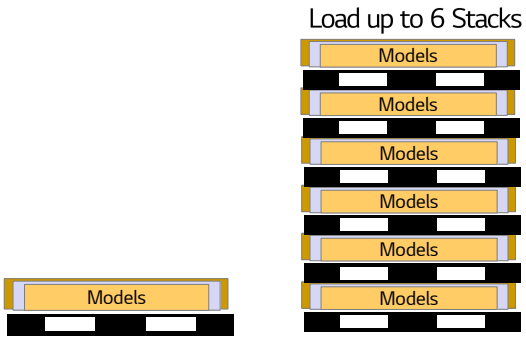


No.	Description	Material
ⓐ	Pallet	Plywood
ⓑ	Carton Plate	Paper(SW)
ⓒ	AL Sheet	AL
ⓓ	Board Ass'y	-
ⓔ	Include TCON 1ea	-
ⓕ	PE Sheet	LDPE
ⓖ	C-PCB Packing	EPS
ⓗ	Bottom Packing	EPS
	AL-Cushion	LDPE+AL
ⓘ	Top Packing	EPS
ⓙ	AL Bag	AL
ⓚ	Label	YUPO
ⓛ	Angle Cover	Paper(SW)
ⓜ	Angle Packing	Paper(SW)
ⓝ	Band	PP
ⓞ	Oxygen Absorber	
ⓟ	Desiccant	

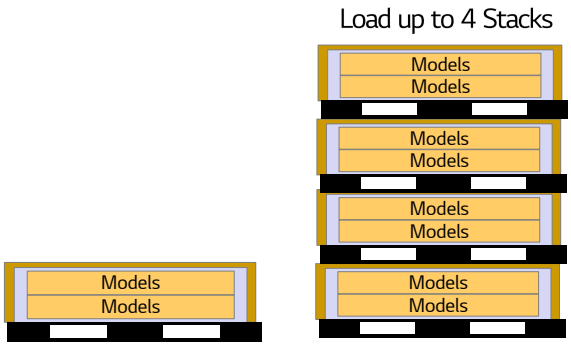
APPENDIX – I-2

■ Non Full Pallet Packing

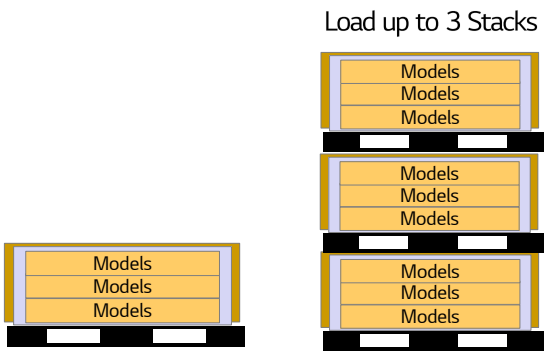
① 1Box Per Pallet



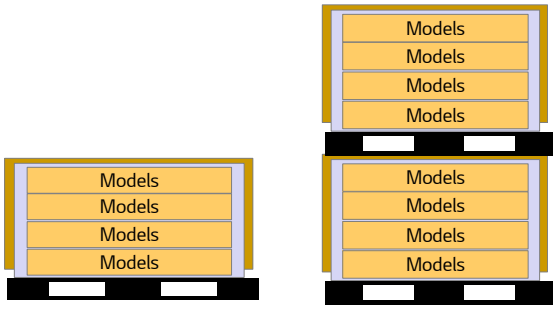
② 2Box Per Pallet



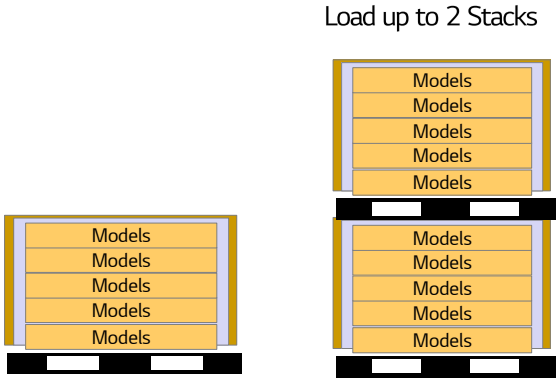
③ 3Box Per Pallet



④ 4Box Per Pallet



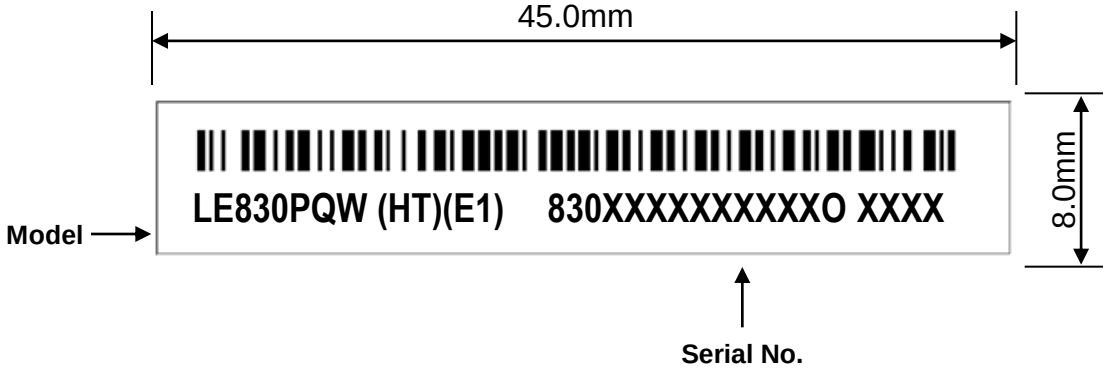
③ 5Box Per Pallet



APPENDIX - II

■ Board Ass'y Label

■ Control PCB Label



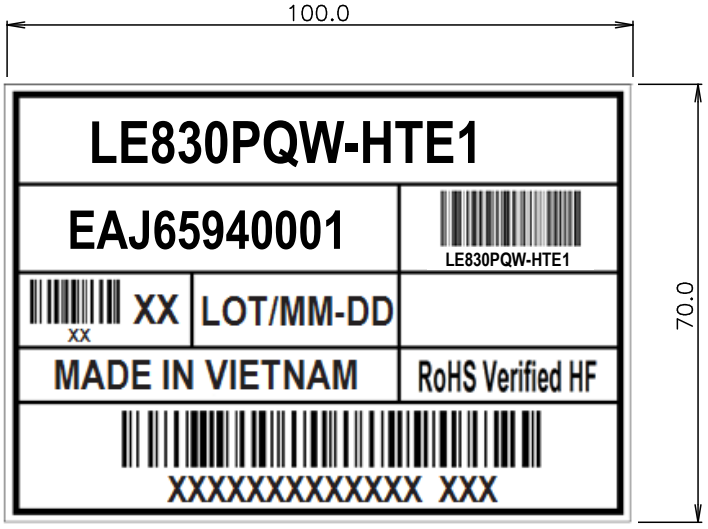
APPENDIX - III

■ Box Pallet Label

If KR(Korea PAJU FAB), “” (Blank).

If CO(China Ghangzhou OLED FAB), “(CO)”

■ Pallet Label

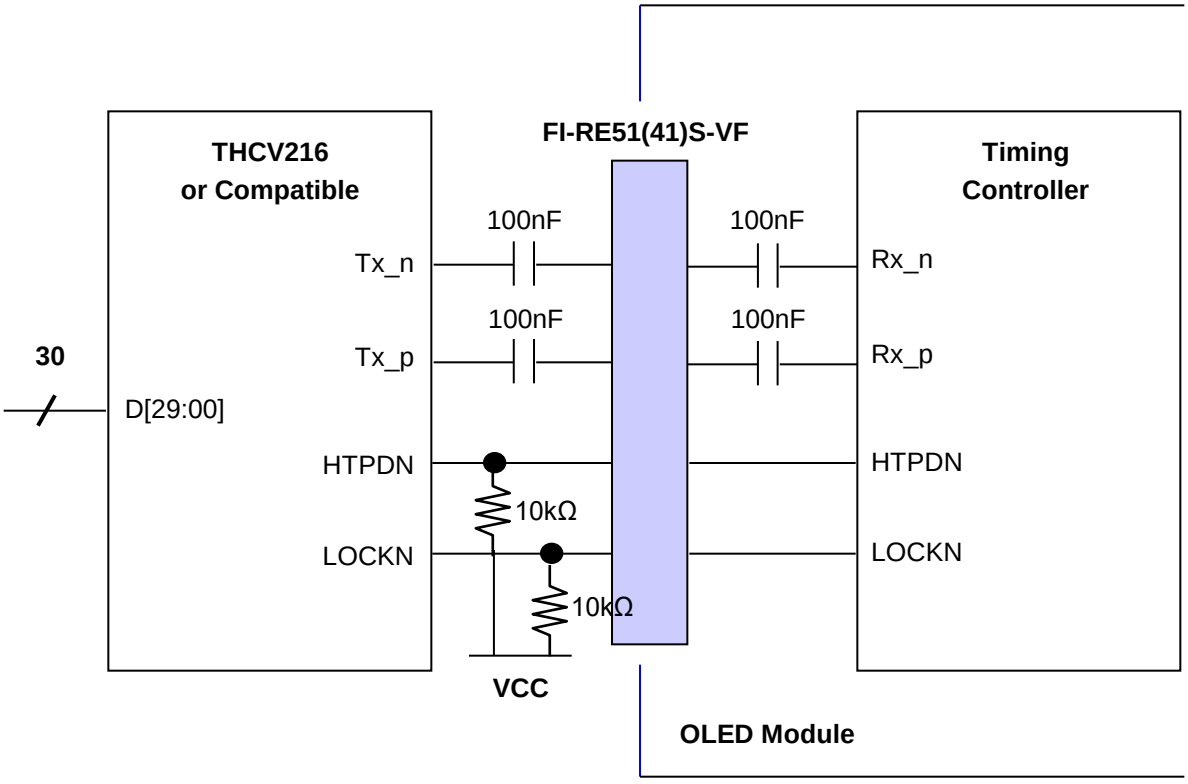


* LGD Haiphong : MADE IN VIETNAM

* LGD Guangzhou : MADE IN CHINA

APPENDIX – Ⅳ

■ Required signal assignment for Flat Link (Thine : THCV215) Transmitter

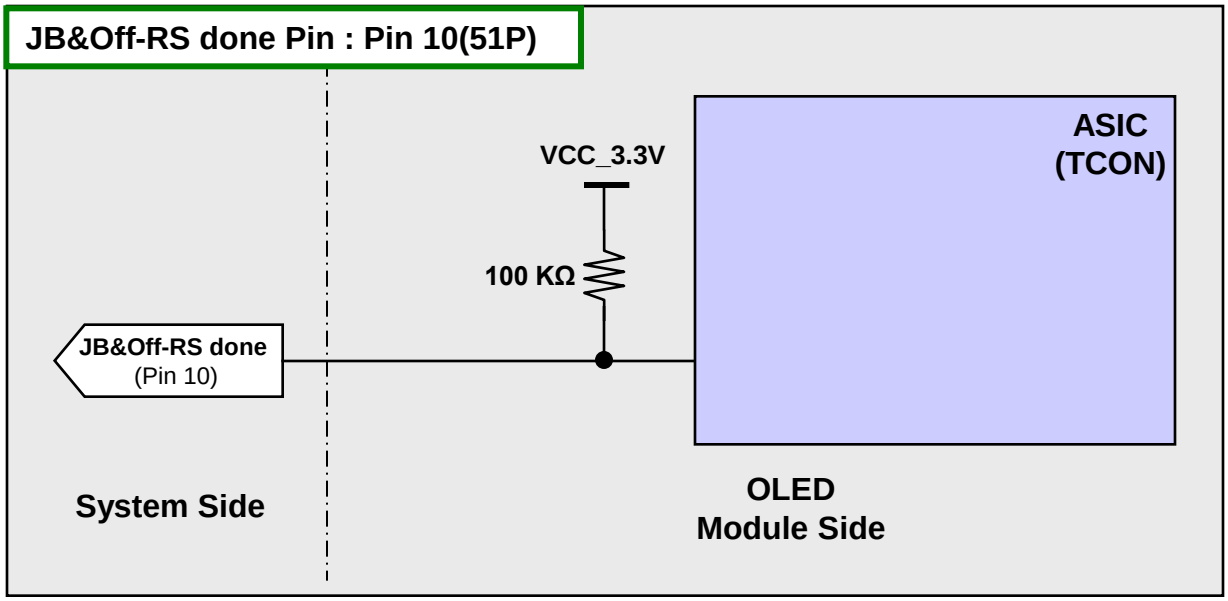


Note: 1. The OLED module uses a 100 nF capacitor on positive and negative lines of each receiver input.
2. Refer to V by One Transmitter Data Sheet for detail descriptions. (THCV216 or Compatible)
3. About Module connector pin configuration, Please refer to the Page 7~8.

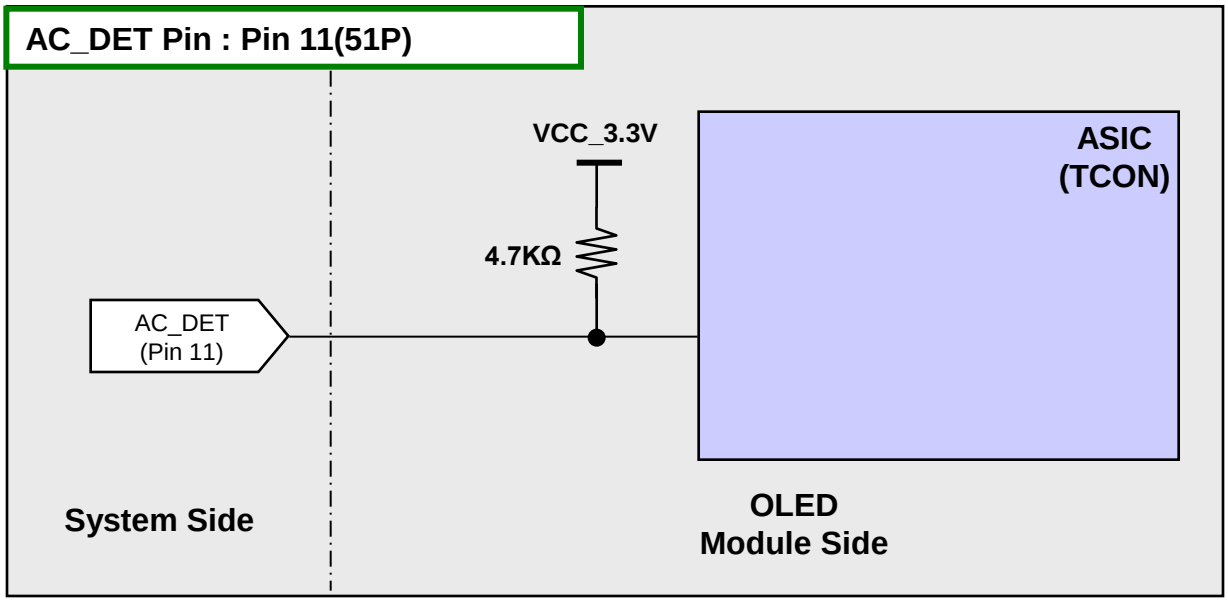
APPENDIX – Ⅴ - 1

■ **Option Pin** Circuit Block Diagram

1) Circuit Block Diagram of **JB&Off-RS done** pin



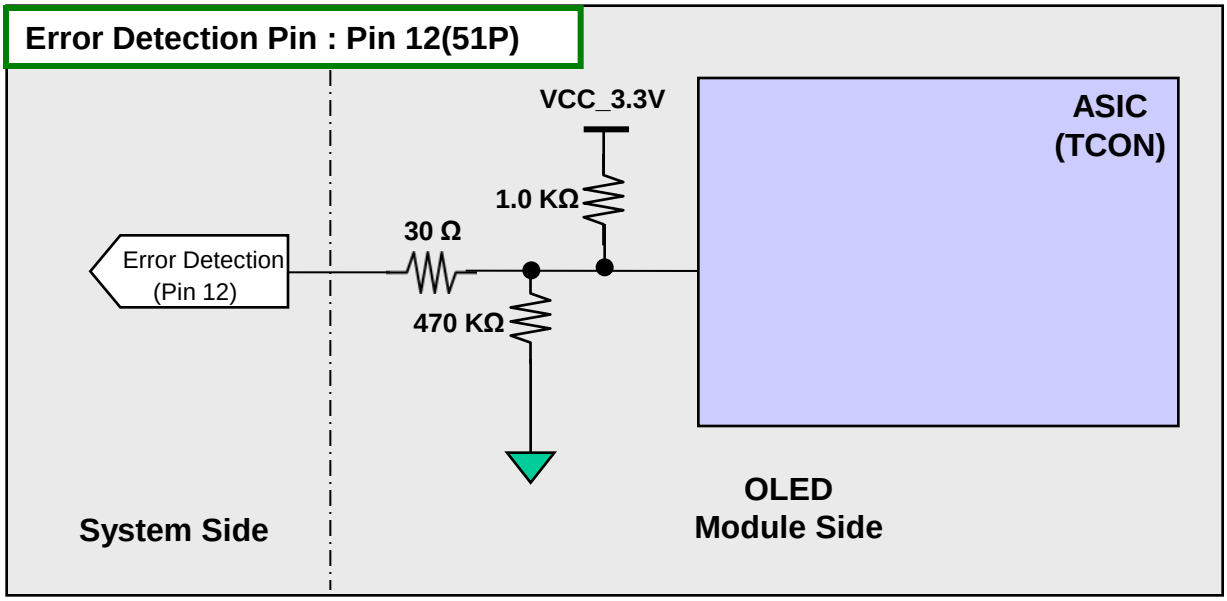
2) Circuit Block Diagram of **ELVDD ON** pin



APPENDIX - Ⅴ - 2

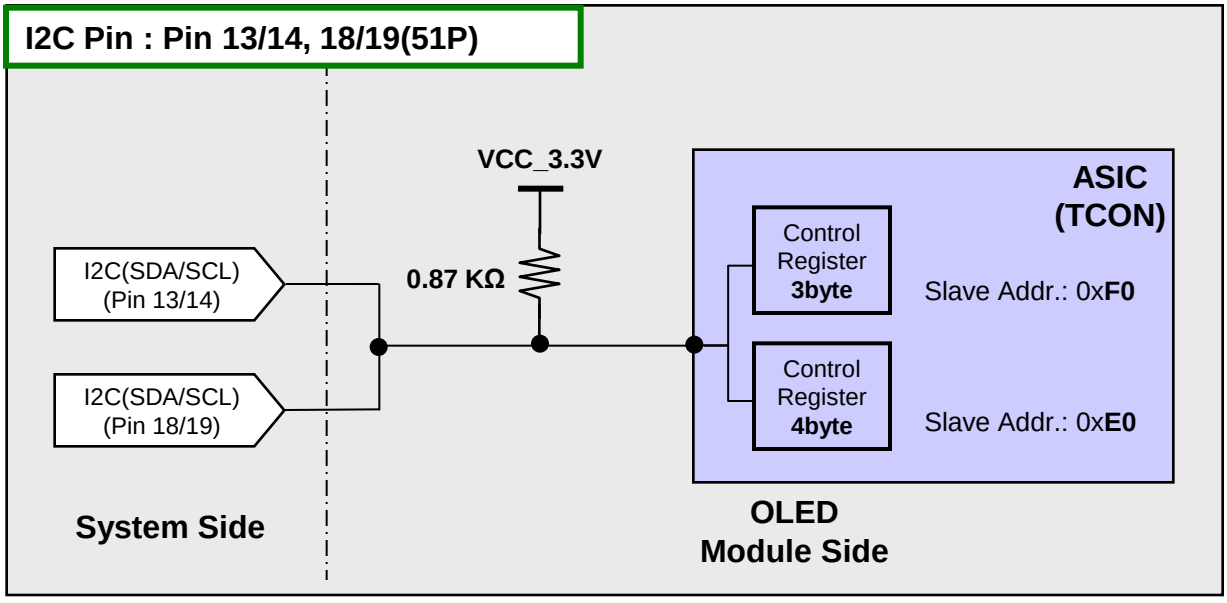
■ Circuit Block Diagram for Option Pin

3) Circuit Block Diagram of **Error Detection** pin



※ It is recommended to turn power off the module immediately when error detection signal is occurred.

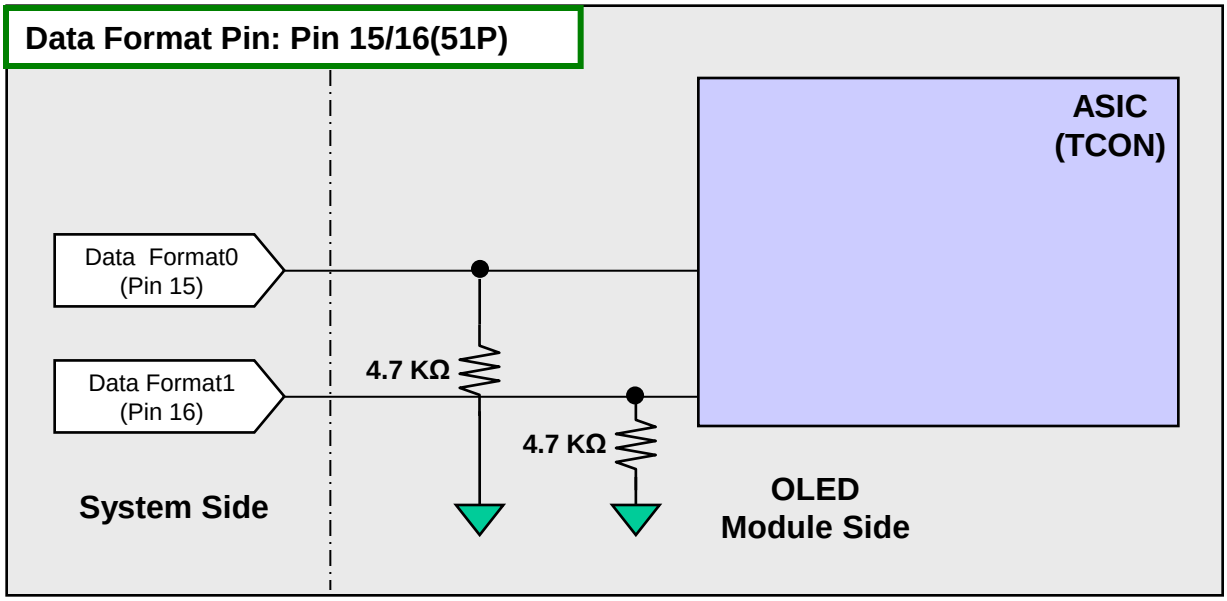
(4) Circuit Block Diagram of **I2C(SDA/SCL)** pin



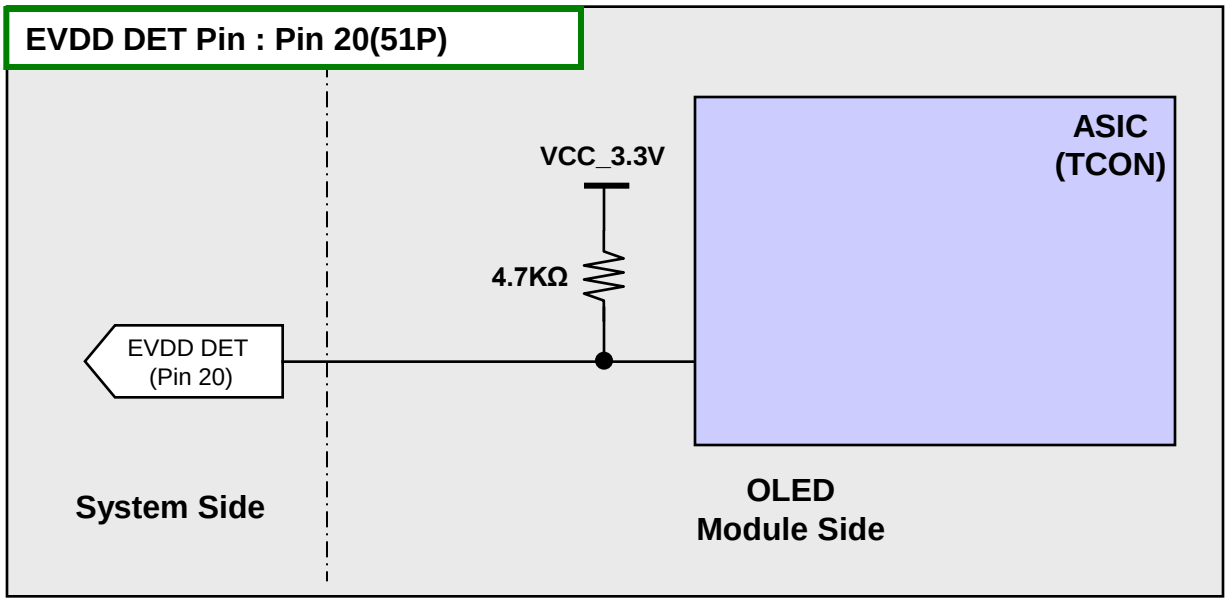
APPENDIX - Ⅴ - 3

■ Circuit Block Diagram for Option Pin

(5) Circuit Block Diagram of Data Format pin



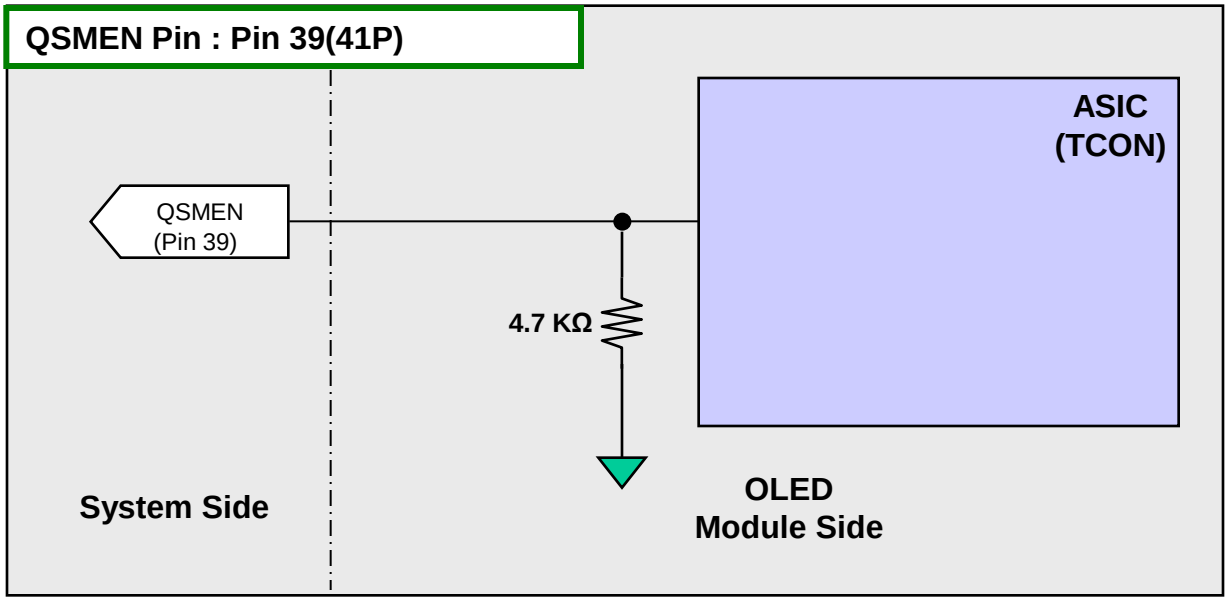
6) Circuit Block Diagram of EVDD DET pin



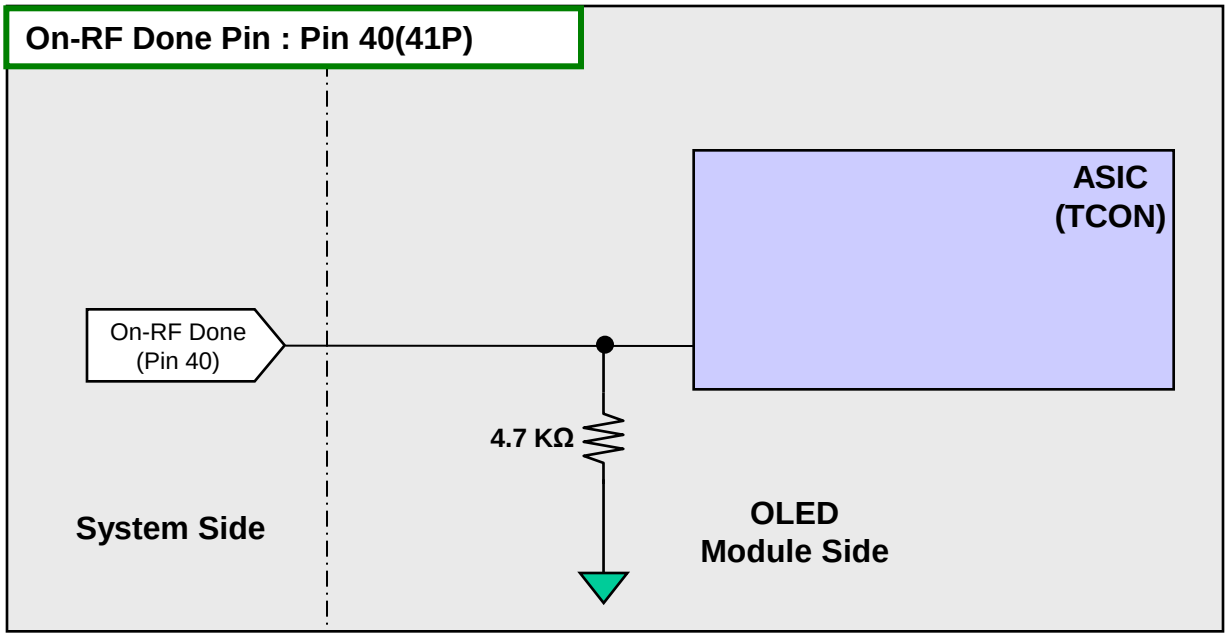
APPENDIX – Ⅴ - 4

■ Circuit Block Diagram for Option Pin

(7) Circuit Block Diagram of **QSMEN** pin



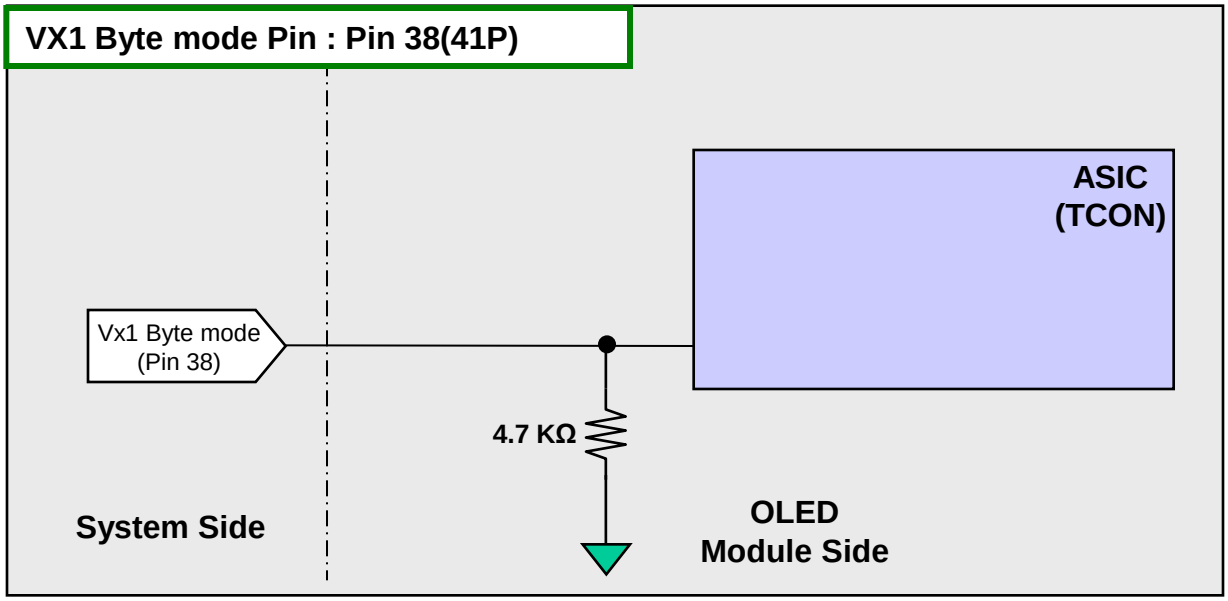
(8) Circuit Block Diagram of **On-RF Done** pin



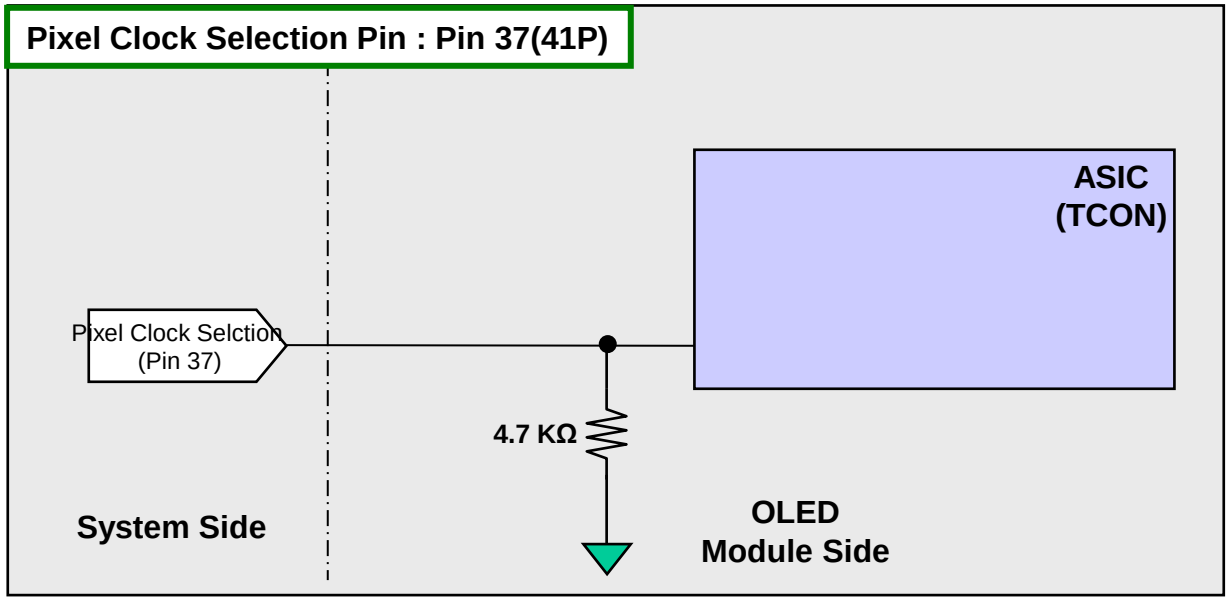
APPENDIX – Ⅴ - 4

■ Circuit Block Diagram for Option Pin

(9) Circuit Block Diagram of Vx1 Byte mode pin



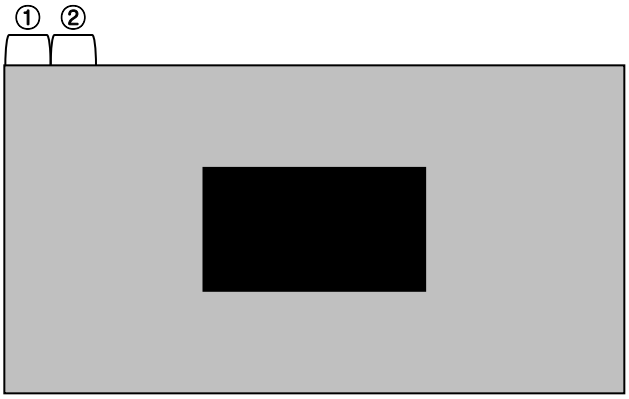
(10) Circuit Block Diagram of Pixel Clock Selection pin



APPENDIX - Ⅵ - 1

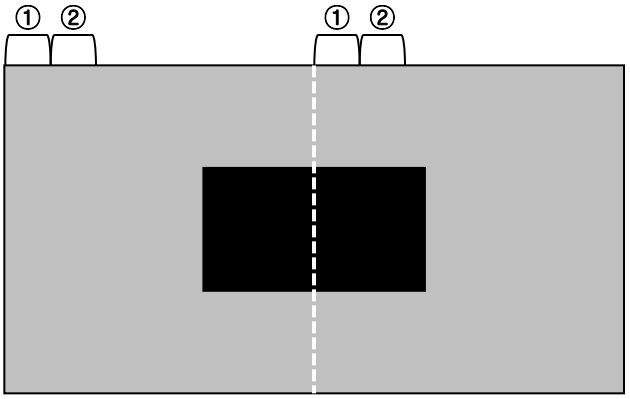
■ Input mode of Pixel Data

Mode 1 : 1-Division Mode



	1'st Data	2'nd Data	…	Data #
Lane00	1	17	…	3825
Lane01	2	18	…	3826
Lane02	3	19	…	3827
Lane03	4	20	…	3828
Lane04	5	21	…	3829
Lane05	6	22	…	3830
Lane06	7	23	…	3831
Lane07	8	24	…	3832
Lane08	9	25	…	3833
Lane09	10	26	…	3834
Lane10	11	27	…	3835
Lane11	12	28	…	3836
Lane12	13	29	…	3837
Lane13	14	30	…	3838
Lane14	15	31	…	3839
Lane15	16	32	…	3840

Mode 2 : 2 Division Mode

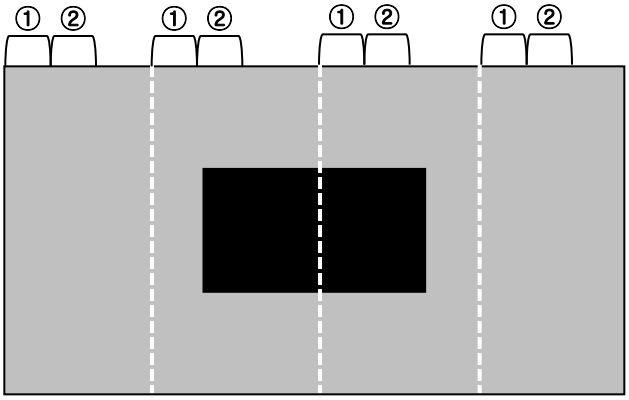


	1'st Data	2'nd Data	…	Data #
Lane00	1	9	…	1913
Lane01	2	10	…	1914
Lane02	3	11	…	1915
Lane03	4	12	…	1916
Lane04	5	13	…	1917
Lane05	6	14	…	1918
Lane06	7	15	…	1919
Lane07	8	16	…	1920
Lane08	1921	1929	…	3833
Lane09	1922	1930	…	3834
Lane10	1923	1931	…	3835
Lane11	1924	1932	…	3836
Lane12	1925	1933	…	3837
Lane13	1926	1934	…	3838
Lane14	1927	1935	…	3839
Lane15	1928	1936	…	3840

APPENDIX – Ⅵ - 2

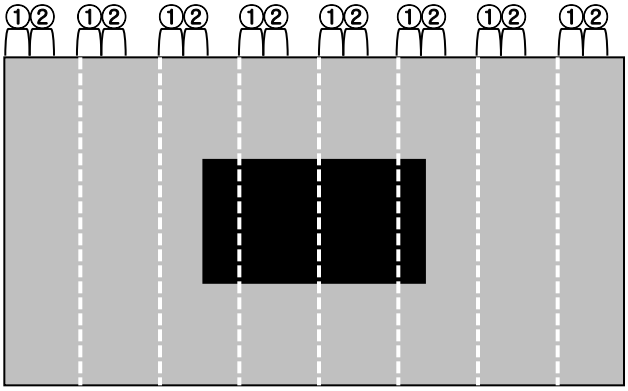
■ Input mode of Pixel Data

Mode 3 : 4 Division Mode



	1'st Data	2'nd Data	…	Data #
Lane00	1	5	…	957
Lane01	2	6	…	958
Lane02	3	7	…	959
Lane03	4	8	…	960
Lane04	961	965	…	1917
Lane05	962	966	…	1918
Lane06	963	967	…	1919
Lane07	964	968	…	1920
Lane08	1921	1925	…	2877
Lane09	1922	1926	…	2878
Lane10	1923	1927	…	2879
Lane11	1924	1928	…	2880
Lane12	2881	2885	…	3837
Lane13	2882	2886	…	3838
Lane14	2883	2887	…	3839
Lane15	2884	2888	…	3840

Mode 4 : 8 Division Mode



	1'st Data	2'nd Data	…	Data #
Lane00	1	3	…	479
Lane01	2	4	…	480
Lane02	481	483	…	959
Lane03	482	484	…	960
Lane04	961	963	…	1439
Lane05	962	964	…	1440
Lane06	1441	1443	…	1919
Lane07	1442	1444	…	1920
Lane08	1921	1923	…	2399
Lane09	1922	1924	…	2400
Lane10	2401	2403	…	2879
Lane11	2402	2404	…	2880
Lane12	2881	2883	…	3359
Lane13	2882	2884	…	3360
Lane14	3361	3363	…	3839
Lane15	3362	3364	…	3840

APPENDIX – Ⅶ

■ ASIC Firmware

Category	FW version Value	Checksum Value
CAS Final	C.0A.01.04.0	0F0A1147

■ Register map

The following register is controlled by I2C Interface.

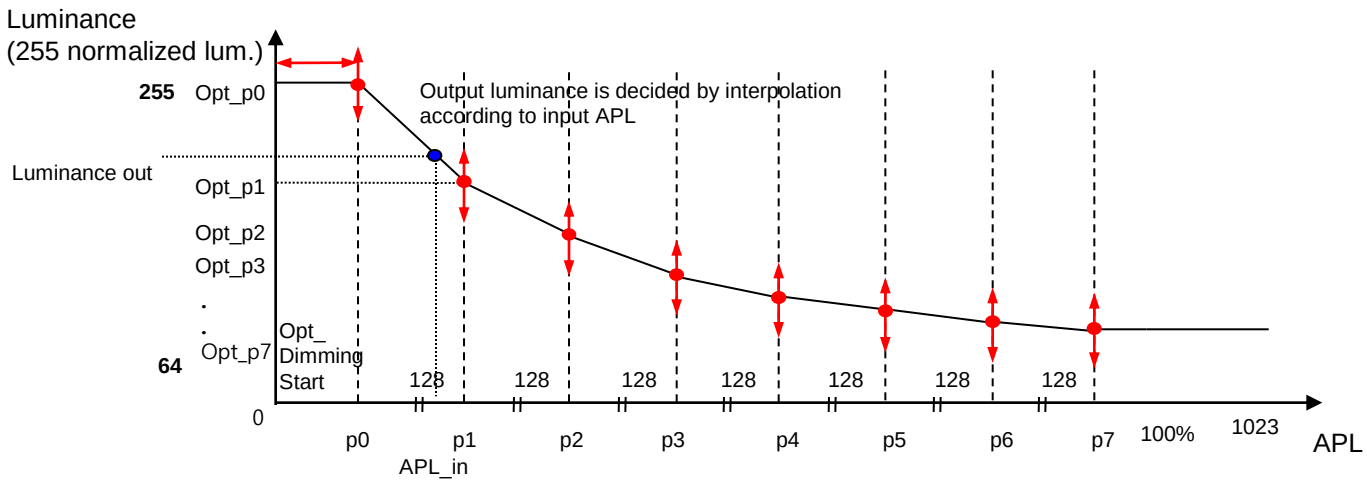
	Bit[7]: MSB	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]: LSB
Addr : 0x001	**CPC EN**	**TPC EN**	**RGB Max APL**	**OFF RS enable**	**APLC EM**	**WAPL enable**	**Opt_ Dimmin_ start[9]**	**Opt_ Dimming start[8]**

Device Address: 0xE0(Control Register 4byte) or 0xF0(Control Register 3byte)

Address [Hex]	Register Name	Description	Remark
0x000	Valid	Read only register (LGD use)	
0x001	[7] : CPC enable	1: enable, 0: disable	
	[6] : TPC enable	1: enable, 0: disable	
	[5] : RGB Max APL	1: RGB, 0: Y (BT.709)	
	[4] : Off RS enable	1: enable, 0: disable	
	[3] : APLC Enable	1: enable, 0: disable	
	[2] : WAPL enable	1: WAPL, 0 : normal APL	
	[1:0] Opt_Dimming_start[9:8]	APL value of P0 point	Value Range: 0~1023
0x002	Opt_Dimming_start[7:0]		
0x003	Opt_p0	APL P0 point corresponds to the 255 normalized luminance	(Opt_p0 /114) * 200 nit
0x004	Opt_p1	APL P1 point corresponds to the 255 normalized luminance	(Opt_p1 /114) * 200 nit
0x005	Opt_p2	APL P2 point corresponds to the 255 normalized luminance	(Opt_p2 /114) * 200 nit
0x006	Opt_p3	APL P3 point corresponds to the 255 normalized luminance	(Opt_p3 /114) * 200 nit
0x007	Opt_p4	APL P4 point corresponds to the 255 normalized luminance	(Opt_p4 /114) * 200 nit
0x008	Opt_p5	APL P5 point corresponds to the 255 normalized luminance	(Opt_p5 /114) * 200 nit
0x009	Opt_p6	APL P6 point corresponds to the 255 normalized luminance	(Opt_p6 /114) * 200 nit
0x00A	Opt_p7	APL P7 point corresponds to the 255 normalized luminance	(Opt_p7 /114) * 200 nit

Address [Hex]	Register Name	Description	Remark
0x00B	[7] Not used	LGD reserved	
	[6:5] LEA mode sel.	b00: Normal operation, **b01 / b10 / b11: LGD reserved**	
	[4] LEA refresh en	1: LEA refresh , 0: Normal LEA	
	[3] : HDR_en	1: Enable, 0: Disable	
	[2] : Not used	LGD reserved	
	[1:0]:Opt WAPL_Dimming_start[9:8]	APL value of P0 point	Value Range: 0~1023
0x00C	Opt_WAPL_Dimming_start[7:0]		
0x00D	Opt_WAPL_p0	APL P0 point corresponds to the 255 normalized luminance	Value Range: 0~255
0x00E	Opt_WAPL_p1	APL P1 point corresponds to the 255 normalized luminance	Value Range: 0~255
0x00F	Opt_WAPL_p2	APL P2 point corresponds to the 255 normalized luminance	Value Range: 0~255
0x010	Opt_WAPL_p3	APL P3 point corresponds to the 255 normalized luminance	Value Range: 0~255
0x011	Opt_WAPL_p4	APL P4 point corresponds to the 255 normalized luminance	Value Range: 0~255
0x012	Opt_WAPL_p5	APL P5 point corresponds to the 255 normalized luminance	Value Range: 0~255
0x013	Opt_WAPL_p6	APL P6 point corresponds to the 255 normalized luminance	Value Range: 0~255
0x014	Opt_WAPL_p7	APL P7 point corresponds to the 255 normalized luminance	Value Range: 0~255

❑ PLC curve parameter



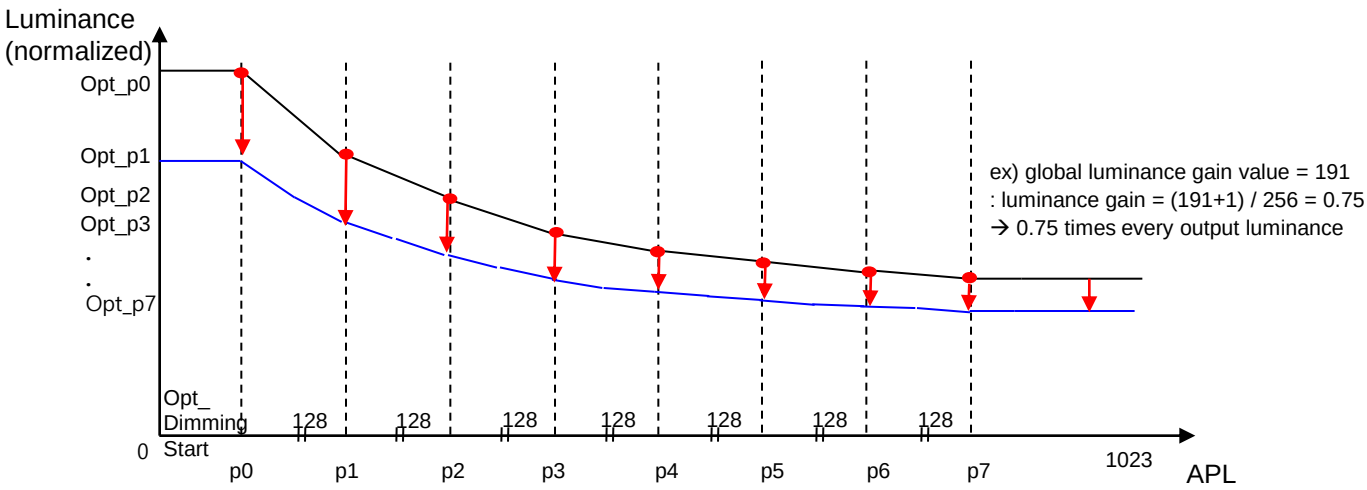
Every interval between each points except P0 is fixed to 128

- Luminance of p7~1023 interval are Opt_p7
- The point over 1023 is discarded

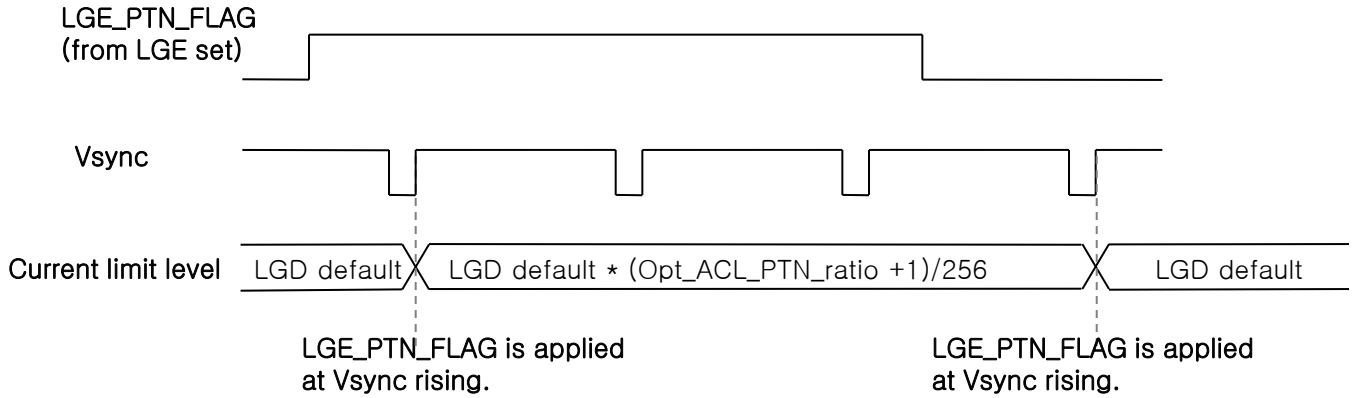
In case customer set luminance level high extending default PLC curve LGD designed, “Image Sticking” may not be guaranteed caused by this setting.

Address [Hex]	Register Name	Description	Remark
0x016	Opt_global_luminance_gain	Adjust global luminance gain 0~1 luminance gain according to 0~255 value (Same luminance gain is applied to every P0~P7 points)	Value Range: 0~255
0x017	Opt_ACL_PTN_ratio	Adjust ACL level gain for LGE PTN detect	Value Range: 0~255
0x054	[7] Power Off Enable	1: Enable, 0: Disable (JB Update)	
	[6:0] Not used	LGD reserved	
0x05D	[7] vsJB_en	1: Enable, 0: Disable	
	[6:0] Not used	LGD reserved	
0x05E	Test_temp1[15:8]	1st temperature sensor	Read only
0x05F	Test_temp1[7:0]		

❑ Global luminance gain



❑ Current limit level changes according to LGE PTN detect



Address [Hex]	Register Name	Description	Remark
0x07F	[7] Not used	LGD reserved	
	[6] Frame delay	1: 0frame, 0:1frame	
	[5] HDR EN@5byte mode only	1:11bit-HDR(HDR PASS mode) On, 0:10bit-HDR on	
	[4] : Reserved	[4] Reserved	
	[3] :144/120hz	1: 144hz, 0:120hz	
	[2] : Hz change Protocol	1:PKT , 0: I2C	
	[1:0] : The number of CTL data	The number of CTL data transmission channel for APL cross check(rage 3~16)	

Address [Hex]	Register Name	Description	Remark
0x1FF4 ~0X1FFF	[7:0] : P-ID	P-ID	Read only

APPENDIX - Ⅷ-1

■ Gray to Gray Response Time Uniformity

This is only the reference data of G to G and uniformity for LE830PQW-HTE1 model.

(1) G to G Response Time :
Response time is defined as FIG. 3 and shall be measured by switching the input signal for "Gray (N) " and "Gray(M)".(32Gray Step at 8bit)

(2) G to G Uniformity
The variation of G to G Uniformity , $\delta_{G\ to\ G}$ is defined as :

$$\text{G to G Uniformity} = \frac{Maximum(GtoG) - Typical(GtoG)}{Typical(GtoG)} \leq 1$$

*Maximum (GtoG) means maximum value of measured time (N, M = 0 (Black) ~ 1023(White), 128 gray step).

	0Gray	127ray	255Gray	…	895Gray	1023Gray
0Gray		TrR:0G→127G	TrR:0G→255G	…	TrR:0G→895G	TrR:0G→1023G
127Gray	TrD:127G→0G		TrR:127G→255G	…	TrR:127G→895G	TrR:127G→1023G
255Gray	TrD:255G→0G	TrD:255G→127G		…	TrR:255G→895G	TrR:255G→1023G
…	…	…	…		…	…
895Gray	TrD:895G→0G	TrD:895G→127G	TrD:895G→255G	…		TrR:895G→1023G
1023Gray	TrD:1023G→0G	TrD:1023G→127G	TrD:1023G→255G	…	TrD:1023G→895G	

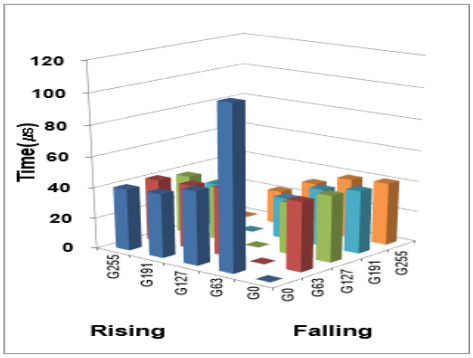
(3) Sampling Size : 2 pcs

(4) Measurement Method : Follow the same rule as optical characteristics measurement.

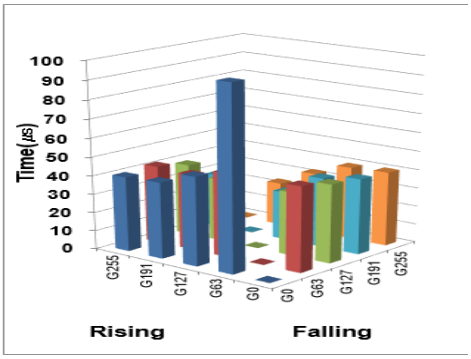
(5) Current Status

Below table is actual data of production on 8. 22. 2024 (LGD PRV Event Sample)

	G to G Response Time [ms]		Average
	Min.	Max.	
# 1	0.02	0.11	0.07
# 2	0.02	0.10	0.06



< # 1 >



< # 2 >

APPENDIX – Ⅷ-2

■ MPRT Response Time Uniformity (δ_{MPRT})

This is only the reference data of MPRT and uniformity for LE830PQW-HTE1 model.

1. MPRT Response Time :
   Response time is defined as FIG. 3

2. MPRT Uniformity
   The variation of MPRT Uniformity , δ_{MPRT} is defined as :

$$\text{MPRT Uniformity} = \frac{Maximum\ (MPRT) - Typical\ (MPRT)}{Typical\ (MPRT)} \leq 1$$

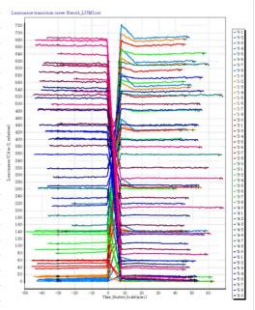
3. Sampling Size : 1 pcs

4. Measurement Method : Follow the same rule as optical characteristics measurement.

5. Current Status

   Below table is actual data of production on 8. 22. 2024 (LGD PRV Event Sample)

MPRT Response Time [ms] CMO Off		Average
Min.	Max.	
5.5	6.7	6.5



MPRT Rawdata

Max. Value
Min. Value

단위 : ms

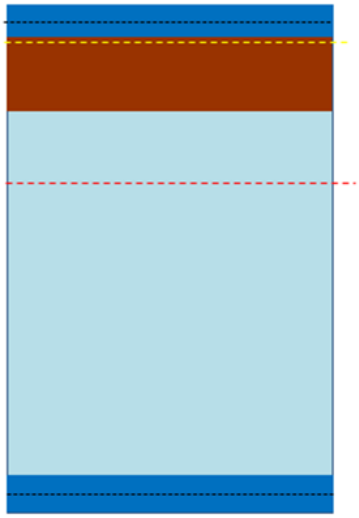
Sample #1		Final Value									Temperature
	Gray	G255	G223	G191	G159	G127	G95	G63	G31	G0	상온
Initial Value	G255	-	6.7	6.6	6.6	6.6	6.6	6.7	6.7	6.7	
	G223	6.7	-	6.6	6.6	6.6	6.6	6.6	6.7	6.7	Average
	G191	6.6	6.6	-	6.6	6.5	6.7	6.6	6.7	6.7	6.5
	G159	6.6	6.6	6.6	-	6.6	6.6	6.6	6.7	6.7	Standard Dev.
	G127	6.6	6.6	6.6	6.5	-	6.6	6.6	6.6	6.7	0.2
	G95	6.6	6.6	6.6	6.6	6.5	-	6.6	6.6	6.7	Maximum
	G63	6.5	6.5	6.5	6.5	6.5	6.4	-	6.5	6.6	6.7
	G31	6.5	6.4	6.4	6.4	6.4	6.3	6.1	-	-	Minimum
	G0	6.3	6.3	6.2	6.2	6.1	5.9	5.5	-	-	5.5

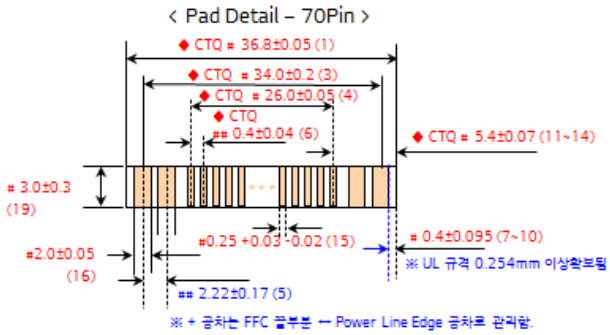
APPENDIX - IX

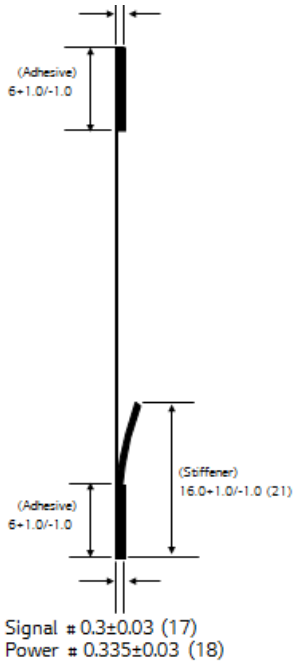
■ FFC INFORMATION (OLED Connector)

- **S-PCB : TF43SWG-66S_4-0.4SH** (manufactured by HIROSE)
- **C-PCB : TF43SWG-66S_4-0.4SH (**manufactured by HIROSE)

■ Drawing



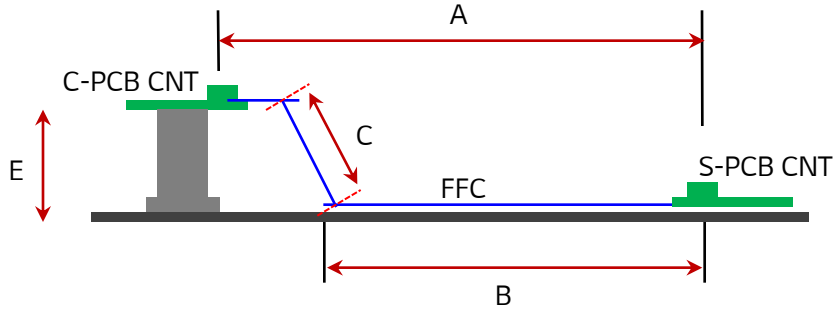


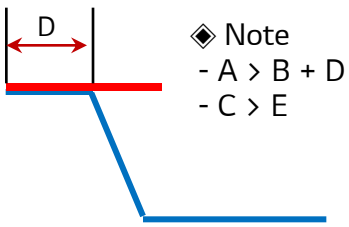


◈ Note
- Pad : GOLD Plating
- # ≥ Cpk 1.0
- ## ≥ Cpk 1.33
- H/F
- Dimension unit : mm

CTQ : Major Quality Control Indicators
Power Line : 2oz
Signal Line : 1oz
Impedance : 100 ohm (IMS Shield is Recommended)

■ Z-Bending guide





◈ Note
- A > B + D
- C > E

The FFC must be folded in a Z-shape to prevent the FFC connector FLIP from being pressed or opened.
In particular, it is necessary to use a gently folded Z-shape FFC for the slim set concept.

APPENDIX - X

■ PLC Curve

(1) It is recommended to the set the TV Set Peak Luminance to 50% of the Module Peak Luminance at P0 point in Default display mode for considering power savings and prevention of Image retention.
(Fig. 1. Set PLC Curve)

- If End users watch videos with fixed images such as broadcast logos for a long time at the level of Module Peak luminance, there is a risk of image retention defects.
Therefore, the shipping mode luminance control can proactively prevent the risk of image retention defects.
- If customer need to promote the Picture Quality, It is recommended to user store mode.
- It is recommended that the HDR function be applied to the module shipment condition, 'HDR Off'.

(2) It is recommended to automatically operate the light sensor 'On' in Set shipping mode.
- It is recommended to prevent the risk of eye fatigue and image retention defects through the user of appropriate illumination depending on the user's environment.

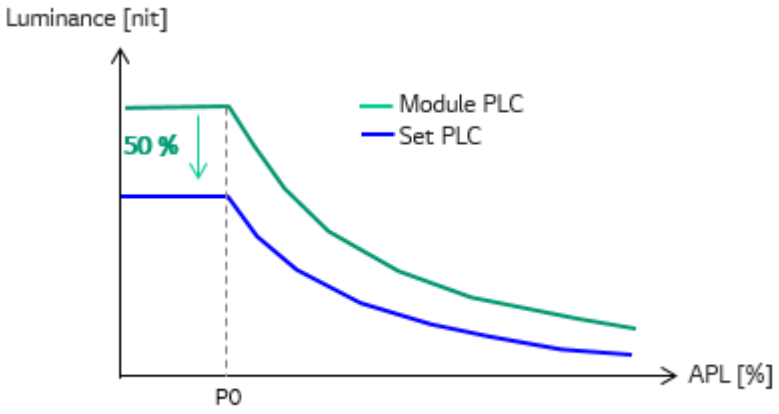


Fig. 1. Set PLC Curve

※ Default Display mode(End-user) : Set Peak Luminance ≤ 50% of Module Peak Luminance
※ Shipment mode : Picture mode first used by end-users after factory shipments
ex) Standard mode

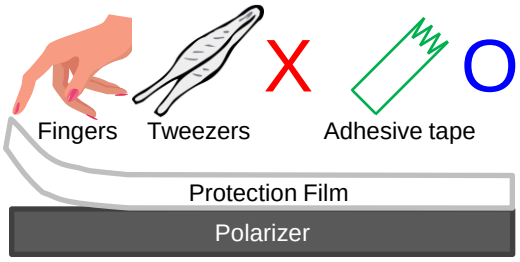
APPENDIX - XI

■ Things to avoid to prevent the polarizer from breakage

Any kind of damage on the edge of the polarizer is not allowed. <Fig.1>

Use an adhesive tape to peel off the protection film from the polarizer. <Fig.2>

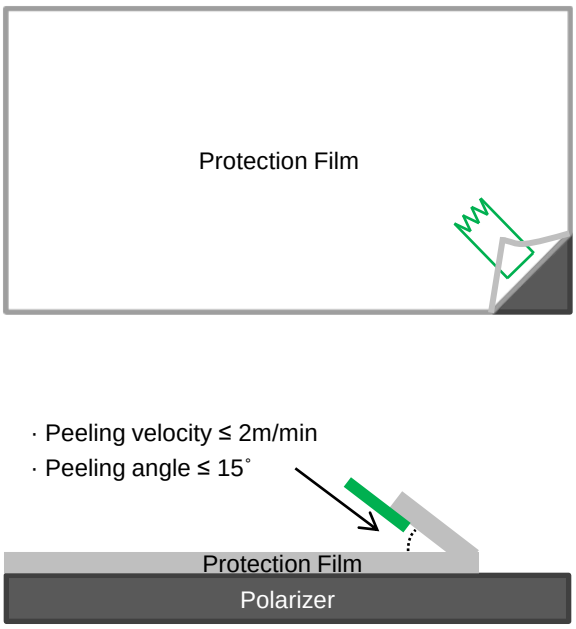
<Fig.1>



<Fig.2>

■ Recommended values for peeling velocity and angle

The values for peeling velocity and angle should be under 2m/min and 15 degrees each. <Fig.3>

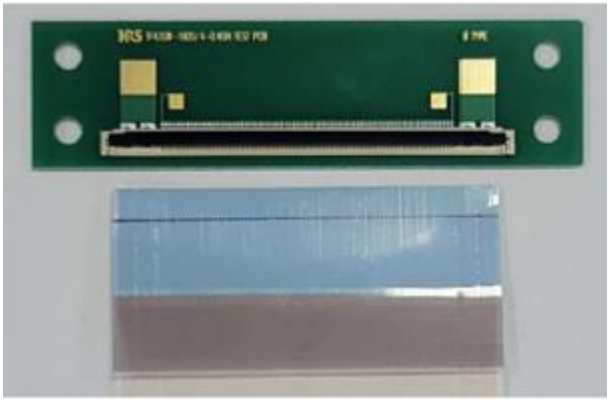


<Fig.3>

APPENDIX- XII

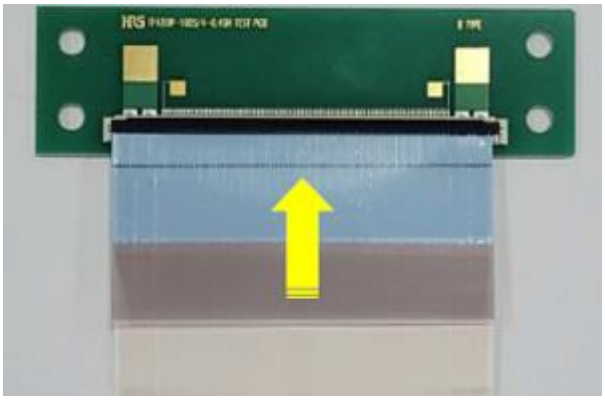
■ Guide for the FFC Connector fastening

1. Preparation for insert



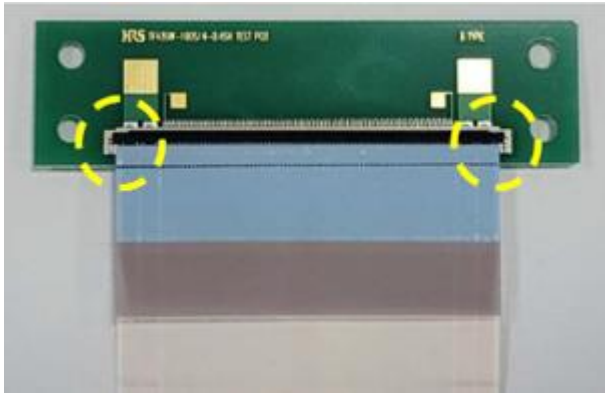
Place the FFC conductor face down
and parallel to the connector.

2. Insertion



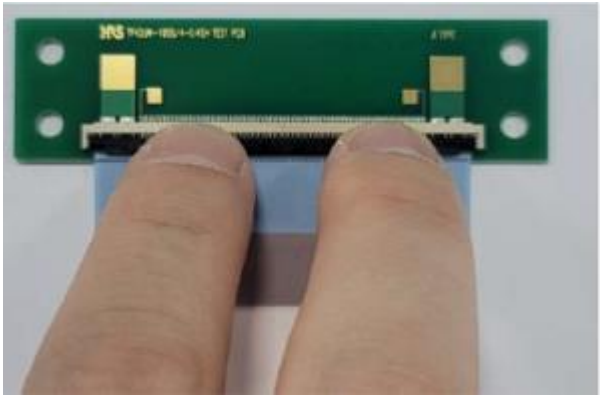
Insert the FFC horizontally and correctly without twisting.
When inserting from the corner as if swinging, it can be deformed by giving damage to the connector.

3. Completion of insertion



After the insertion, check the left and right sides Whether there is any abnormality.
(Non-inserted, twisted, inserted position)

4. Fastening



Fasten the actuator by closing the central part as if rotating.
(Because the connector is long, please close it using two fingers.)

APPENDIX - XIII

■ Integrated Power Measurement

FIG.x shows additional information concerning the Integrated power measurement equipment and method.

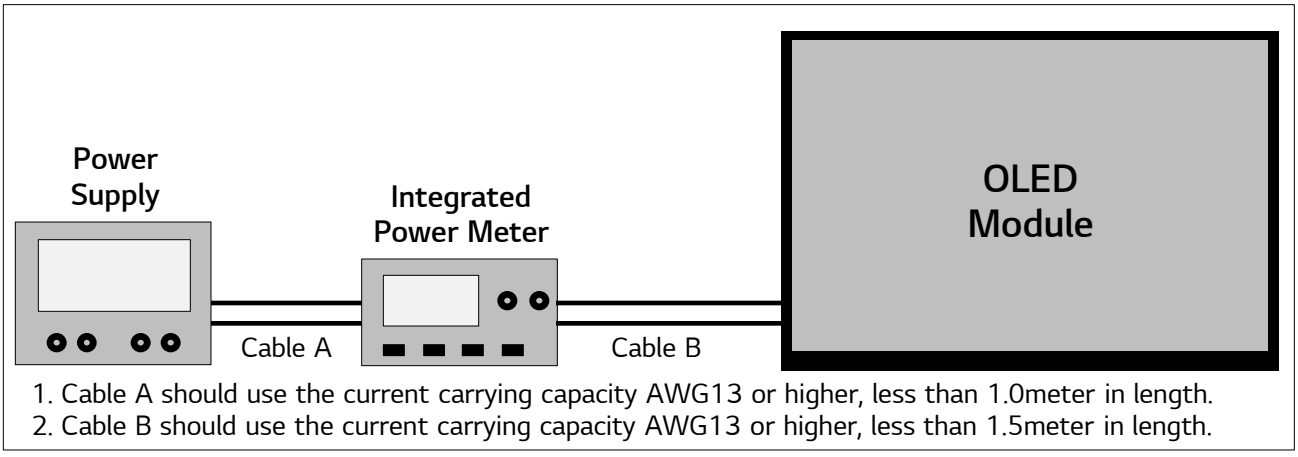


FIG.x Integrated Power Measurement Equipment and Method

■ Measurement Procedure

FIG.xx shows additional information concerning the Integrated power measurement procedure.

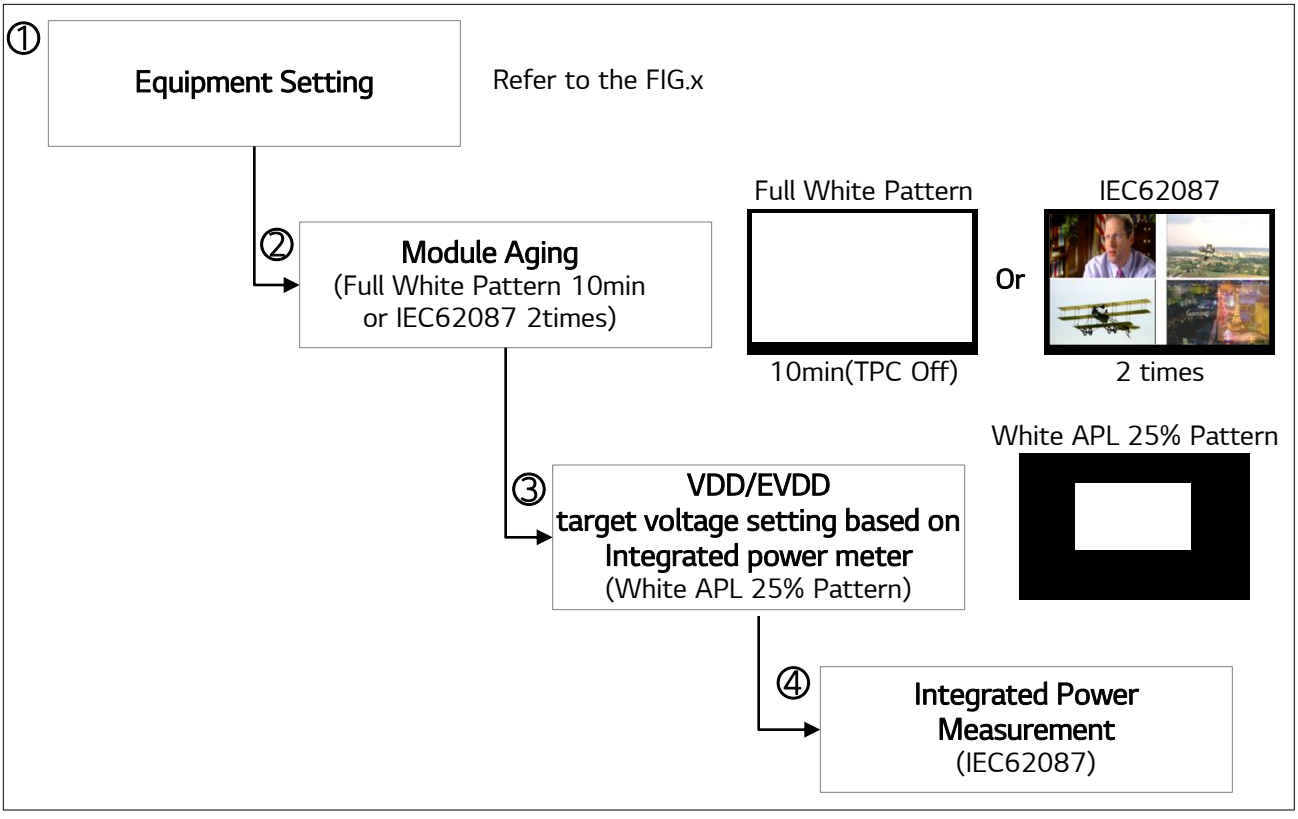


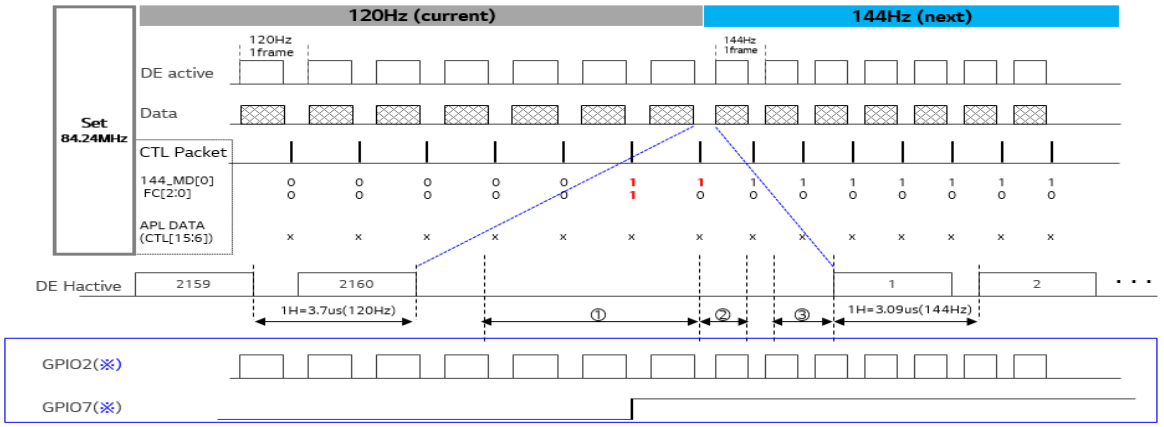
FIG.xx Integrated Power Measurement Procedure

APPENDIX – XIV-1

■ 144Hz 변환 Guide

V24 SET 120Hz ⟶ 144Hz CTL PKT 전환 Sequence

You Dream, We Display.



SET는 Vblank내에 CTL PKT 을 1번만 보내야함
CTL PKT을 통한 모드 전환 사용시 최소 4frame 동안 정상적인 sync를 보내야함

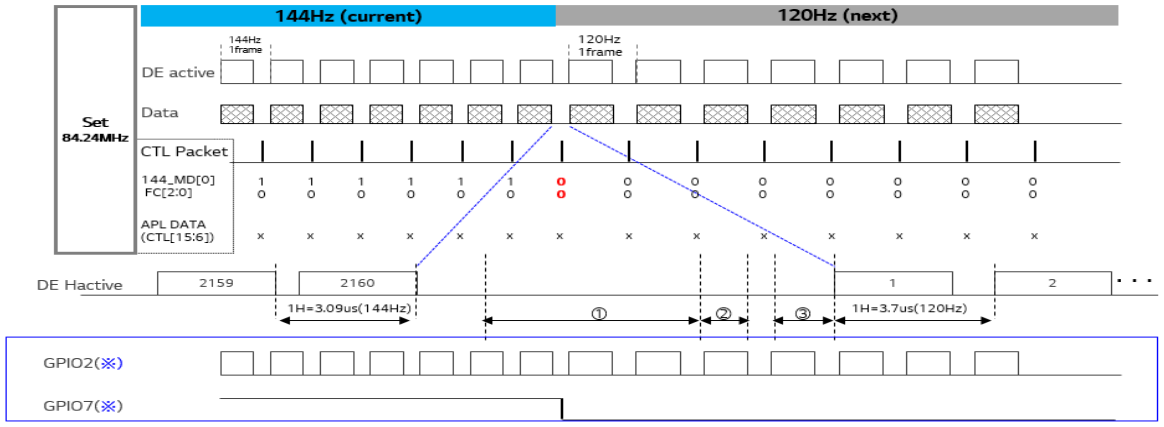
Setting	Value
addr : 0x7F[2]	1
en_891	H
5Byte_en	don't care

Order	Timing Spec.	
① CTL PKT 전송	Last De+16~60H(@120Hz)	range.
② LGD 144Hz Setting	5H(@120Hz)	Min.
③ SET Vx1 Tx clk 전환 (To 144Hz)	Last De+80H(@120Hz)	Min.

※Test Point 용 I2C셋팅(23.07.26 LGE 요청에 의해 가이드에 포함)
- 0xE0 addr 0xC800 data 0x00
- 0xE0 addr 0x1FB8 data 0x01
- 0xE0 addr 0x1FC0 data 0x01
- 0xE0 addr 0x1FBD data 0x16
- 0xE0 addr 0x1FC5 data 0x02

V24 SET 144Hz ⟶ 120Hz CTL PKT 전환 Sequence

You Dream, We Display.



SET는 Vblank내에 CTL PKT 을 1번만 보내야함
CTL PKT을 통한 모드 전환 사용시 최소 4frame 동안 정상적인 sync를 보내야함

Setting	Value
addr : 0x7F[2]	1
en_891	H
5Byte_en	don't care

Order	Timing Spec.	
① CTL PKT 전송	Last De+16~60H(@144Hz)	range.
② LGD 120Hz Setting	5H(@144Hz)	Min.
③ SET Vx1 Tx clk 전환 (To 120Hz)	Last De+80H(@144Hz)	Min.

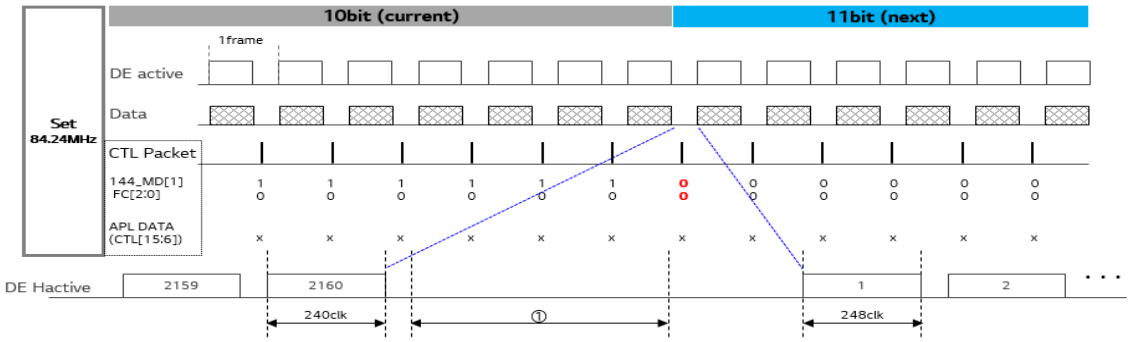
※Test Point 용 I2C셋팅(23.07.26 LGE 요청에 의해 가이드에 포함)
- 0xE0 addr 0xC800 data 0x00
- 0xE0 addr 0x1FB8 data 0x01
- 0xE0 addr 0x1FC0 data 0x01
- 0xE0 addr 0x1FBD data 0x16
- 0xE0 addr 0x1FC5 data 0x02

APPENDIX – XIV-2

■ 144Hz 변환 Guide

V24 SET 10bit ⟶ 11bit CTL PKT 전환 Sequence

You Dream, We Display.



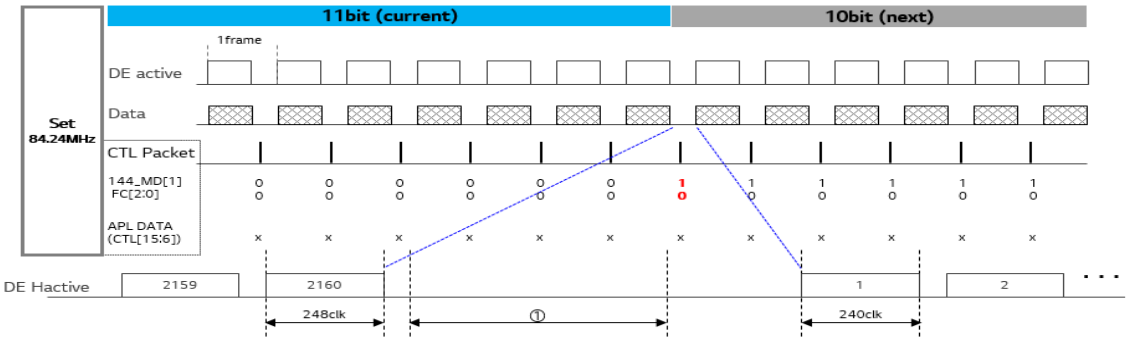
SET는 Vblank내에 CTL PKT 을 1번만 보내야함
CTL PKT을 통한 모드 전환 사용시 최소 4frame 동안 정상적인 sync를 보내야함

Setting	Value
addr : 0x7F[2]	1
en_891	H
5Byte_en	H

Order	Timing Spec.	
① CTL PKT 전송	Last De+16~60H	range.

V24 SET 11bit ⟶ 10bit CTL PKT 전환 Sequence

You Dream, We Display.



SET는 Vblank내에 CTL PKT 을 1번만 보내야함
CTL PKT을 통한 모드 전환 사용시 최소 4frame 동안 정상적인 sync를 보내야함

Setting	Value
addr : 0x7F[2]	1
en_891	H
5Byte_en	H

Order	Timing Spec.	
① CTL PKT 전송	Last De+16~60H	range.